# Understanding and Optimizing Equalizers (EQ) in PCI Express®

Webinar, May 12, 2020

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# Who We Are

## Granite River Labs (GRL)

- Recognized world leader in Test Services and Automation Solutions for connectivity and charging.
- Founded 2010, HQ in Silicon Valley, 8 labs around the world, ~200 employees.
- GRL provides compliance testing, official certification, and troubleshooting services for PCI Express, USB, Ethernet, and many other high-speed data connectivity and charging technologies.
- GRL provides Signal and Power Integrity services including VNA/TDR measurement and analysis, modeling and simulation, and design consultation.
- GRL has been a Keysight Solutions Partner since 2011.

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## Keysight Technologies

Keysight Technologies, Inc. (NYSE: KEYS) is a leading technology company that helps enterprises, service providers and governments accelerate innovation to connect and secure the world. Keysight's solutions optimize networks and bring electronic products to market faster and at a lower cost with offerings from design simulation, to prototype validation, to manufacturing test, to optimization in networks and cloud environments. Customers span the worldwide communications ecosystem, aerospace and defense, automotive, energy, semiconductor and general electronics end markets. Keysight generated revenues of $4.3B in fiscal year 2019.

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# Today's Presenters

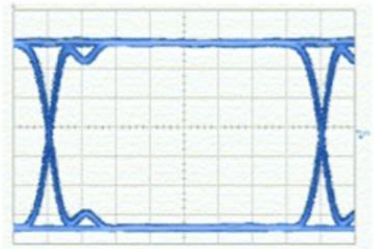
**Mike Resso** is the Signal Integrity Application Scientist in the Internet Infrastructure Solution Group of Keysight Technologies and has over thirty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high-speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including two books on signal integrity. Mike has been awarded one US patent and has twice received the Agilent "Spark of Insight" Award for his contribution to the company. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

**Miki Takahashi** is Executive Vice President of Engineering at Granite River Labs and has over 20 years of experience in high speed SerDes design, signal integrity design and measurement, as well as interface modeling and simulation. Miki has been working on and contributing to the PCI Express standard since v1.0. An expert in memory bus technologies, Miki chairs the SD Association UHS Task Group driving next-generation high speed memory card PHY standards, received the SD Association Innovation and Technology Award in 2014, and has authored numerous technical whitepapers and seminars. He received a M.S. in Material Physics from Nagoya University.

# Agenda

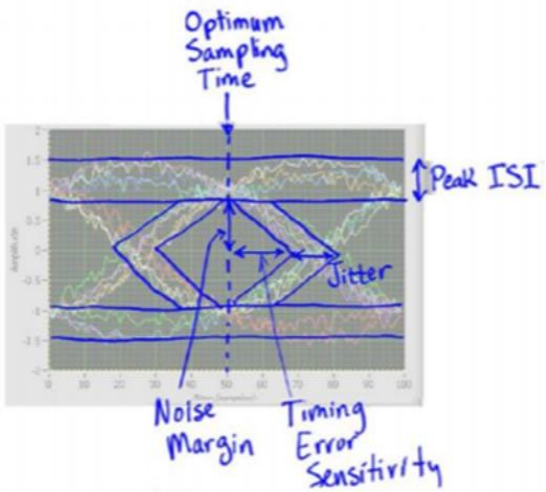
- Signal Integrity Overview
  - Essential Signal Integrity Analyses
  - Critical Steps to Taking a Measurement
  - Reference Plane Discussion
- PCI Express Design Case Study
  - Challenges in Latest PCI Express
  - Equalization Techniques For PCI Express Link
  - Dynamic Equalization
  - PCI Express Gen4 Equalization Case Study

# Signal Integrity is All Around Us






© Asfiakhan | Dreamstime.com - 3d People Communication Metallic Tin Can Phone Concept Photo

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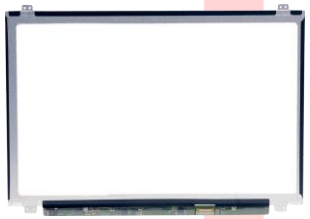
# Signal Integrity in Digital Communication Channel

CPU

Graphic card

Cable

On board video processor



LED display

Interconnects

> Signal integrity is about the problems interconnects introduce and how to avoid them.
>
> – Dr. Eric Bogatin

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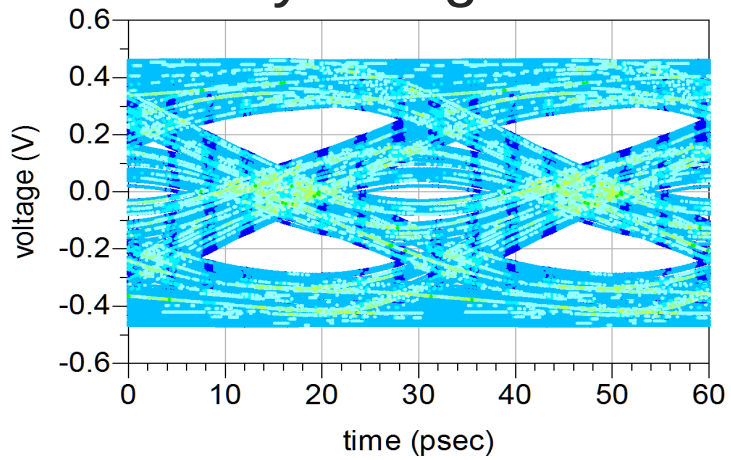
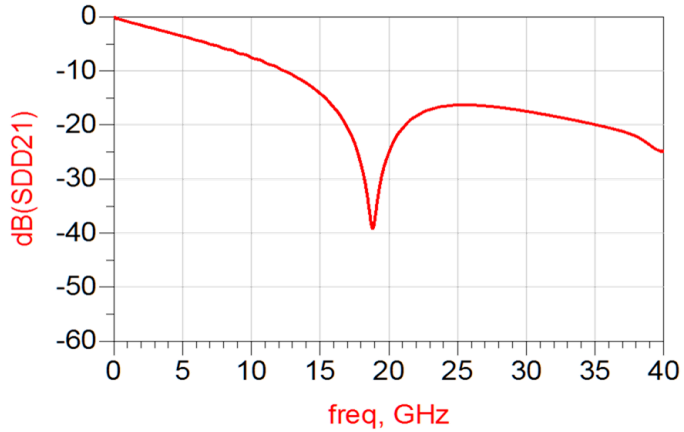
# Essential Signal Integrity Analyses in Simulation

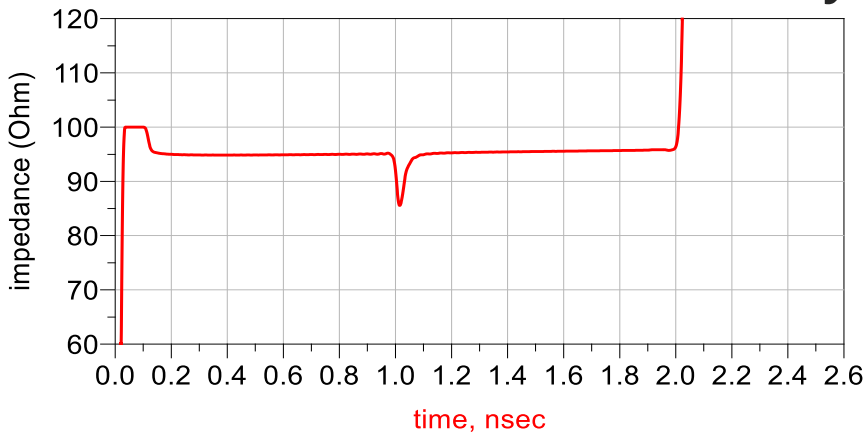
## Eye diagram



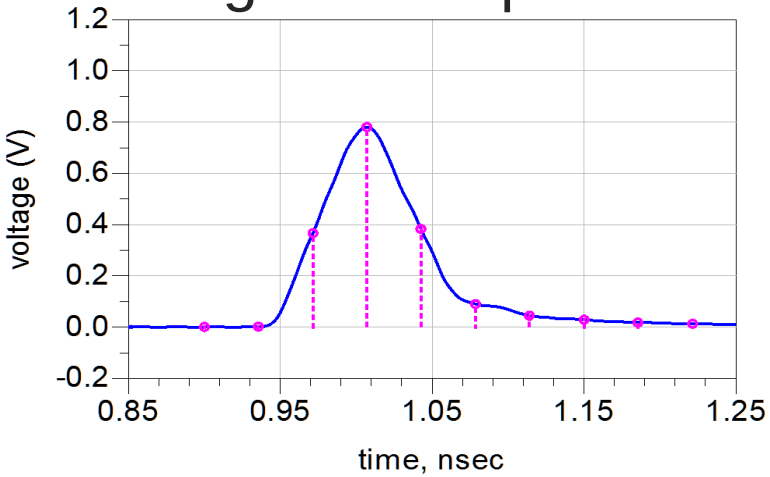

## Mixed-mode S-parameters




## Time domain reflectometry




## Single bit response

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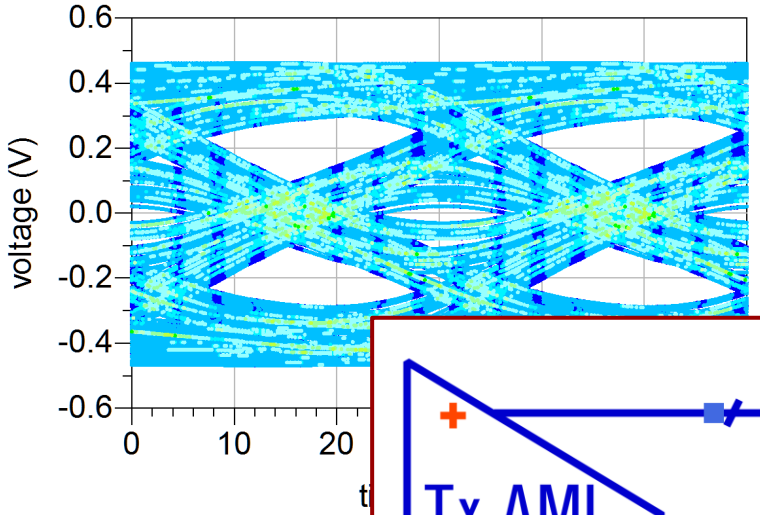
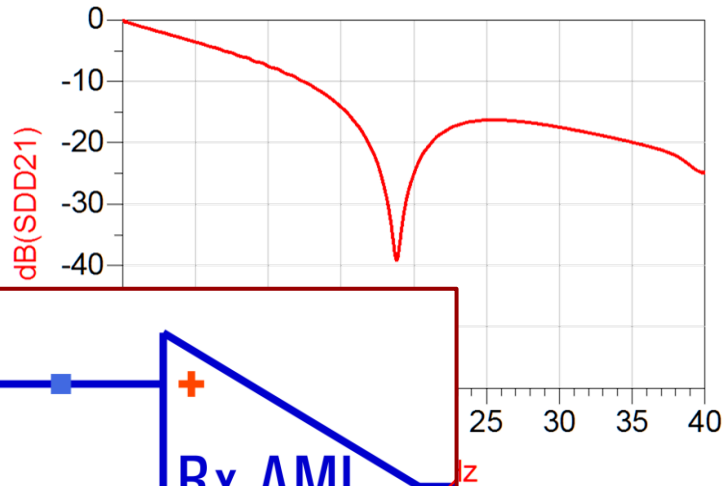
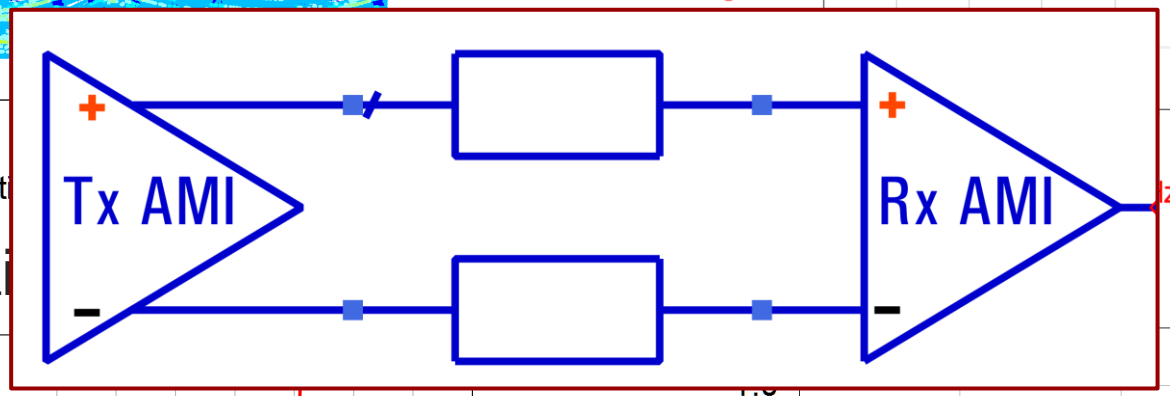
# Essential Signal Integrity Analyses in Simulation

Eye diagram



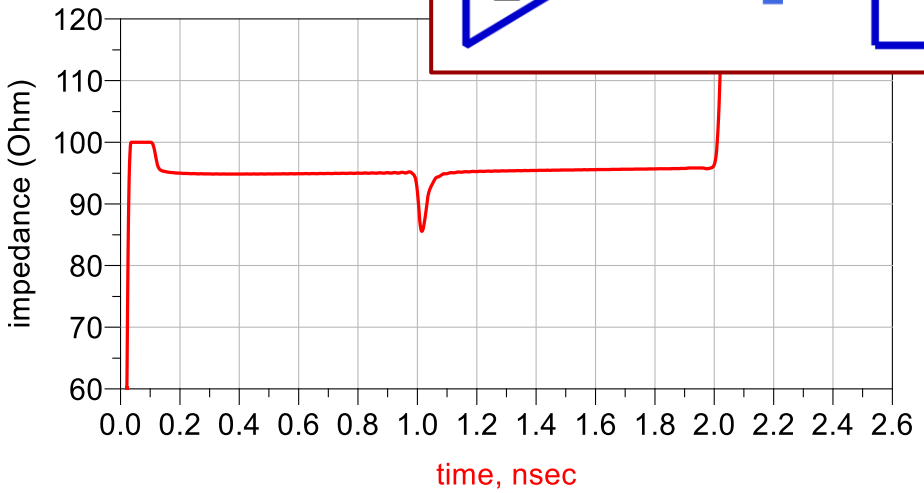

Mixed-mode S-parameters

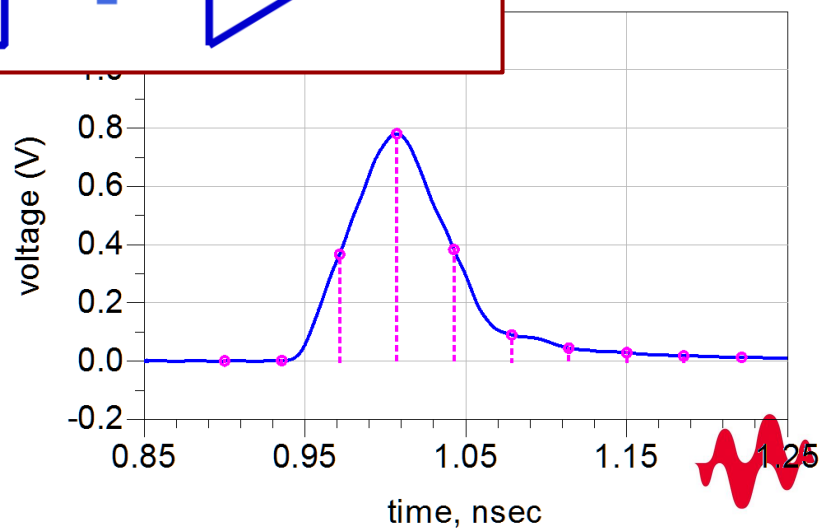



Time domai

response

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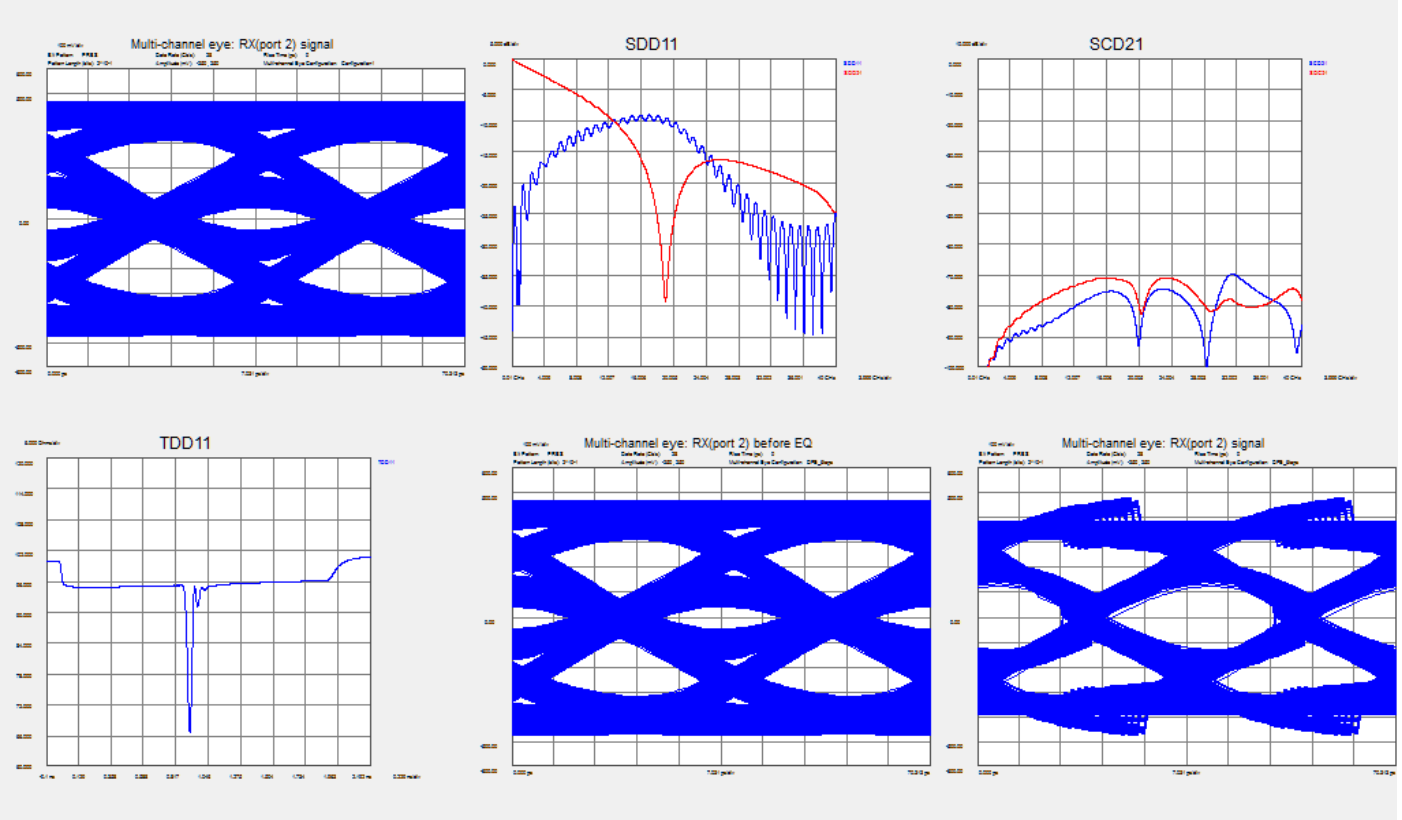
# Essential Signal Integrity Analyses in Measurement





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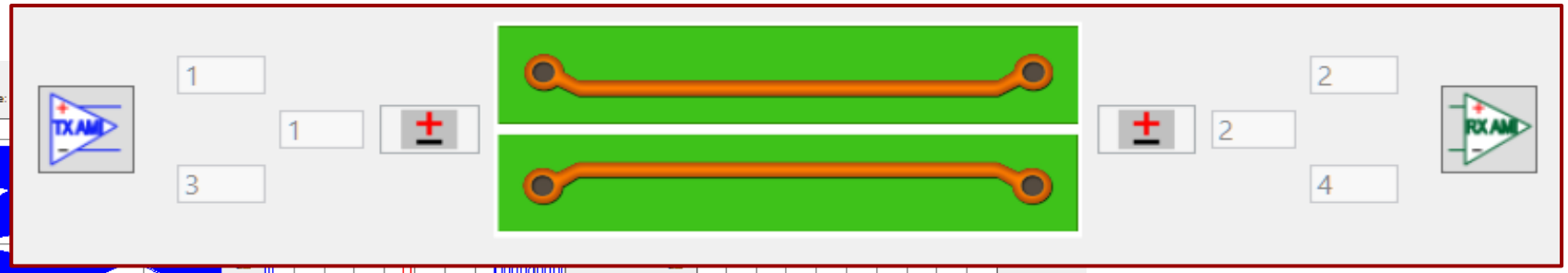
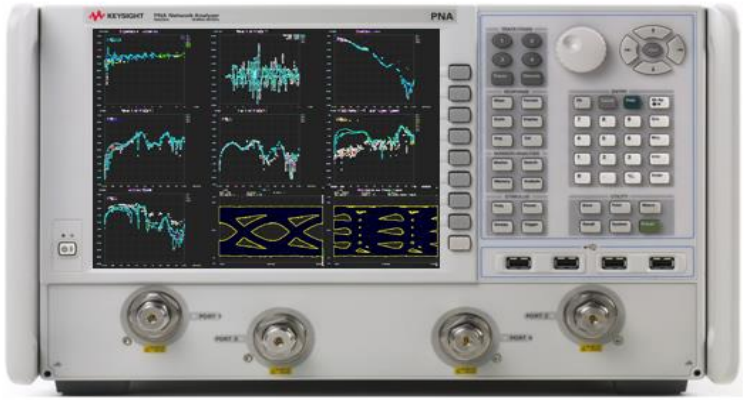
# Essential Signal Integrity Analyses in Measurement

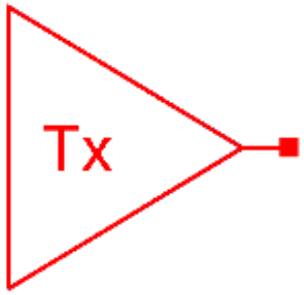


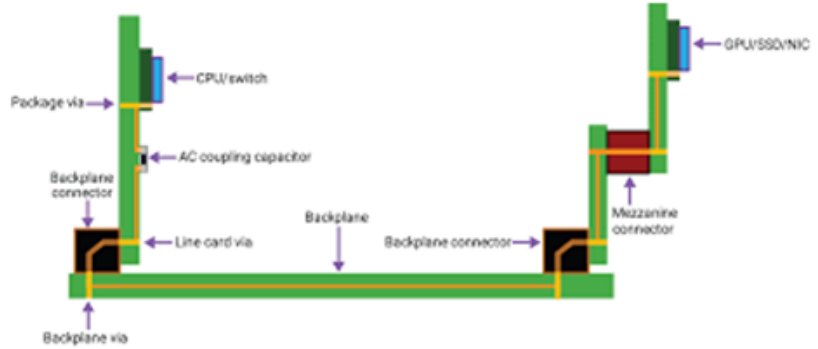


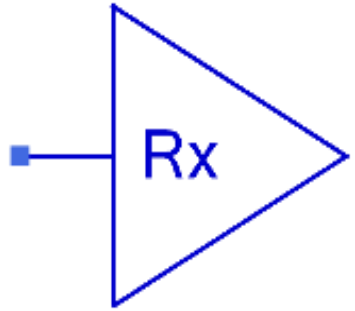


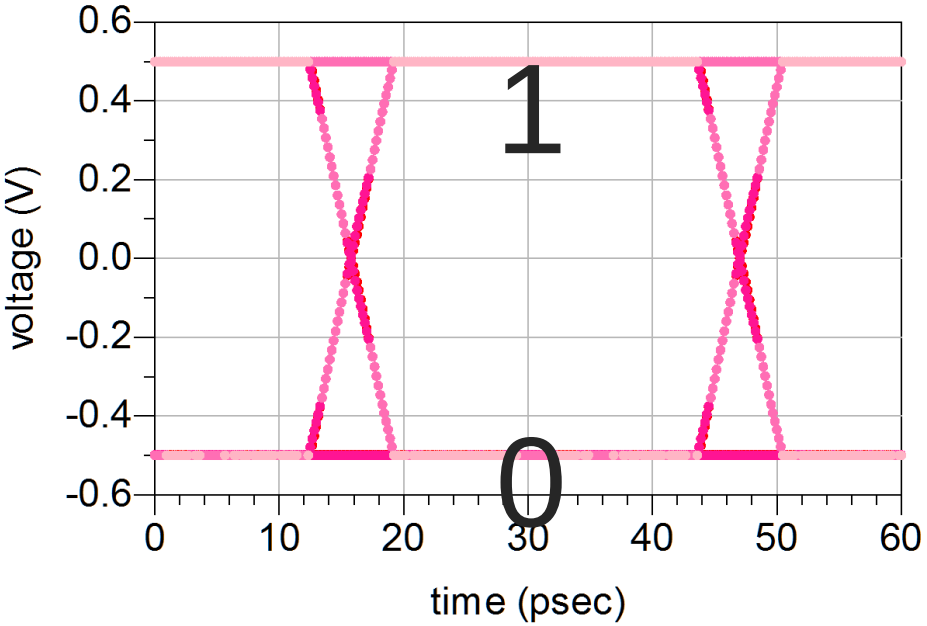


# Use Eye Diagram Simulation to Evaluate a Channel

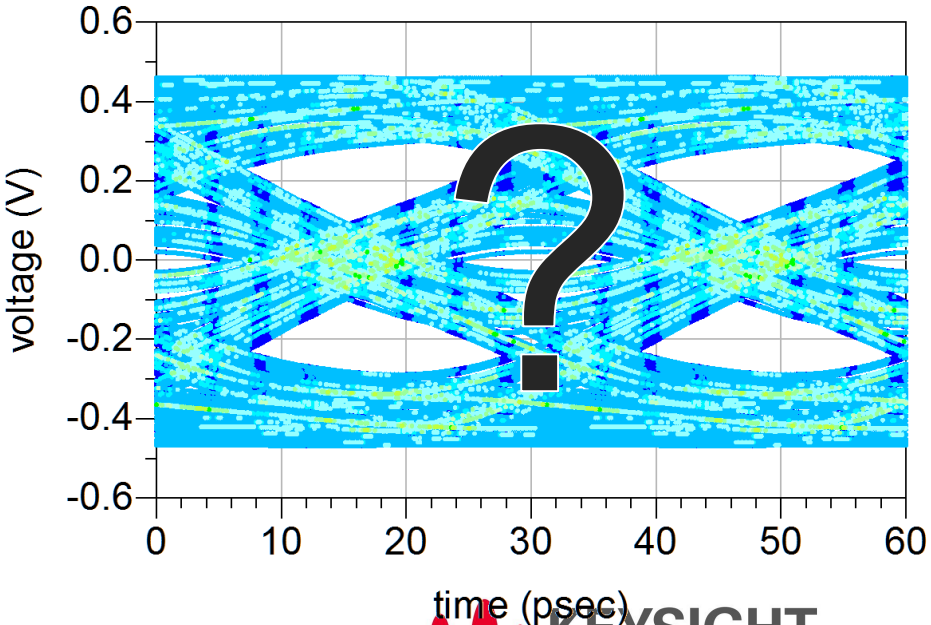


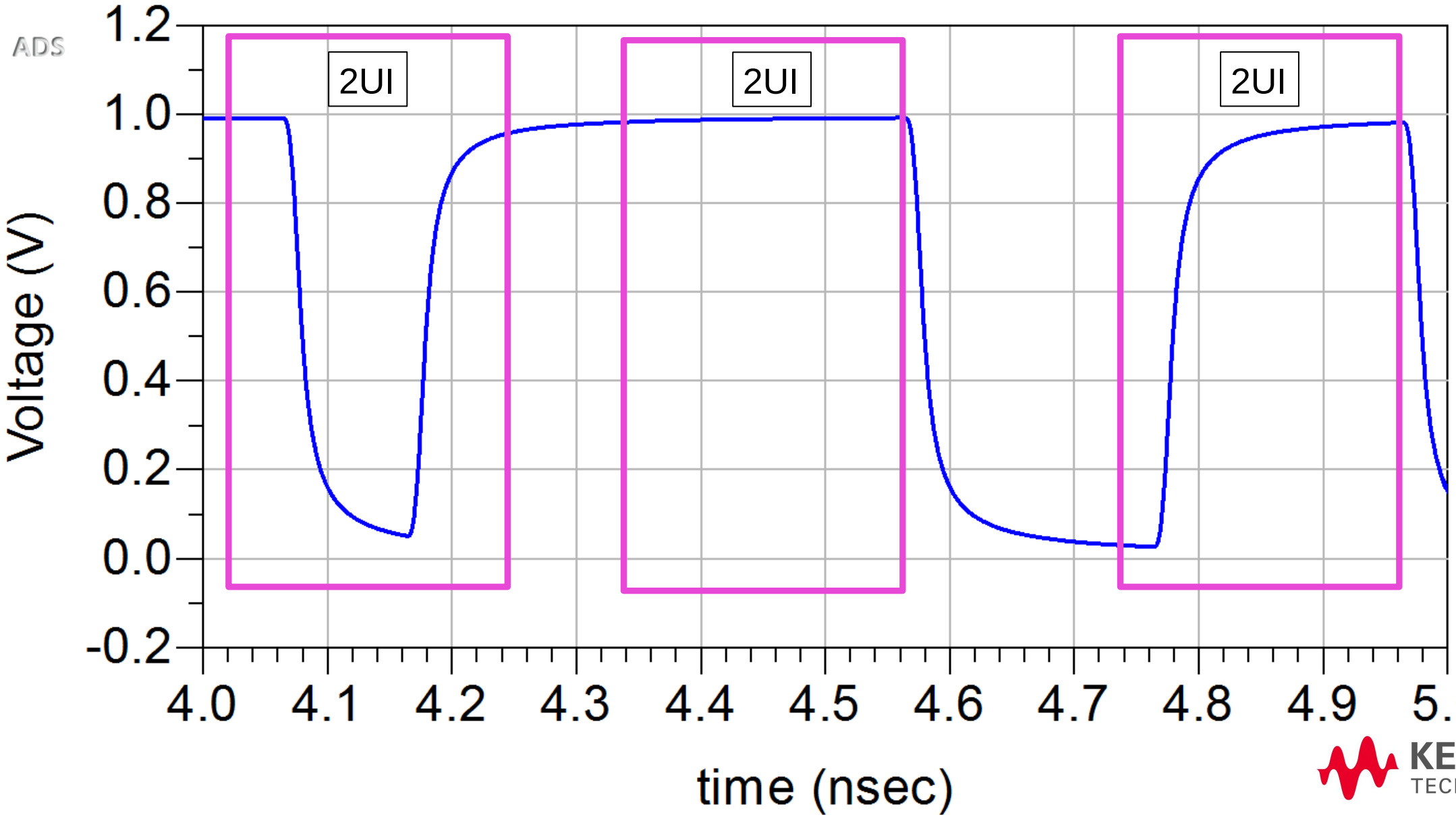




Channel



# Partition PRBS Pattern by Unit Intervals

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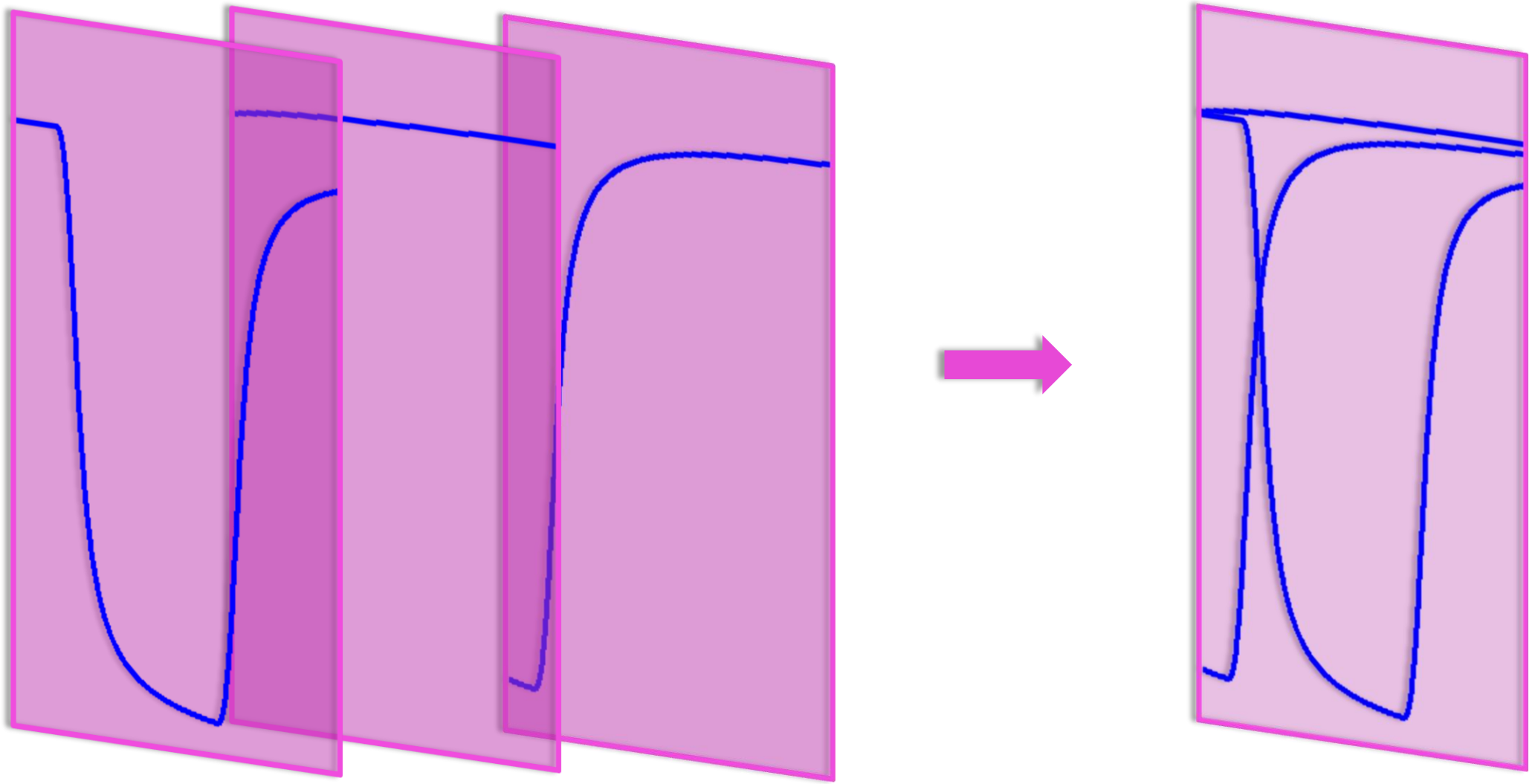
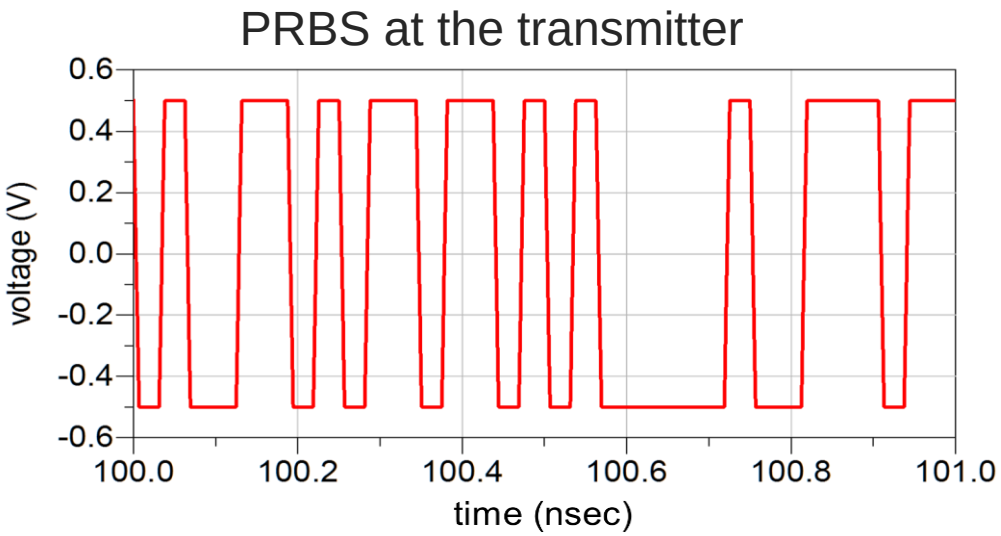
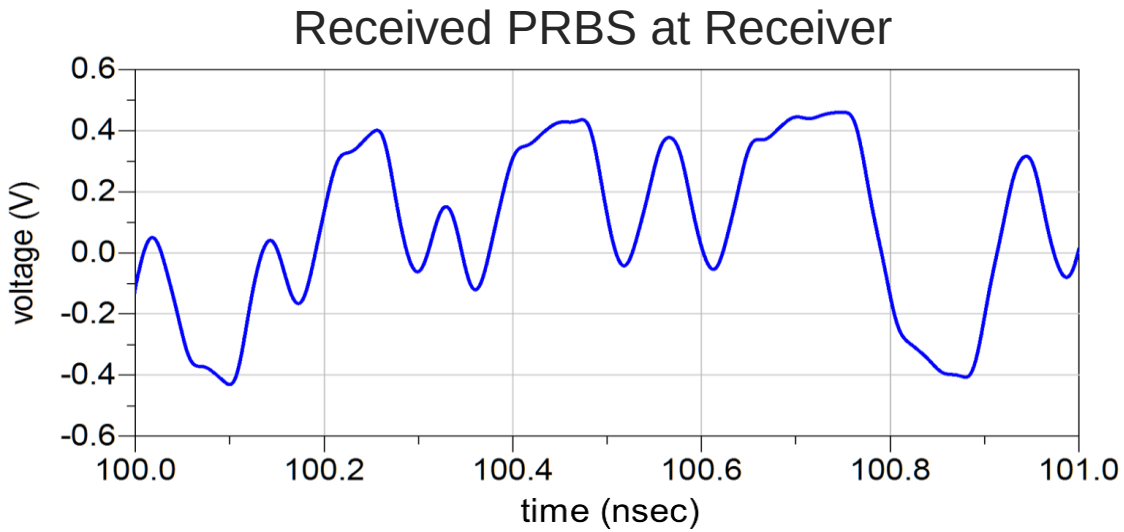
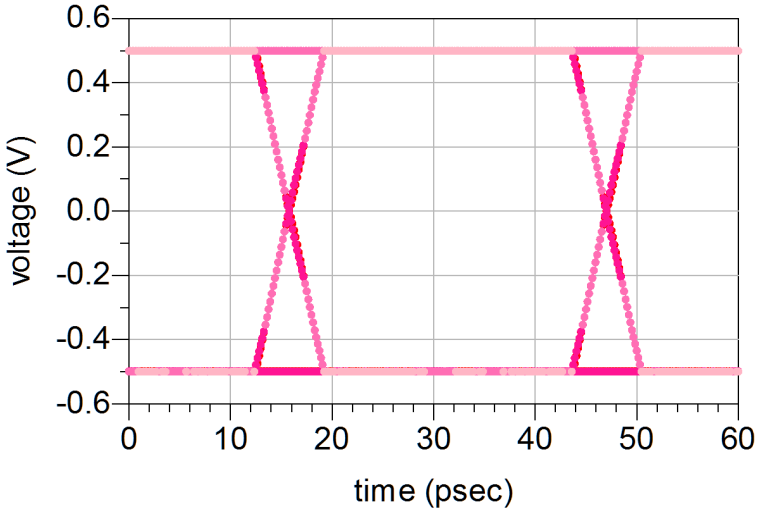
# Overlay Partitioned PRBS Slices to Create the Eye

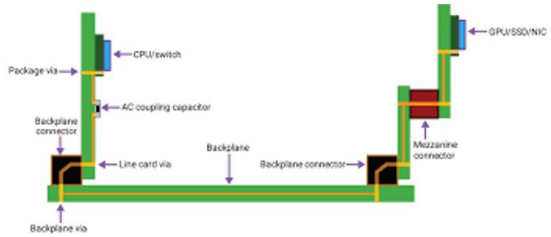


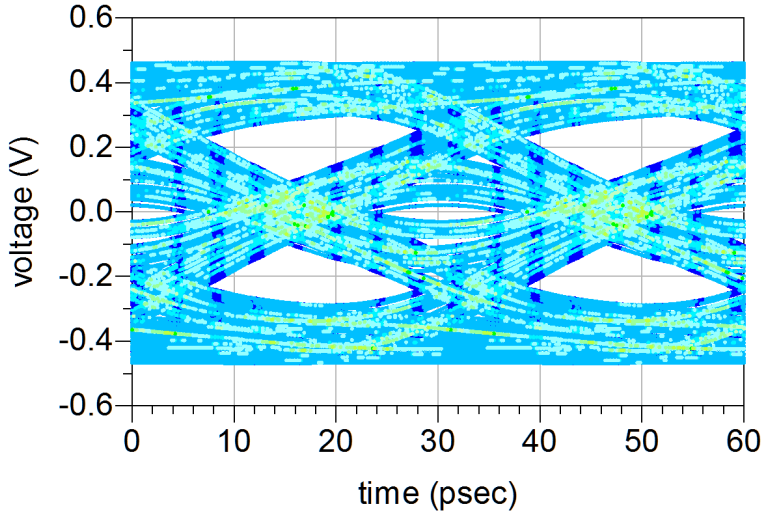
# Closed Eye at the Receiver: Signal Integrity Problem

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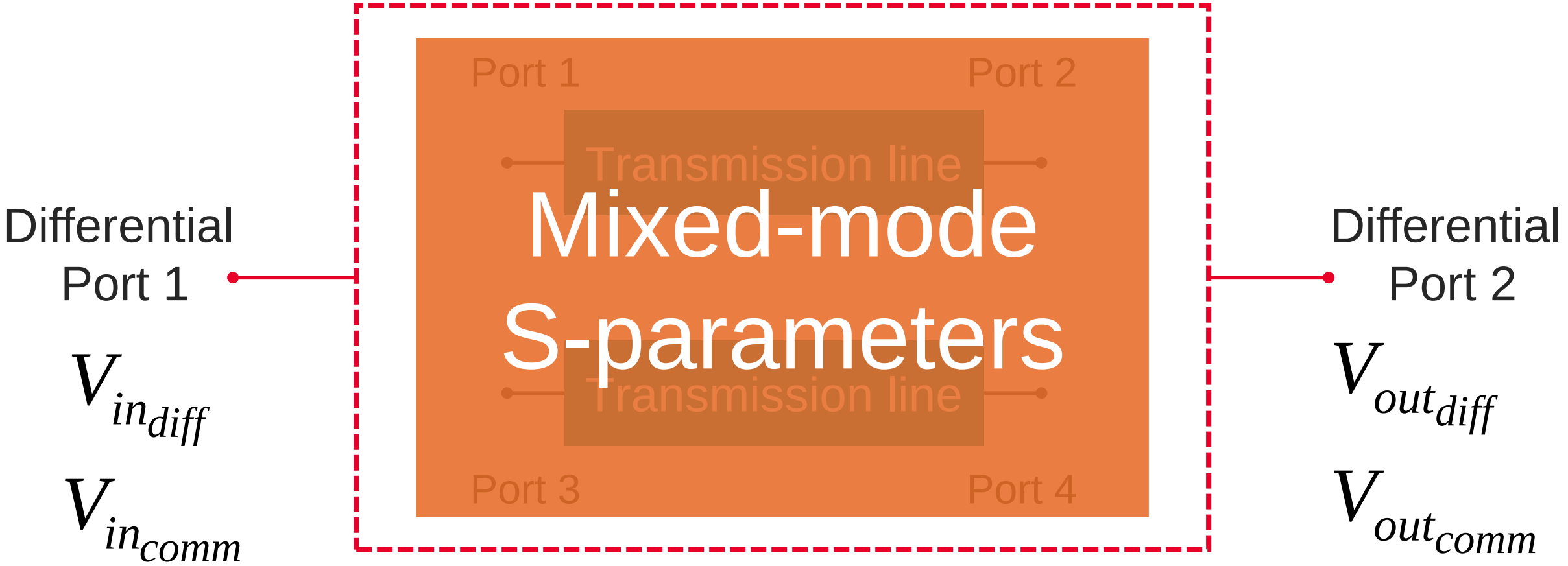
# Use Mixed-mode S-parameters for Differential Channels



# Stimulus and Responses in Mixed-mode S-parameters

$$[S_{\text{mixed-mode}}]$$

| | Differential Signal Stimulus | Common Signal Stimulus |
|---|---|---|
| Differential Response | $S_{DD11}$ $S_{DD12}$<br>$S_{DD21}$ $S_{DD22}$ | $S_{DC11}$ $S_{DC12}$<br>$S_{DC21}$ $S_{DC22}$ |
| Common Response | $S_{CD11}$ $S_{CD12}$<br>$S_{CD21}$ $S_{CD22}$ | $S_{CC11}$ $S_{CC12}$<br>$S_{CC21}$ $S_{CC22}$ |

# Important Mixed-mode S-parameters

$S_{DD11}$ Differential response at port 1, excited by Differential input at port 1.

$S_{DD11}$ Related to differential return loss.

$S_{DD21}$ Related to differential insertion loss.

$S_{CD21}$ Mode-conversion: EM generation.

$S_{DC21}$ Mode-conversion: EM susceptibility.

# Critical Steps to Taking a Measurement in the Real World

**Establish a Robust Signal Integrity Measurement and Simulation Workflow**
https://connectlp.keysight.com/DesignConKEF2018

**Prepare instrument for measurement**

- Calibration
- Fixture removal (de-embedding)

→ **Anticipate the measured result**

**Acquire channel data**

- Multi-port S-parameter measurement

**Analyze channel performance**

- Single-ended vs. differential
- Eye diagrams (NRZ, PAM4)
- COM

# Comparison Between Calibration and De-embedding

| | Calibration | De-embedding |
|---|---|---|
| Objective | | |
| Target | | |
| Reference Structures | | |
| Techniques | | |

# Comparison Between Calibration and De-embedding

| | Calibration | De-embedding |
|---|---|---|
| Objective | Move reference plane | |
| Target | | |
| Reference Structures | | |
| Techniques | | |

# Comparison Between Calibration and De-embedding

| | Calibration | De-embedding |
|---|---|---|
| **Objective** | **Move reference plane** | |
| **Target** | Instrument | Measurement |
| **Reference Structures** | | |
| **Techniques** | | |

# Comparison Between Calibration and De-embedding

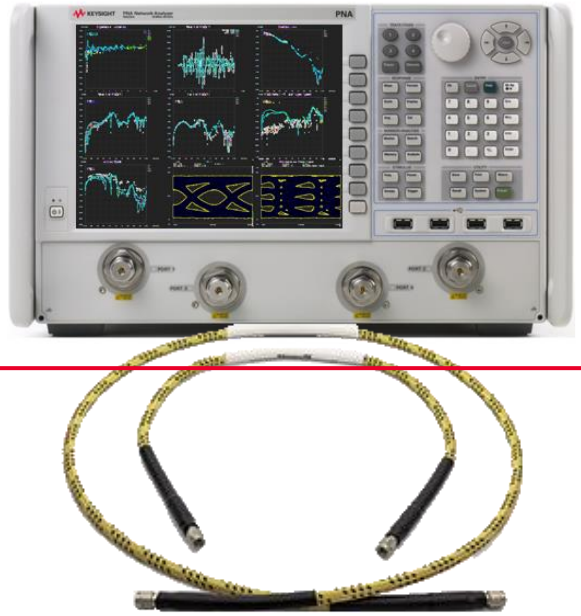
| | Calibration | De-embedding |
|---|---|---|
| **Objective** | **Move reference plane** | |
| **Target** | Instrument | Measurement |
| **Reference Structures** | | |
| **Techniques** | | |

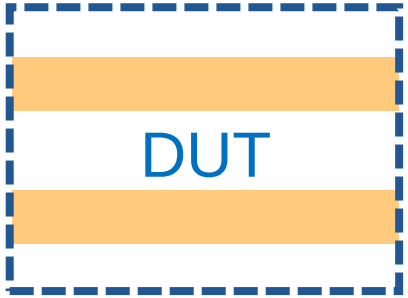
# Comparison Between Calibration and De-embedding

| | Calibration | De-embedding |
|---|---|---|
| **Objective** | **Move reference plane** | |
| **Target** | Instrument | Measurement |
| **Reference Structures** | • Short, Open, Load, Thru (SOLT)<br>• Thru, Reflect, Line (TRL)<br>• Thru, Reflect, Match (TRM) | • 2x Thru<br>• 1x Open, 1x Short |
| **Techniques** | • Mechanical Calibration<br>• Electronic Calibration | • Automatic Fixture Removal<br>• Measurement-based Model |

# Calibration Moves the Instrument Reference Plane

Reference Plane

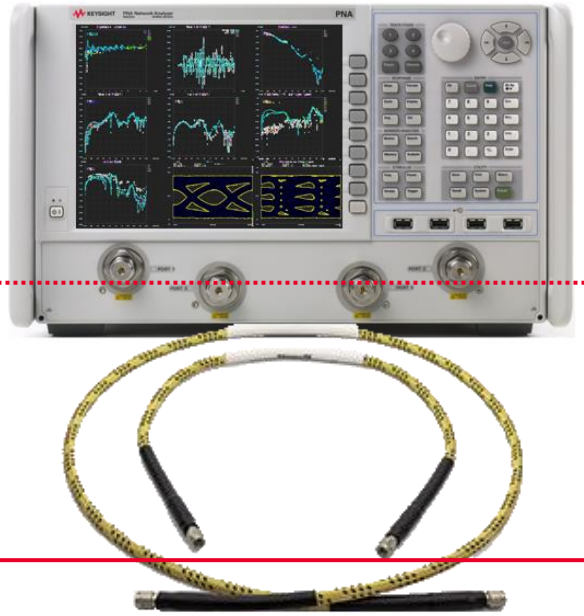




# Calibration Moves the Instrument Reference Plane

Calibration

Reference Plane



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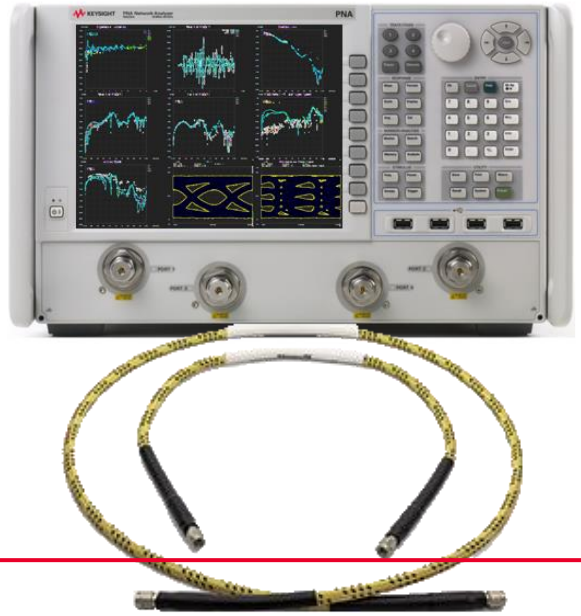
# Calibration Moves the Instrument Reference Plane



## Reference Plane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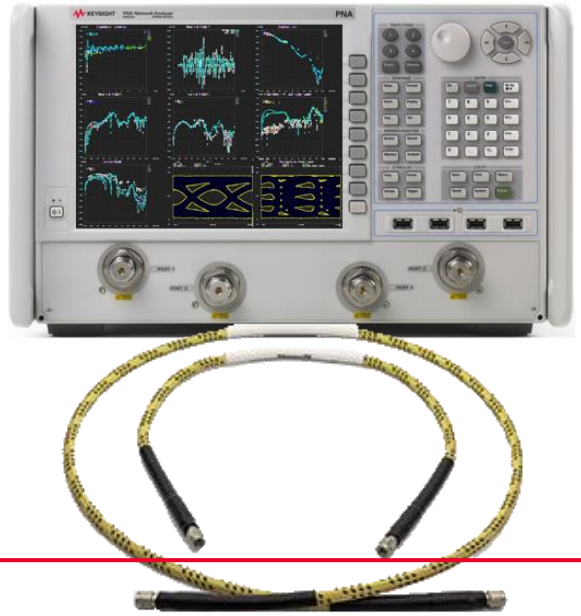
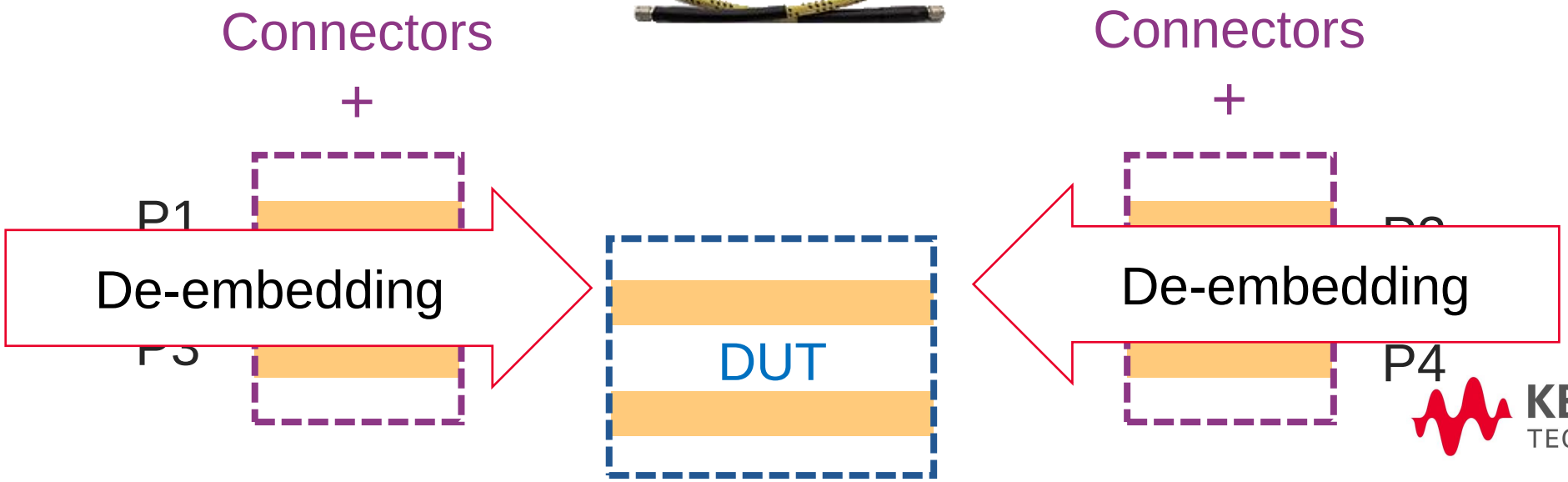
# Calibration Moves the Instrument Reference Plane



## Reference Plane



# Agenda

- Challenges in the Latest PCI Express
- Equalization Techniques For PCI Express Link
  - -FFE
  - -CTLE
  - -DFE
- Dynamic Equalization
- PCI Express Gen4 Equalization Case Study

# Challenges in Latest PCI Express

- Increasingly it becomes much more challenging to successfully transmit signal through channel essentially the same channel that was used for PCIe Gen1 (2.5 GT/s). But the data rate for PCIe Gen5 is 12.8 times faster than PCIe Gen1.

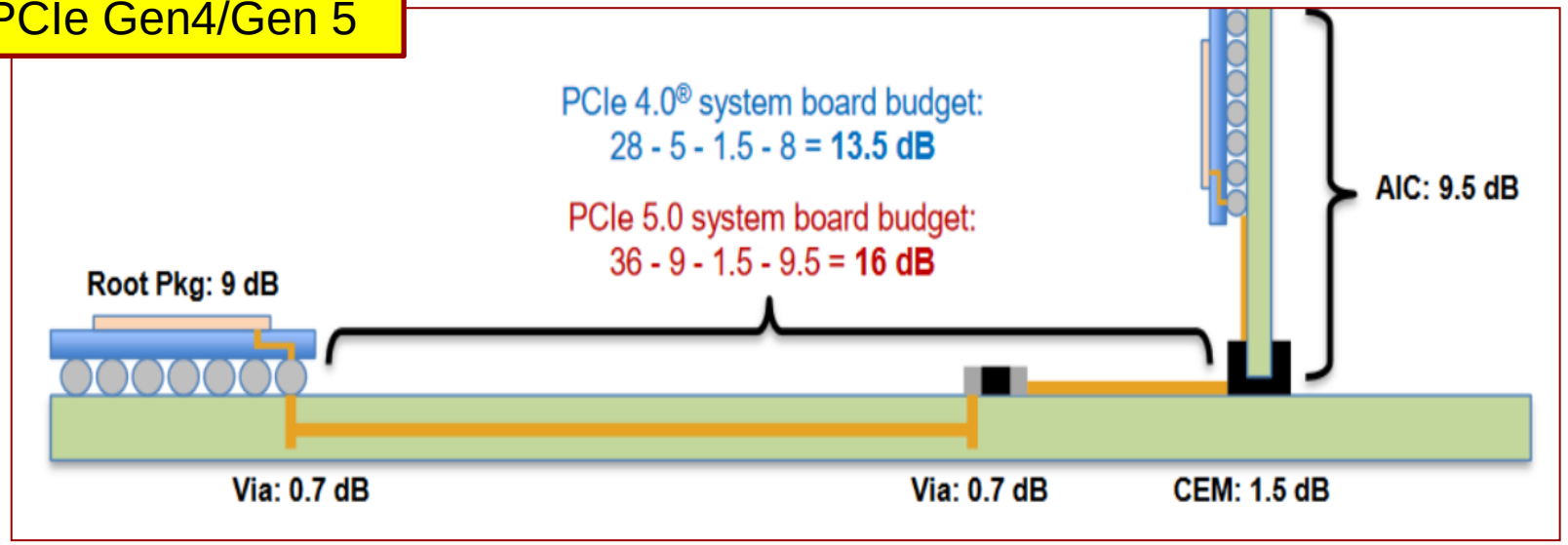
- For PCIe Gen5, Loss Budget (at Nyquist) is approximately -36dB.

36dB loss means that if 500mV@16GHz p-p sine wave goes into the channel, only 8mV p-p comes out.

# Challenges in Latest PCI Express

| PCIe Rev | Total Channel Loss Budget | Root Package | Non-root package | CEM Connector | Add-In Card (AIC) | Budget for system Board |
|---|---|---|---|---|---|---|
| Gen 5.0 (32 GT/s) | **36 dB** | 9.0 dB | 4.0 dB | 1.5 dB | 9.5 dB | 16.0 dB |

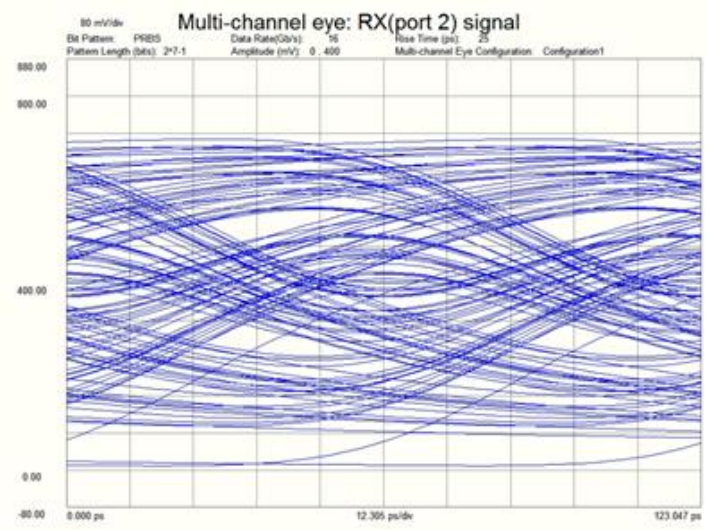
Loss Budget for PCIe Gen4/Gen 5

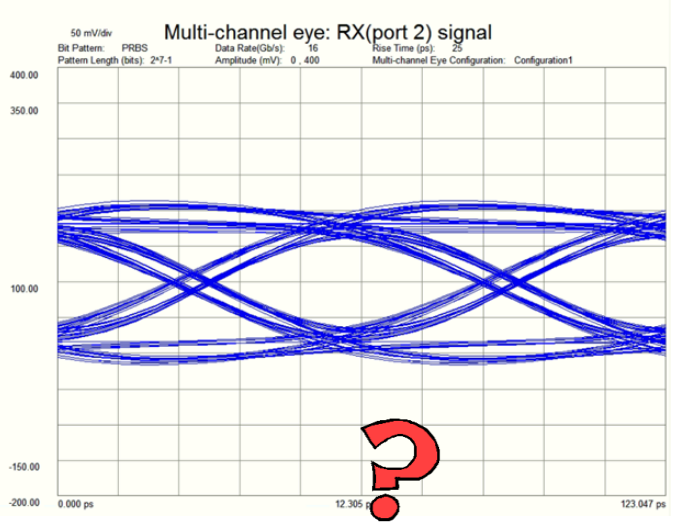


# Challenges in Latest PCI Express

Due to ISI, Eye is completely closed at far end of the channel, making impossible for Receiver to make correct bit decisions…

With “equalization”, Eye is now opened for Receiver to make correct bit decision…



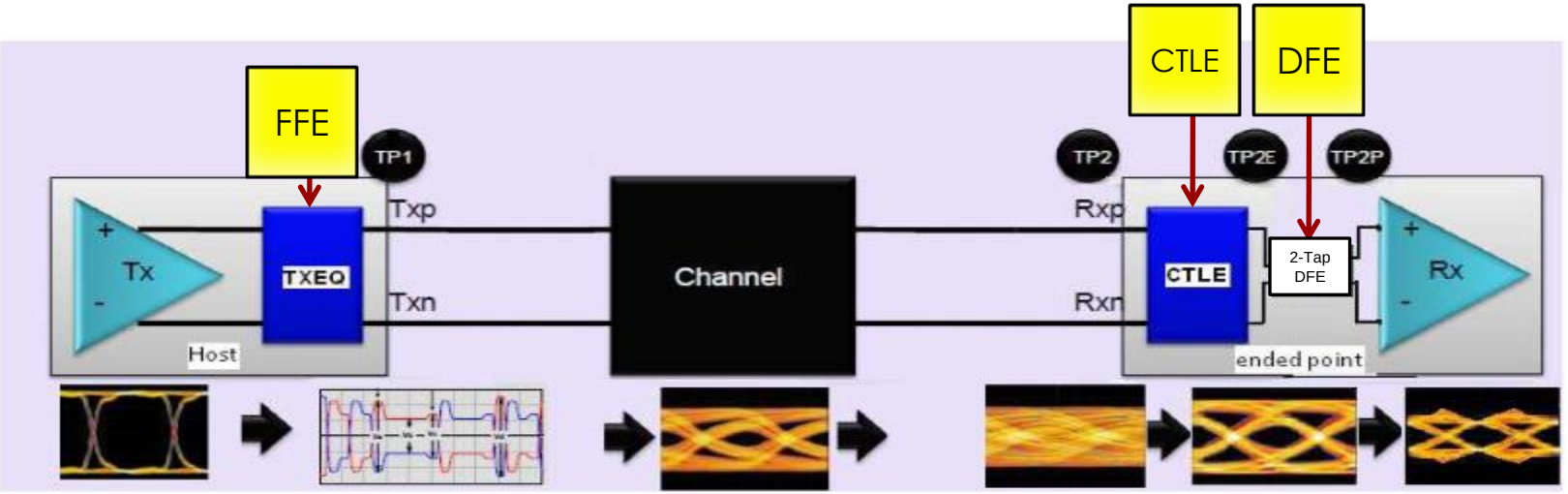

*How does a PCIe link open the eye with Equalizers?*

# Equalization Techniques for PCI Express Gen4/Gen5 Link

There are three (3) main techniques that PCIe uses to compensate for Intersymbol Interference (ISI) at data rates above 5Gbps:

- **CTLE (Continuous-Time Linear Equalizer)**
- **FFE (Feed-Forward Equalizer)**
- **DFE (Decision Feedback Equalizer)**

Each technique of offers advantages and disadvantages, but, when combined, offer power compensation for channel degradation



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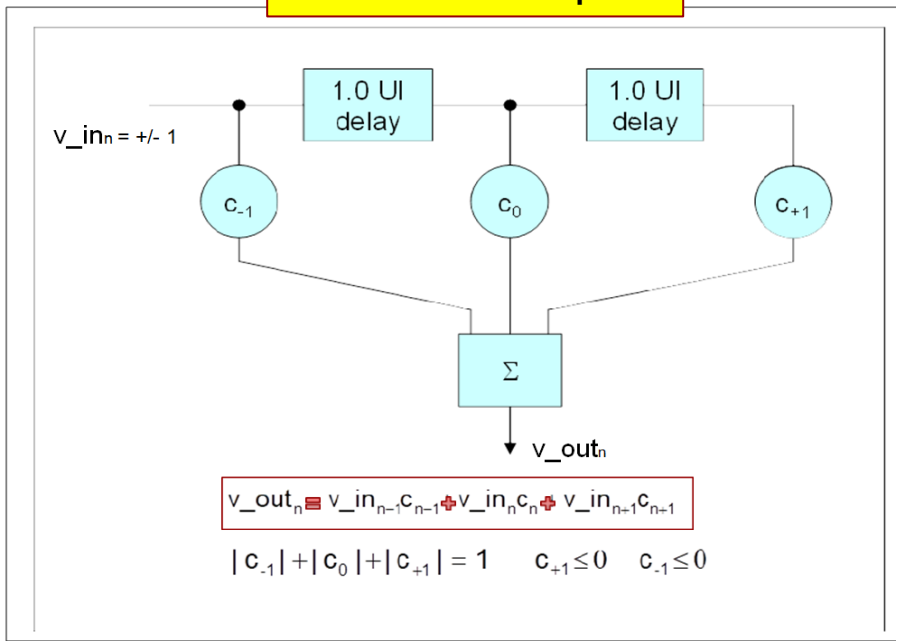
# Equalization Techniques for PCI Express Gen4/Gen5 Link

| PCIe version | Gen-1/2 | Gen-3 | Gen-4 | Gen-5 |
|---|---|---|---|---|
| Transmitter Equalization | Fixed De-Emphasis | 3-Tap FFE | 3-Tap FFE | 3-Tap FFE |
| Ref. Receiver CTLE | N/A | 1st Order CTLE<br>Gain: -6 to -12dB | 2-pole, 1-zero<br>Gain: -1 to -9dB | 4-pole, 2-zeros<br>Gain: -5 to -15dB |
| Ref. Receiver DFE | N/A | 1-Tap DFE | 2-Tap DFE | 3-Tap DFE |

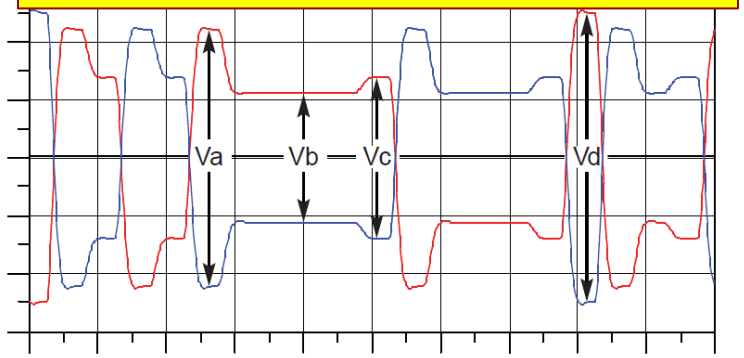
# FFE: Feed-Forward Equalizer

- An *FFE* modifies the amplitudes of symbols surrounding transitions while keeping the transmitted power constant.
- In principle, FFE  increase the ratio of high frequency to low frequency signal components compensate for the typical lowpass response of the channel.
- PCIe Spec defines preset values for TX FFE (10 presets).

FIR filter: 3 taps




FFE signal in time domain




De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb



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# CTLE: Continuous Time Linear Equalizer

- *CTLE* is a linear filter applied at the receiver that attenuates low-frequency signal components, amplifies frequency components around the Nyquist frequency, and filters off higher frequencies.

- CTLE gain (*Adc*) can be adjusted to optimize the ratio of low frequency attenuation to high frequency amplification

- PCIe uses 2nd Order CTLE (order of CTLE is defined by the poles/zeroes)

CTLE for 32GT/s with two (2) zeroes and four (4) poles

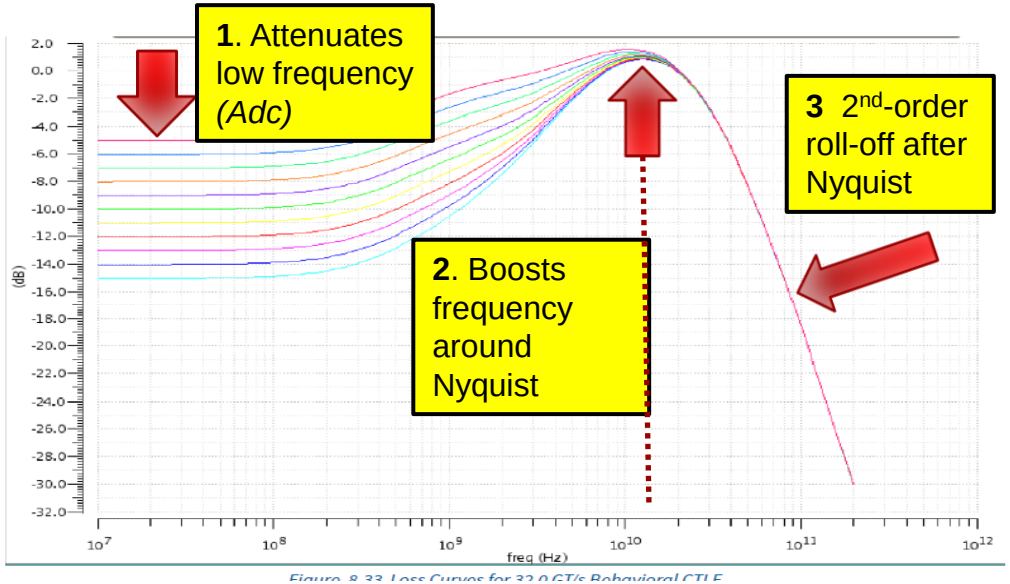


Figure 8-33 Loss Curves for 32.0 GT/s Behavioral CTLE

$$H(s) = \frac{\omega_{P1} \times \omega_{P3} \times \omega_{P4}}{\omega_{Z1}} \times \frac{(s + \omega_{Z1})(s + \omega_{P2} \times A_{DC})}{(s + \omega_{P1})(s + \omega_{P2})(s + \omega_{P3})(s + \omega_{P4})}$$

$\omega_X = 2\pi \times F_X$

$F_{P1} = 1.65 \times F_{Z1}$

$F_{P2} = 9.5$ GHz

$F_{P3} = 28$ GHz

$F_{P4} = 28$ GHz

$F_{Z1} = 450$ MHz

$F_{Z2} = \text{mag}(\text{DC gain}) \times F_{P2}$



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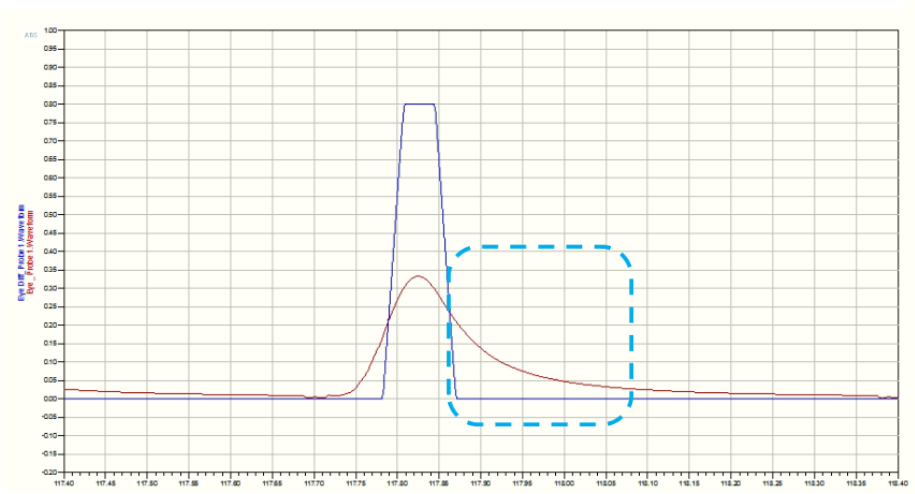
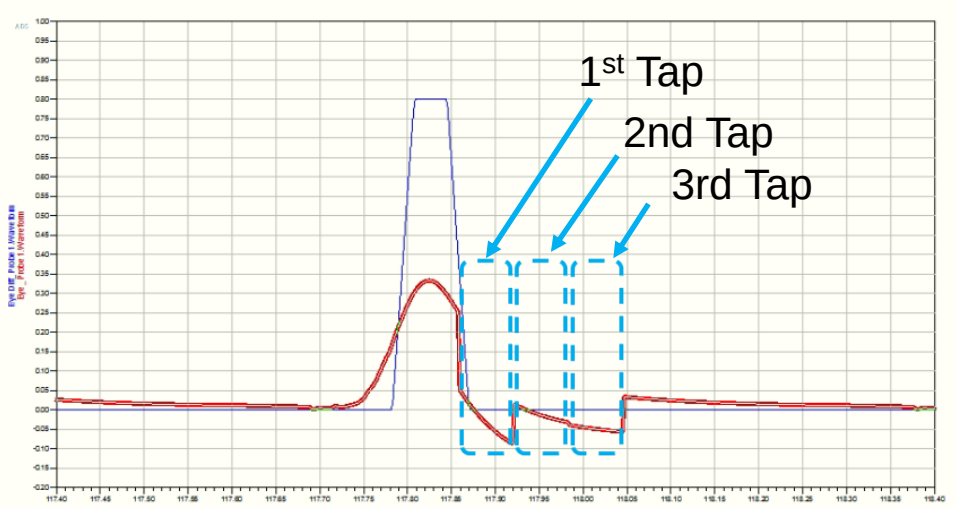
# DFE: Decision Feedback Equalizer

- *DFE* is implemented at the receiver
- Implicitly nonlinear, DFE feeds a sum of logic or previous symbol decisions back to the symbol decoder
- DFE is not able to cancel the precursor ISI thus, typically, needs to be paired with FFE (in transmitter or receiver)
- DFE is most effective way to cancel postcursor ISI because it does not reduce the transmit peak voltage budget nor amplify channel noise
- PCIe implements 1-3 tap implementation depending on the generation



Before DFE




After DFE



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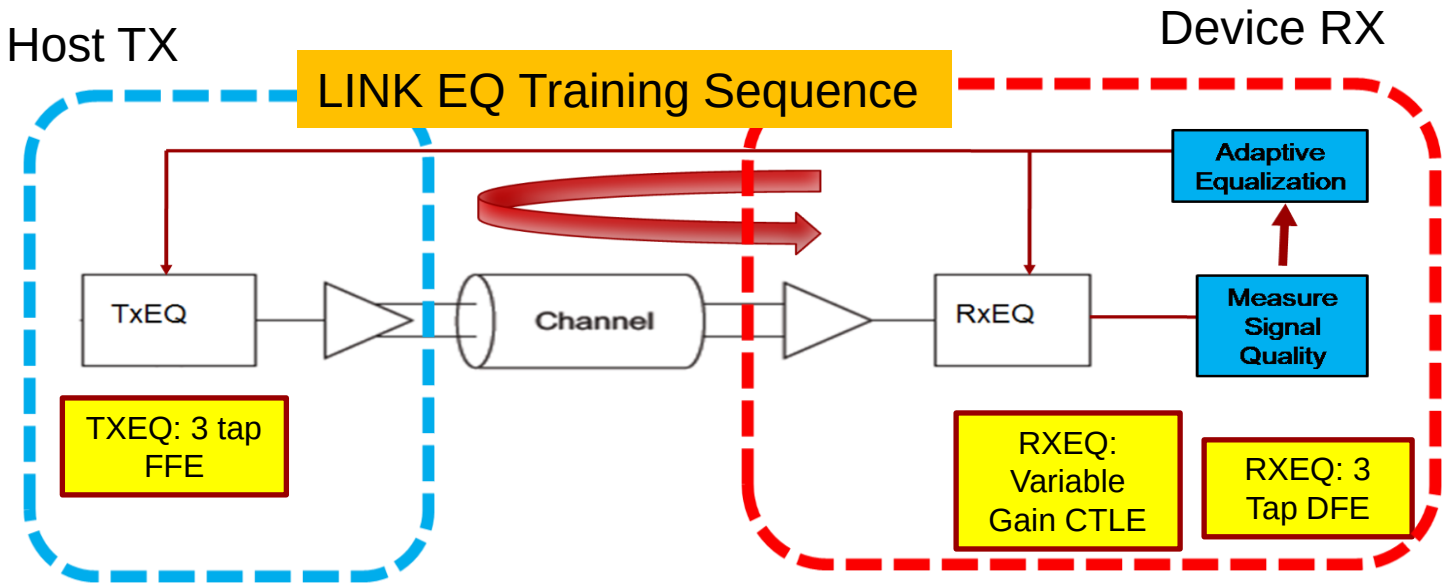
# Dynamic Equalization

## Transmitter and Receiver negotiate optimal EQ settings

### The Receiver and Transmitter optimize link through the Channel:

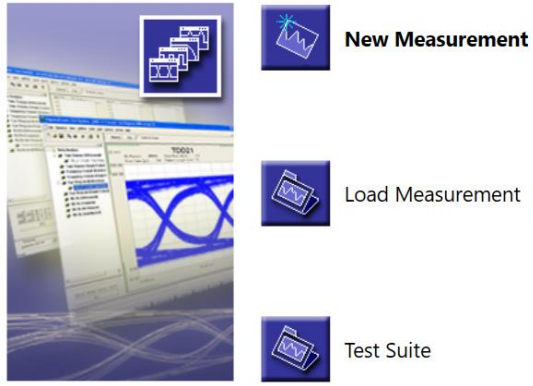
1. Receiver requests TXEQ setting from Transmitter
2. Transmitter applies requested TXEQ
3. Receiver adjusts its equalization (CTLE gain, DFE) with the updated TXEQ applied from Transmitter
4. Receiver determines its signal quality through BER or other methods
5. Depending on Signal Quality, the Receiver will adjust its equalization and then request and updated TXEQ setting from the Transmitter
6. This process is repeated until optimal Link is generated



# PCI Express Gen4 Equalization Case Study

**Instruments used in the analysis**

-Keysight 50GHz VNA N5225A
-Keysight PLTS
-Keysight Pathwave ADS




# PCIe Gen4 Case Study (ISI Channels)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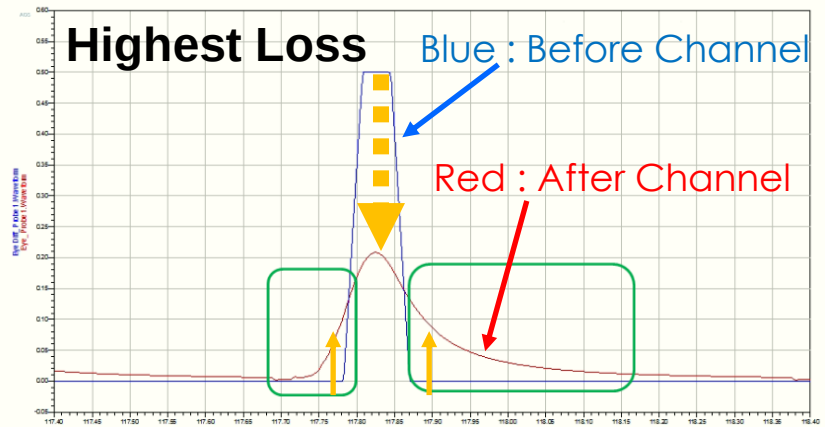
# PCIe Gen4 Case Study (Pulse Response)


Higher Channel Loss Causes Higher Attenuation and Slower Signal Transition beyond the Pulse Width.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# PCIe Gen4 Case Study

Pulse Response gives you the information what equalization is needed and how strong equalizer should be used.


What you can see from this pulse response?

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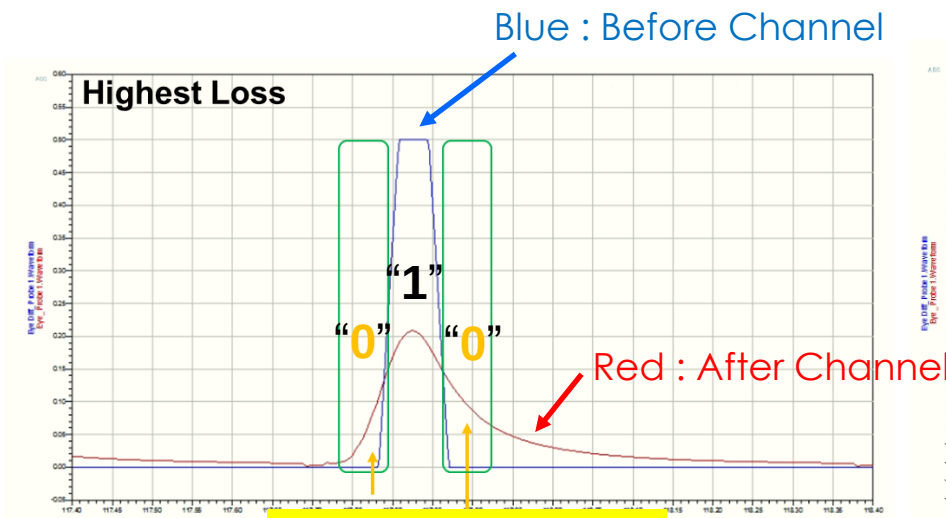
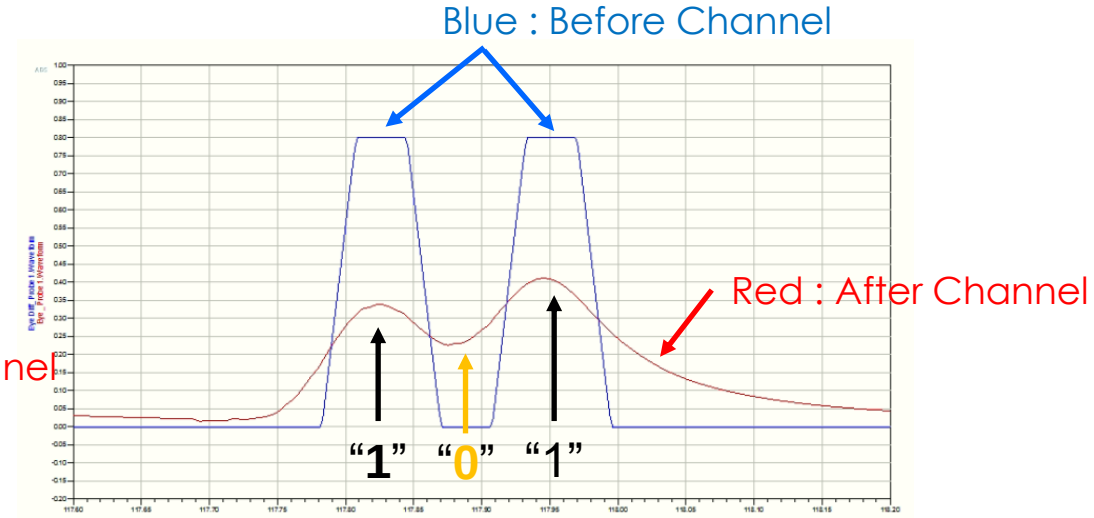
# PCIe Gen4 Case Study




Pulse Response




When bits "101" is transmitted

1. Signal Peak is attenuated.
2. Pulse spreads beyond 1UI. It may cause bit error.
3. When bits "101" is transmitted, **bit "0" is lost**.
4. Slow transition is observed "before" the pulse
5. Slow transition is observed "after" the pulse. Transition time after the pulse is longer than before the pulse.

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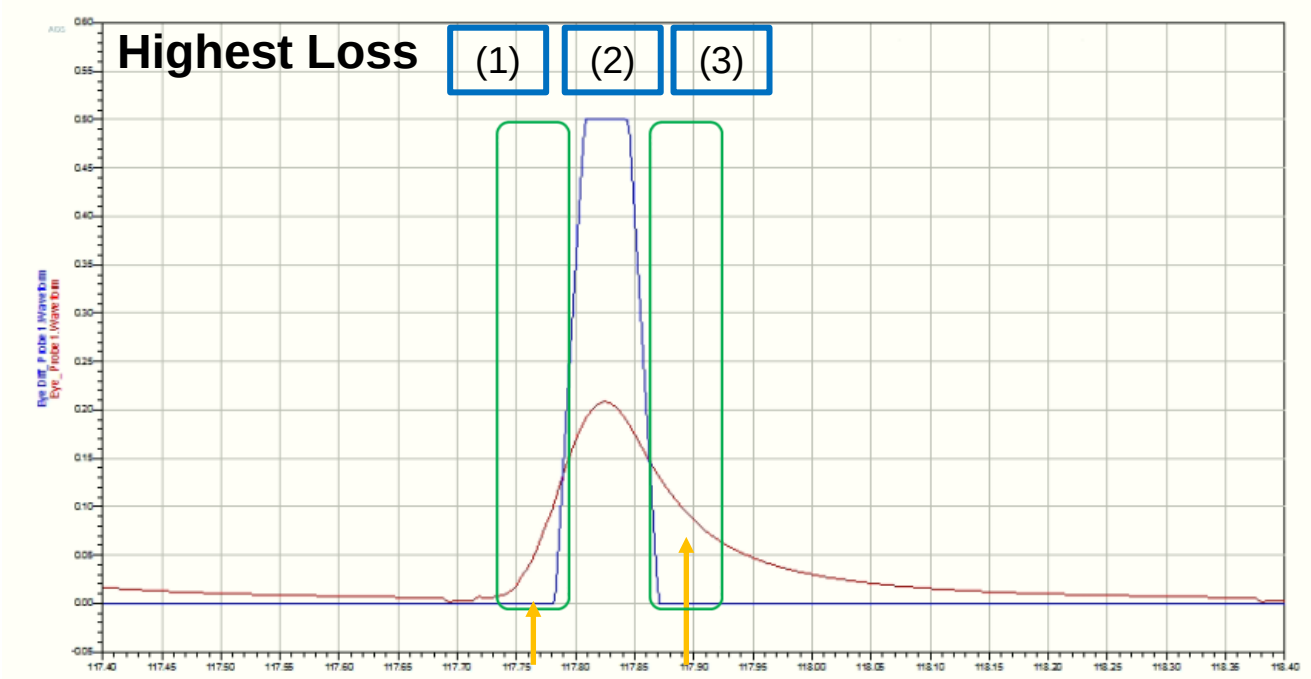
# PCIe Gen4 Case Study




The important thing is sending “A Pulse” without bit corruption and affecting pulses before/after the pulse.

These (1), (2) and (3) are corresponding to “pre-cursor”, “main-cursor” and “post cursor” in equalizer definition. If you use higher taps in the equalizer you can compensate more bits before/after the bit.

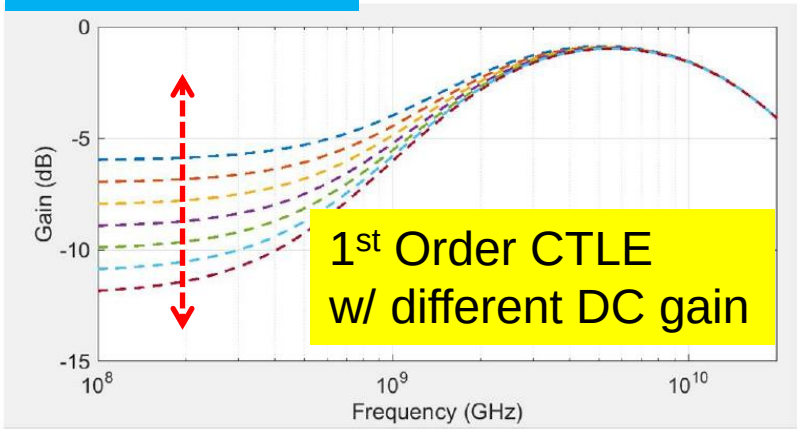
# PCIe Gen4 Case Study

## Equalizer Pre-Set in the PCI Express Specification

### TX FFE

| Preset # | Preshoot (dB) | De-emphasis (dB) | c-1 | c+1 | Va/Vd | Vb/Vd | Vc/Vd |
|---|---|---|---|---|---|---|---|
| P4 | 0.0 | 0.0 | 0.000 | 0.000 | 1.000 | 1.000 | 1.000 |
| P1 | 0.0 | -3.5 ± 1 dB | 0.000 | -0.167 | 1.000 | 0.668 | 0.668 |
| P0 | 0.0 | -6.0 ± 1.5 dB | 0.000 | -0.250 | 1.000 | 0.500 | 0.500 |
| P9 | 3.5 ± 1 dB | 0.0 | -0.166 | 0.000 | 0.668 | 0.668 | 1.000 |
| P8 | 3.5 ± 1 dB | -3.5 ± 1 dB | -0.125 | -0.125 | 0.750 | 0.500 | 0.750 |
| P7 | 3.5 ± 1 dB | -6.0 ± 1.5 dB | -0.100 | -0.200 | 0.800 | 0.400 | 0.600 |
| P5 | 1.9 ± 1 dB | 0.0 | -0.100 | 0.000 | 0.800 | 0.800 | 1.000 |
| P6 | 2.5 ± 1 dB | 0.0 | -0.125 | 0.000 | 0.750 | 0.750 | 1.000 |
| P3 | 0.0 | -2.5 ± 1 dB | 0.000 | -0.125 | 1.000 | 0.750 | 0.750 |
| P2 | 0.0 | -4.4 ± 1.5 dB | 0.000 | -0.200 | 1.000 | 0.600 | 0.600 |
| P10 | 0.0 | Note 2. | 0.000 | Note 2. | 1.000 | Note 2. | Note 2. |

### RX CTLE




### RX DFE

2tap-DFE

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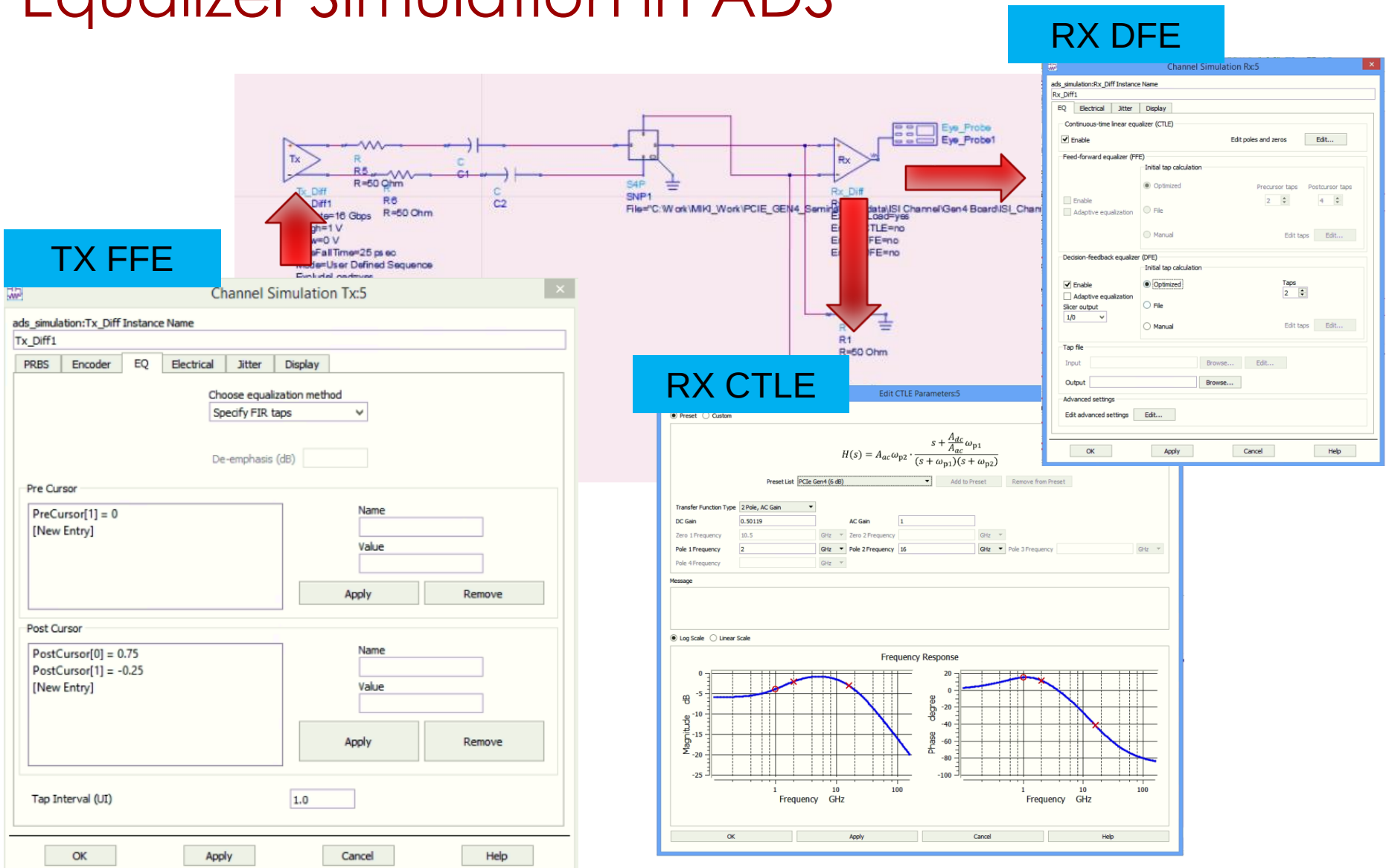
# PCIe Gen4 Case Study

## Equalizer Simulation in ADS

RX DFE

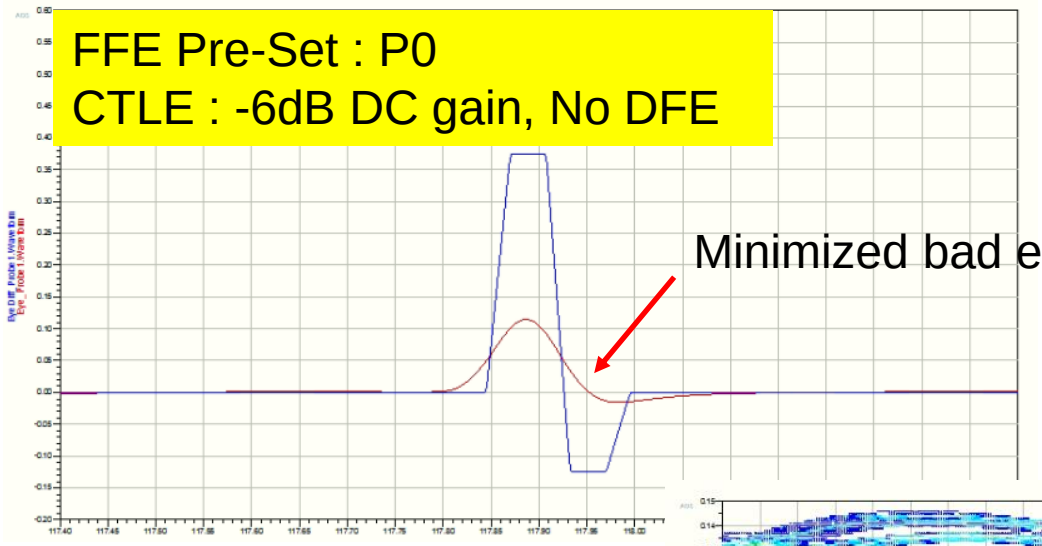
TX FFE

RX CTLE

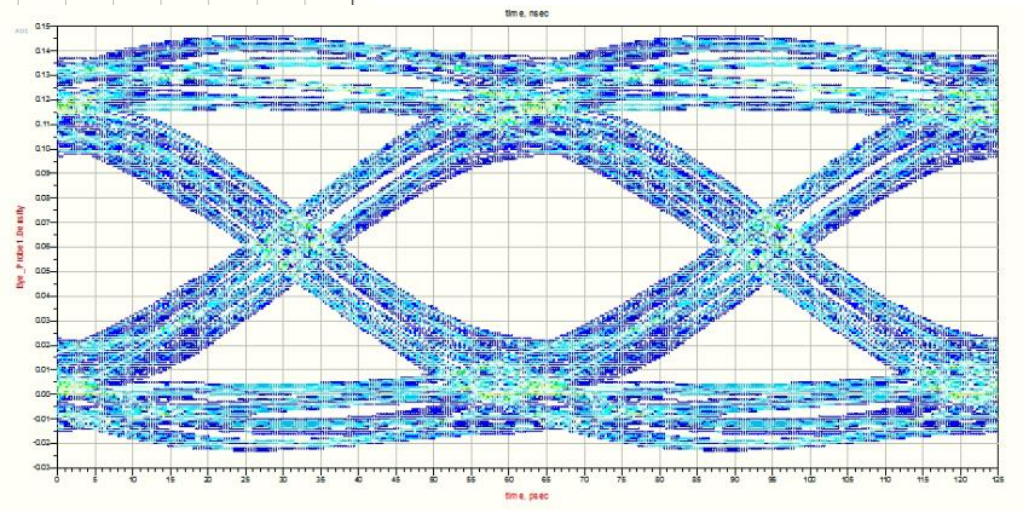


# PCIe Gen4 Case Study
## Equalizer Simulation in ADS

FFE + CTLE : Pulse Response was improved.




Eye is opened widely



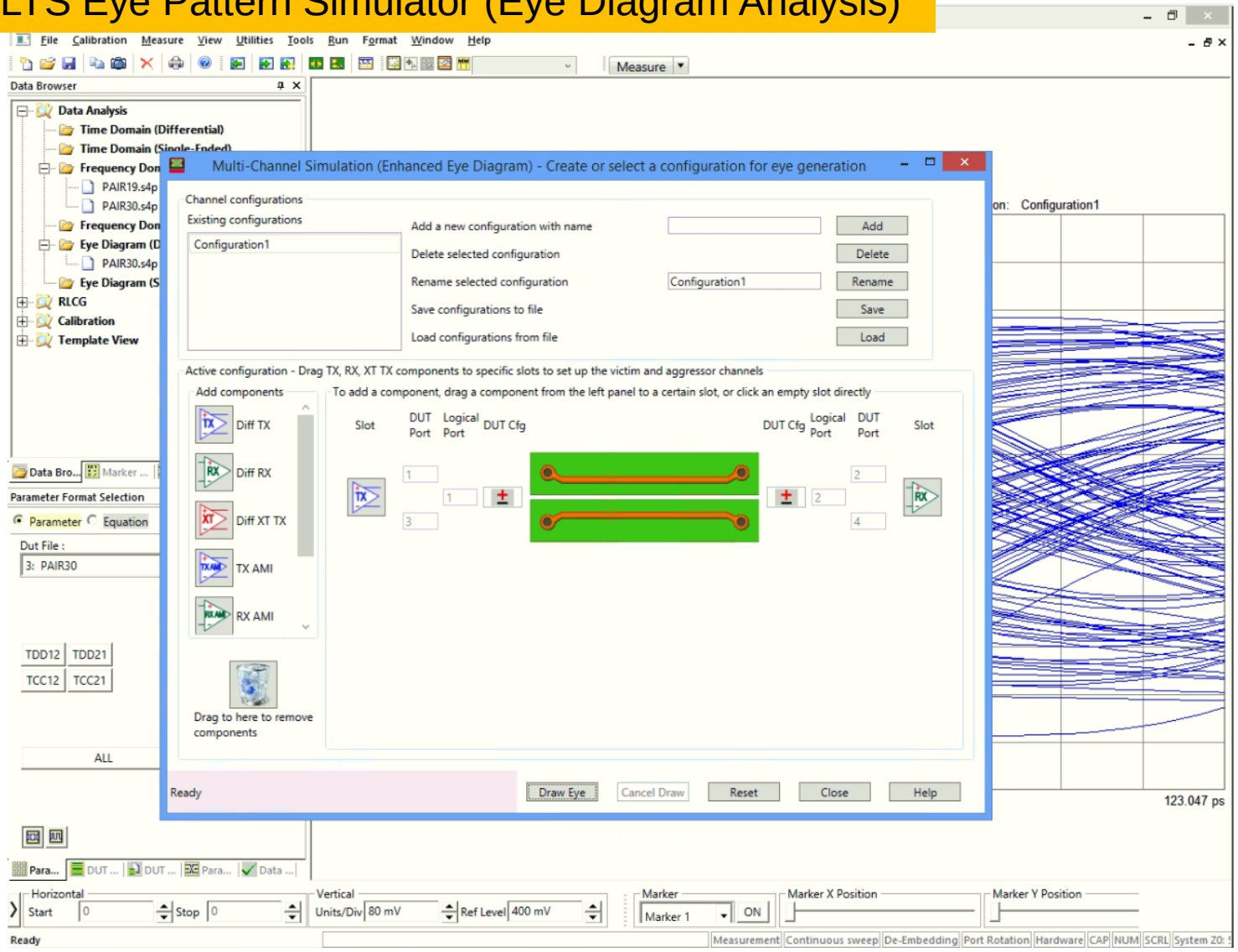
# PCIe Gen4 Case Study
## Equalizer Simulation on ADS

But any easy way to find proper equalizer setting to set or to start with?

# PCIe Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

PLTS Eye Pattern Simulator (Eye Diagram Analysis)

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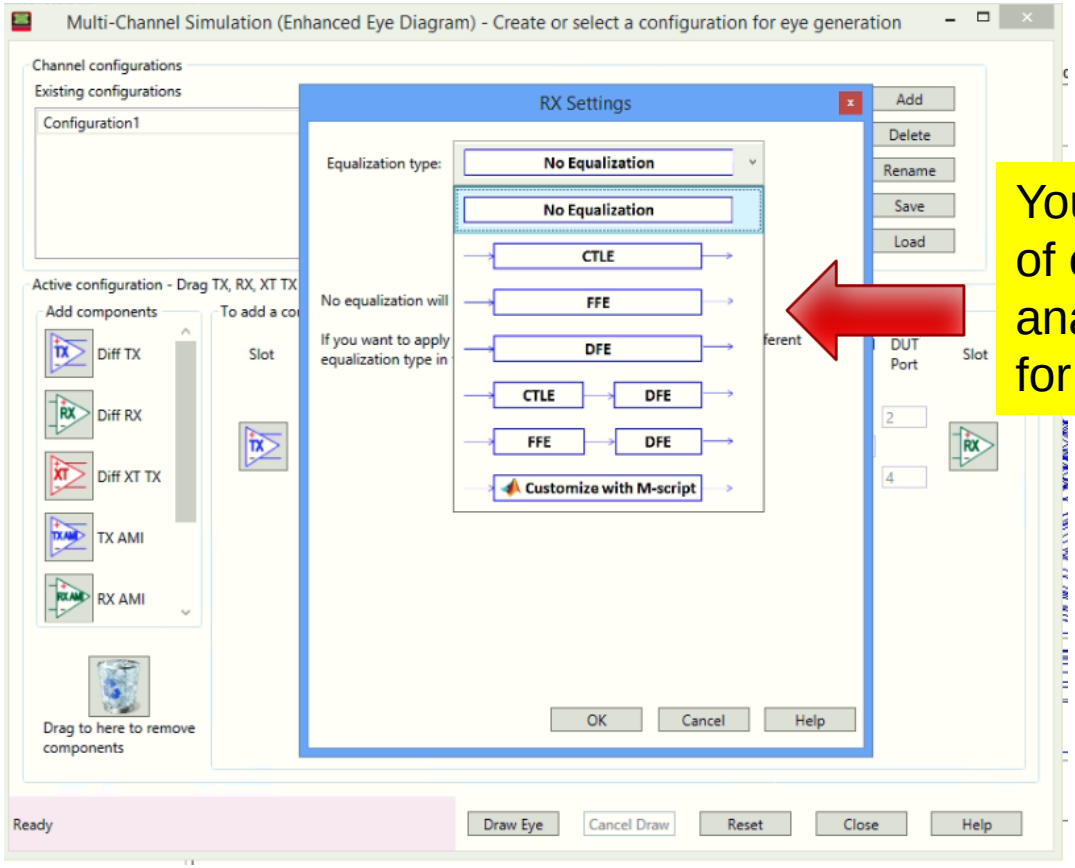
# PCIe Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

### Equalizer Optimization in PLTS Eye Simulator




You can choose the combination of equalizers and PLTS will analyze optimized EQ parameter for the channel.

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# PCIe Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

### Optimization Process (1)

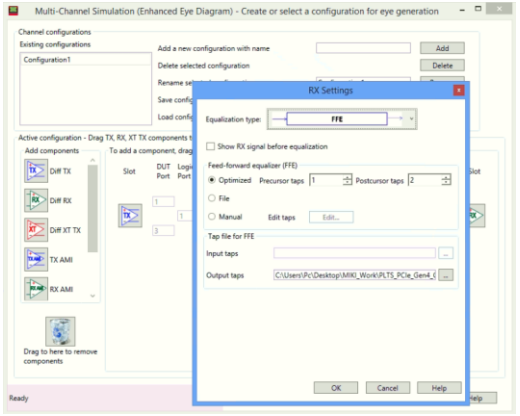
Only FFE is chosen to see what FFE setting is required for the channel. After running the optimization for FFE PLTS gave following parameters for highest Loss ISI.

Pre-Cursor : 0.03

Post Cursor : 0.80

What we leaned from PLTS's feedback is that pretty large compensation for post-cursor is required and the compensation for pre-cursor is not needed.

However, TX FFE pre-set in PCIe spec doesn't have such a strong setting. The strongest one for post-cursor is preset "P0" so P0 is set for TX FFE.




| Preset # | Preshoot (dB) | De-emphasis (dB) | c-1 | c+1 | Va/Vd | Vb/Vd | Vc/Vd |
|---|---|---|---|---|---|---|---|
| P4 | 0.0 | 0.0 | 0.000 | 0.000 | 1.000 | 1.000 | 1.000 |
| P1 | 0.0 | -3.5 ± 1 dB | 0.000 | -0.167 | 1.000 | 0.668 | 0.668 |
| P0 | 0.0 | -6.0 ± 1.5 dB | 0.000 | -0.250 | 1.000 | 0.500 | 0.500 |
| P9 | 3.5 ± 1 dB | 0.0 | -0.125 | 0.000 | 0.750 | 0.750 | 1.000 |
| P8 | 3.5 ± 1 dB | -3.5 ± 1 dB | -0.125 | -0.125 | 0.750 | 0.500 | 0.750 |
| P7 | 3.5 ± 1 dB | -6.0 ± 1.5 dB | -0.100 | -0.200 | 0.800 | 0.400 | 0.600 |
| P5 | 1.9 ± 1 dB | 0.0 | -0.100 | 0.000 | 0.800 | 0.800 | 1.000 |
| P6 | 2.5 ± 1 dB | 0.0 | -0.125 | 0.000 | 0.750 | 0.750 | 1.000 |
| P3 | 0.0 | -2.5 ± 1 dB | 0.000 | -0.125 | 1.000 | 0.750 | 0.750 |
| P2 | 0.0 | -4.4 ± 1.5 dB | 0.000 | -0.200 | 1.000 | 0.600 | 0.600 |
| P10 | 0.0 | Note 2. | 0.000 | Note 2. | 1.000 | Note 2. | Note 2. |

TX FFE Preset (P0)

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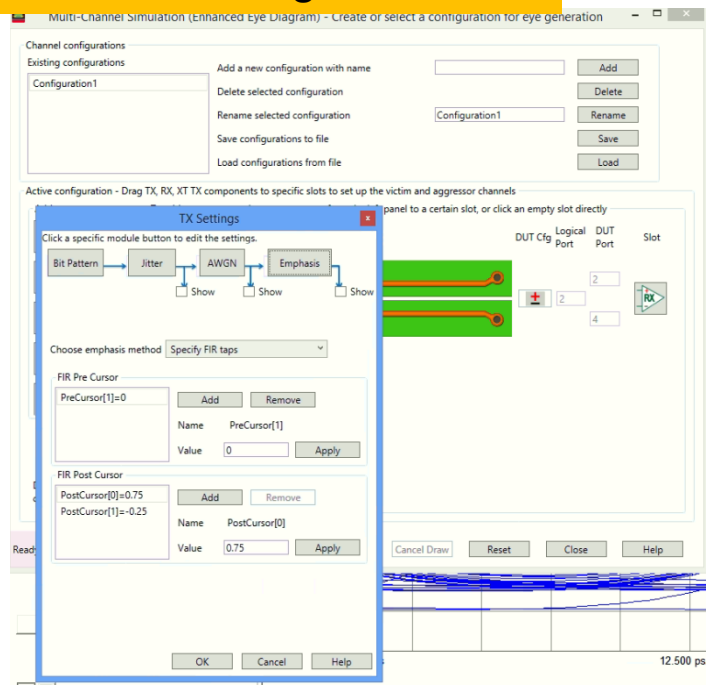
# PCIe Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

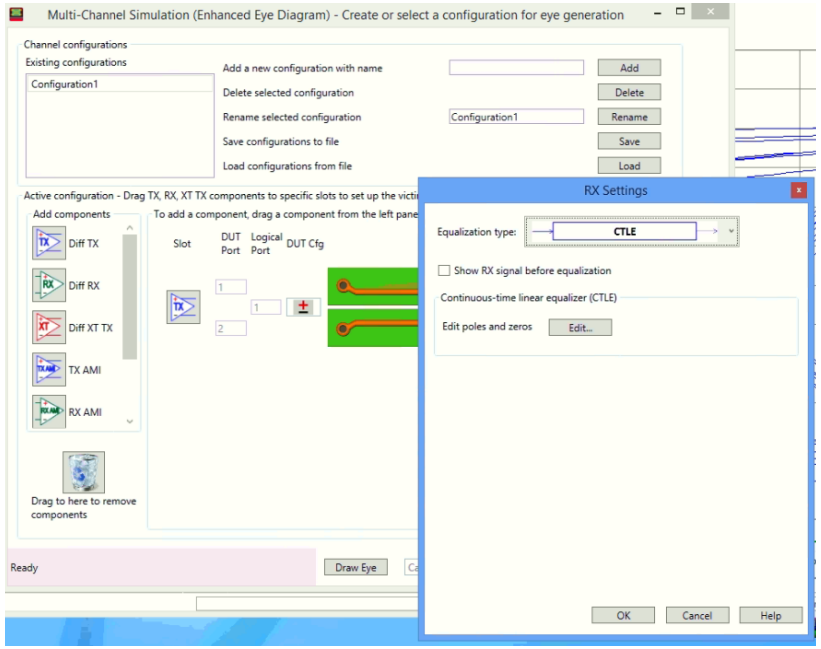
## Optimization Process (2)

P0 is the strongest TX FFE for post cursor. But it is not enough to compensate bad effect in post-cursor compared to what PLTS suggested in the analysis. Another equalization is needed so we enabled CTLE on PLTS Eye Simulator in addition to TX FFE (P0).

TX FFE Setting Window




RX CTLE Setting Window

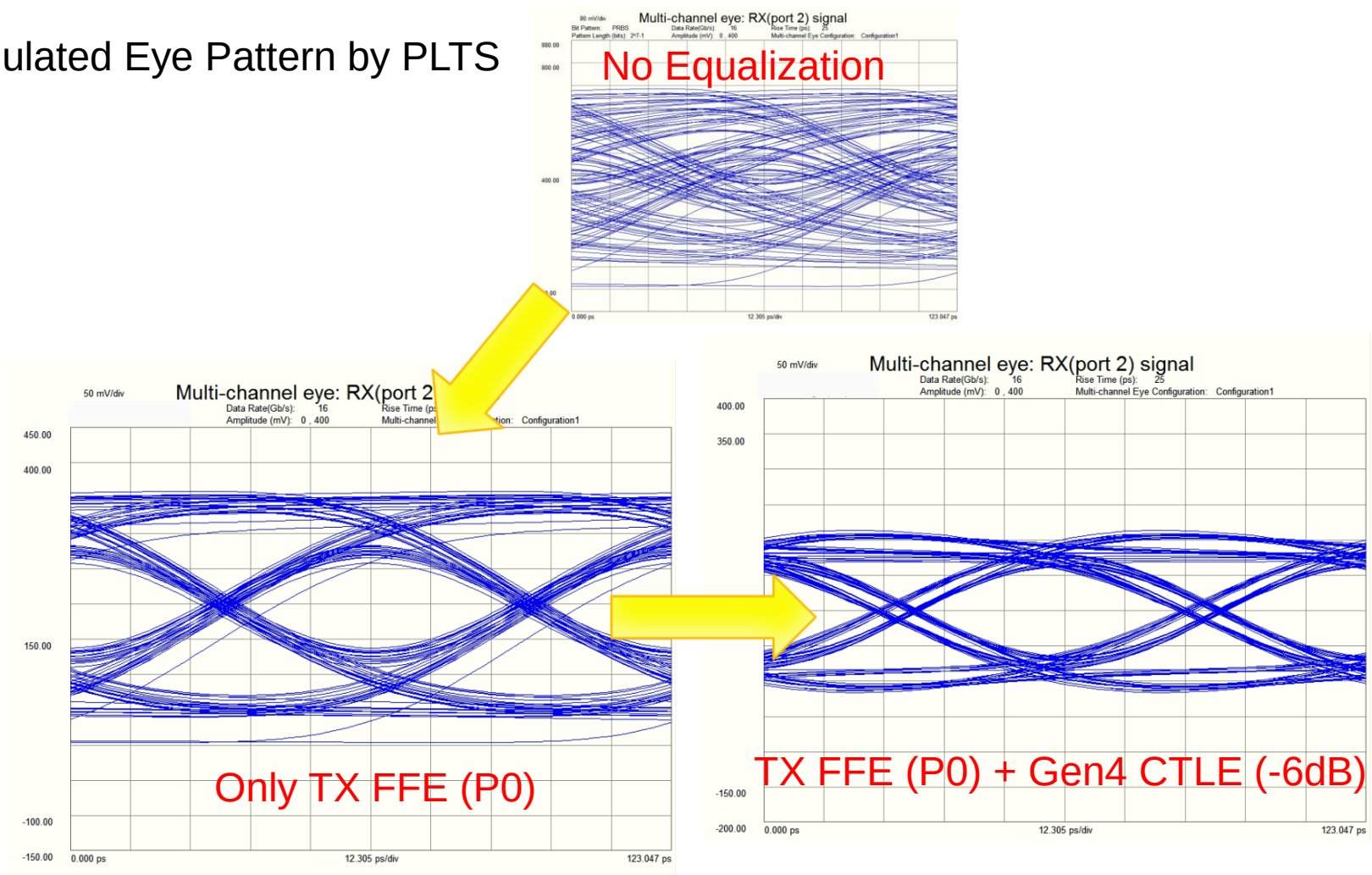



You can configure PCIe Gen4 CTLE.

# PCIE Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

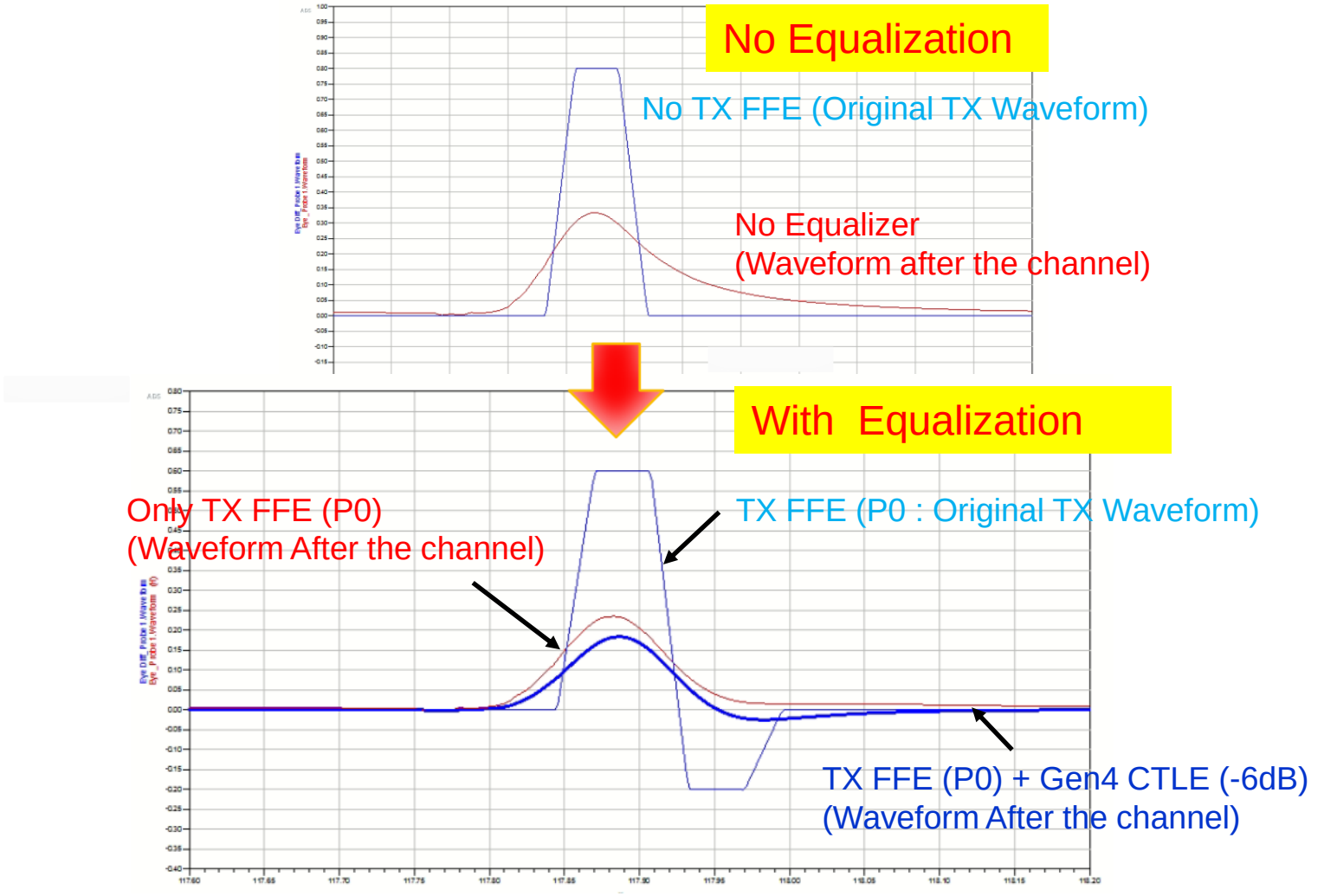
Simulated Eye Pattern by PLTS



# PCIe Gen4 Case Study

## Equalizer Optimization using Keysight PLTS

Simulated Pulse Response by ADS

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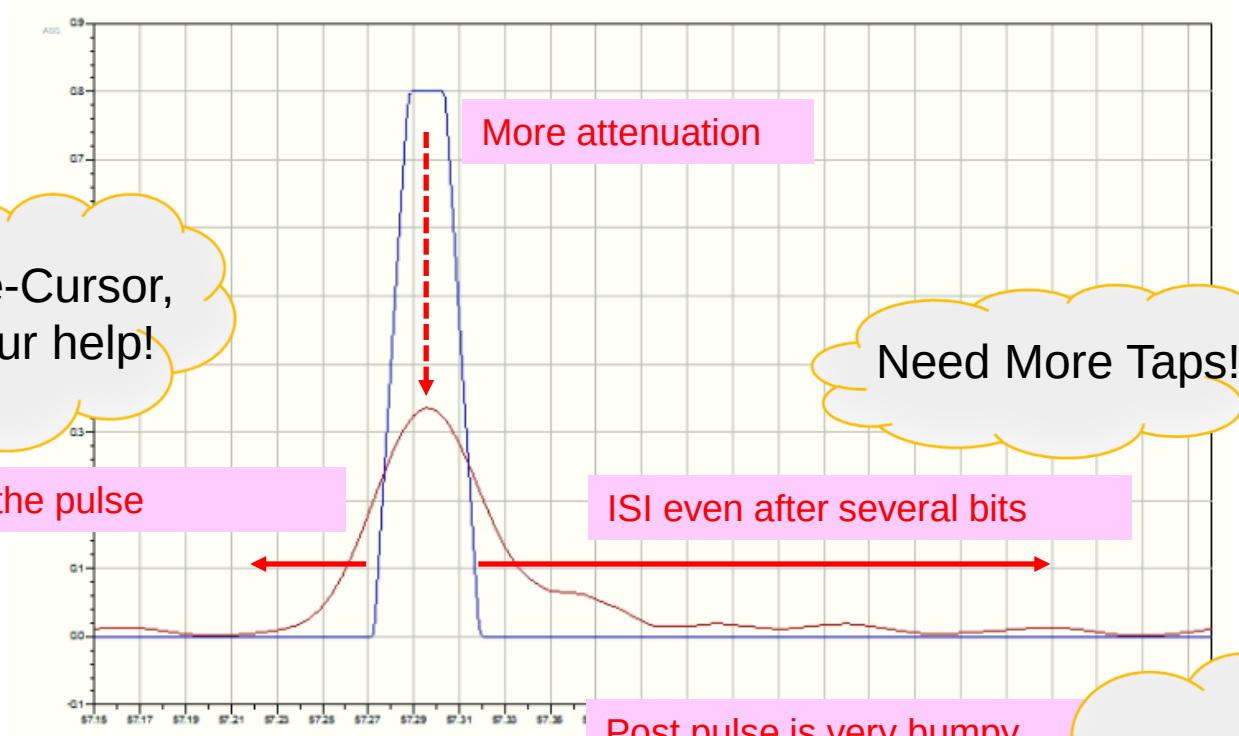
# PCIe Gen4 Case Study

## Are you ready for the challenge of PCI Express Gen5?

32Gbps Pulse Response

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# PCIe Gen4 Case Study
## Summary

1. Dynamic Equalization is available for the PCI Express Link. But it is important to make sure that the system is within the capability of PCIe Equalization.

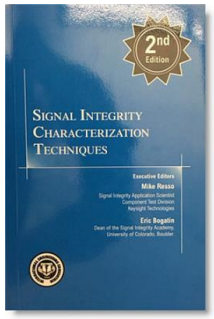
2. Pulse Response Analysis is an effective way to understand channel characteristics and required equalizer.

3. Eye simulation is an easy way to simulate the effect of the equalizer.

4. Keysight PLTS equalizer optimization is very useful to find proper equalizer setting to start with or set to.

# Questions?

# Resources




- Physical Layer Test System Home: www.keysight.com/find/plts
- Digital Interconnect Test System: www.keysight.com/find/diref
- Free Signal Integrity Book: www.keysight.com/find/RessoBook

- Latest Keysight PathWave ADS: www.keysight.com/find/eesof-ads-latest-downloads
- Signal Integrity Workshop: https://events.keysight.com/profile/39388

S-parameters: Signal Integrity Analysis in the Blink of an Eye

https://tinyurl.com/ycmbvbgx


https://tinyurl.com/y9wah5ak

# Thank you for your time!


Quintin Anderson, Co-Founder & COO
qanderson@graniteriverlabs.com
+1-408-627-7608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