PCI Express® 5.0 and the Road to PAM4

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Presenters

Hiroshi Goto has over 25 years of experience as a high speed and optical Engineer at Anritsu Company holding a variety of positions including Design Engineer, Product Marketing Engineer and currently high speed and optical Product Manager and Business Development Manager. Mr. Goto holds a Bachelor's degree in Physics from Aoyama Gakuin University. He resides in the Dallas area and has authored numerous industry application notes and white papers and frequently speaks on the topic of signal integrity.

Darren Gray is Engineering Fellow of GRL, based in GRL's Santa Clara headquarters where he supports test programs for a wide breadth of high-speed customer designs, and serves as global product manager for GRL's PCIe Express Receiver Test Automation Solutions. Darren spent over 8 years at Tektronix/Synthesys Research where he was a senior application engineer, and before that was an engineer for JDSU. Darren is an expert in receiver testing and optical transceiver characterization, and his wide-breadth of expertise in high-speed serial data standards include IEEE 802.3 Ethernet, PCI Express, USB, DisplayPort, and MIPI.

Eugene Sushansky is Director of Global Engineering at GRL headquarters in Santa Clara where he manages all technical aspects of GRL's global testing activities and represents GRL on the PCI-SIG and other standards groups. Prior to GRL, Eugene spent over two years at Toshiba America Electronic Components (TAEC) where he was a Senior Hardware Engineering Validation Manager, and over 13 years at PLX Technology (now Broadcom) as Senior Design Manager. Eugene is an expert in silicon and discrete component characterization, as well as SERDES and discrete components validation. He has extensive expertise in electrical characterization of PCI Express, SAS, SATA, and other high-speed data standards.

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Who We Are

Granite River Labs (GRL)

- Recognized World Leader in Test Services and Automation Solutions for Connectivity and Charging.
- Founded 2010, HQ in Silicon Valley, 8 labs around the world, ~200 employees.
- GRL develops RX Test Automation Solutions for the Anritsu MP1900A, compatible with Tektronix & Keysight scopes. Our current portfolio includes:
  - PCI Express 5.0/4.0/3.0
  - USB 3.2 10G/5G
  - SAS-4
  - Thunderbolt 3
  - DisplayPort 1.4
  - IEEE 802.3
  - Custom

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- Anritsu is a global provider of innovative communications test and measurement solutions for 120 years. Anritsu's "2020 VISION" philosophy engages customers as true partners to help develop wireless, optical, microwave/RF, and digital instruments, as well as operation support systems for R&D, manufacturing, installation, and maintenance applications. Anritsu also provides precision microwave/RF components, optical devices, and high-speed electrical devices for communication products and systems.
- The company develops advanced solutions for 5G, M2M, IoT, as well as other emerging and legacy wireline and wireless communication markets. With offices throughout the world, Anritsu has approximately 4,000 employees in over 90 countries.

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Agenda

- Evolution of PCI Express Technology
- The Challenge of PCIe Gen 5: NRZ at 32 GT/s
- PCIe Base vs. CEM Testing
- PCIe Transmitter Test Overview
- PCIe G4/G5 Receiver Test
  - Calibration
  - Link EQ Test
  - Jitter Tolerance Test
  - TX LEQ Response Time
- Transition to PCIe 6.0: 64GT/s PAM4 Design and Test Considerations
- Q&A

We will focus on the PCI Express physical layer.

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The Evolution of PCI Express

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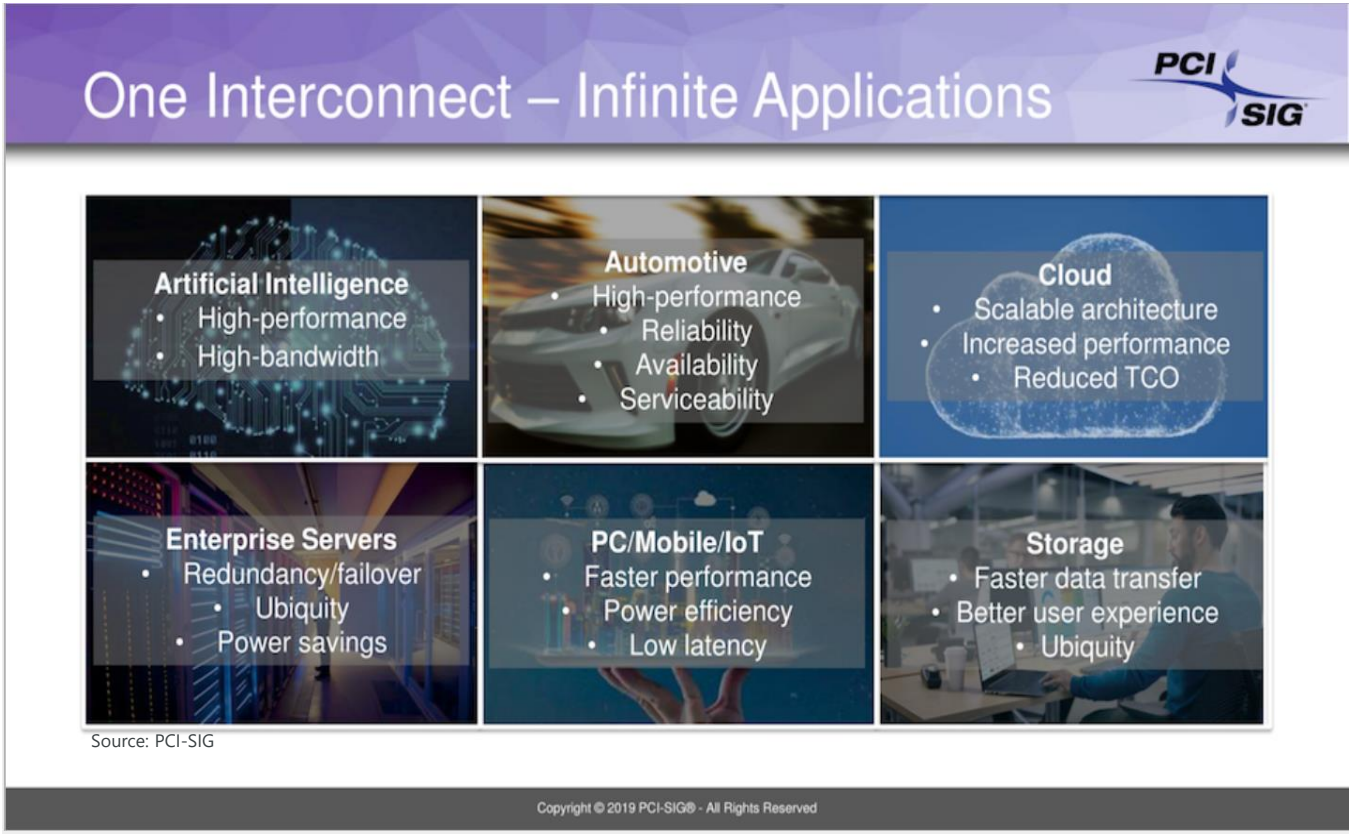
Higher Data Rates Being Driven by Many Applications Using PCIe as the Interconnect



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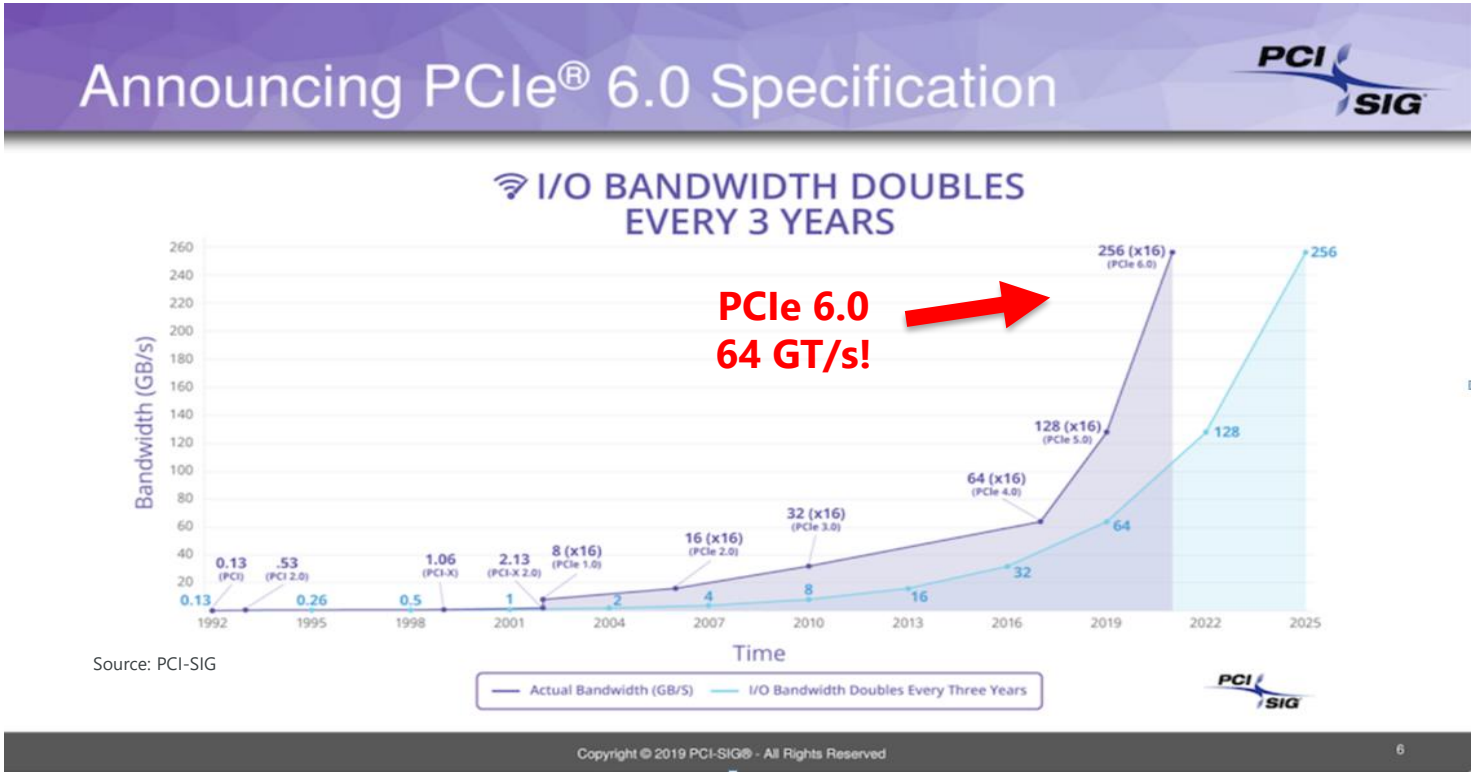
PCIe Continues to Push for Higher Data Rates



PCI-SIG continues to push for higher data rates, doubling every 2-3 years!

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A Closer Look at PCIe Data Rates: Gen1 thru 6.0

PCIe Rev	Modulation	Link Transfer Rate	Link Data Rate	Encoding	Specification Release Year
1.0	NRZ	2.5 GT/s	2 Gb/s	8b/10b	2003
2.0	NRZ	5GT/s	4 Gb/s	8b/10b	2007
3.0/3.1	NRZ	8GT/s	~8 Gb/s	128/132	2010
4.0	NRZ	16GT/s	~16 Gb/s	128/132	2017
5.0	NRZ	32GT/s	~32 Gb/s	128/132	2019
6.0	PAM4	64GT/s	~64 Gb/s	128/132*	Est. 2021

- Data rate has consistently doubled with each spec release.
- NRZ modulation prevails through Gen 5, then PAM4 starting with 6.0.

*6.0 includes low-latency Forward Error Correction (FEC) encoding with additional mechanisms to improve bandwidth efficiency.

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Today: PCIe 4.0 vs. PCIe 5.0

	PCIe 4.0	PCIe 5.0
Data rate	16 GT/s	32 GT/s
Modulation scheme	NRZ	
Bit encoding scheme	128B/130B	
Channel loss	-27 to -30 dB	**-34 to -37 dB**
Common clock (RefClk) phase jitter	≤ 0.5 ps rms	**≤ 0.15 ps rms**
Transmitter Equalization	3-Tap FFE	
Ref. receiver CTLE	2-pole, 1-zero, gain : -1 to -9 dB	**4-pole, 2-zeros, gain: -5 to -15 dB**
Ref. receiver DFE	2-Tap DFE	**3**-Tap DFE
Minimum Post Eq EH12	15 mV	15 mV
Minimum Post Eq EW12	18.75 ps	**9.375 ps**
BER	≤ 10^{-12}	
Eye at Receiver input	Closed	

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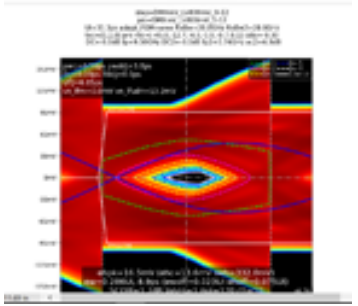
The Challenges of NRZ at 32 GT/s

- **Up to 36 dB of loss (@ 16GHz) at the prescribed BER ≤ 1E-12**
- **Most 30+ GT/s standards use PAM4, PCIe 5.0 sticks with NRZ**
  - PCIe 6.0 will use PAM4 at 64 GT/s (more in later slides)
  - Interesting that NRZ modulation was chosen for this data rate given other high-speeds have switched to PAM4 for data rates above 25G.
- **Post-equalization eye-opening as low as 10-15 mV with calibrated stresses (RJ, SJ, ISI, Random Noise, Sinusoidal Interference)**
  - Re-timers for loss > 36 dB
- **PCIe Gen 4.0 and PCIe Gen 5.0 have *very similar* compliance tests and channel configuration:**
  - Stricter requirements in connector loss and reflections
  - Small improvements in equalization
- **But don't be fooled! Going from 16 → 32 GT/s is difficult.**



PCIe 5.0 RX Stressed Eye
(Base Spec)

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PCIe Base vs. CEM Testing

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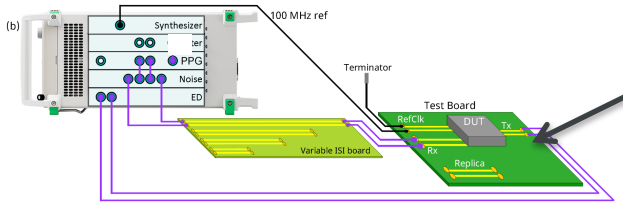
PCIe Standards Terminology

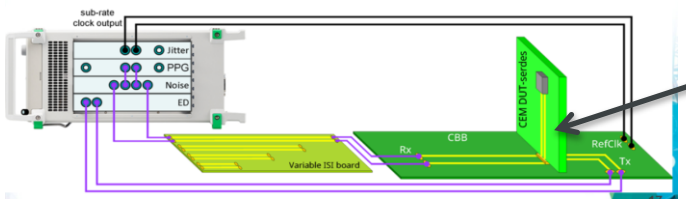
PCIe Standards: Follow the appropriate spec for your design.

Base Specification ➔ Contains the technical details of the architecture, protocol, Link Layer, Physical Layer, and software interface. Defines electrical conformance at the **Chip level**. No official compliance program or test fixtures.



User-defined breakout board for Base (chip-level) testing

CEM (Card Electromechanical) Specification ➔ Defines mechanical requirements and electrical compliance for **completed product**, ie Component (End point, Bridge/Switch, Root Complex), Add-in Card or System (aka "Host"). Test fixtures and test-tools well-defined and supplied by PCI-SIG. Testing and compliance governed by Compliance Test Specification (CTS).



PCI-SIG Test fixtures required for Add-In Card and System testing

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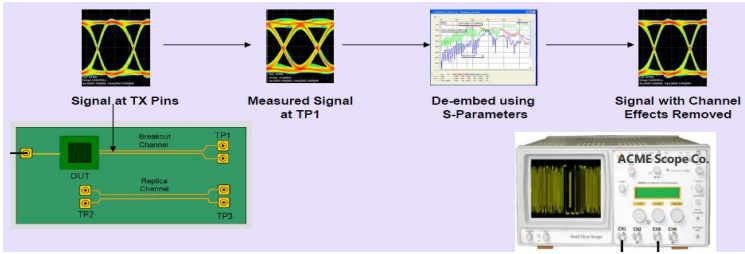
Base vs CEM Spec Testing

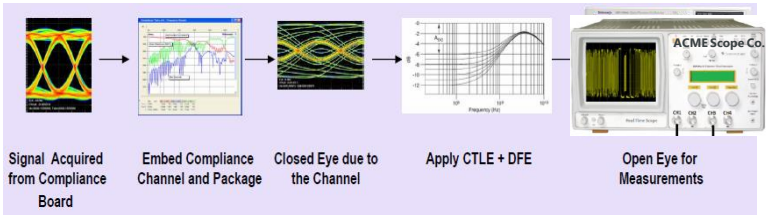
- **Base and CEM testing are similar but differ significantly in test point definition, methodology, and degree of formality.**
- **Base Specification Measurements are defined at the pins of the Transmitter and Receiver.** Signal access at the pins is often not possible.
  - No official Base Specification compliance program.

Base Spec Test Flow (TX example)



- **CEM Spec Measurements are defined at of the CTS test points.**
  - All official PCI-SIG integrators list testing is done to the CEM spec.
  - Requires embedding the compliance channel and package, as well as application of the behavioral equalizer.
  - SigTest analysis software is required to perform TX waveform post-processing, RX stressed eye calibration, and compliance measurement calculations.
    - TE vendors' packed automation software tools incorporate SigTest.

CEM Spec Test Flow (TX example)



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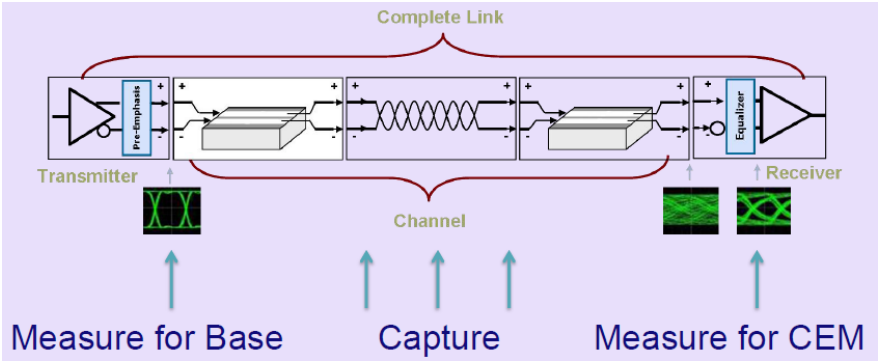
PCIe Base vs CEM – What Test Spec to Follow?

- **Final product developer: CEM spec.**
- **Chip developer - GRL's advice:**
  - If your chip (or IP) will be used in multiple final product designs, test to the Base Spec.
  - If your chip will be used in only one final product, then just testing to the CEM may be OK…
  - BUT GRL recommends testing your chip to the Base Spec first. CEM spec assumes that the chip is Base spec compliant. Base spec requirements are challenging.



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PCIe Transmitter Test Overview

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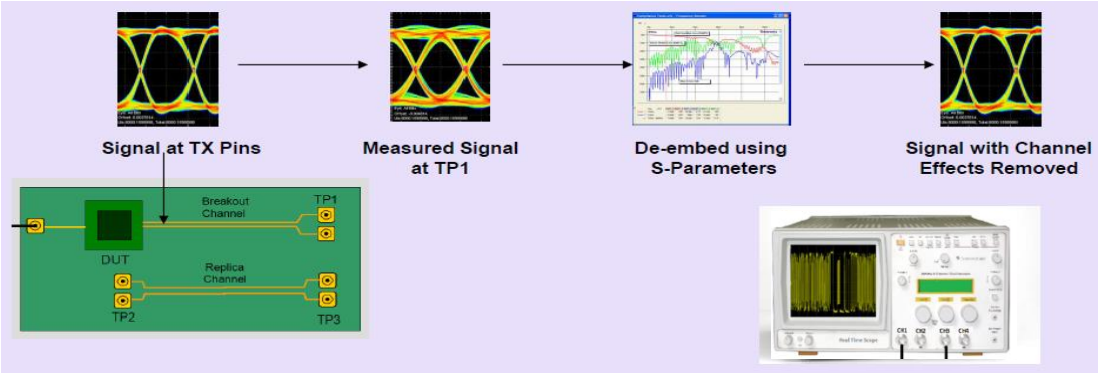
Base Spec Testing – Transmitter (TX)

- For TX testing, de-embedding is required to see what the signal looks like at the pins of the chip, without the added effects of the channel.
  - A custom Evaluation Board with coaxial connectors and replica channel is needed.
  - PCI-SIG specific test board not needed (but *is* needed for RX Base spec testing starting with 4.0)
  - Scope vendors provide tools for creating the automated channel de-embedding and signal post-processing.
- Key Measurements:
  - PCIe Transmitter Eye and Jitter
  - PCIe Preset (P0-P10) Measurements
  - PLL



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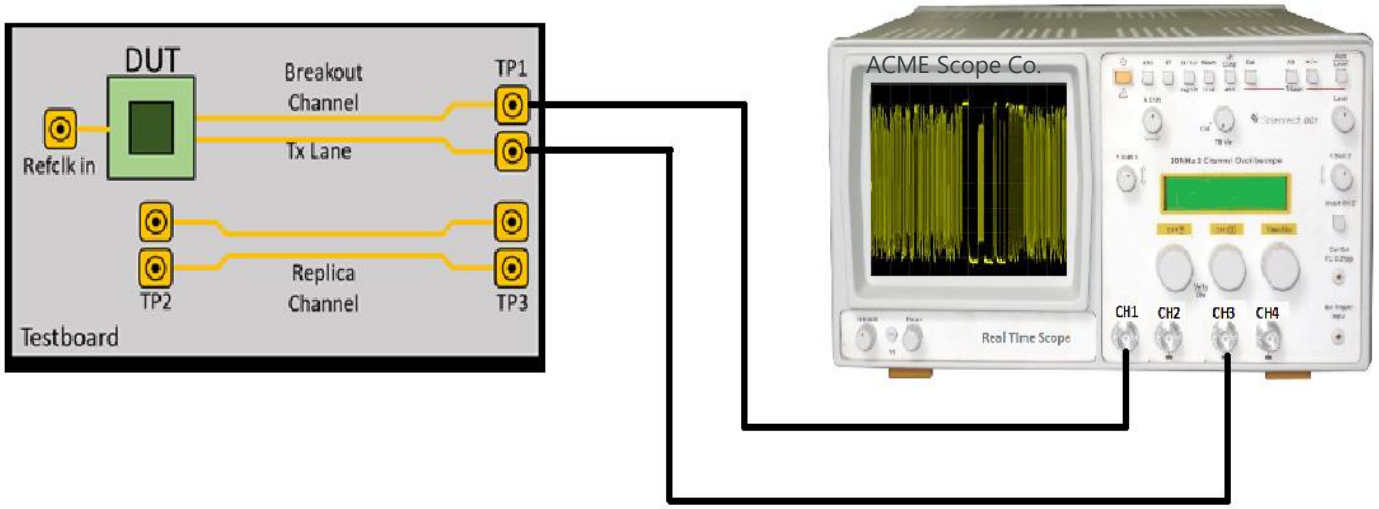
Base Spec Testing – Transmitter (TX)

PCIe Base Spec Test Setup – A closer look



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PCIe TX Base Spec Tests

Tests Category	Measurements
UI and Jitter	UI Time, T_{TX-UTJ}, $T_{TX-UDJDD}$, T_{TX-RJ}, $T_{TX-UPW-TJ}$, $T_{TX-UPWDJDD}$, DDj, $T_{TX-CH-UPW-RJ}$, $T_{TX-CH-UPW-DJ}$
Common Mode Voltage	$V_{TX-AC-CM-PP}$, $V_{TX-AC-CM-PP}$
Full Swing TX with no TxEQ & Min Swing during EIEOS for Full Swing	$V_{TX-CH-FS-NO-EQ}$, $V_{TX-CH-RS-NO-EQ}$, $V_{TX-EIEOS-FS}$, $V_{TX-EIEOS-RS}$
Pseudo Package Loss	$ps21_{TX}$
Differential Peak-to-Peak Tx Voltage	$V_{TX-DIFF-PP-FS}$, $V_{TX-DIFF-PP-RE}$
Tx Preset	P0 – P10

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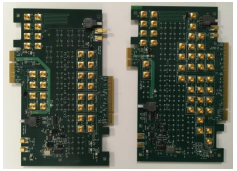
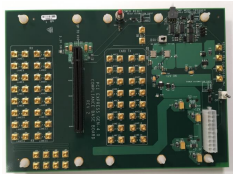
CEM Spec Testing – Transmitter (TX)

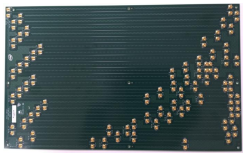
- Key CEM spec TX measurements:
  - PCIe Transmitter Signal Quality
    - Template Test (Eye Mask)
    - Jitter Measurements
    - Voltage Characteristic measurements
  - PCIe Preset (P0-P10) Measurements
  - PLL Measurements



CLB
(Compliance Load Board)



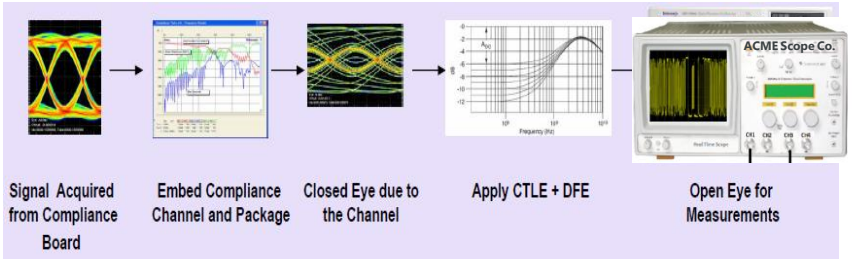
CBB
(Compliance Base Board)



ISI Channel

- Requires PCI-SIG official Test Fixture

- CEM test methodology entails embedding the compliance channel and package model



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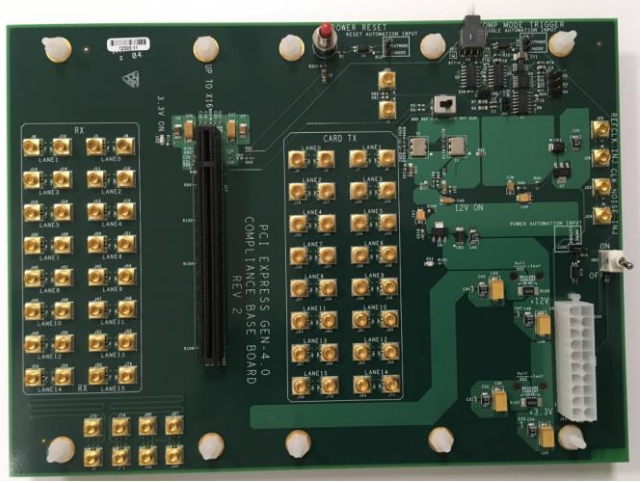
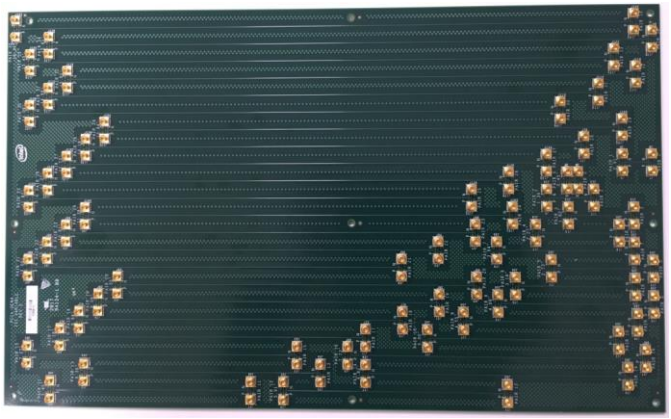
PCI Express CEM Specification Test Fixtures - A Closer Look

CLB
(Compliance Load Board)



CBB
(Compliance Base Board)

ISI Channel



PCI-SIG 4.0 Fixture Set
(5.0 fixtures under development)

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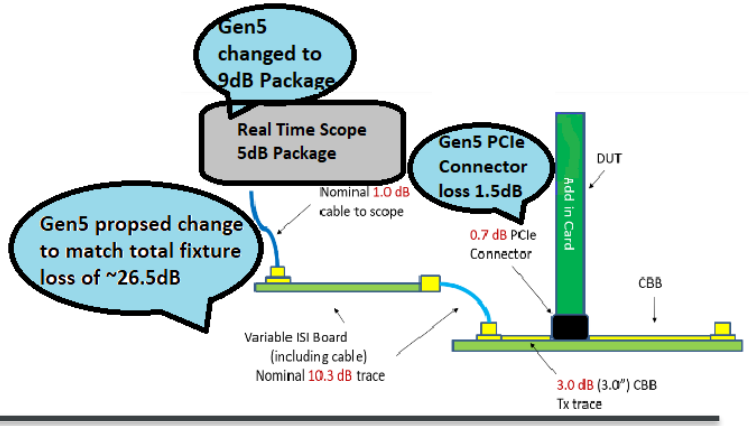
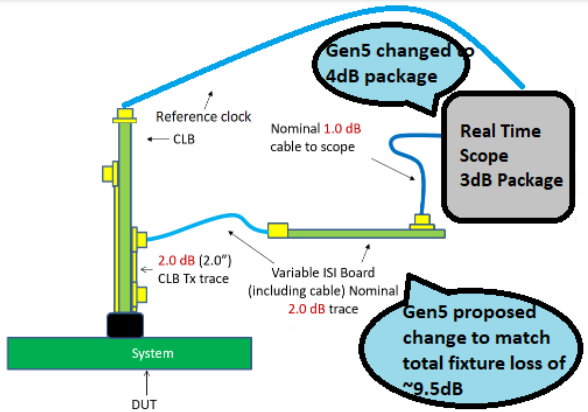
CEM Spec Testing – Transmitter (TX)

CEM Spec Add-In Card
TX Far-End Setup



CEM Spec System
TX Far-End Setup



Note: Above represent PCIe 4.0 CEM Setup
(PCIe 5.0 CEM changes shown in blue callouts)

PCIe 4.0/5.0 Receiver Test

- Calibration
- Link EQ test
- Jitter Tolerance test
- TX LEQ response time

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Object of RX Test

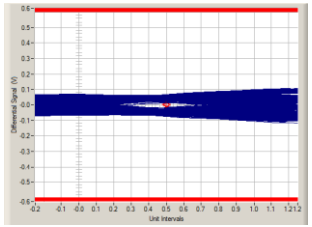
- DUT needs to make Link Equalization Training successfully under the specific stressed eye condition
  - ✓ Optimize the equalizer (Preset and CTLE)
  - ✓ Go to Loopback Status (Loopback Active Master)
  - ✓ BER 1E(-12)

RX LEQ Test Procedure

Steps of Receiver Testing

Step1: Calibration

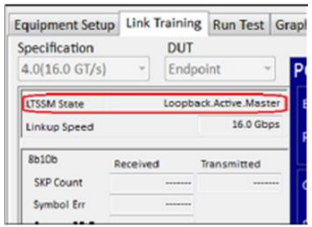
- Channel Loss by VNA
- Eye Amplitude, Preset, SJ and RJ by BERT and RTO
- DM-I and Eye Height/Eye Width by BERT and RTO

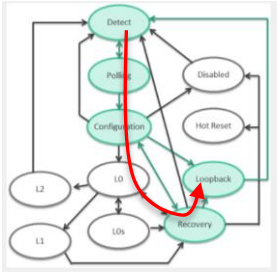


	Min	Max
EH	13.5 mV	16.5 mV
EW	18.25 ps	19.25 ps

Step2: Link Training

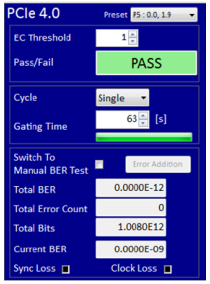
- Make DUT looped-back-mode by BERT through Recovery State.
- Troubleshooting

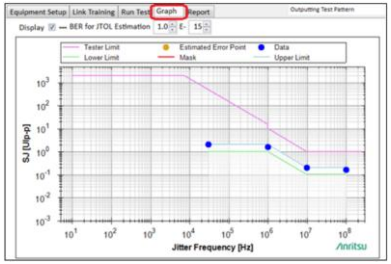




Step3: Measurement

- Checking BER <1E-12 with Stressed EYE (Mandatory)
- Jitter Tolerance Testing (Optional)





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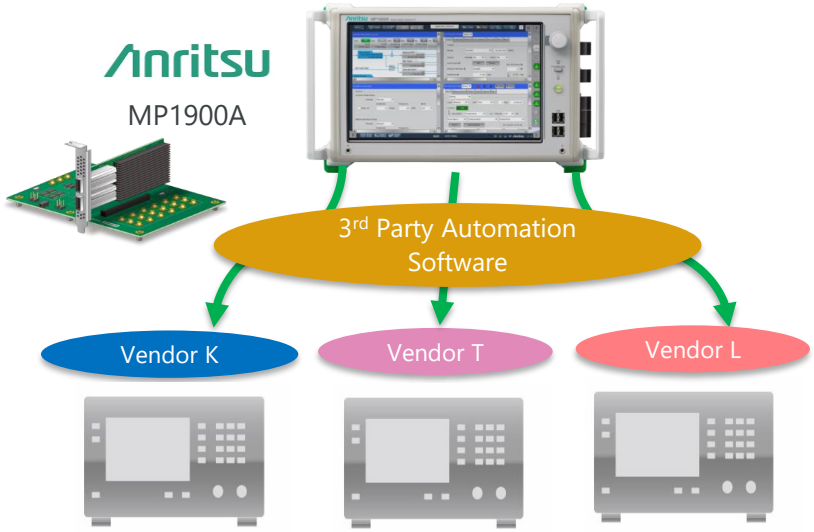
PCIe Tx LEQ/Rx Compliance Test

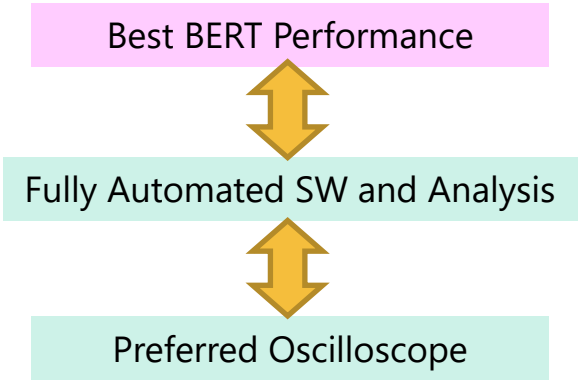
Combination of best-performance BERT MP1900A and preferred oscilloscope

Shorter test times and reduced investment cost

- Supports Combination with Lecroy/Tektronix/Keysight Real-Time Oscilloscopes (MOI available from SIG home page)
- Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- High-Expandability 32G Multichannel BERT for PCIe1 to 5



Customers' Real-Time Oscilloscopes



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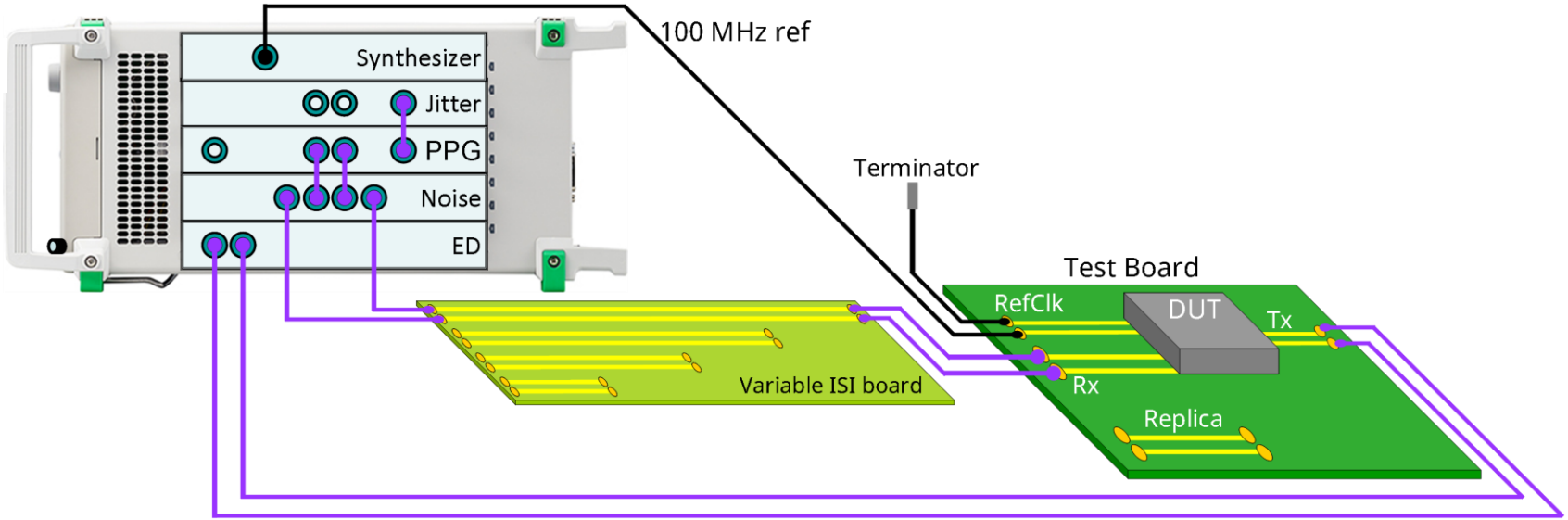
Block Diagram of RX LEQ Test

- MP1900A is ALL in One BERT
- No External Components are required for PCI G4/G5 LEQ test
  - PPG has Built-in Emphasis and ISI with Jitter, noise, and SSC injection
  - Error Detector has Build in CDR and CTLE with 10mV sensitivity



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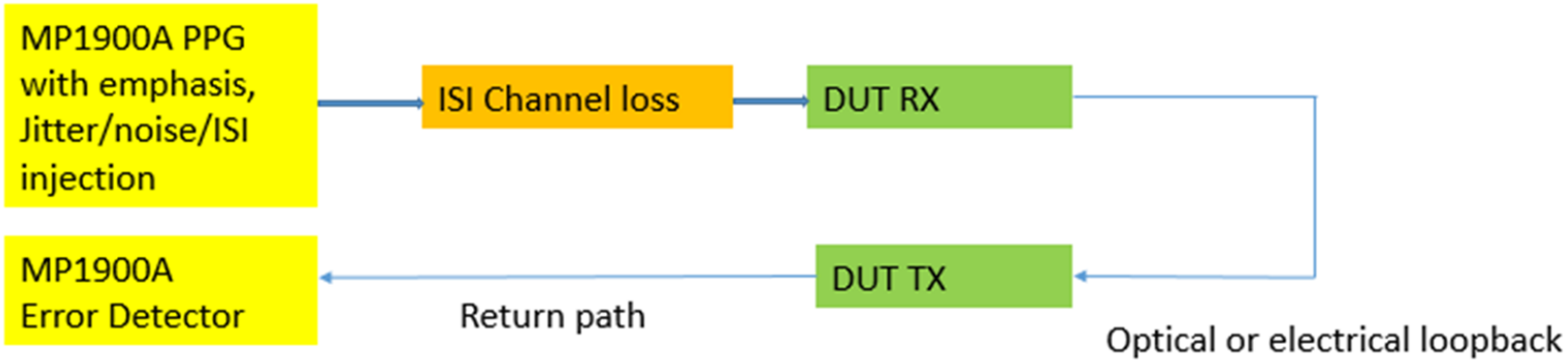
First Thing to do for Stable and Repeatable RX Tests

Establish the return path:

- First and most critical for Stable and Repeatable RX Test
- Minimize loss and ISI to isolate the error source
  - Ideally error free otherwise the best achievable BER



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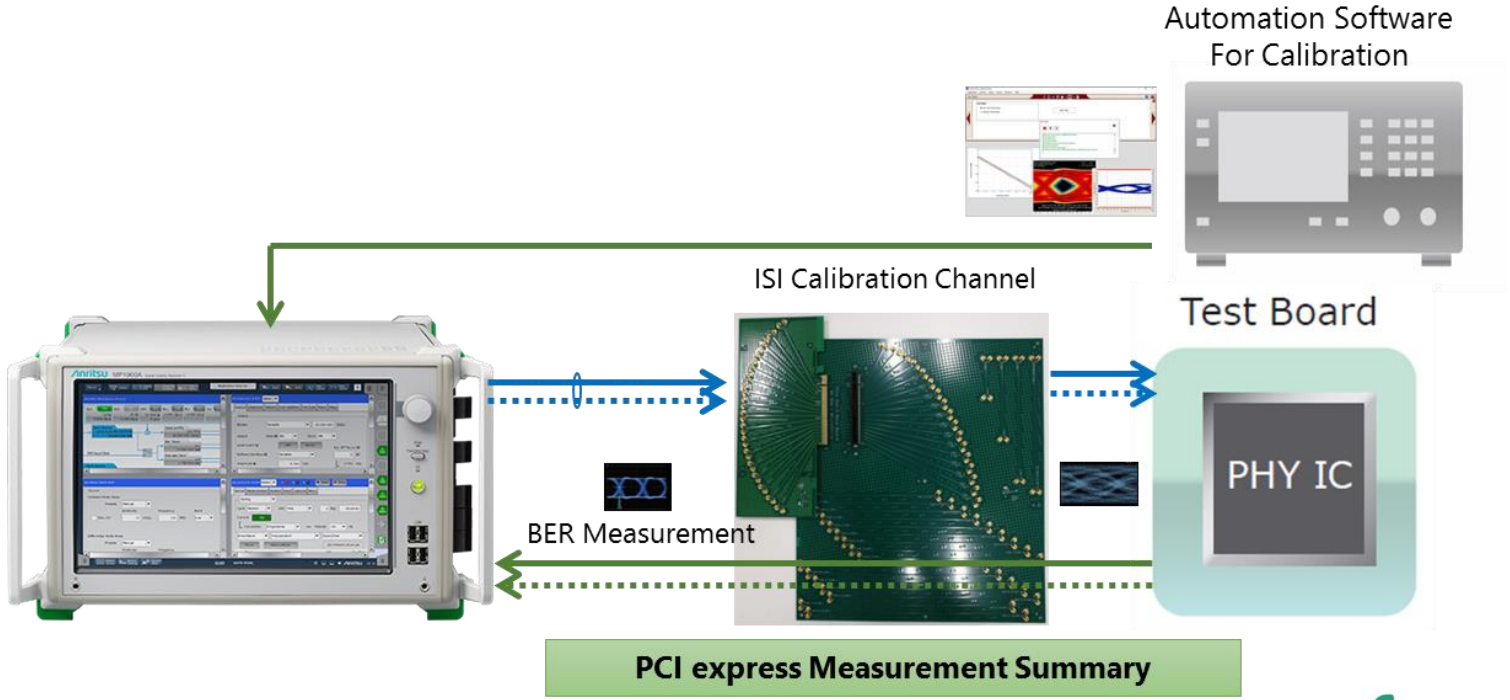
PCI Express Gen5 Rx Test Outline

PCI Express PHY IP Device Rx Test Sequence

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test



PCI express Measurement Summary

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PCI Express Gen5 Calibration Points (1/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

TP2 Stressed Eye Calibration

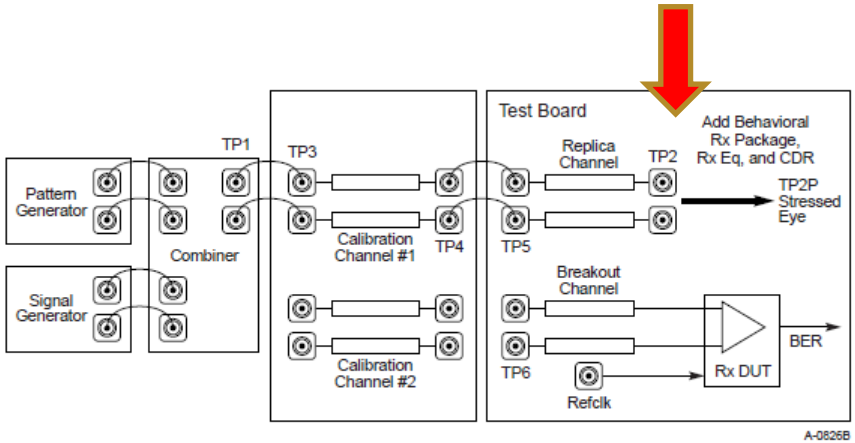

Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

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PCI Express Gen5 Calibration Points (2/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

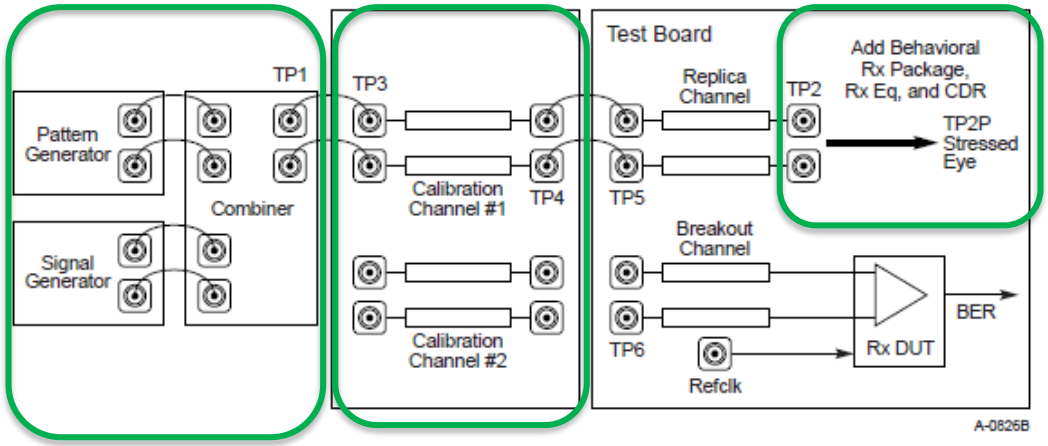

Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

MP1900A

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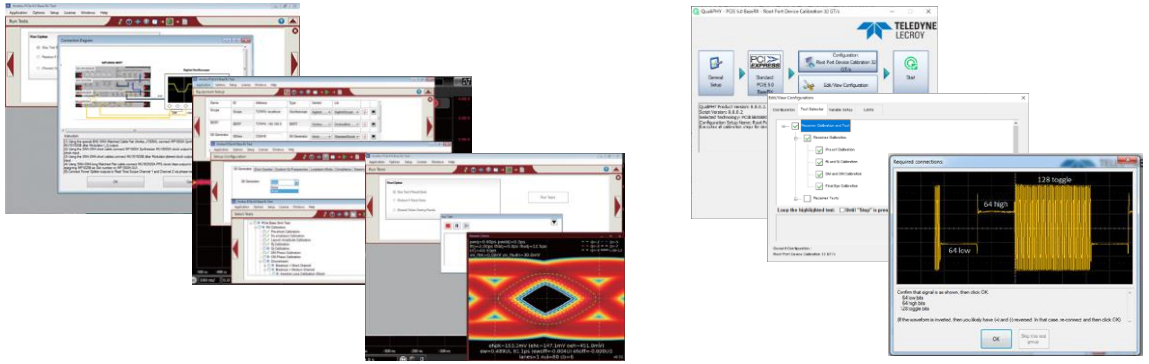
PCI Express Gen5 Calibration Points (3/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

Stress Signal Calibration

Automation Software GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx Features



Examples of Calibration Setting and Measurement Screens

One-touch Calibration of Stress Input Signal and Testing using Automation software

- Supports PCIe-Gen5 Rev1.0 Devices
- Executes Calibration of High-reproducibility Test Signal and Rx Test

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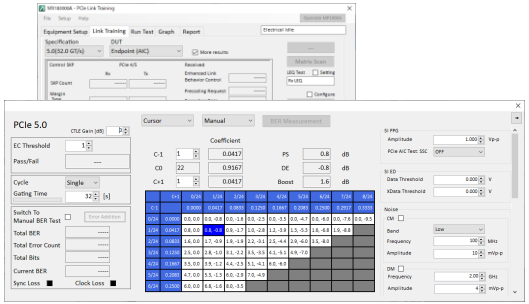
PCI Express Gen5 Link Training

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

Link Training using MX183000A-PL025



PCI Express Link Training Screen

PPG Pattern Control using MX183000A

- Screen Functions for Easy Setting of Measurement Conditions and Test Execution
- Controls PCI Express Device Status and Supports Logical Sub Block Evaluation
- 8B/10B, 128B/130B, Scramble SKIP Insertion

Item	MX183000A-PL025 Specification
Supported Standard	Gen5 (32 GT/s)
Test Pattern	Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31)
LTSSM State	Transition to Detect, Polling, Configuration, Recovery, Loopback
Loopback Through	Configuration, Recovery
TS Set Pattern	SKP Insertion/Filtering, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling

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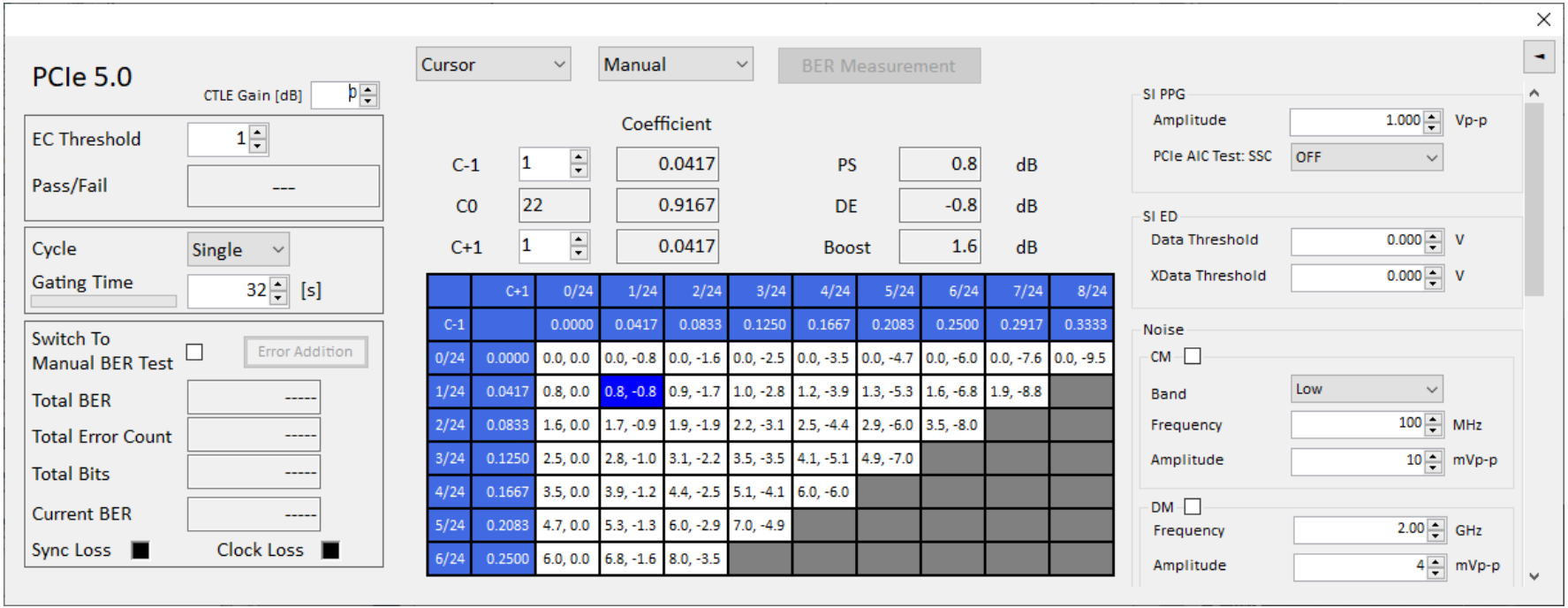
Troubleshooting Using Cursor



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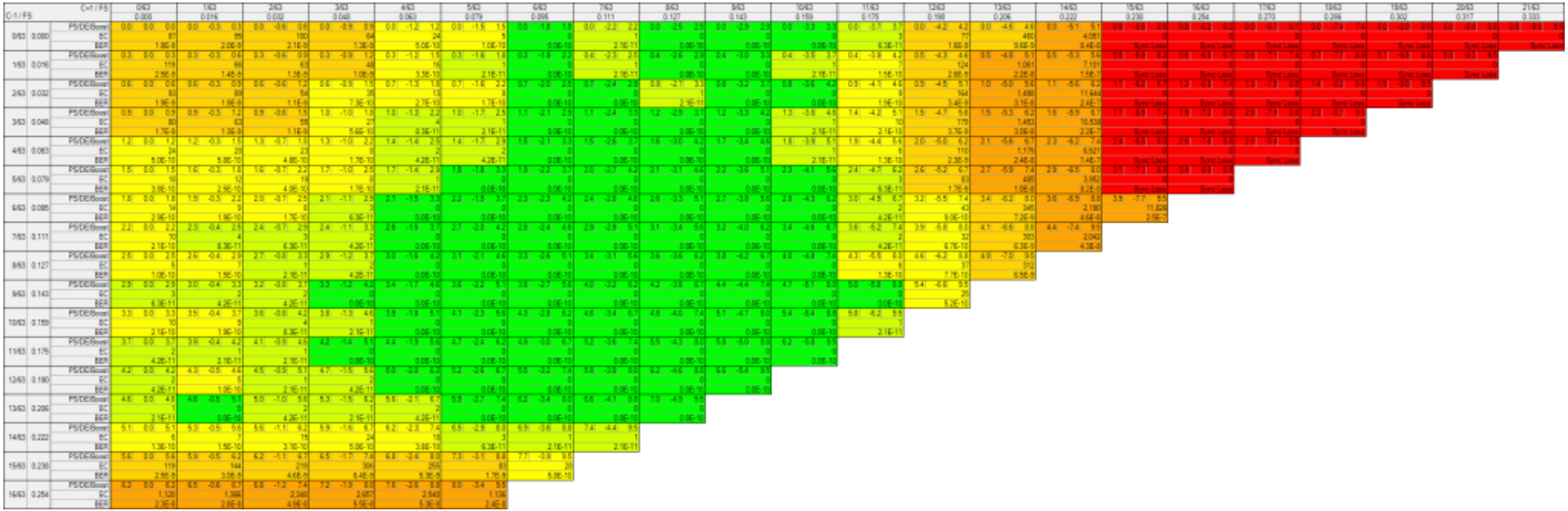
Auto Cursor Matrix Scan



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PCI Express Gen5 Link Training

Added and Changed Several Parameters Affecting Link Training

Requirement	Description
Enhanced Link Behavior Control	Added TS parameter for LEQ to PCIe 5.0
Precoding	Receiver can request precoding from transmitter to operate at data rates of 32.0 GT/s or higher
SKP OS/EIEOS/EIEOSQ	SKP OS Identifier changed from AAh to 99h 32G EIEOS has same frequency compared to 16G Two consecutive EIEOS for data rates of 32.0 GT/s
MCP 5.0	EIEOS changed to EIEOSQ

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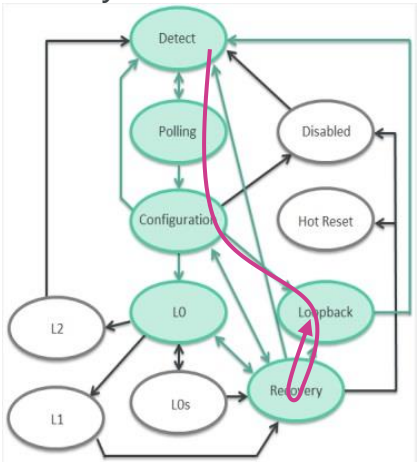
PCI Express Gen5 Link Training

Stress Signal Calibration → **Transition to Loopback Status** → Stress Signal Input Test

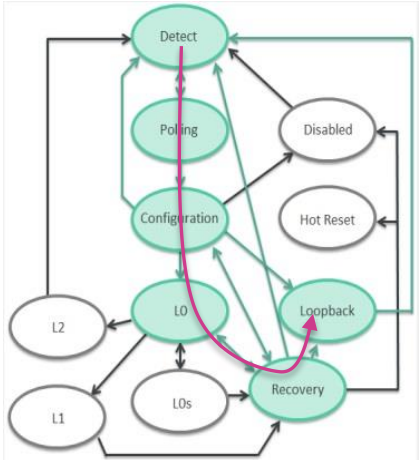
Enhanced Link Behavior Control

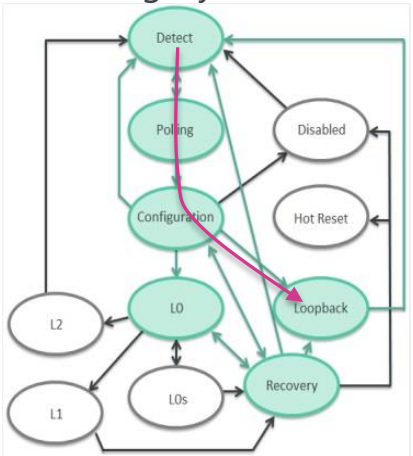
Defined option to perform Recovery Equalization when selecting loopback through configuration route

Only for 32 GT/s (New)



8, 16, and 32 GT/s (Legacy)





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PCI Express Gen5 Link Training

- Precoding
  - At 32.0 GT/s, an optional precoding mechanism is provided, which receivers can enable optionally, to reduce the risk of DFE-related error bursts in high transition data patterns causing silent data corruption.
  - The receiver can request precoding from its transmitter for operation at data rates of 32.0 GT/s or higher.
  - Precoding can be applied independently to either Tx or Rx

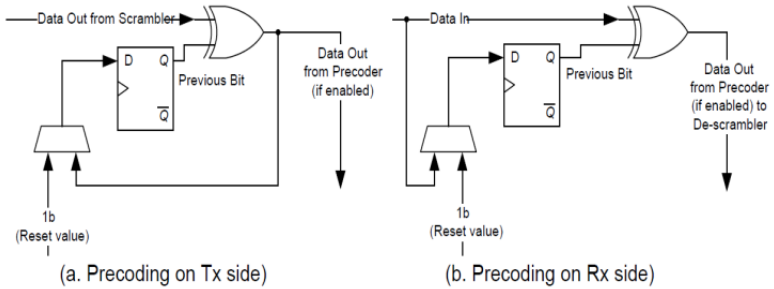


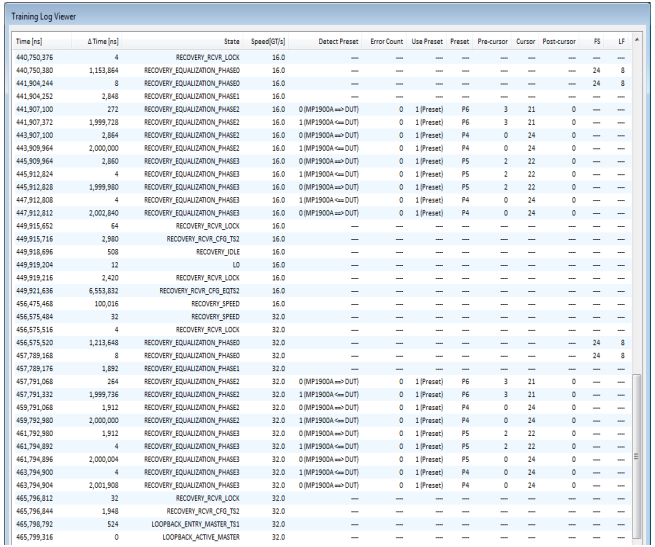
Figure 4-20 Precoding working the scrambler/ de-scrambler

PCI Express Gen5 Link Training

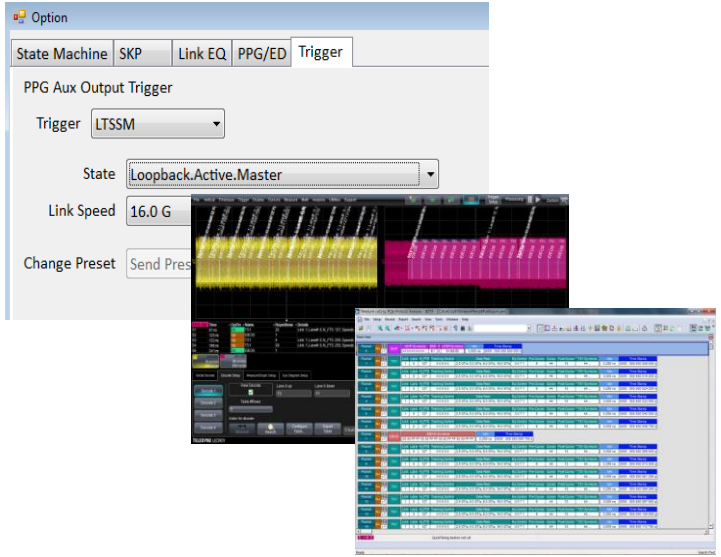
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

Strong MX183000A Support for Customer Debugging

LTSSM Log Viewer



LTSSM Trigger



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LTSSM Details

Training Log Viewer

Time [ns]	ΔTime [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	L0	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQTS2	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	0	24	0	---	---
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---

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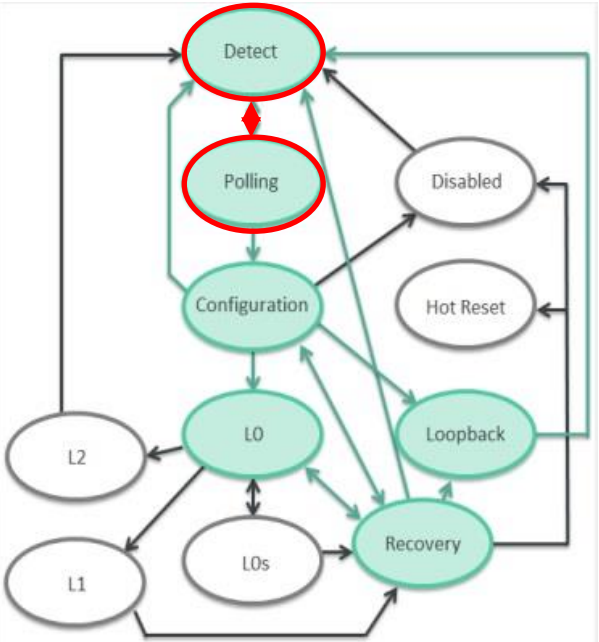
2.5GT/s Link Failure

- LTSSM times-out at Polling Active and repeatedly performs the operation for returning to Detect.
- The Gen1 2.5 GT/s Symbol Lock is not obtained.

Time[ns]	Delta Time[ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor
0	13552	INITIAL	8	----	----	----	----	----	----	----
13552	8738088	DETECT_QUIET	8	----	----	----	----	----	----	----
8751640	3261912	DETECT_QUIET	2.5	----	----	----	----	----	----	----
12013552	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
12013568	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
36013568	16	INITIAL	2.5	----	----	----	----	----	----	----
36013584	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
48013584	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
48013600	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
72013600	16	INITIAL	2.5	----	----	----	----	----	----	----
72013616	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
84013616	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
84013632	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
108013632	16	INITIAL	2.5	----	----	----	----	----	----	----
108013648	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
120013648	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
120013664	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----



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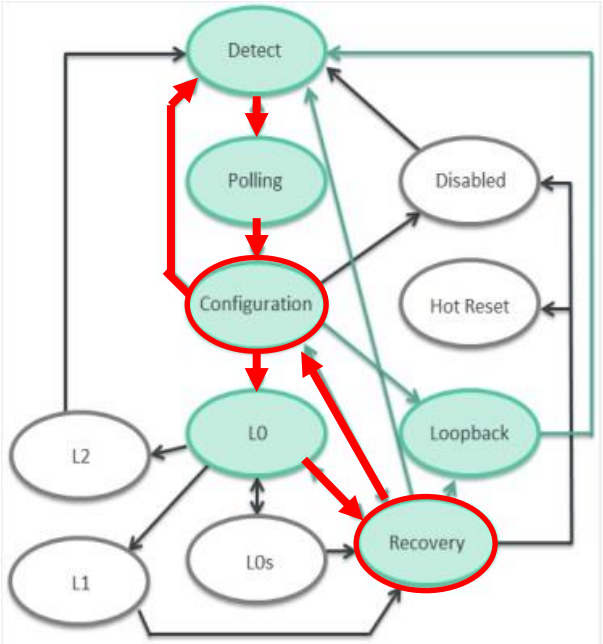
Speed Change Failure

- The Recovery Phase1 state is entered but times-out and returns to Initial.
- Symbol synchronization is not achieved at Gen3 8G.

Time[ns]	Delta Time[ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor
156013696	16208048	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
172221744	66088	POLLING_CONFIGURATION	2.5	----	----	----	----	----	----	----
172287832	3880	CONFIGURATION_LINKWIDTH_START	2.5	----	----	----	----	----	----	----
172291712	128	CONFIGURATION_LINKWIDTH_ACCEPT	2.5	----	----	----	----	----	----	----
172291840	3920	CONFIGURATIONS_LANE_WAIT	2.5	----	----	----	----	----	----	----
172295760	128	CONFIGURATIONS_LANE_ACCEPT	2.5	----	----	----	----	----	----	----
172295888	4832	CONFIGURATION_COMPLETE	2.5	----	----	----	----	----	----	----
172300720	448	CONFIGURATION_IDLE	2.5	----	----	----	----	----	----	----
172301168	24	L0	2.5	----	----	----	----	----	----	----
172301192	4472	RECOVERY_RCVR_LOCK	2.5	0	0	1	7	0	0	0
172305664	3976	RECOVERY_RCVR_CFG_EQTS2	2.5	----	----	----	----	----	----	----
172309640	9636200	RECOVERY_SPEED	2.5	----	----	----	----	----	----	----
181945840	32	RECOVERY_SPEED	8	----	----	----	----	----	----	----
181945872	8	RECOVERY_RCVR_LOCK	8	0	0	1	7	0	0	0
181945880	24000000	RECOVERY_EQUALIZATION_PHASE1	8	----	----	----	----	----	----	----
205945880	8741256	RECOVERY_SPEED	8	----	----	----	----	----	----	----
214687136	32	RECOVERY_SPEED	2.5	----	----	----	----	----	----	----
214687168	24000008	RECOVERY_RCVR_LOCK	2.5	0	40867	1	7	0	0	0
238687176	24000000	CONFIGURATION_LINKWIDTH_START	2.5	----	----	----	----	----	----	----
262687176	16	INITIAL	2.5	----	----	----	----	----	----	----



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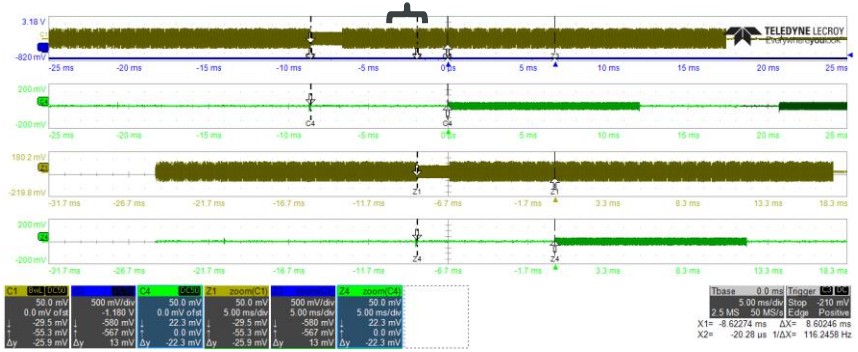
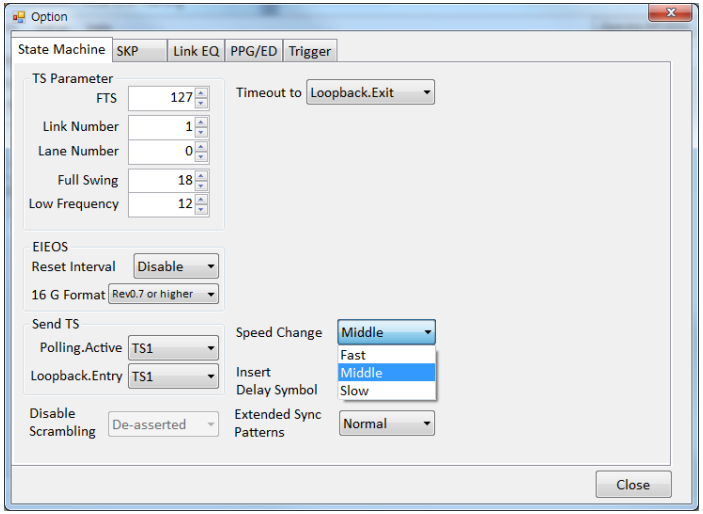
Speed Change Failure

Does the speed change time meet the standard?

- Although the standard specifies that the speed change time should be **within 12 ms (AIC) or 24 ms (System),** some devices have a shorter time-out.
- The BERT can select a Generation change time from three levels:
  - Fast: 1.8 ms
  - Middle: 6.5 ms
  - Slow: 11 ms

Times out at about 3 ms without waiting for response from partner





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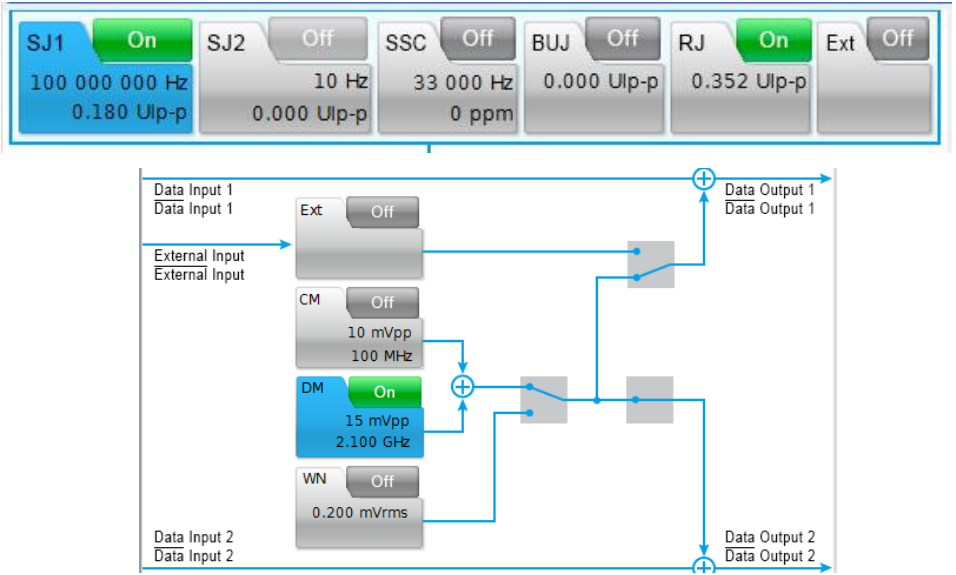
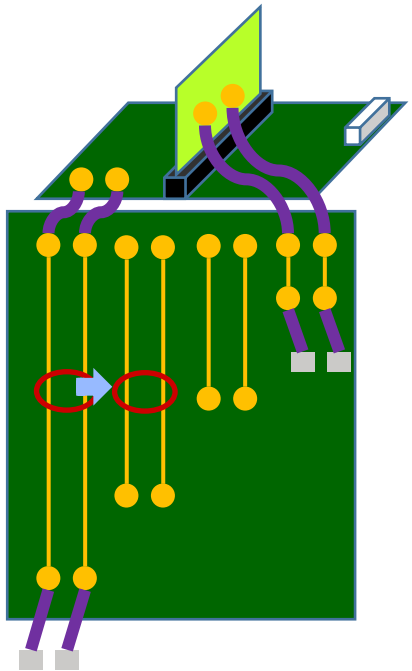
Never Become Error-Free

Reduce the Loss and Stress. Usually the degree of effect is in the order

ISI Loss > DMI > RJ > SJ.

Decrease each of the values gradually until the error-free status is confirmed.





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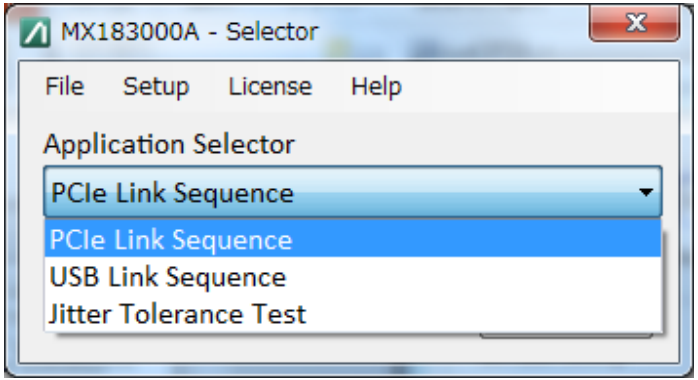
PCI Express Gen5 Rx JTOL Test

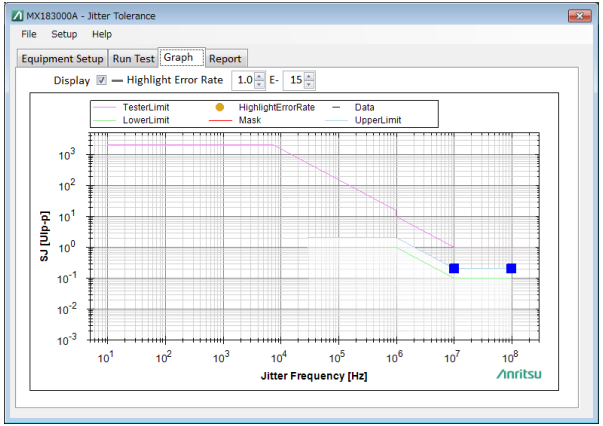
Stress Signal Calibration → Transition to Loopback Status → **Stress Signal Input Test**

Stress Signal Input Test (Jitter Tolerance Margin Test

Jitter Control and Tolerance Measurement using MX183000A

- Impresses SJ and Tests PHY Device Jitter Tolerance
- Tests Device Margin using Low BER Estimation
- Outputs Measurement Results in HTML and CSV Formats





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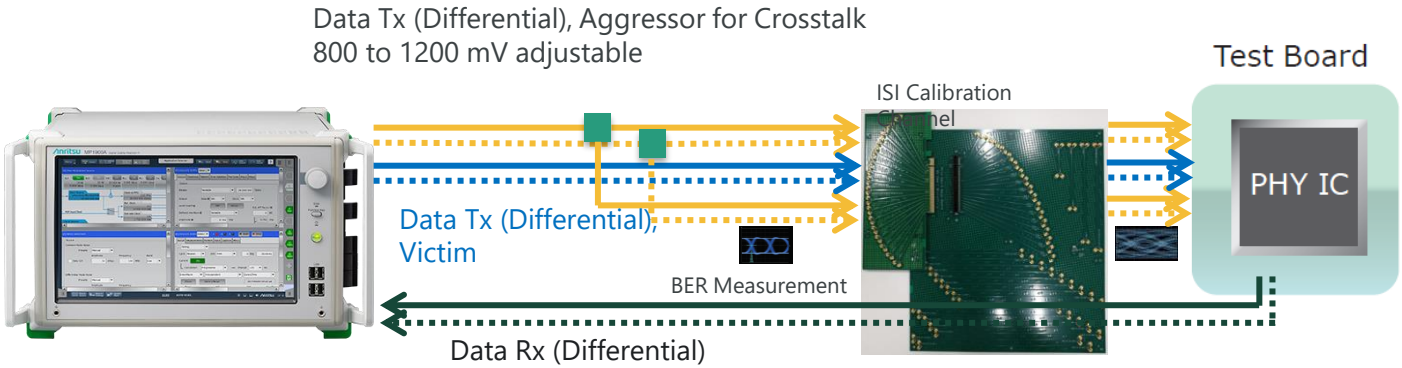
PCI Express Gen5 Rx JTOL Test with X-talk

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

MP1900A Generates Aggressor Signal using Multichannel Generator

- All-in-one BERT with multichannel signal generator
- Supports DUT requests to send MCP



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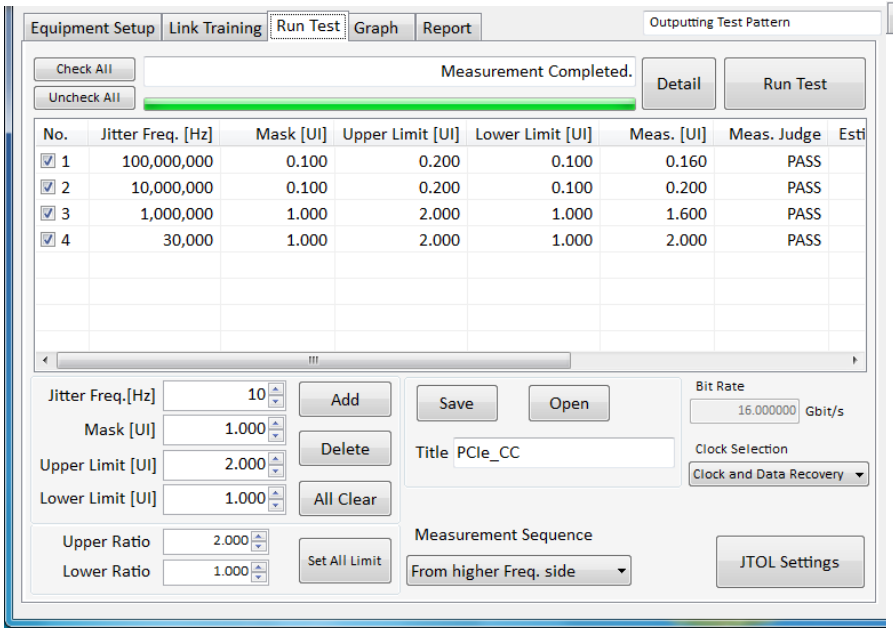
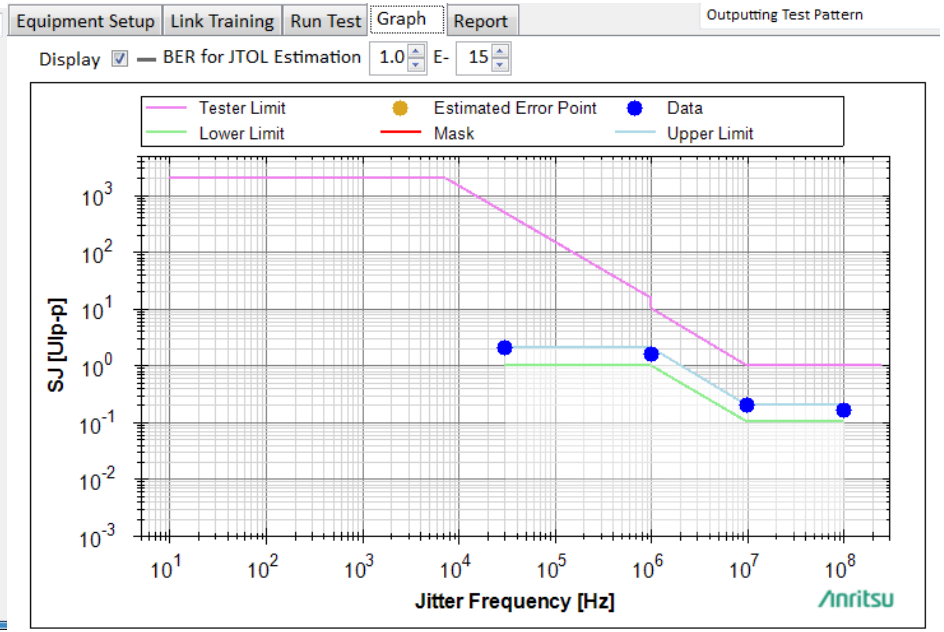
Jitter Tolerance Test Example

This test is optional for PCIe compliance test.





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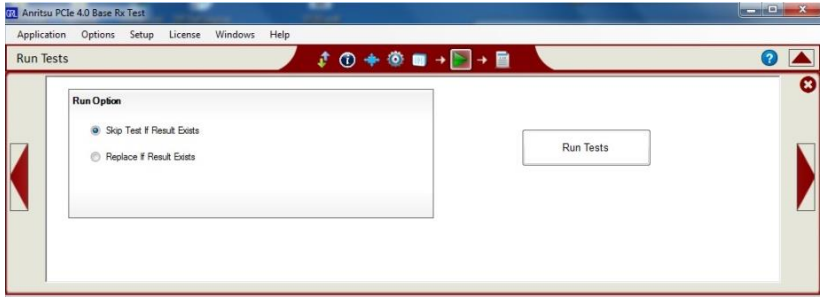
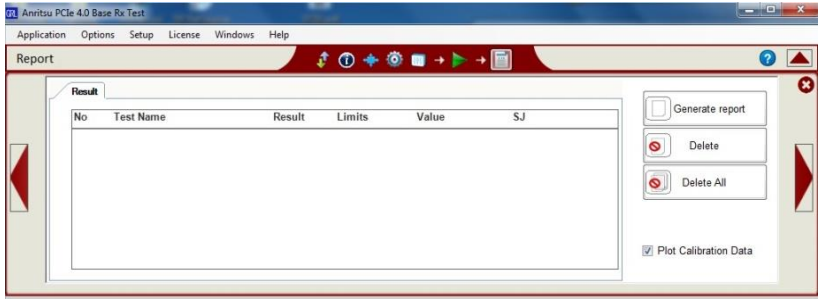
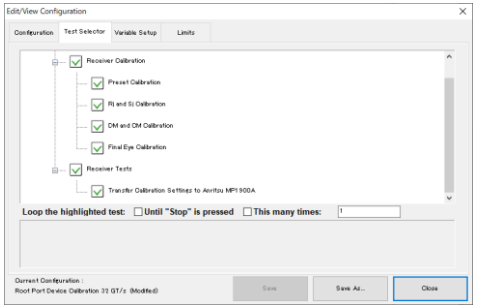
PCI Express Gen5 Test Report

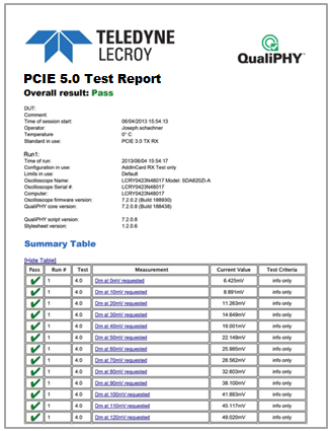
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

Stress Signal Input Test









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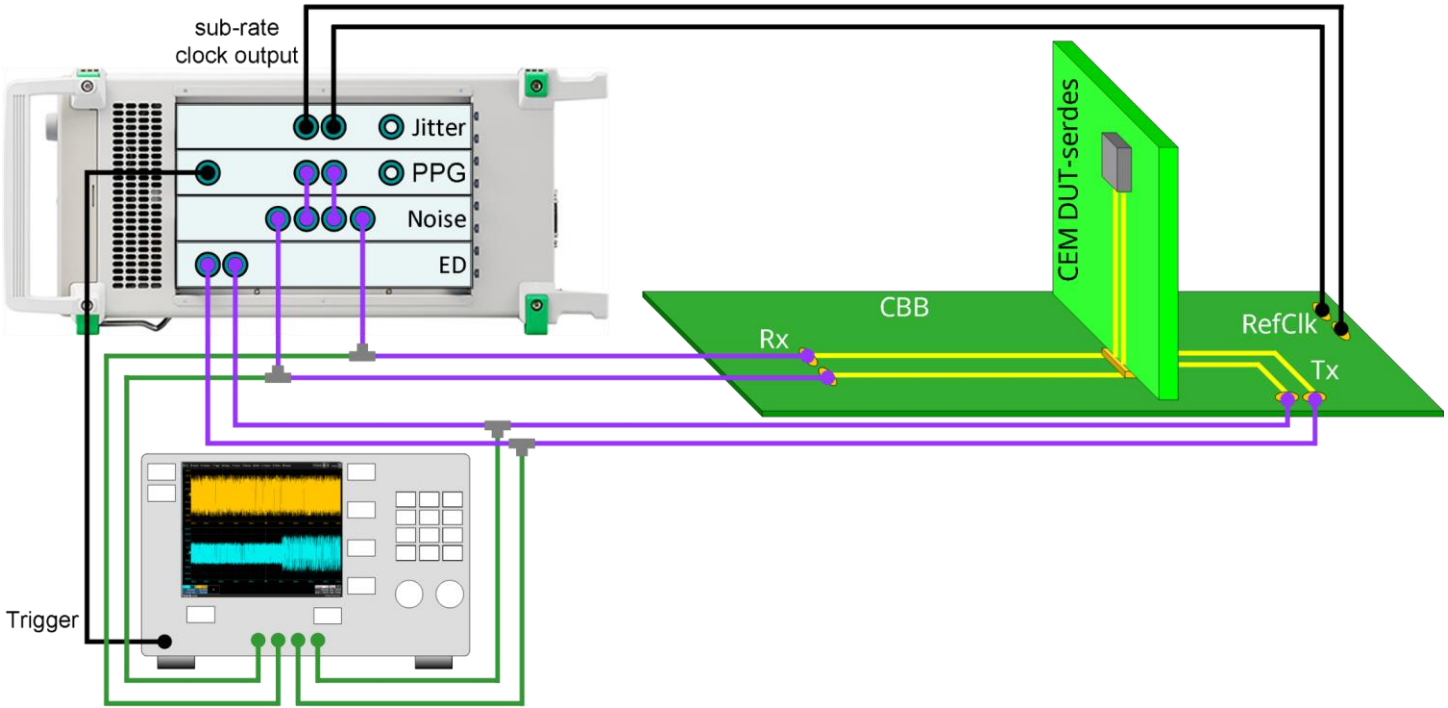
Transmitter Link EQ Response Time Setup



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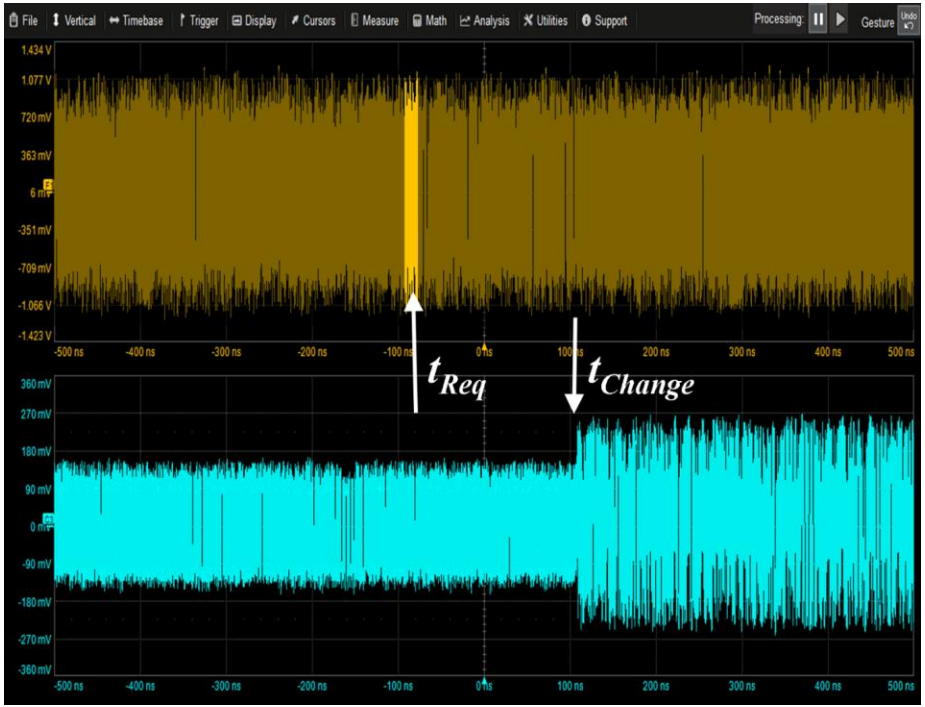
Transmitter Link Equalization Response

t_{Req} = time of request

t_{Change} = time FFE taps change

Require:

$t_{Change} - t_{Req} < 500$ ns



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Transition to PCIe 6.0: 64GT/s PAM4 Design and Test Considerations

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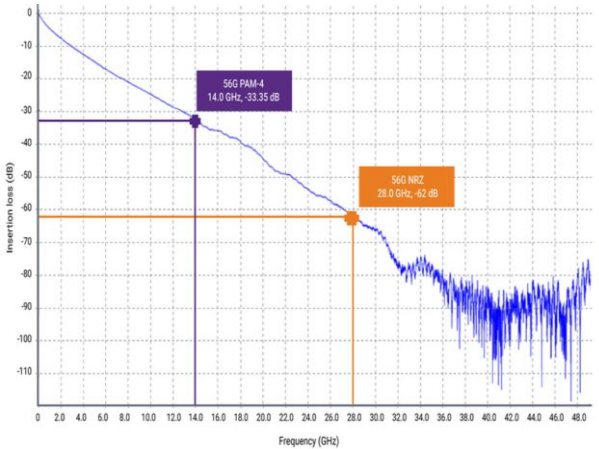
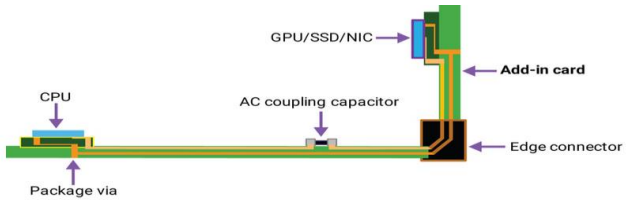
But, the Ever-increasing Data Rates Run Into a Problem…

Insertion Loss at higher Nyquist frequencies becomes prohibitive with NRZ modulation.

- For example,
  - @28 Gbps:
    - Nyquist 14GHz : IL = 33.3 dB
  - @ 56 Gbps
    - Nyquist 28GHz : IL =62dB

This amount of Insertion Loss becomes prohibitive for the current PCIe Channel model to compensate (without a re-driver)





If the channel remains the same, then the need for different modulation format to accommodate increasing data rates becomes pressing…

Enter PAM4.

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PCI-SIG® Announces PCIe 6.0

PCI Express® 6.0 Specification Details

Targeting completion in 2021; Designed to meet the evolving capacity needs of industry

- **Key Features:**
  - Doubles bandwidth to 64 GT/s (PCIe 6.0) from 32 GT/s (PCIe 5.0)
  - Implements PAM4 signaling (PCIe 6.0) rather than NRZ (PCIe 5.0)
    - Pulse Amplitude Modulation (PAM) allows PCIe 6.0 technology to pack more bits into the same amount of time on a serial channel
  - Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency
  - Maintains backward compatibility with all previous generations of PCIe technology
  - Delivers similar channel reach as PCIe 5.0
  - More than two dozen member companies of the PCI-SIG Electrical Work Group attended a Face-to-Face Meeting in May

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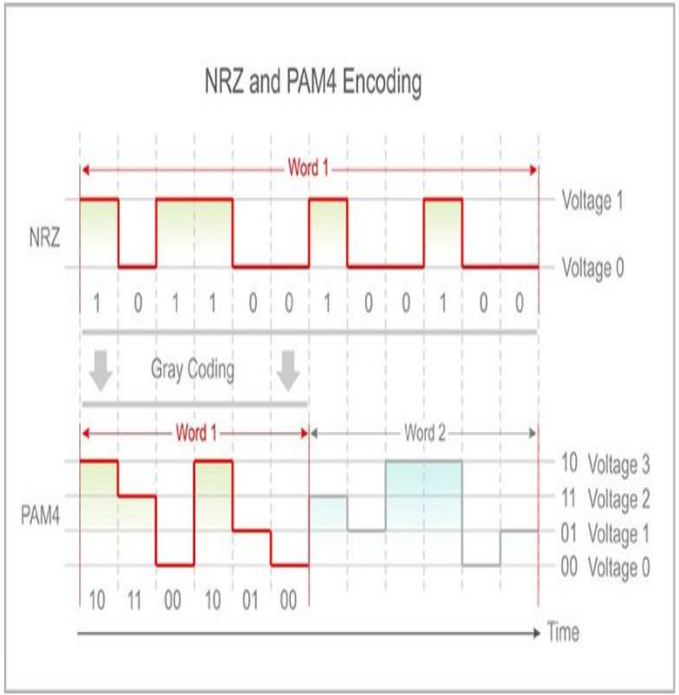
PAM4 – A Slam Dunk to Achieve 64 GT/s?

PAM4 offers multiple enhancements over NRZ:

- **Every two (2) bits are mapped to one symbol**
  - 2-bits has 4 unique combinations → four (4) signal levels
- **Requires 1/2 the bandwidth compared to NRZ**
  - Ex. NRZ (32GT/s) Fnyquist = 16GHz; PAM4 (32Gbaud/4) Fnyquist = 8GHz)
- **Mapping can be "Linear" or "Gray" encoding**
  - Default encoding typically for PAM4 in IEEE/OIF-CEI
  - Gray encoding reduces potential number of bit errors
- **Not a new modulation technology**
  - PAM is has been used in 10BASE (3 levels), 100BASE-T(3 levels), 1000BASE-T, (5 levels) for many years …
  - PAM4 adopted in IEEE 802.3 and OIF high speed networking standards



This all seems positive. Maybe all the work is done and we can all relax and enjoy the easily obtainable, higher data rate! Right?

Not so fast….

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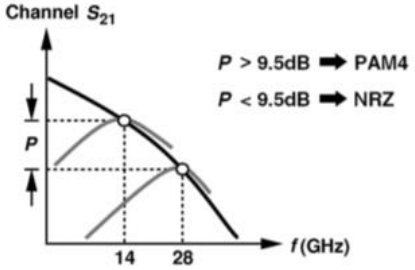
Challenges and Changes with adopting PAM4 in PCIe 6.0

- ✓ Reduces Signal to Noise Ratio vs prior NRZ-based versions
- ✓ Increased sensitivity to Crosstalk
- ✓ Increased sensitivity to Noise
- ✓ Introduction of Forward Error Correction (FEC)
- ✓ Backward compatibility with Gen1, Gen2, Gen3, Gen4
- ✓ Miscellaneous…cost, DFE taps, FEC
- ✓ Overall increased complexity

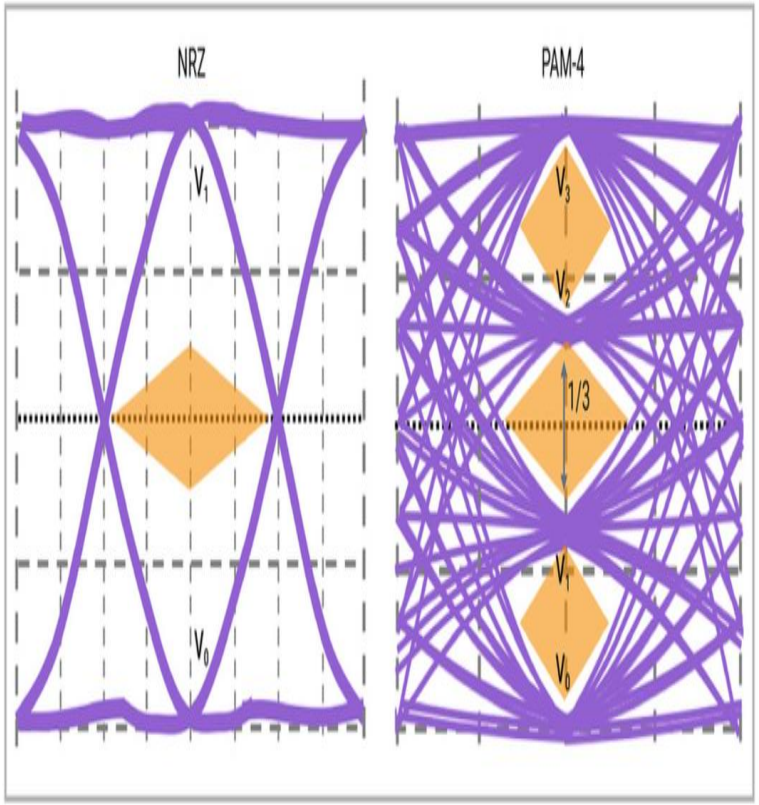
PAM4 Reduces Signal-to-Noise vs NRZ

- For same level of NRZ amplitude, each Eye Height is 1/3 of NRZ Eye Height which cause the SNR ratio to degrade by over 20 log 1/3) = 9.5dB



Simple judgement on different data formats.

- This 66% reduction in vertical eye opening will reduce the signal's tolerance to crosstalk and reflections which can lead to higher bit rate:
  - For Gen5: 10 -15mV Eye Height @ BER 1E-12
- Trade-off of lower Nyquist for reduced SNR



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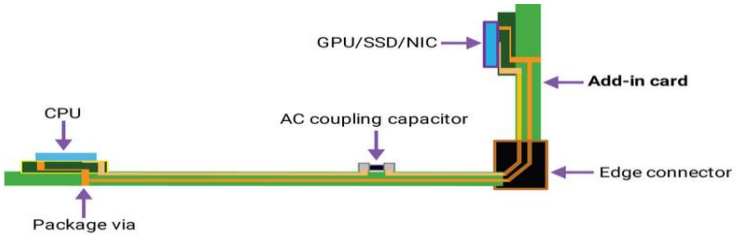
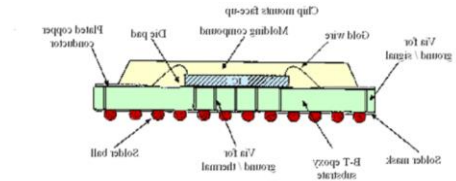
Crosstalk a Big Concern at 64GT/s PAM4

- Crosstalk (XT) which is noise coupled through vias, connectors, packages, etc. may be more harmful than channel insertion loss in setups
- XT is usually characterized by the following parameters:
  - PSXT: power sum of crosstalk (usually defined for NEXT and FEXT)
  - ICR: insertion loss to crosstalk ratio
  - ICN: integrated crosstalk noise
  - Above usually measured on VNA
- XT is a substantial contributor to jitter at the Receiver.
- PAM4 maximum signal swing is similar to NRZ and therefore the noise level from the aggressor signal is the same for both PAM4 and NRZ.
- PAM4 vertical eye opening is 33% of NRZ and therefore the victim signal's tolerance for crosstalk is less.
- What is the effect of 16 lanes of PAM4 Transmitter and Receiver operational at the same time on ball grid array?
  - Crosstalk margin?





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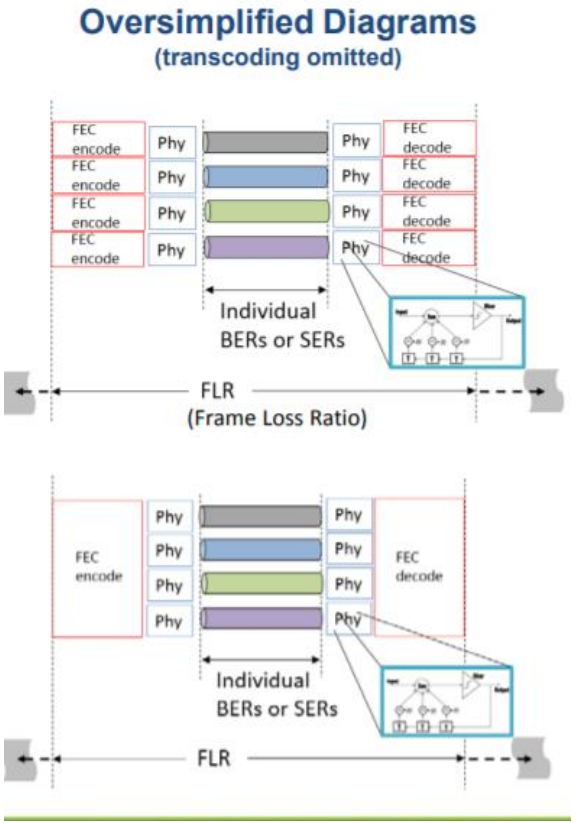
PCIe 6.0 and Forward Error Correction (FEC)

Testing methodology and measurements will need to be revamped to consider FEC

- Standard RX tests of testing for 1E-12 will likely not be feasible
- IEEE standards prescribe testing for 1E-4 – 1E-06 with FEC on current test equipment…and assume that addition of FEC will indeed improve BER as expected
  - No BERT today supports FEC on the Error Detector.
  - How will PCIe 6.0 address the question of testing RX with/without FEC?

Also note:

- The addition of FEC overhead at the transmit end and FEC decoding at the receive end could cause latency in signal transmission.
  - Error correction takes additional time…error must detected and then must be corrected
  - How much latency is tolerable?



Source: DesignCon 2016

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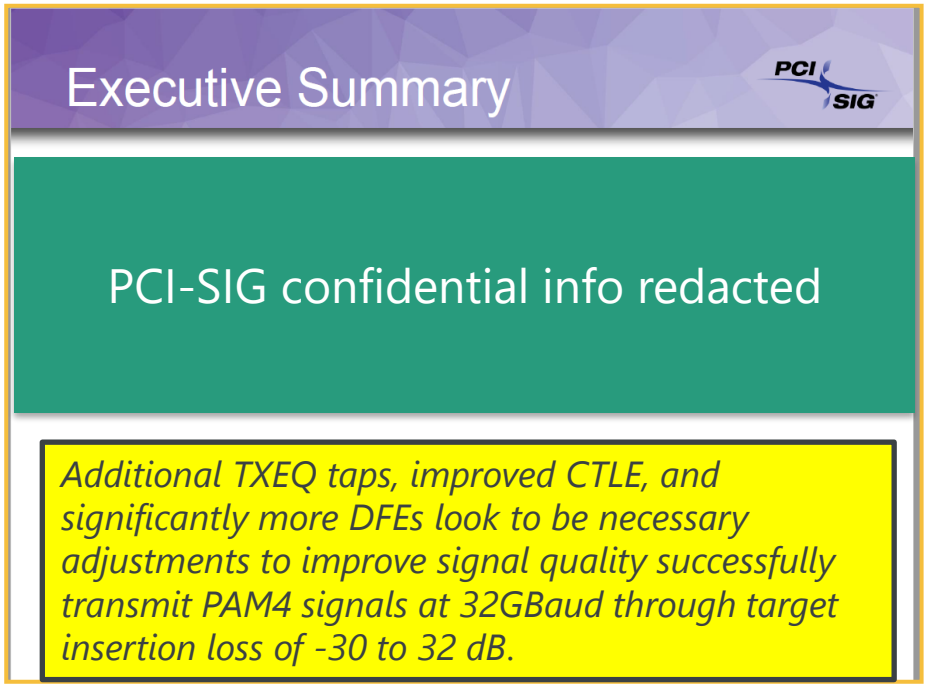
6.0 Backwards Compatibility Challenge

- According to PCI-SIG press release: “Deliver similar channel reach as PCIe Gen5”
  - Implies CEM connector (with enhancements and improvements) will remain the same
  - PCIe Gen 5 allowed channel loss of up to 36dB @ Nyquist, but not clear what “similar channel reach” means
  - Less “reach” than Gen 5?
- Also for backward compatibility, it seems to imply that a single PHY should:
  - Support operation from 2.5GT up to 64G
  - Transmitter to support both NRZ (2.5 thru 32GT) and PAM4 (64GT)
  - Receiver to support NRZ and PAM4
- With PAM4
  - Requires 3 slicers to detect three eye diagrams
  - Requires increased Error Detector sensitivity

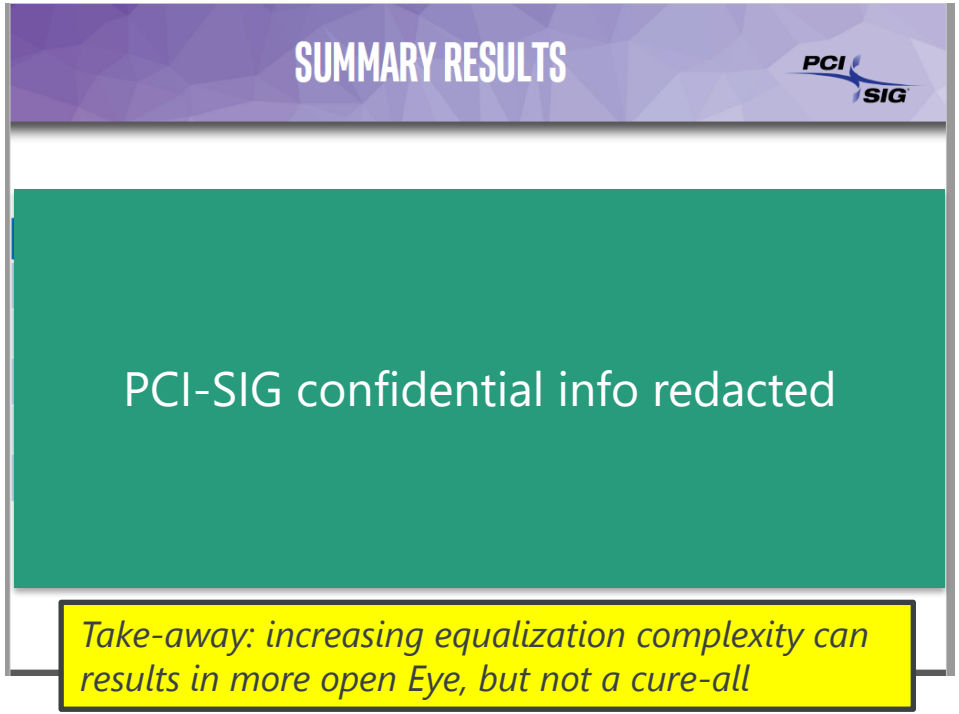
Looking to the 6.0 and Future:
Current Proposed Equalization Configuration

Currently proposed Equalization configuration for 6.0 (April 2020) in 6.0 Specification, Version 0.7:



Looking to the 6.0 and Future:
Current Proposed Equalization Configuration (con't)

Comparison of proposed equalization Specification 6.0: Version 0.5 vs. 0.7:



Take-away: increasing equalization complexity can results in more open Eye, but not a cure-all

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Other Questions Looking to PCIe 6.0 and the Future

- Continue to support backward compatibility back to 2.5Gbps for every data rate increase?
- Current CEM connector…maintain this for how much longer?
- Transition to different board materials?
- Should transitioning to PAM4 be the “clean” break with NRZ?
- Cables vs. Board? Cables offer much better IL profile compared to typical board material

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Questions?

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Thank you for your time!

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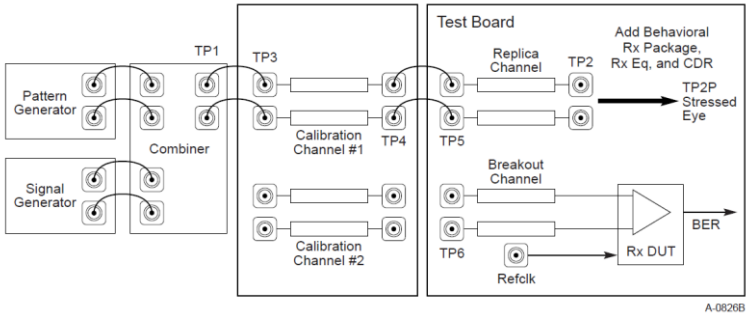
https://www.anritsu.com/en-US/test-measurement/support/talk-to-anritsu

Base Spec Testing - Receiver (RX)

- Base Spec does not enforce a particular RX implementation. Chip vendors can make their own choices with respect to equalization, package and receiver sensitivity/minimum acceptable width.
- However, Base Spec reference RX defines the minimum eye opening of an RX input signal that must still be detected with bit error ratio (BER) of 1E-12.
- The stressed eye for RX jitter tolerance testing is calibrated **using the coupon or replica RX trace on the PCB to provide part of the ISI channel.**
  - RX stresses may be calibrated using "Seasim" statistical simulation tool. Seasim incorporates behavioral RX package, RX EQ, and CDR models and optimizes simulated EQ of the reference RX for maximum eye opening.
  - The test setup incorporates the relevant impairments until the desired eye-opening (eye height and eye width) are reached. These values are then transferred to the signal generator and each impairment is calibrated individually.
- During RX jitter tolerance testing, the PCB replica channel is replaced by the actual RX trace to the DUT so the signal at TP2 at the end of the replica channel will be equivalent to the signal at the chip's RX pins.
  - Starting at 16 GT/s, the PCIe edge connector (ie the physical hardware) must be included in the RX calibration trace for Base spec RX calibration and testing.



Source: PCI-SIG

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