



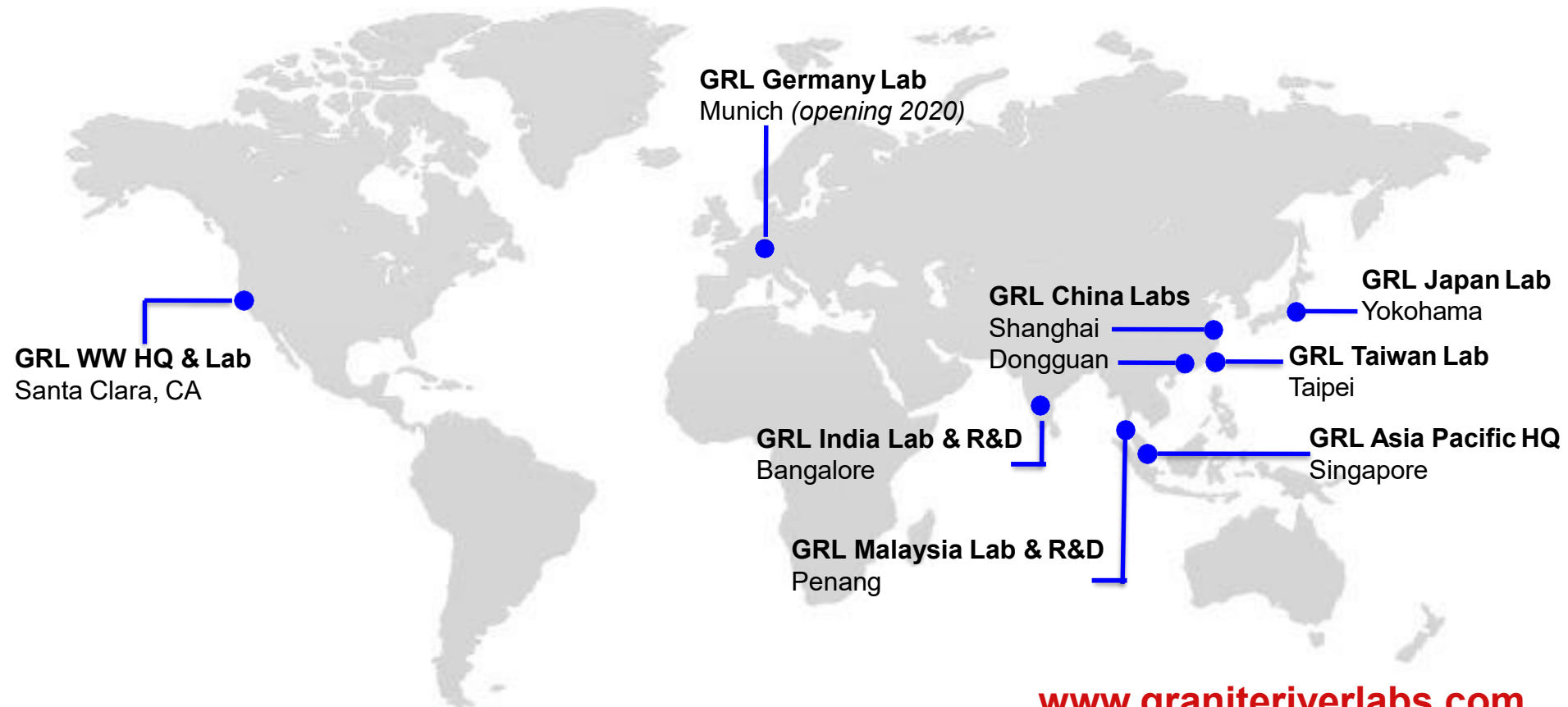
USB4™ Technical Introduction and Compliance Test Overview

May 5-6, 2020

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GRL – Who We Are

- Founded 2010, Silicon Valley HQ, 8 labs around the world, ~200 employees
- Recognized World Leader in Test Services and Automation Solutions for Connectivity and Charging
- GRL operates more USB-IF authorized test labs than any other company in the world



www.graniteriverlabs.com

Presenters



Nikhil Acharya manages GRL's USB and USB Power Delivery test programs world-wide, serving as GRL's chief liaison to the USB-IF and key USB customers and ecosystem partners. As GRL's lead USB expert, Nikhil ensures timely, consistent and technically sound implementation of USB test programs in GRL's global labs, and oversees technical execution of all USB test projects in GRL's Silicon Valley headquarters lab. Additionally, Nikhil serves as North America technical sales engineer for all of GRL's USB, USB Power Delivery, and wireless charging test automation solutions. Nikhil started his career as an intern at GRL after earning a M.S. in Electrical Engineering from Santa Clara University.



Darren Gray is an Engineering Fellow of GRL, based in GRL's Santa Clara headquarters where he supports test programs for a wide breadth of high-speed customer designs. Darren spent over 8 years at Tektronix/Synthesys Research where he was a senior application engineer, and before that was an engineer for JDSU. Darren is an expert in receiver testing and optical transceiver characterization, and his wide-breadth of expertise in high-speed serial data standards include USB, IEEE 802.3 Ethernet, PCI Express, DisplayPort, and MIPI. Darren earned a B.S. in Electrical Engineering from Carnegie Mellon University.

Disclaimer





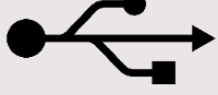





















- GRL is presenting informational materials in these presentations and/or webpages that provide details about official USB-IF programs and processes.
- **DISCLAIMERS:**
 - This information is provided for convenience only. This information is not and should not be relied upon as an official communication of USB Implementers Forum (USB-IF). Official communications of USB-IF are available at its website at usb.org or otherwise directly from USB-IF.
 - This disclaimer will help companies certifying a product with USB-IF to avoid any confusion about the official requirements and processes involved in USB-IF Compliance Programs.
 - USB-IF has translated the above disclaimer in Simplified-Chinese and Traditional-Chinese so this important notice is available in the appropriate regional dialect of our ITLs. You can find the translated versions below.
 - The source for the information in this presentation is from the USB-IF Developers Conference materials and USB Specifications which can be found on the USB-IF website located at <http://www.usb.org>.
 - Please note: GRL is not USB-IF authorized to test products for USB4 certification testing at this time as the Compliance Testing Program is under development.
- **GRL is presenting material that originated in a USB specification i.e. USB Type-C® Cable and Connector, USB Power Delivery and/or USB4™**

Agenda

- **USB4™ Overview**
- **USB4™ Link Process**
 - Discovery and Entry
 - USB4 Link Training
- **USB4™ Compliance Testing Overview**
 - USB4 Hub & Docks/ Host/Device
 - USB4 Cable Connector
- **USB4™ Electrical Testing**
- **Design & Test Considerations**
- **Q & A**

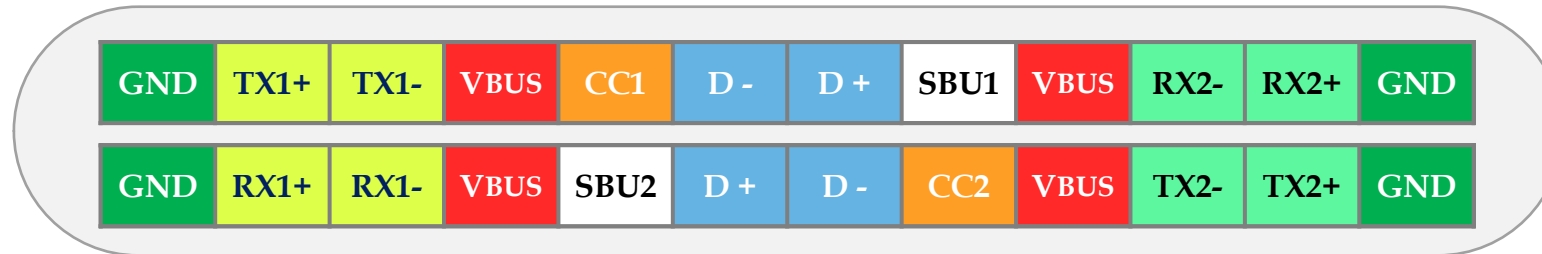
USB Family Overview

Revision	Issue Date	Brand Name	Bits/sec	Package Logo	Port & Cable Logo	USB-C® Trident Charging Logo
USB 1.0	Jan 1996	Low Speed Full Speed	1.5 Mbps 12 Mbps			
USB 1.1	Aug 1998	Full Speed With updated	1.5 Mbps 12 Mbps			
USB 2.0	April 2000	High Speed	480 Mbps			
USB 3.0 USB 3.2 Gen 1x1	Nov 12, 2008	SuperSpeed USB 5Gbps	5 Gbps			
USB 3.1 USB 3.2 Gen 2x1	July 26, 2013	SuperSpeed USB 10Gbps	10 Gbps			
USB 3.2 USB 3.2 Gen 2x2	Sep 22, 2017	SuperSpeed USB 20Gbps	20 Gbps			
USB4 USB4 Gen 2x2	Sep 3, 2019	USB4™ 20Gbps	20 Gbps			
USB4 USB4 Gen 3x2	Sep 3, 2019	USB4™ 40Gbps	40 Gbps			

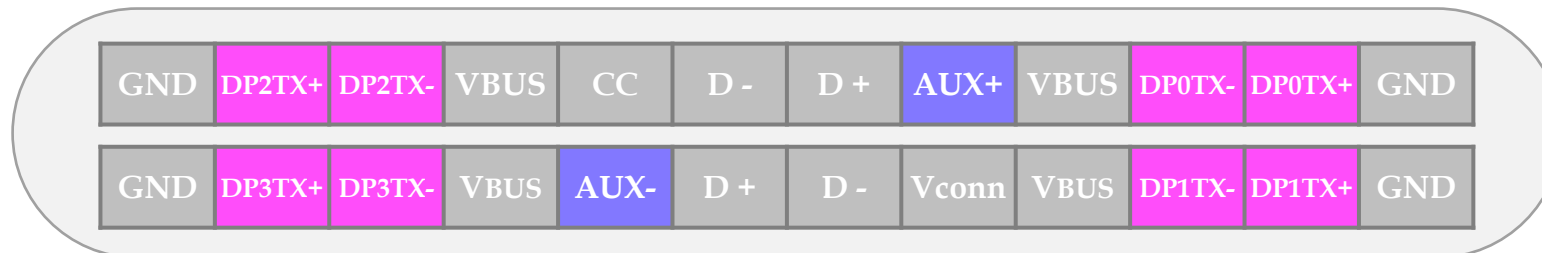
Pinout of USB-C®/DPC/USB4™ Connector



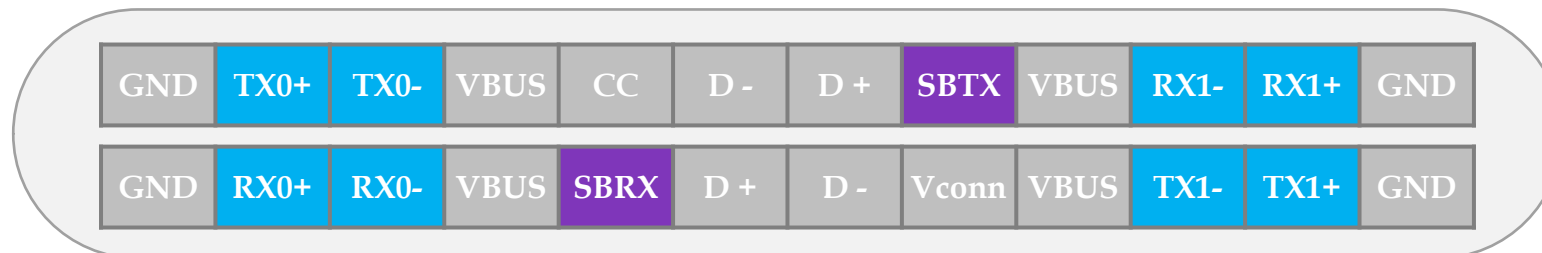
USB-C Receptacle Front View



DPC Pinout

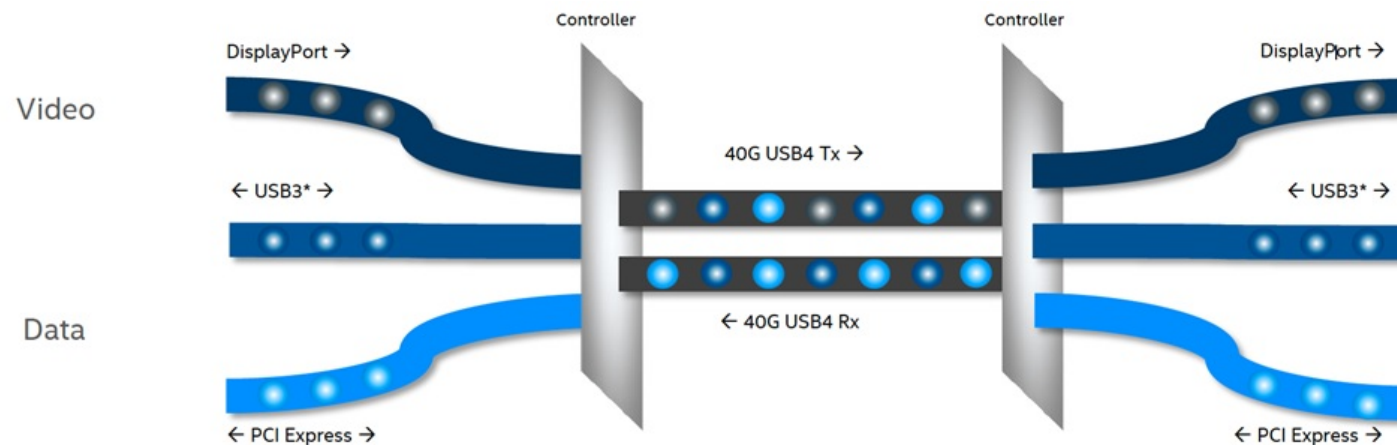


USB4 Pinout



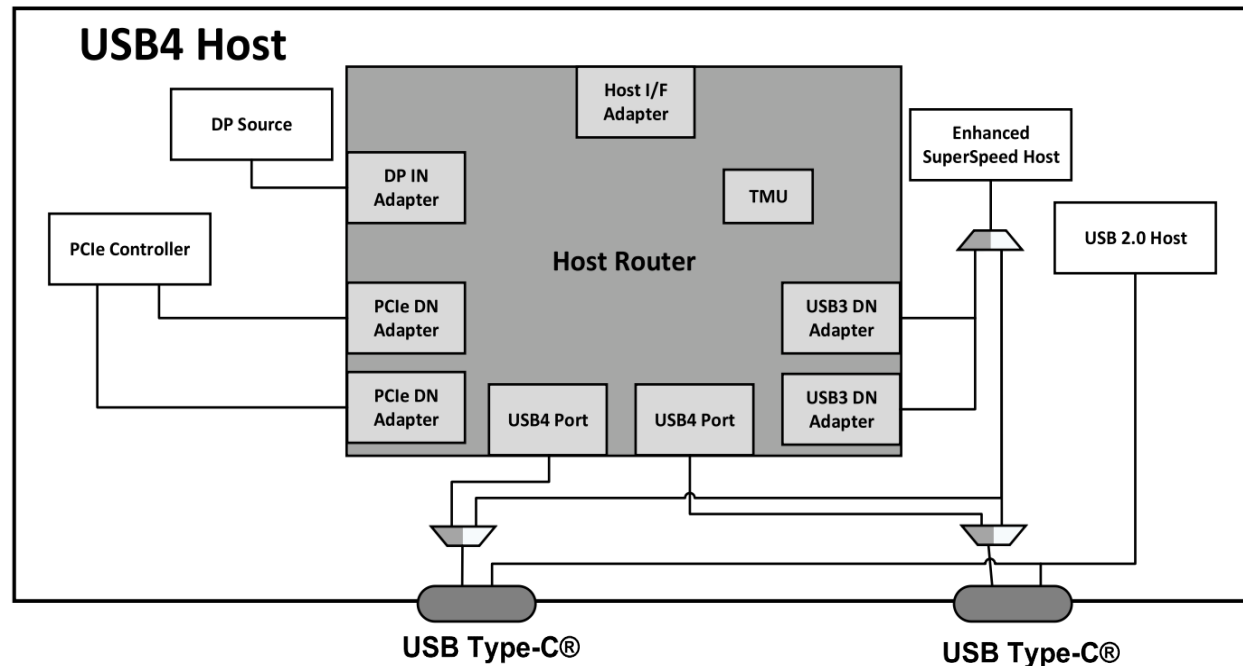
USB4™ Overview

- **40Gbps Maximum Speed** over **USB Type-C®**
 - USB4 Gen2: 20G(10G x2)
 - USB4 Gen3: 40G(20G x2)
- **Compatible with USB and Thunderbolt 3 products**
- **Supports USB 3.2/DP/PCIe tunneling**



USB System Description

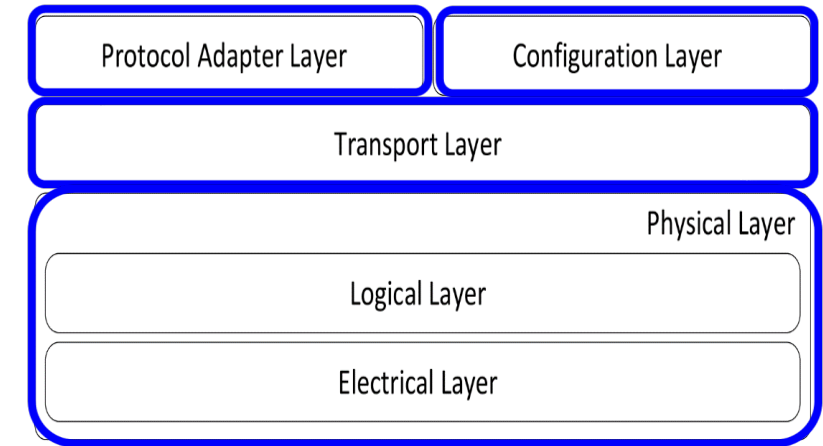
- **Router (similar to TBT controller):** A Router maps Tunneled Protocol traffic to USB4™ packets and routes packets through the USB4 Fabric.
- **Adapter:** Each Router contains up to 64 Adapters. Adapters provide an interface between a Router and an external entity.
- **Time Management Unit (TMU):** The functional block in each Router that is used to distribute and synchronize time throughout the USB4 Fabric.



USB4™ Functional Stack Layers

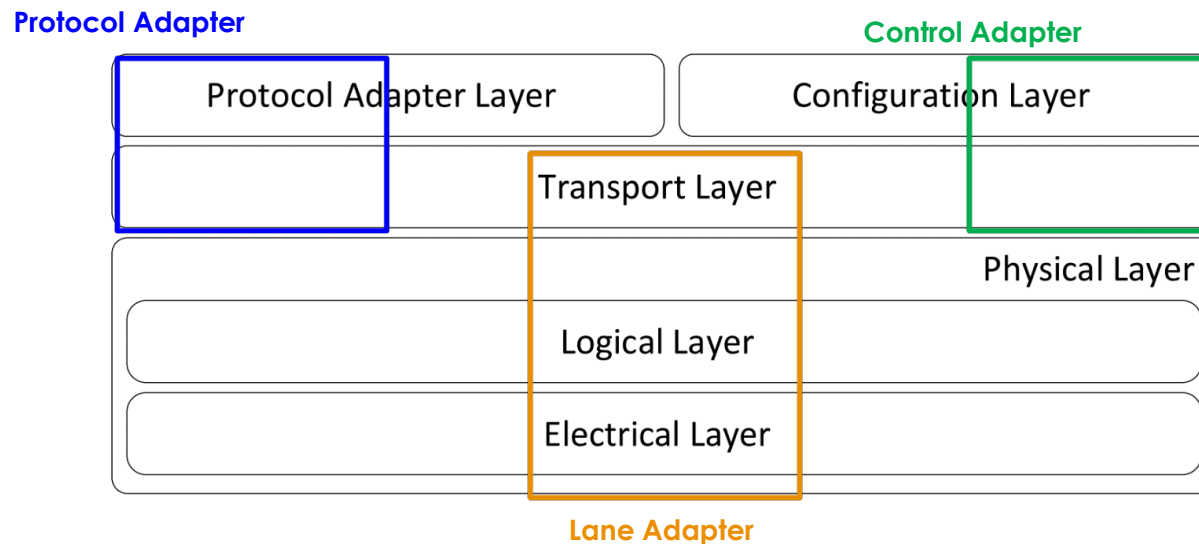


- **Protocol Adapter Layer:** Maps an I/O protocol (PCIe, DP, USB, Host Interface) to USB4.
- **Configuration Layer:** Performs Router setup, configuration and management.
- **Transport Layer:** Forwards Tunneled Packets and Control Packets through the bus.
- **Physical Layer:**
 - Logical Layer: Establishes a High-Speed Link between two routers, encodes/decodes byte streams, and performs Link PM services.
 - Electrical Layer: Defines Electrical signaling across High Speed Lanes.



USB4™ Adapters

- **Protocol Adapter:** Maps a Tunneled Protocol to USB4.
 - USB 3.2 Adapter / DP Adapter / PCIe Adapter / Host Interface Adapter
- **Control Adapter:** Configuration and management interface.
- **Lane Adapter:** Provides an interface for a Lane. A USB4 Port has two Lane Adapters



Main Differences: USB4™ vs. TBT3 vs. USB 3.2



■ USB4 vs. USB 3.2

- USB4 40Gbps (20GX2), USB 3.2 20Gbps (10GX2)
- Tunneling Architecture
- Transfer Data and Video simultaneously
- Host-to-host interface

■ USB4 vs. TBT3

- TBT3 Tunneled: DP & PCIe
- USB4 tunneled: DP & PCIe & [USB 3.2](#)
- USB4 protocol: Based on TBT3 protocol (CIO Protocol)

USB4™ / TBT3 / USB 3.2 Comparison



	USB4		TBT3		USB 3.2	
Data Rate	Gen2	Gen3	Gen2	Gen3	Gen1	Gen2
	10G x2	20G x2	10.3125G x2 10.0G x2	20.625G x2 20.0G x2	5G	10G
SSC	30~ 33 kHz		35~ 37 kHz (Legacy) 30~ 33 kHz (Rounded)		30~ 33 kHz	
Coding	Gen2: 64b/66b Gen3: 128b/132b				8b/10b	128b/132b
CDR DF@Freq	0.94@5MHz				0.707@4.9MHz	0.707@7.5MHz
TxFFE	3-Tap FIR (P0~P15)				-3.5dB	-3.1dB/2.1 dB
Rx EQ	CTLE + DFE				CTLE	CTLE + DFE
Cable Length C-C	Gen2: 2 m / Gen3: 0.8 m				2 m	1 m
Loss budget at Nyquist Host + Cable + Device (dB)	Gen2: 5.5 + 11.5 +5.5 / Gen3: 7.5 + 7.5 + 7.5				6.5 + 7 +6.5	8.5 + 6 +8.5
Sideband	1Mbps				NA	
LFPS	Use for CLx Exit				LFPS	LFPS SCD1/2

Protocol Tunneling Support

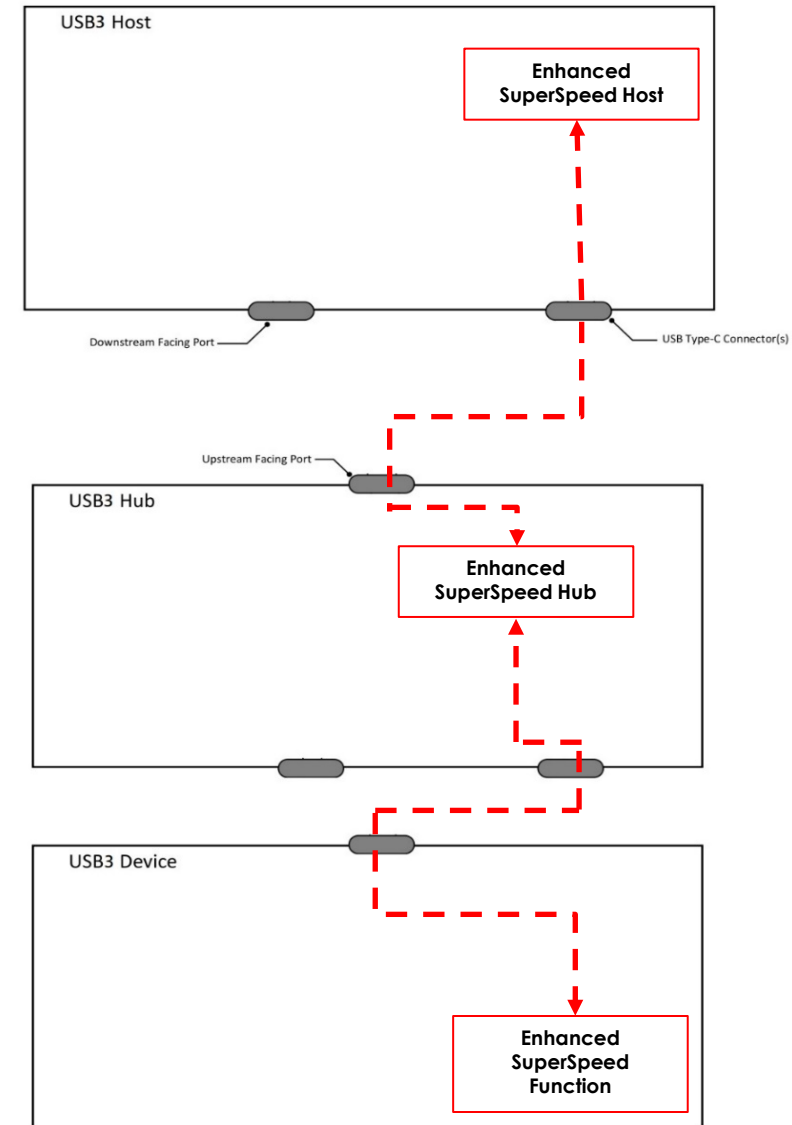


- USB 3.2
- DisplayPort
- Host-to-Host
- PCI Express
- Thunderbolt™ 3

	USB3 Tunneling	DisplayPort Tunneling	Host-to-Host Tunneling	PCI Express Tunneling	TBT3 Compatibility
USB4 Host	V	V	V	optional	optional
USB4 Hub/Dock	V	V	Pass through	V	V
USB4 Device	optional	optional	X	optional	optional

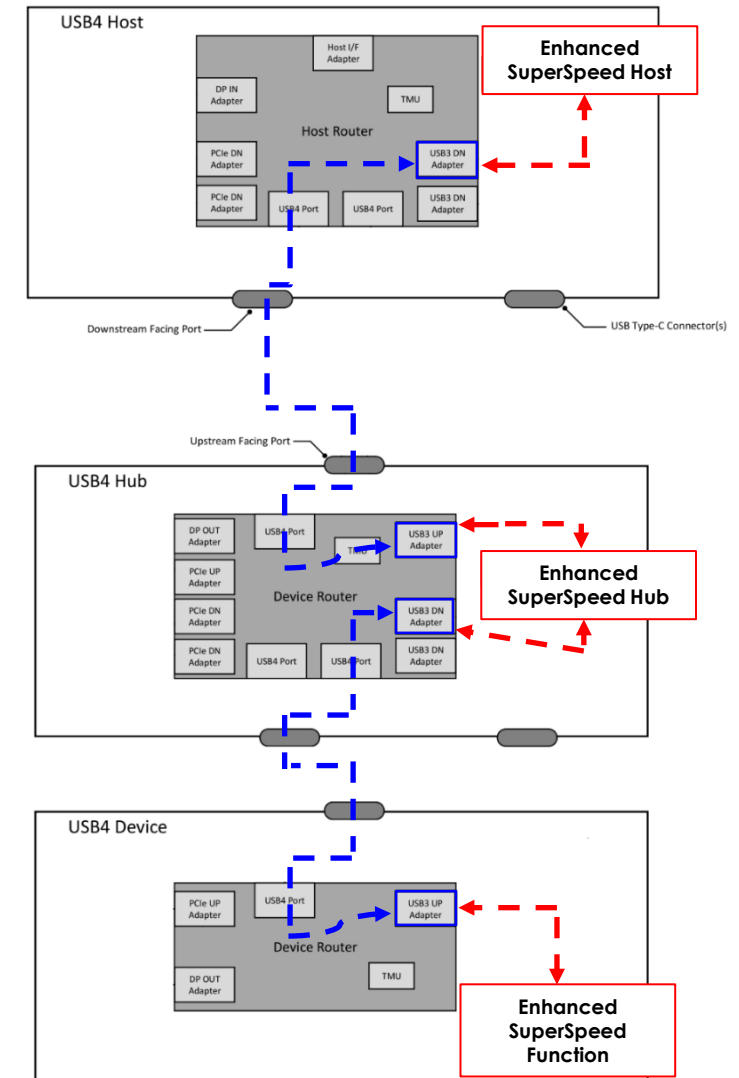
USB 3.2 Native

- Originates and consumed as **Native** Enhanced SuperSpeed protocol.
- From USB 3.2 SW perspective, the USB3 topology remains the same.



USB 3.2 Native and Tunneling

- USB 3.2 Adapters are the translators within each Router that allows USB 3.2 protocol to travel back and forth from **Native** to **Tunneled**.
- Internal USB 3.2 device ports that interface with a USB 3.2 Adapter differ from the USB 3.2 Spec
 - No Physical Layer
 - No Scrambling
 - No SKIP Ordered-Set
 - Link Layer
 - Must support Gen 2 Single-Lane (2x1)
 - May support Gen 2 Dual-Lane (2x2)



Agenda

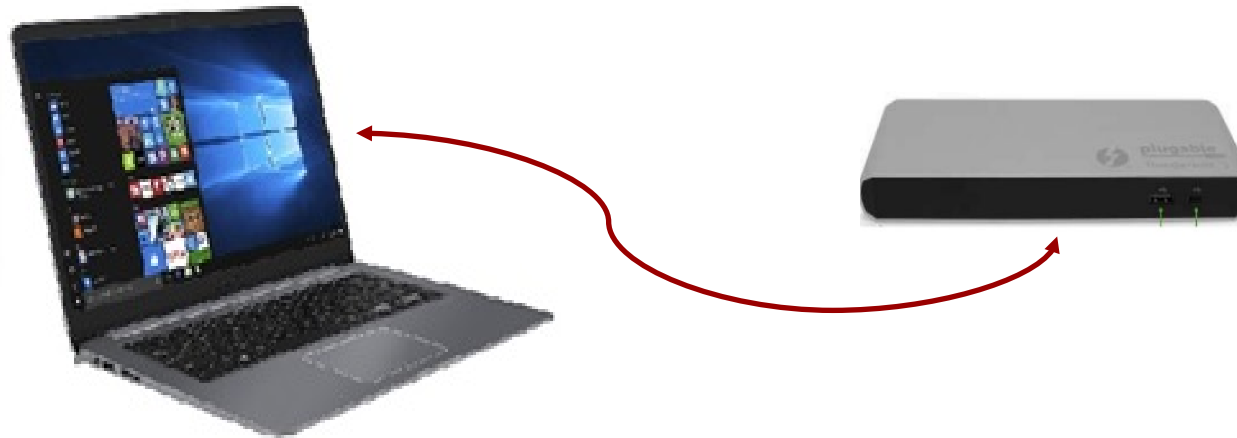
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- **Design & Test Considerations**
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Discover Identity



Header No. of Data Objects = 4-7 ¹	VDM Header	ID Header VDO	Cert Stat VDO	Product VDO	0..3 ² Product Type VDO(s)
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- Existing mechanism for discovering information related to Power Delivery devices and cables
- Extended existing Passive and Active Cable Product Type VDOs to include USB4™
- Added Product Type VDOs for DFP and UFP with USB4 related information



USB4™ Passive Cable

■ USB4 Gen3 Passive Cable Length up to 0.8m

Table 3-1 USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	USB Power Delivery	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported	Optional
CC2-5					5 A		Required
CC3G1-3	C	C	USB 3.2 Gen1 and USB4 Gen2	≤ 2 m	3 A	Supported	Required
CC3G1-5					5 A		
CC3G2-3	C	C	USB 3.2 Gen2 and USB4 Gen2	≤ 1 m	3 A	Supported	Required
CC3G2-5					5 A		
CC4G3-3	C	C	USB4 Gen3	≤ 0.8 m	3 A	Supported	Required
CC4G3-5					5 A		

- Resource from Universal Serial Bus Type-C Cable and Connector Specification Release 2.0 -

Cable Vendor Defined Data Objects (VDO)



- Passive and Active Cable VDO
 - Minimum change to add USB4 support
 - Gen2 is the same for USB 3.2 and USB4
 - Gen3 gets a new value

Bit(S)	Field	Description
...		
B2...0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 100b...111b = Reserved, Shall Not be used

UFP / DFP Vendor Defined Data Objects (VDO)



- UFP VDO
 - Device capability at each speed
 - Highest USB Speed supported
- DFP VDO
 - Host capability at each speed
 - Port Number

Bit(s)	Field	Description										
...												
B27...24	Device Capability	<table><tr><th>Bit</th><th>Description</th></tr><tr><td>0</td><td>[USB 2.0] Device Capable</td></tr><tr><td>1</td><td>[USB 2.0] Device Capable (Billboard only)</td></tr><tr><td>2</td><td>[USB 3.2] Device Capable</td></tr><tr><td>3</td><td>[USB4] Device Capable</td></tr></table>	Bit	Description	0	[USB 2.0] Device Capable	1	[USB 2.0] Device Capable (Billboard only)	2	[USB 3.2] Device Capable	3	[USB4] Device Capable
		Bit	Description									
		0	[USB 2.0] Device Capable									
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		2	[USB 3.2] Device Capable									
3	[USB4] Device Capable											
B2...0	USB Highest Speed	000b = [USB 2.0] only, no SuperSpeed support 001b = [USB 3.2] Gen1 010b = [USB 3.2]/ [USB4] Gen2 011b = [USB4] Gen3 100b...111b = Reserved, Shall Not be used										

Bit(s)	Field	Description								
...										
B26...24	Host Capability	<table><tr><th>Bit</th><th>Description</th></tr><tr><td>0</td><td>[USB 2.0] Host Capable</td></tr><tr><td>1</td><td>[USB 3.2] Host Capable</td></tr><tr><td>2</td><td>[USB4] Host Capable</td></tr></table>	Bit	Description	0	[USB 2.0] Host Capable	1	[USB 3.2] Host Capable	2	[USB4] Host Capable
		Bit	Description							
		0	[USB 2.0] Host Capable							
		1	[USB 3.2] Host Capable							
2	[USB4] Host Capable									
B4...0	Port Number	Unique port number to identify a specific port on a multi-port device.								

USB4™ Discovery and Entry Process



1. CC Connection for DFP/UFP
2. Initial VBUS and VCONN power applied
3. USB Power Delivery establish Power Contract



For All USB Connection

4. DFP Discovery Identity **Port Partner SOP** Capability
5. DFP Discovery Identity **Cable SOP** Capability
6. If the cable and port partner both support USB4, DFP issue USB Power Delivery **“Enter_USB”** Message to enter USB4 operation.

7. If both port partners are DRD capable, Data-role Swap will be initiated if the port partners wants to change to host/device role

USB Power Delivery Requirement

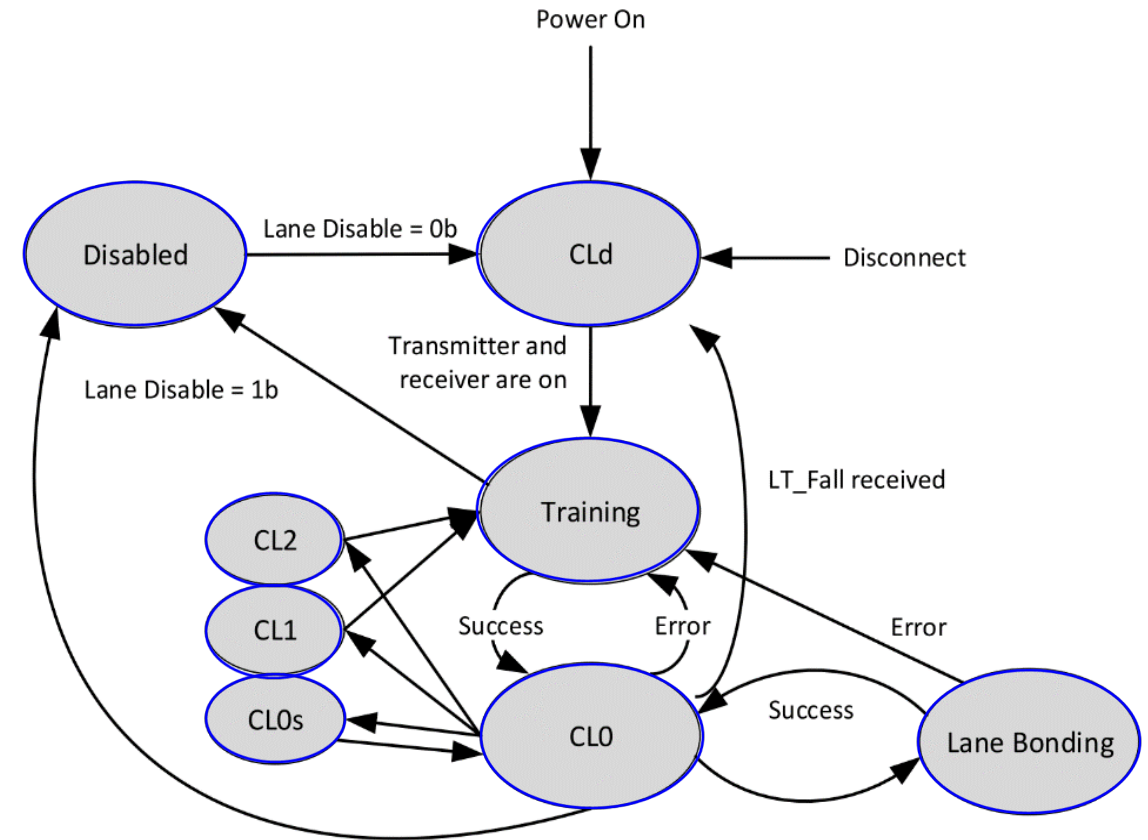


- Support of both USB Power Delivery 2.0 and USB Power Delivery 3.0 is still required
- Originally there were three specs:
 - Two for USB Power Delivery 2.0 and one for USB Power Delivery 3.0
 - Compliant device must pass all three
- New USB Power Delivery 3.0 Compliance spec:
 - Combines three existing specs into a single document
 - Single approach for all tests required for USB Power Delivery 3.0 device
 - Adds requirement to run certain tests in both USB Power Delivery 2.0 and USB Power Delivery 3.0 modes
 - Specifies how the Tester shall respond to all UUT initiated messages, regardless of whether they are part of the normal test steps

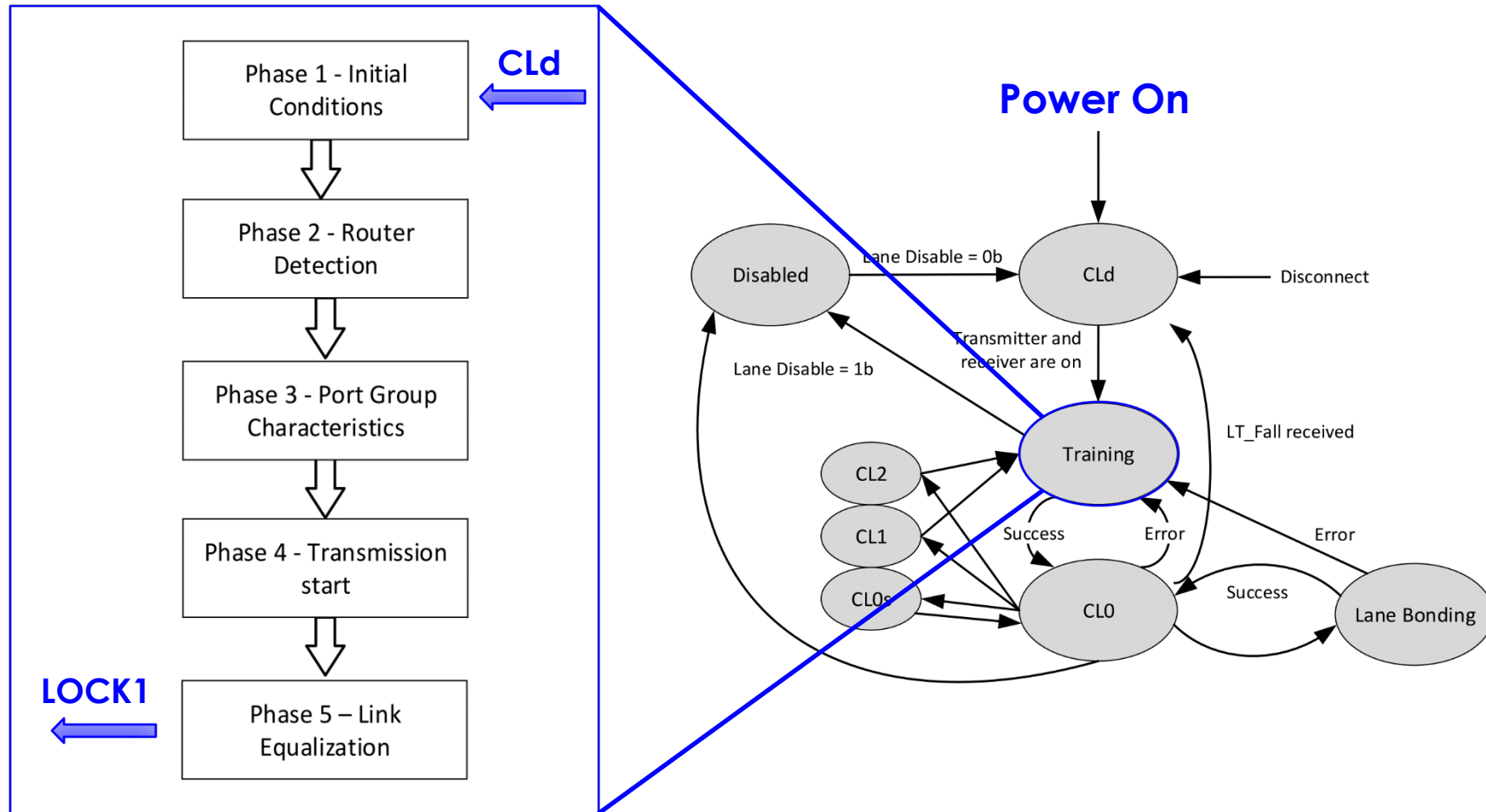
USB PD 2.0_Communication Engine USB PD Compliance
USB PD 2.0 _Deterministic USB PD Compliance
USB PD 3.0 CTS

Logical Layer State Machine

- **Disabled state** – The Lane Adapter disables the Lane.
- **CLd state** – Lane Adapter transmitter and receiver are inactive.
- **Training state** – The Lane Adapter performs Symbol synchronization and transfer of Lane parameters.
- **CL0 state** – The Lane Adapter can transmit and receive Transport Layer Packets across the Lane.
- **Lane Bonding state** – bonds two Single-Lane Links into a Dual-Lane Link.
- **CL0s, CL1, CL2 states** – low power states.



Lane Initialization



Agenda

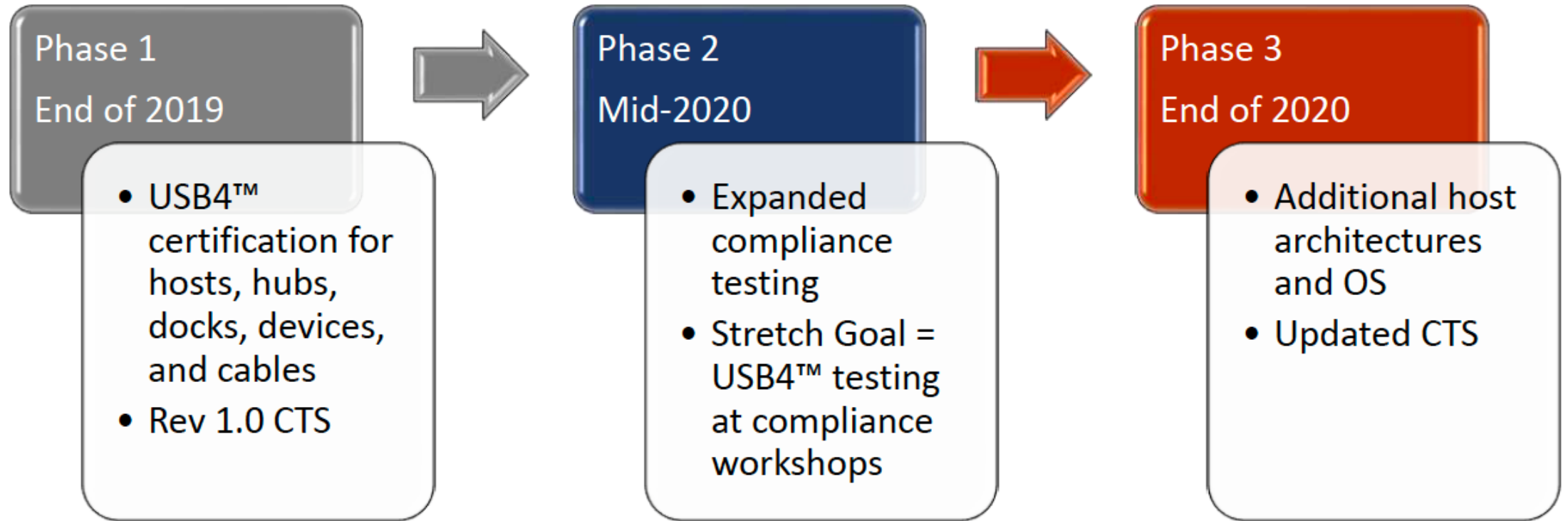
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USB4™ Compliance Testing Overview



- **USB4 spec is based on Thunderbolt™ 3**
 - Electrical Compliance Test is similar to TBT3
 - Test Items include all supported features
- **USB4™ Compliance Test items - Summary:**
 - USB PD Compliance
 - USB Type-C® Compliance
 - USB 2.0 Compliance
 - USB 3.2 Compliance
 - USB4™ Compliance

USB4™ Compliance Timeline



USB4™ Certification Process



1. Pass USB 2.0, USB 3.2, USB Power Delivery, and USB Type-C® compliance tests
2. Complete USB4™ Pre-Certification testing and requirements
3. Submit product for certification
4. Perform USB4 Compliance testing at test lab
5. Send test results to USB-IF
6. Get notification from USB-IF with status (pass or fail)



Pre-Certification Testing and Requirements

- **Generate Vendor Info File (VIF)**
- **Show that used certified components**
 - Certified Connector
 - Certified Silicon (if end product)
- **Run subset of USB4™ compliance tests and produce logs**

Will be posted on www.USB.org

USB4™ Certification Categories

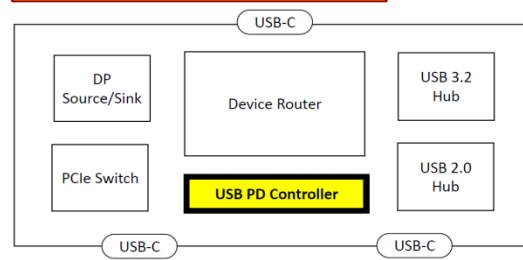


		
USB4 Host	✓	✓
USB4 Hub	Not Allowed	✓
USB4-Based Dock	Not Allowed	✓
USB4 Peripheral Device	✓	✓
USB4 Active Cable	✓	✓
USB4 Passive Cable	✓	✓

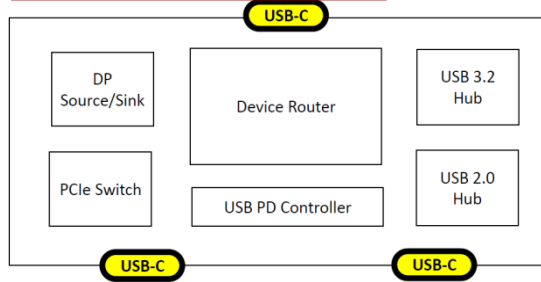
Required Testing – USB4™ Hubs/Docks

- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- USB 3.2 Compliance
- USB4™ Compliance
 - Tunneling
 - TBT3-Compatibility

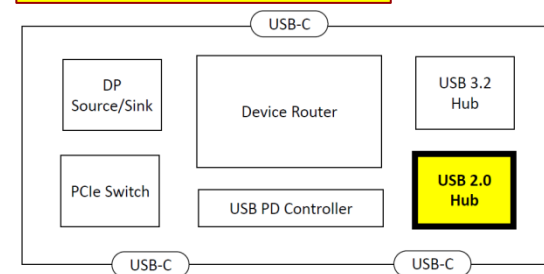
USB PD Compliance



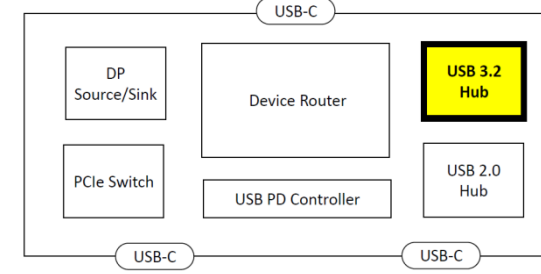
Type-C Compliance



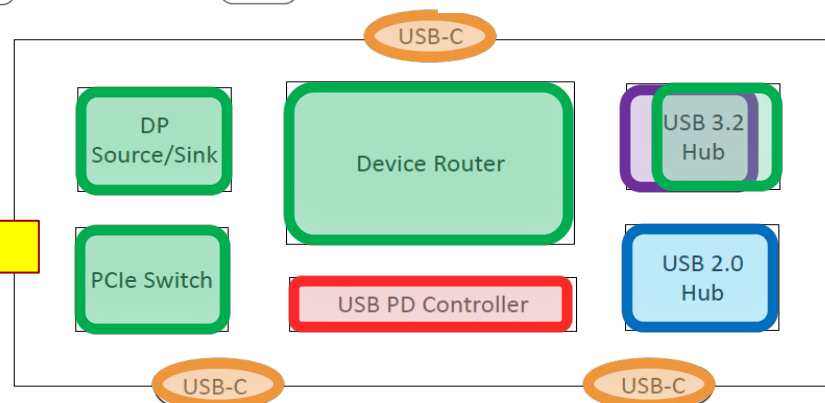
USB 2.0 Compliance



USB 3.2 Compliance

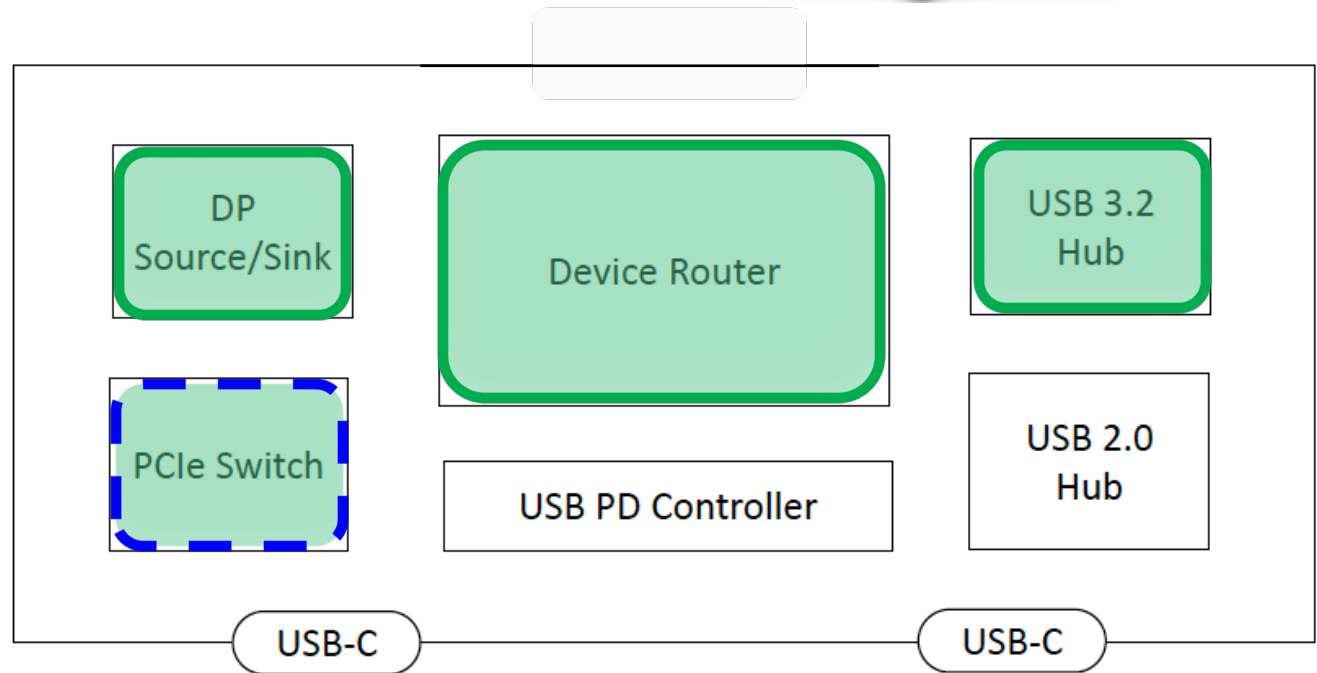


USB 4 Compliance



Required Testing – USB4™ Hosts

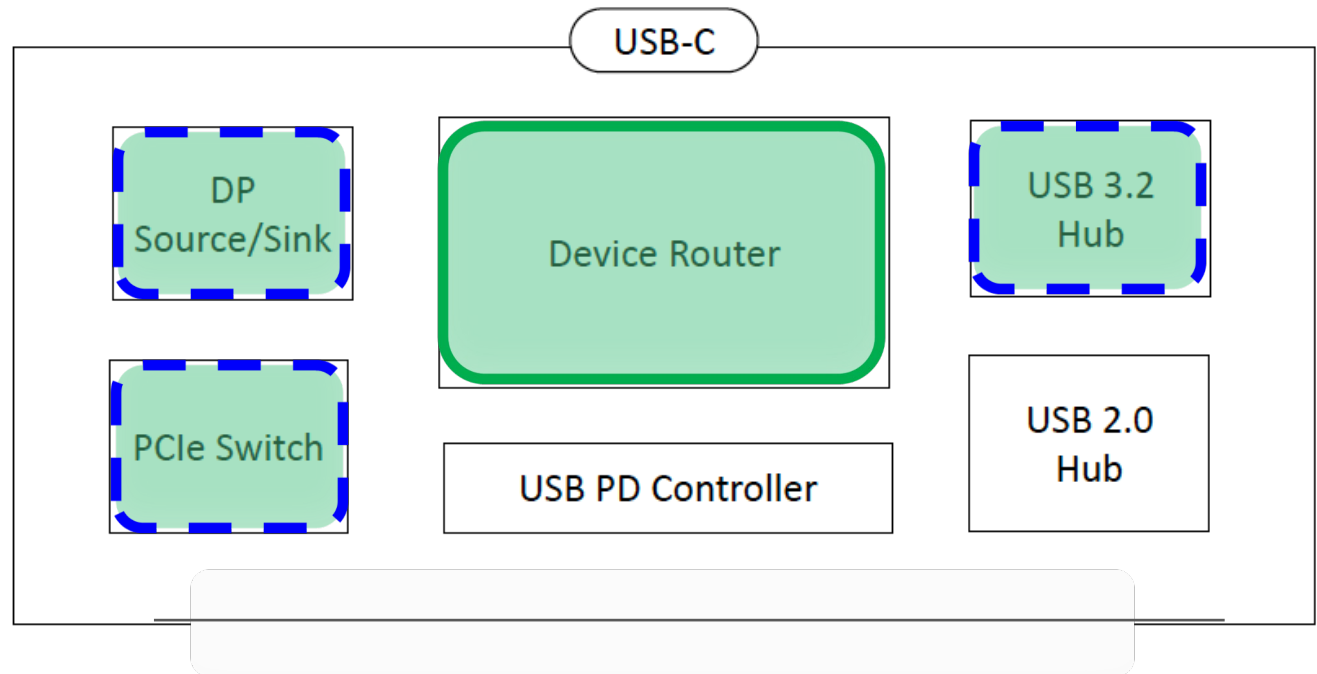
- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- USB 3.2 Compliance
- **USB4™ Compliance**
 - DP & USB 3.2 Tunneling
 - **If Supported:**
 - **PCle Tunneling**
 - **TBT3-Compatibility**



Required Testing – USB4™ Devices



- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- **USB 3.2 Compliance**
 - If Supported
- **USB4™ Compliance**
 - If Supported:
 - DP Tunneling
 - USB 3.2 Tunneling
 - PCIe Tunneling
 - TBT3-Compatibility



Silicon vs. End Product



Silicon



Physical component that gets integrated into product

End Product



Product that end user can go buy

USB4™ Test Matrix



	Host Silicon	Host End Product	Dock Silicon	Dock End Product	Hub Silicon	Hub End Product	Device Silicon	Device End Product
Electrical	✓	✓	✓	✓	✓	✓	✓	✓
Logical Layer	✓	✓	✓	✓	✓	✓	✓	✓
Protocol	✓	✗	✓	✗	✓	✗	✓	✗
TMU	✓	✗	✓	✗	✓	✗	✓	✗
H2H Tunneling	✓	✓	✗	✗	✗	✗	✗	✗
USB3 Tunneling	✓	✓	✓	✓	✓	✓	If Supported	If Supported
DP Tunneling	✓	✓	✓	✓	✓	✓	If Supported	If Supported
PCIe Tunneling	If Supported	If Supported	✓	✓	✓	✓	If Supported	If Supported
USB4 Interop	✓	✓	✓	✓	✓	✓	✓	✓
TBT3-Compatability	If Supported	If Supported	✓	✓	✓ (DFP only)	✓ (DFP only)	If Supported	If Supported

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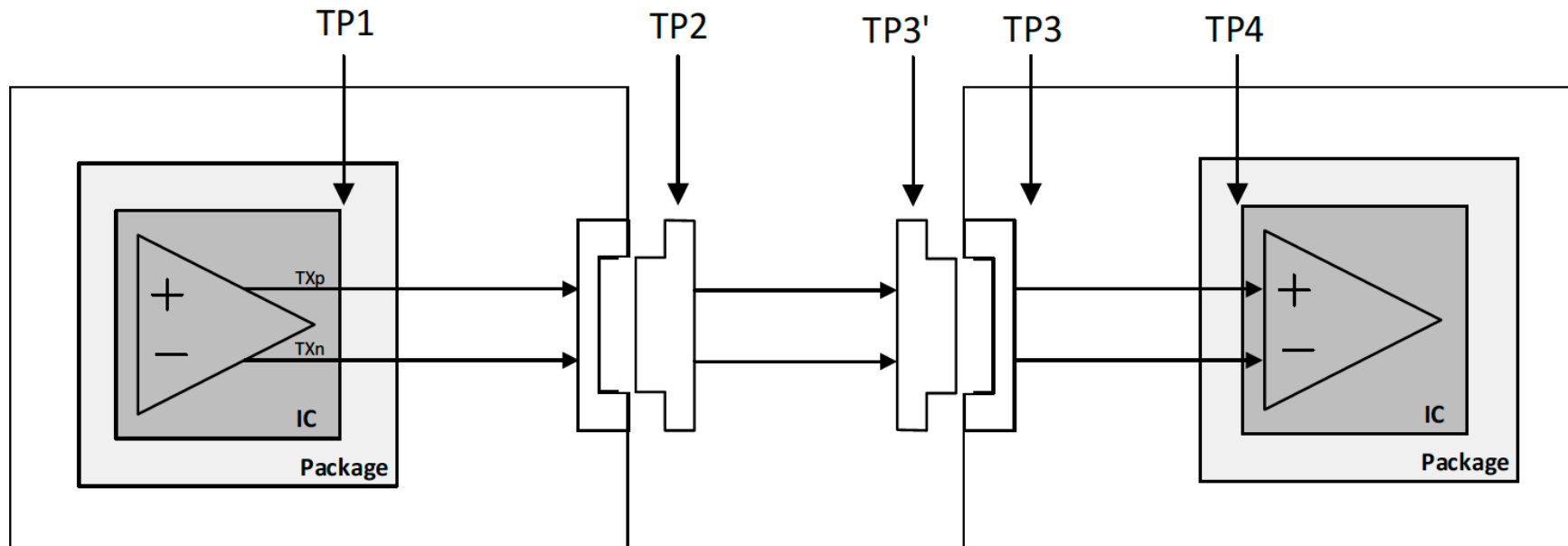
USB4™ Electrical Compliance Points Definition

■ Tx Test Point

- **TP2**: at the plug connected to the Router Assembly TX output.
- **TP3**: at USB Type-C receptacle output on the far-end side of passive cable.

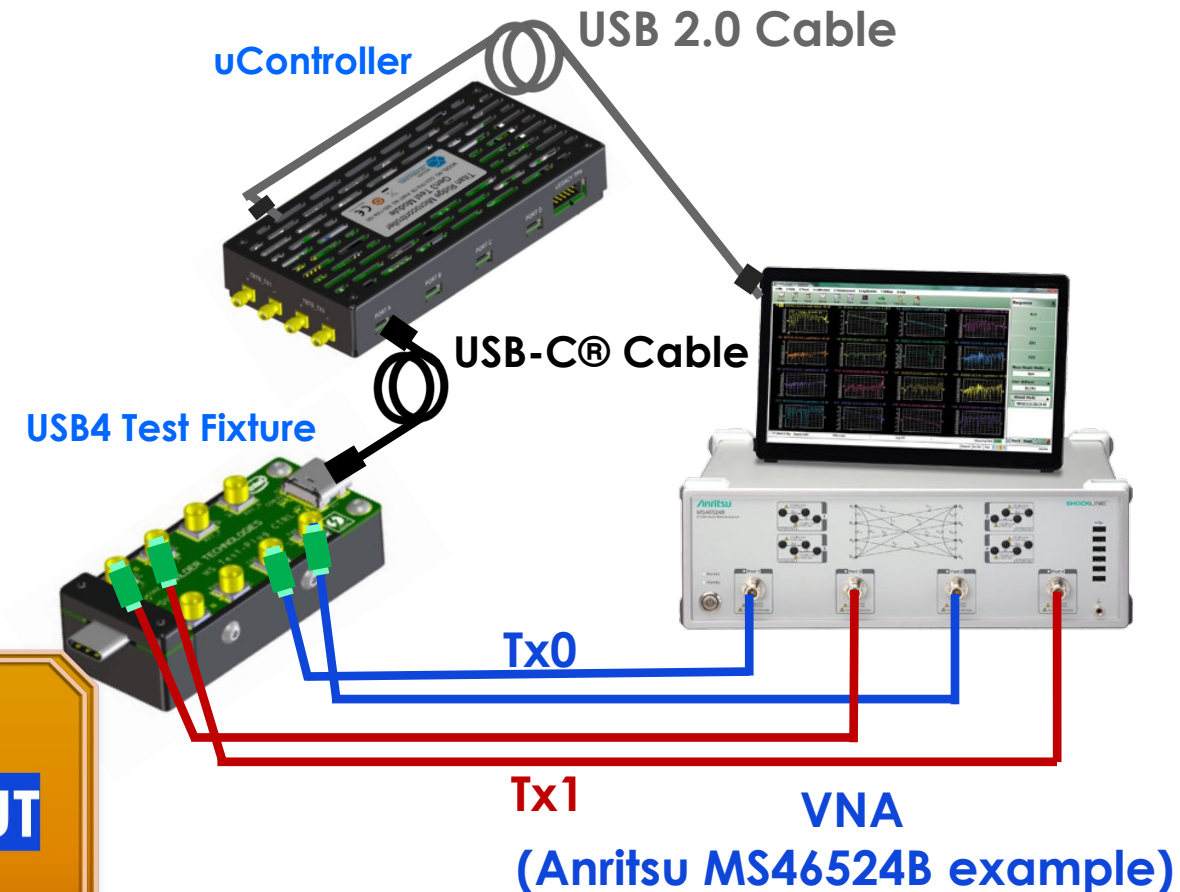
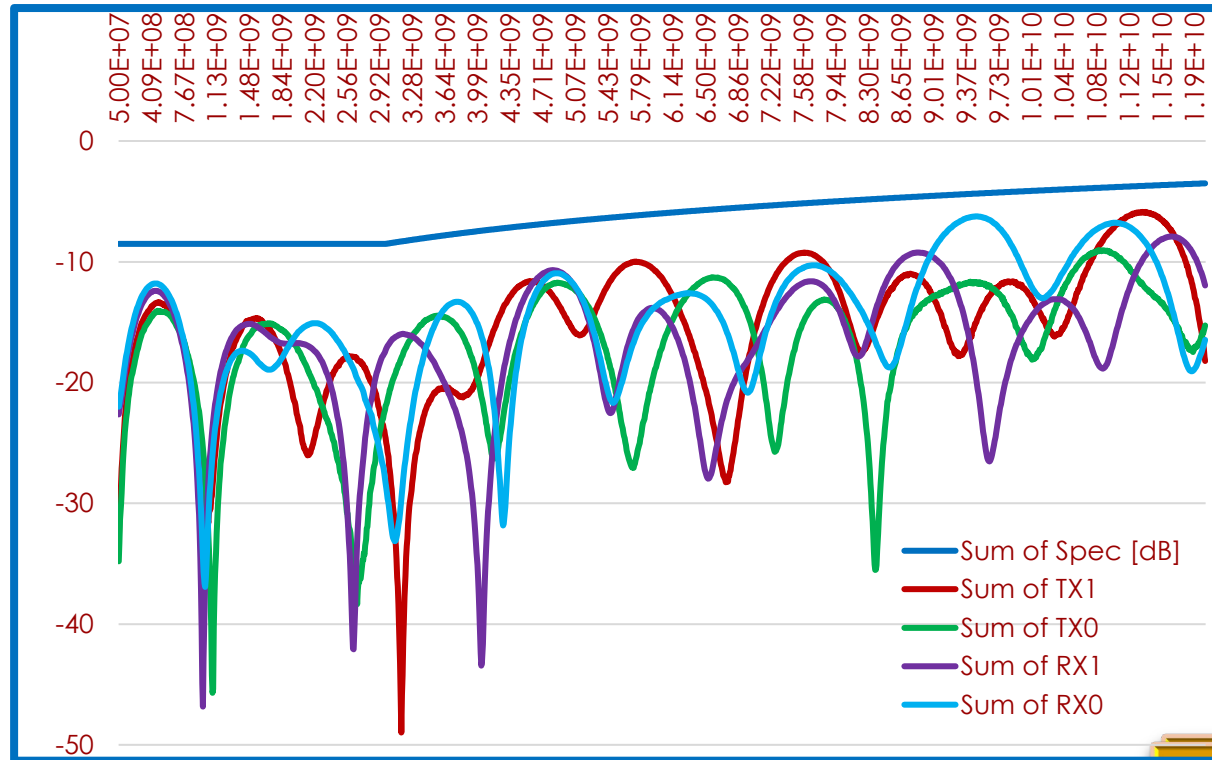
■ Rx Test Point

- **TP3'**: At the plug side of the Router Assembly RX input.
- **TP3**: at USB Type-C receptacle output on the far-end side of passive cable.



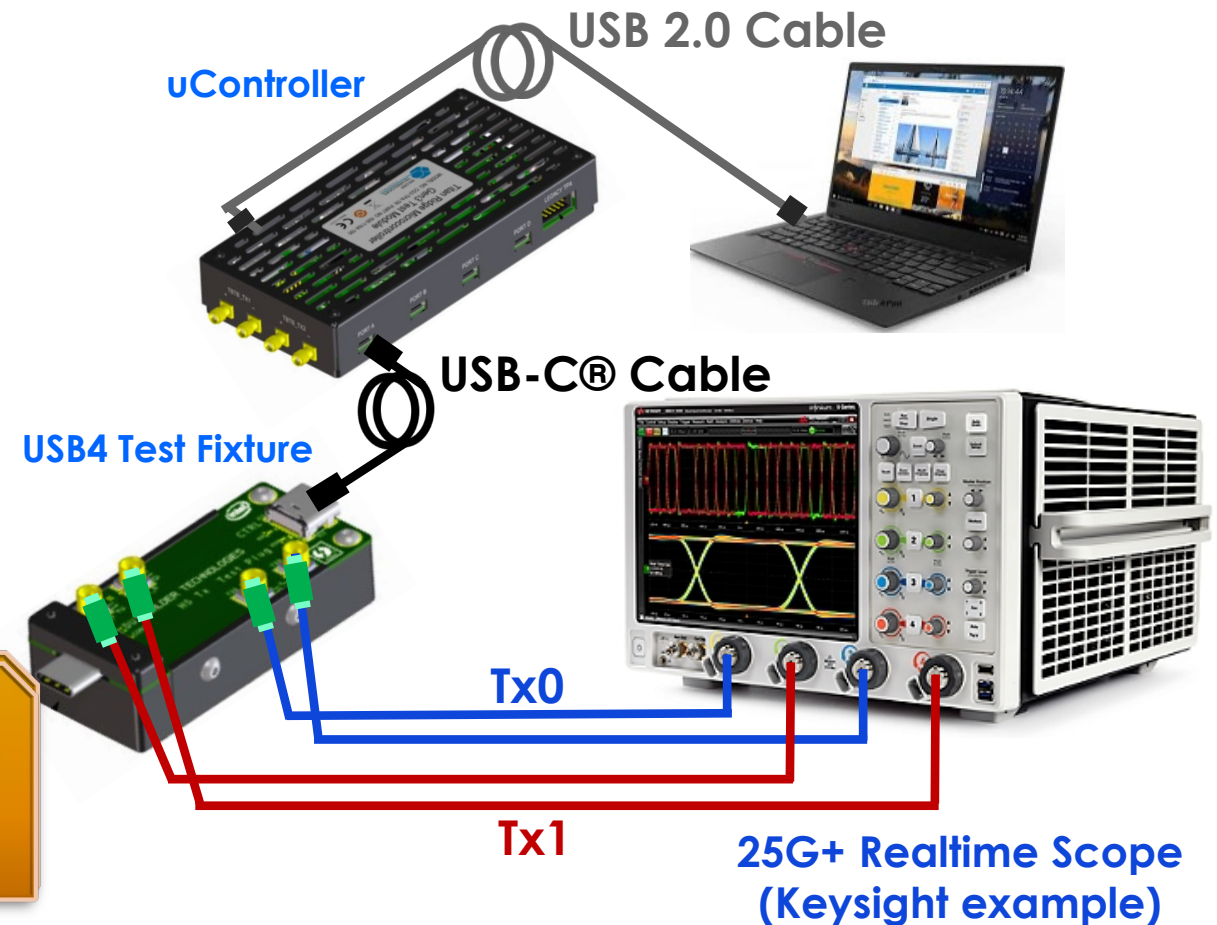
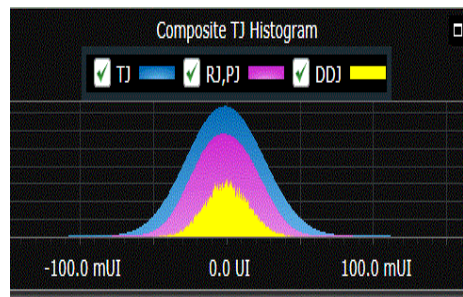
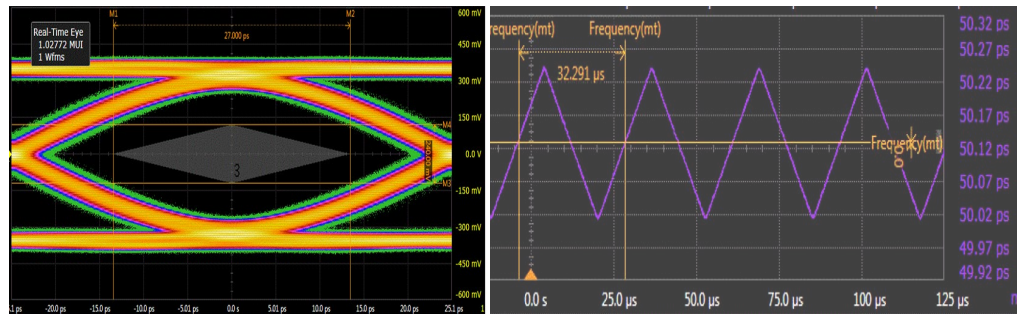
USB4™ Electrical Testing – Return Loss

■ Test with DUT Transmitting PRBS31 Pattern



USB4™ Electrical Testing - Transmitter

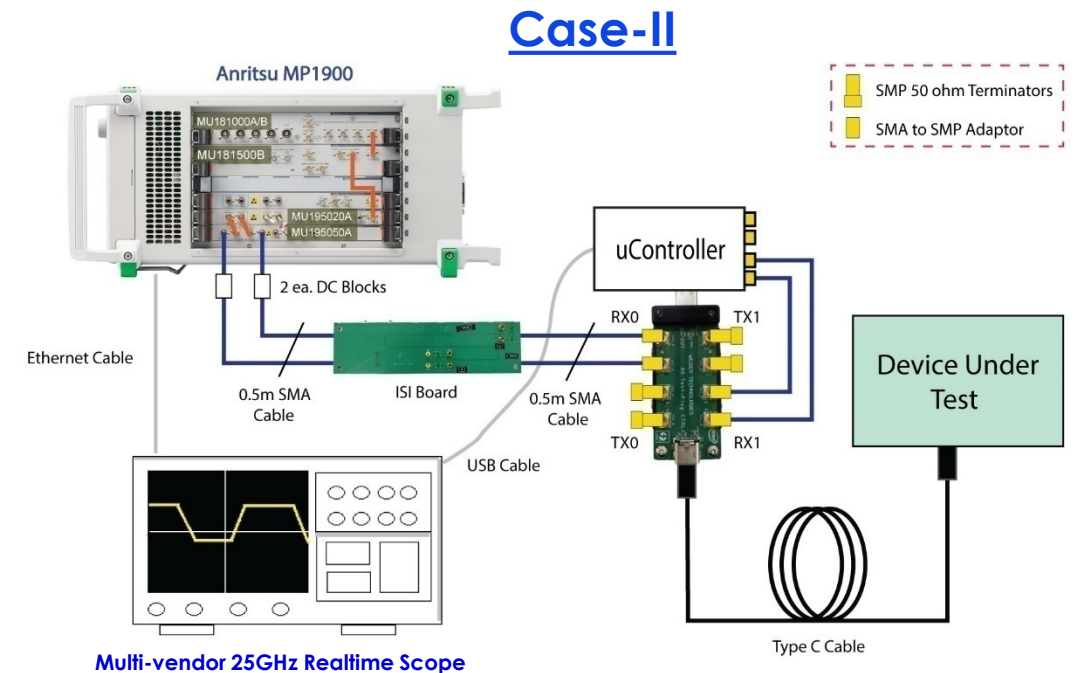
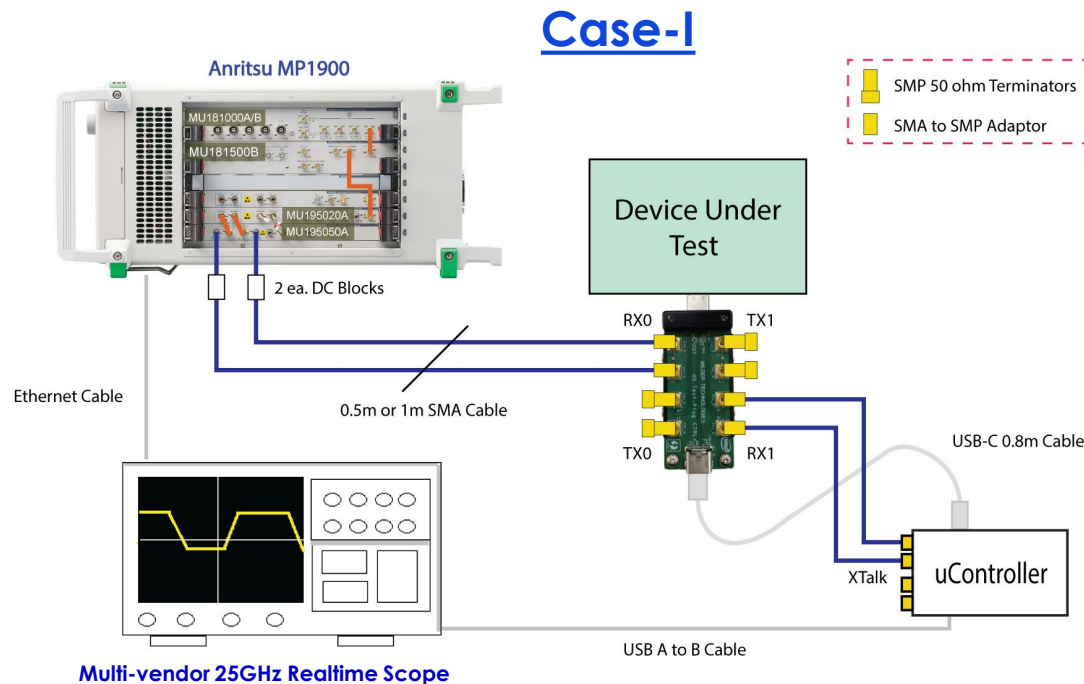
- Tx FFE
- Unit Interval
- SSC
- Rise/Fall Time
- E-Idle Voltage
- Jitter
- ACCM
- Eye Diagram



USB4™ Electrical Testing - Receiver

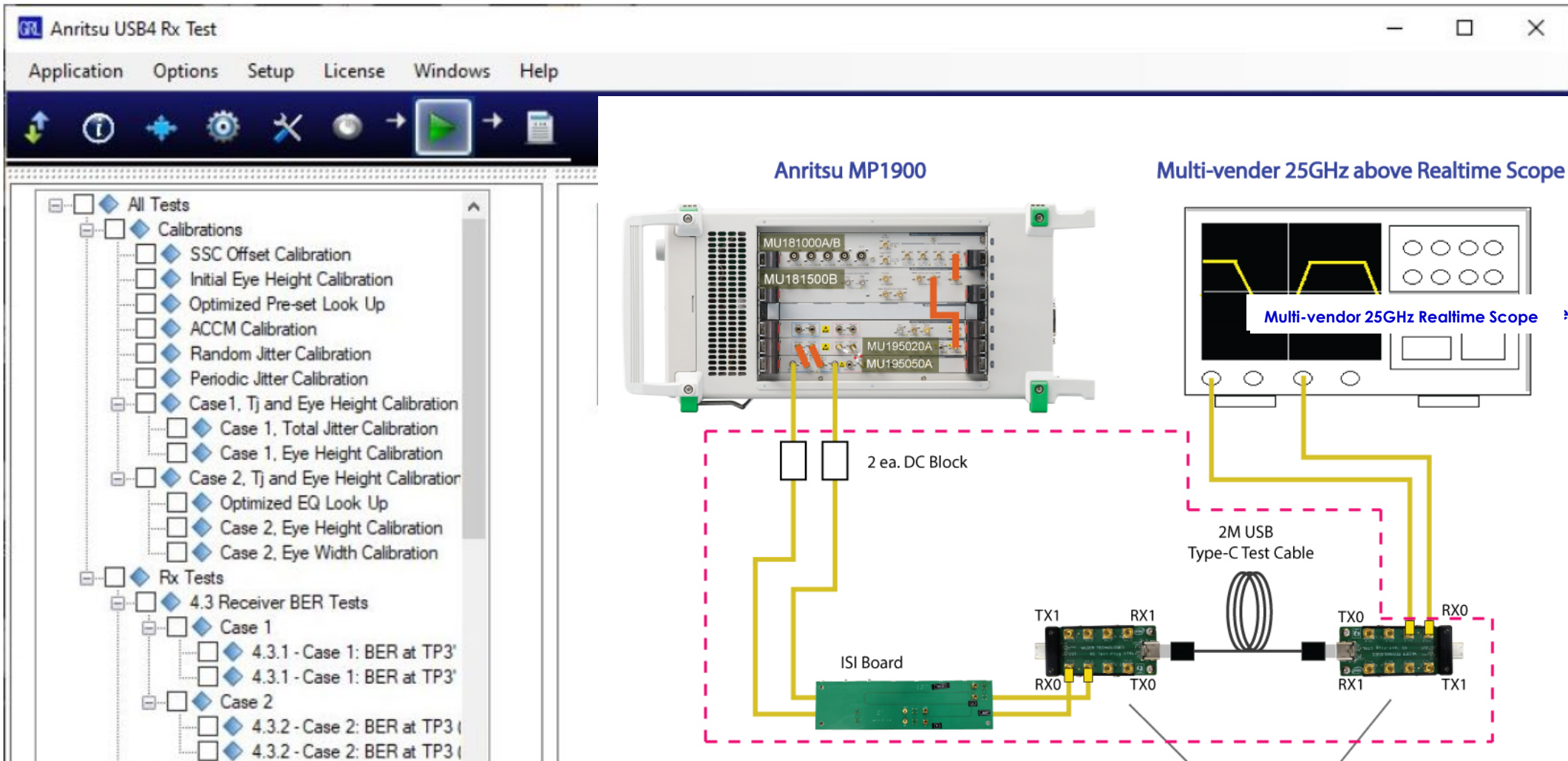
■ Rx Stress Signal (20 stress conditions)

- 10G Case-I : 5 * $S_j = 1/2/10/50/100\text{MHz}$
- 10G Case-II : 5 * $S_j = 1/2/10/50/100\text{MHz}$
- 20G Case-I : 5 * $S_j = 1/2/10/50/100\text{MHz}$
- 20G Case-II : 5 * $S_j = 1/2/10/50/100\text{MHz}$



GRL TBT3 & USB4™ Receiver Test Software

for Anritsu MP1900A and Tek/Keysight Scopes



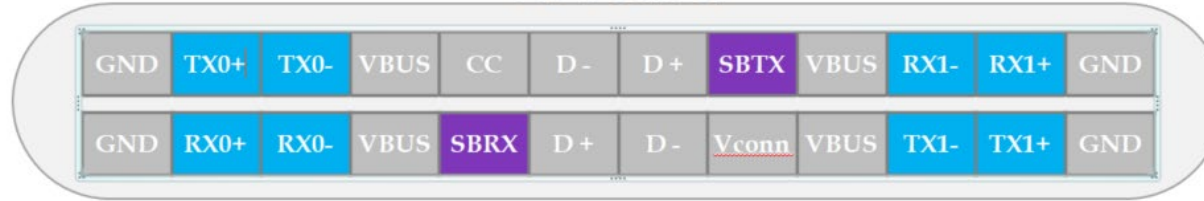
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USB4™ Electrical Testing- Sideband Signal

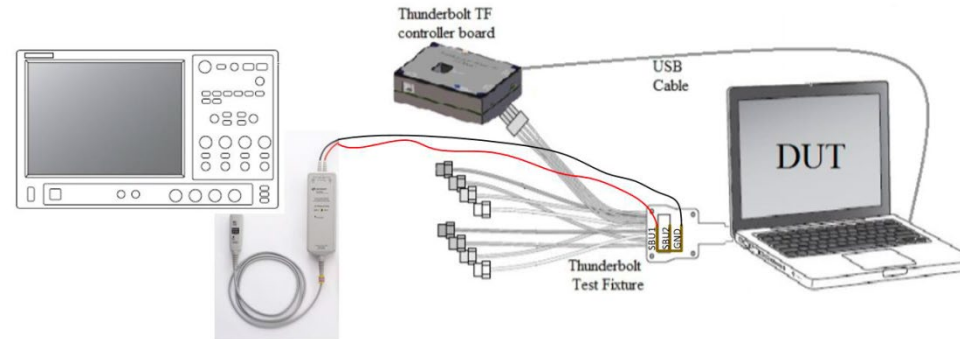


USB4 Pinout



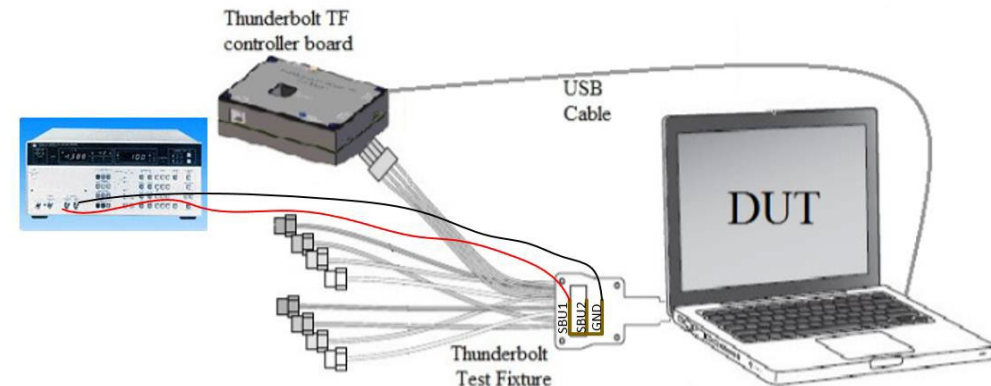
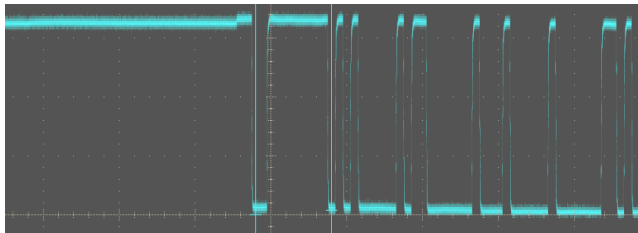
■ Sideband Tx Test

- High/Low Voltage
- Rise/Fall Time
- UI Duration



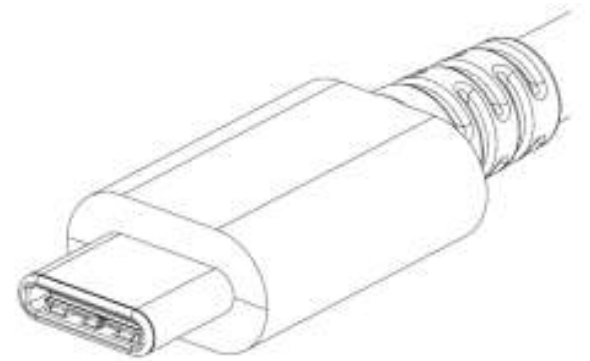
■ Sideband Rx Test

- Should Detect Voltage $\geq 2.0V$
- Shouldn't Detect Voltage $\leq 0.65V$




USB Type-C® Cables and Connectors Testing

- No change on mechanical spec



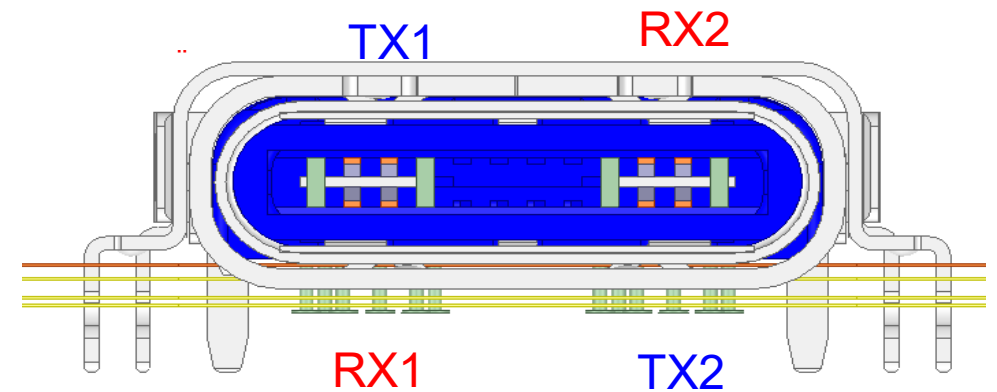
Looking into the product receptacle:



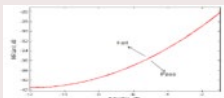
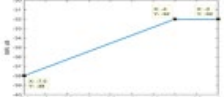
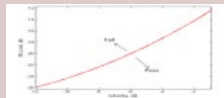
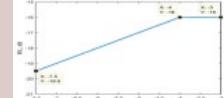
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Mated Connector Electrical Spec:

- USB 3.2 and USB4™ Gen 2: Informative
- USB4 Gen3: Normative



USB Type-C® CableConn Spec

USB4	USB4 Gen2 Conn (Informative)	USB4 Gen3 Conn (Normative)	USB4 Gen2 Cable USB3.2 Gen2 Cable	USB4 Gen3 Cable
ILfitatNq	≥ -0.6 dB @ 2.5 GHz ≥ -0.8 dB @ 5.0 GHz ≥ -1.0 dB @ 10 GHz	≥ -0.6 dB @ 2.5 GHz ≥ -0.8 dB @ 5.0 GHz ≥ -1.0 dB @ 10 GHz ≥ -1.25 dB @ 12.5 GHz ≥ -1.5 dB @ 15 GHz	USB4 Gen2 (2m) ≥ -7 dB @ 2.5 GHz ≥ -11.5 dB @ 5.0 GHz USB3.2 Gen2 (1m) ≥ -4 dB @ 2.5 GHz ≥ -6 dB @ 5.0 GHz ≥ -11 dB @ 10 GHz	USB4 Gen3 (0.8m) ≥ -1 dB @ 100 MHz ≥ -4.2 dB @ 2.5 GHz ≥ -6 dB @ 5.0 GHz ≥ -7.5 dB @ 10 GHz ≥ -9.3 dB @ 12.5 GHz ≥ -11 dB @ 15 GHz
IMR	-40 dB	-39 dB	Normative 	Informative 
INEXT	-44 dB	-43 dB	-40 dB@INEXT	-43 dB @ INEXT -50 dB @ INEXT_p2p
IFEXT	-44 dB	-43 dB	-40 dB@IFEXT	-43 dB @ IFEXT -50 dB @ IFEXT_p2p
IRL	-18 dB	-15 dB		
Differential Crosstalk on D+/D-	-40dB@100M~5G -40dB@5G to -36dB @7.5G	-50 dB	IDDXT_1NEXT + FEXT ≤ -34.5 IDDXT_2NEXT ≤ -33 dB	Same as Gen2 and Add DP mode: 3 FEXT
SCD12 / SCD21 Mode Conversion	-30 dB@ 100M~2.5G -25 dB@ 2.5G~7.5G -20 dB@ 7.5G~10G	-20 dB @100M~10G	-20 dB @ 100M~10G	-17 dB @ 100M~10G

USB Type-C® Cable Compliance Test for USB4 (not yet final)



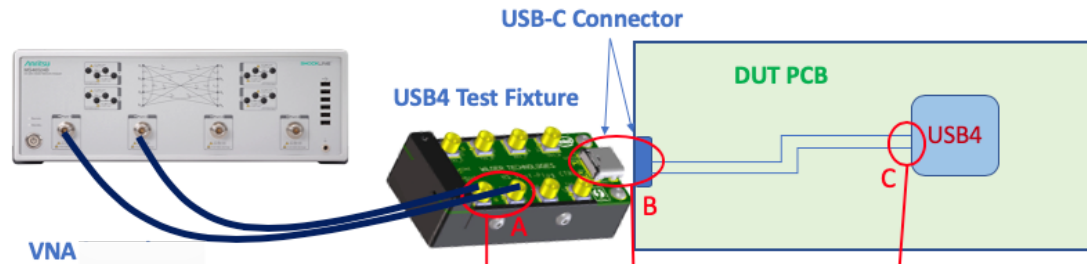
- The USB Type-C Cable/Connector Compliance Spec for USB4™ is still under development.
- The main spec items for USB Type-C cables in support USB4 Gen3 are:
 - Insertion fit (normative)
 - IMR (informative)
 - IRL (normative)
 - IXT_USB/IXT_DP (normative)
 - Mode conversion
 - Shielding effectiveness
 - COM (Channel Operation Margin) (normative)
- USB-IF will provide necessary supporting collaterals to extract/calculate the spec parameters

Agenda

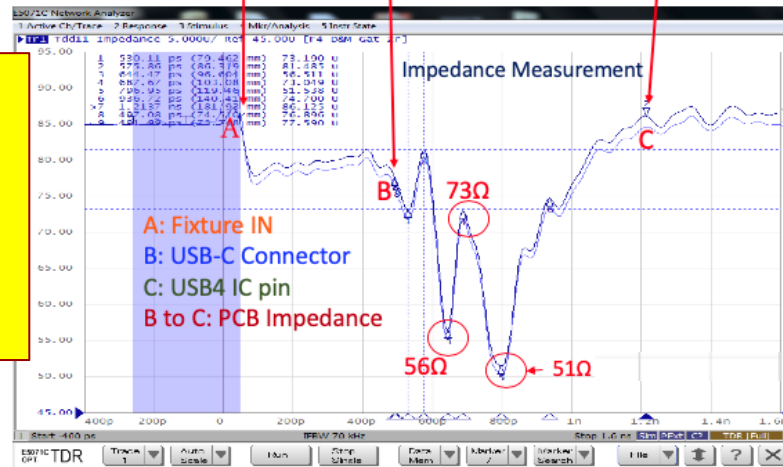
- **USB4™ Overview**
- **USB4™ Link Process**
 - Discovery and Entry
 - USB4 Link Training
- **USB4™ Compliance Testing Overview**
 - USB4 Hub & Docks/ Host/Device
 - USB4 Cable Connector
- **USB4™ Electrical Testing**
- **Design & Test Considerations**
- **Q & A**

Case Study: Transmitter Test Eye Diagram Failure

- Eye Diagram
 - Eye Mask @ 20Gbps: **Marginal Fail**
 - Return Loss: **Marginal Pass**

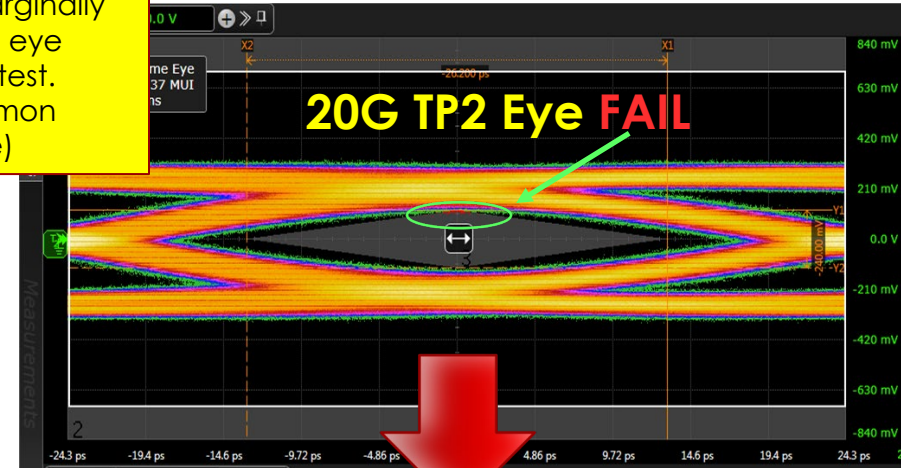


3. Additional investigation using TDR analysis shows fairly dramatic discontinuities between B-C on DUT PCB

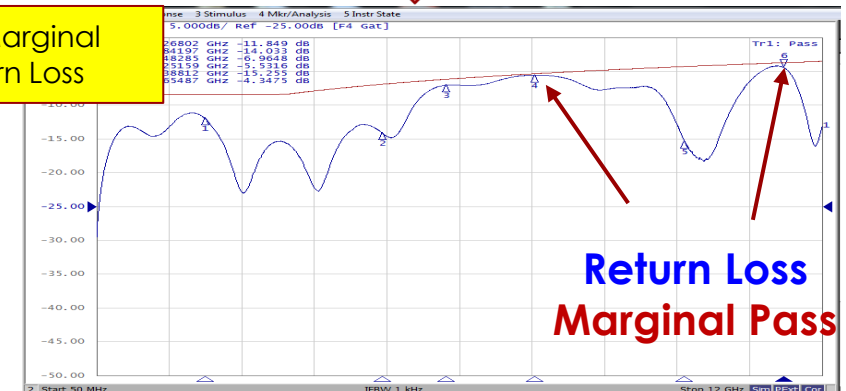


Impedance Measurement (not required by CTS)

1. Marginally failing eye mask test. (common failure)



2. Marginal Return Loss



Return Loss
Marginal Pass

Return Loss Measurement

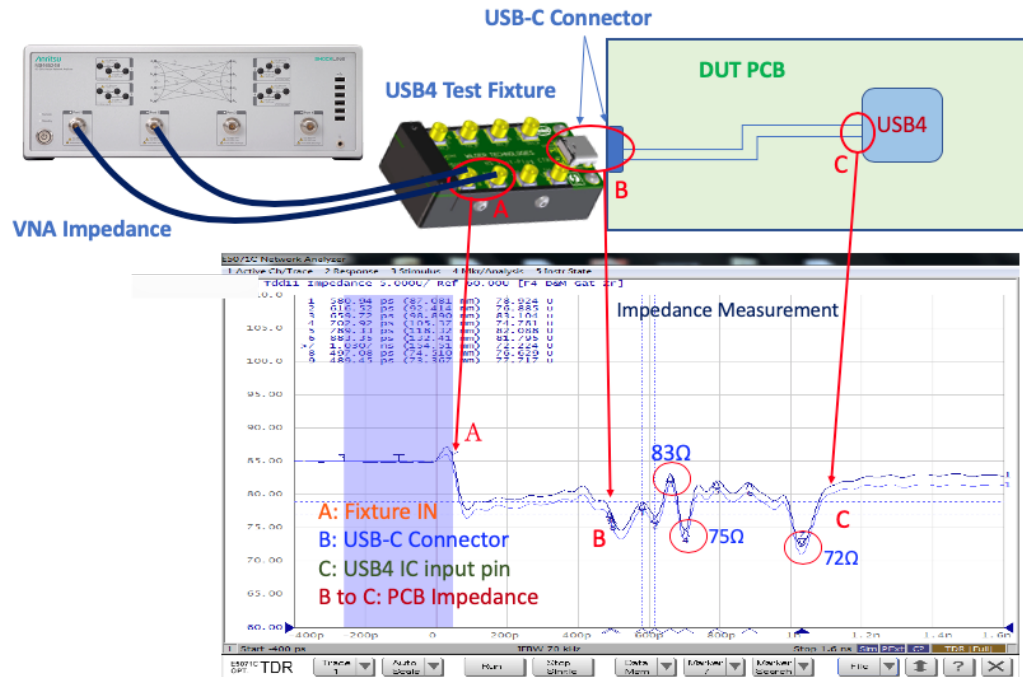
Investigation with Return Loss and TDR measurements shows dramatic discontinuities on path between B-C on DUT PCB.

Case Study: Transmitter Test Eye Diagram Failure

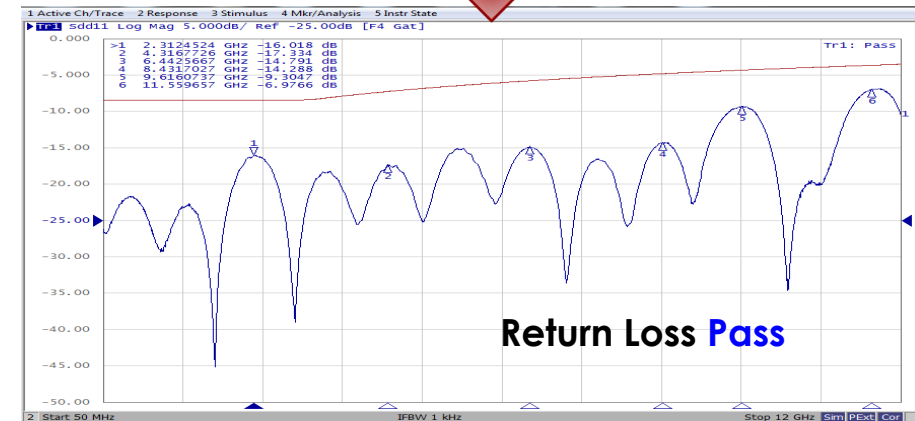
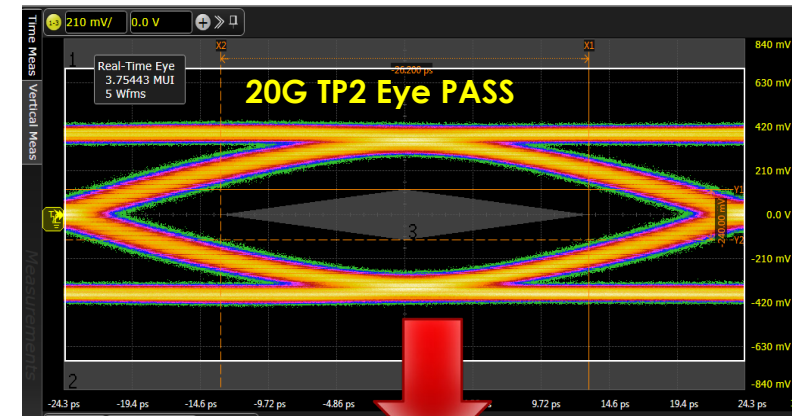
- **PCB re-design and improvements on B-C path allowed the DUT to pass the Eye Mask test**
 - Required changes in capacitor size – 0402 to 0201
 - Placement of components on B-C path—moved closer to Type C connector

■ Eye Diagram

- Eye Mask @ 20Gbps: **PASS**
- Return Loss: **PASS**



Impedance Measurement
(big dip between B-C addressed)



Return Loss Measurement
(improved margin at higher frequencies)

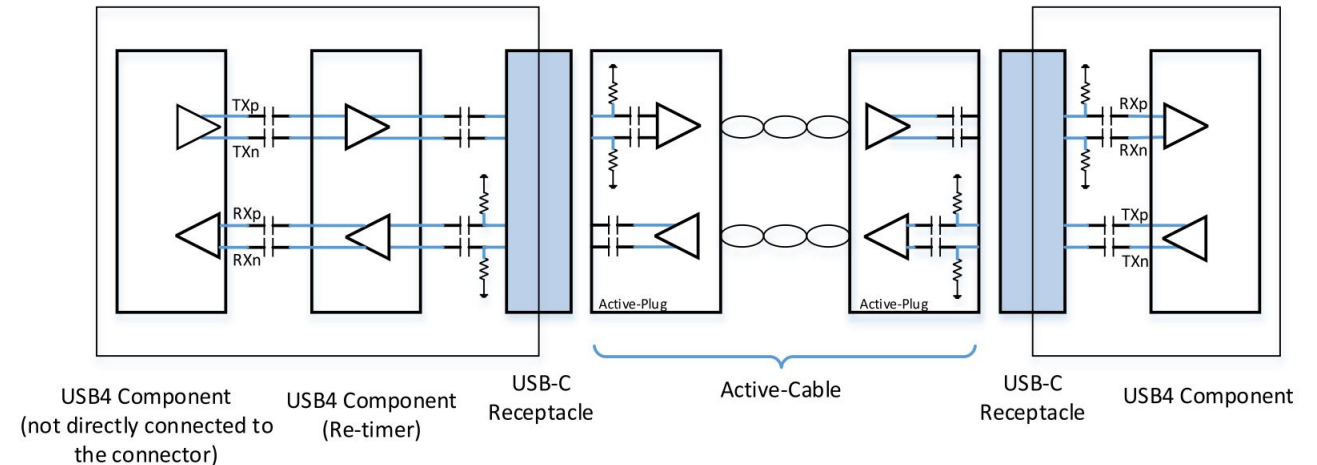
USB4™ Component Selection

■ AC-Caps and Discharge Resistors

- Smaller size components (e.g. 0201) with better return loss (smaller parasitic) than larger ones (0402)

■ ESD

- $RL < -13\text{dB}@10\text{GHz}$ &
- Differential IL > $0.3\text{dB}@10\text{GHz}$



■ PCB Material

- PCB Thickness: The tradeoff for thinner PCBs is higher trace loss
- Optimizing trace geometry
- PCB dielectric material and copper has large impact to trace loss at USB4



Questions?

Thank you for your time!

Quintin Anderson, Co-Founder & COO

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Vamshi Kandalla, EVP & GM

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GRL is your end-to-end USB4™ partner:

- **USB4™ Compliance Testing & Debugging Lab Services World-Wide**
- **USB4™ Compliance Test Automation Solutions**
 - *User-friendly, efficient, flexible, multi-vendor*



Anritsu
MS46524B VNA



Anritsu
MP1900 BERT



Multi-vendor
25G Realtime Scope

Return Loss Test SW
GRL-USB4RL-AN

Tx & Rx Test SW
GRL-USB4-RXA
GRL-USB4-TX

