Granite River Labs

GRL-PCIE5-CEM-RXA PCI Express Card Electromechanical (CEM) 5.0 (32 GT/s)

Receiver Compliance Test Automation Solution User Guide and MOI

Using GRL-PCIE5-CEM-RXA Automation Test Software, Anritsu MP1900A BERT, and High Performance Oscilloscope

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1 Introduction

This user manual provides information using the GRL-PCIE5-CEM-RXA test automation solution to set up and test an electrical receiver (Rx) device to meet PCI Express Card Electromechanical (CEM) 5.0 compliance for 32 GT/s as per PCI Express (PCI-SIG) Standards.

The main body of this documentation first describes how to configure the GRL-PCIE5-CEM-RXA test software to calibrate the stressed eye at the receiver of the device under test (DUT) in the PCIe Gen 5.0 system. This includes calibration to be performed at both the physical Test Point 3 (TP3) and the Long Channel at TP2. The GRL software will automate calibration without channel effect at TP3 before measuring the eye opening due to trace length. It also enables running the SigTest and Seasim post processing analysis application to ensure signal quality compliance. The final calibrated eye diagram uses both the SigTest and Seasim software to achieve the final stressed eye calibration.

After completing calibration, the GRL-PCIE5-CEM-RXA software will automate compliance testing for the receiver using Bit Error Ratio (BER) as a metric. The receiver path is tested with worst case eye to ensure a BER of less than 1E-12 can be achieved. The software also provides an optional SJ margin search test for the DUT.

The GRL-PCIE5-CEM-RXA software performs test automation according to PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes and Anritsu BERT using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's). The GRL software is run from the computer or oscilloscope to provide automation control to test the DUT for PCIe CEM 5.0 Rx electrical compliance. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

Note: For manual test methodology, refer to Appendix of this documentation or PCI-SIG for approved Method of Implementation (MOI's) as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS AND ACCESSORIES

System & Accessory	Qty.	Description/Key Spec Requirement
High Performance Real-time Oscilloscope [a]	1	≥ 50 GHz bandwidth [b]
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer [c] • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator, or MU196020A 64.2G bit/s or 64.2G baud PAM4 Pulse Pattern Generator [d] • MU195040A 21G/32G bit/s SI Error Detector • MU195050A Noise Generator
PCI-SIG Compliance Base Board (CBB) or PCI-SIG Compliance Load Board (CLB)	1	For add-in cards For host system boards
ISI Source Generator	1	Compliant Variable ISI channel
Power Splitter (K241C) or Pick-off Tee (J1510A)	2	For connecting scope to CLB/CBB Tx lanes to perform link equalization tests
Terminator	1	J1632A Coaxial Terminator, for termination of unused MU195020A/MU196020A Aux Out connector during link equalization testing
V(m) - K(f) Adapter	*2*	*34VKF50A Coaxial Adapter, only required if using a PAM4 Pulse Pattern Generator*

System & Accessory	Qty.	Description/Key Spec Requirement
PCIe5 Re-Driver		J1890A [e] PCIe5 Re-Driver Set with AH54192A [e] 56Gbaud Differential Linear Amplifier or G0430A PCIe5 Re-Driver Set [f] For Return Path optimization in the System Tx/Rx Link Equalization Test
Computer (laptop or desktop)	1	Windows 7+ OS For automation control

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

[c] MU181000B Option 02 is required for testing the System Board DUT.

[d] The GRL-PCIE5-CEM-RXA software supports PAM4 PPG in NRZ mode.

[e] The J1890A and AH54192A are packaged separately. Check the contents of both boxes. The AH54192A is supplied as a set with dedicated power supply AH54192A-01. See Appendix B for more details.

[f] See Appendix C for more details.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable [a]	Qty.
SMA-to-SMA cable	4
SMA coaxial cables	1 pair
Phase matched K-K coaxial cables	3 pairs
J1746A K-K cable set *(to connect between MU195020A and MU195050A)*	1
J1627A GND connection cable	1
BNC-to-SMA cable	1

[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
GRL-PCIE5-CEM-RXA	Granite River Labs PCI Express Card Electromechanical 5.0 (32 GT/s) Automated Receiver Calibration and Compliance Test Solution – www.graniteriverlabs.com
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-PCIE5-CEM-RXA software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
MX183000A	Anritsu High-Speed Serial Data Test Software – For loopback BER testing of the PCIe Gen 5 CEM DUT receiver. This software is located in the MP1900A BERT.
SigTest Application	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html
Seasim	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software) – www.pcisig.com

3 Setting Up GRL-PCIE5-CEM-RXA Automation Software

This section provides the procedures to start up and pre-configure the GRL-PCIE5-CEM-RXA automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the GRL software, follow the procedures in the following sections.

3.1 Download GRL-PCIE5-CEM-RXA Software

Download and install the GRL software as follows:

1. If the GRL software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where GRL-PCIE5-CEM-RXA is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIECEMGen5_AN_PatternFilesInstallationxxxxxxxxxSetup.exe** – Run this on the Anritsu MP1900A BERT Signal Quality Analyzer to install the pattern setup files.
   - **PCIECEMGen5_AN_RxTestApplicationxxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the application.
   - **PCIECEMGen5_AN_RxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

3.2 Launch and Set Up Software

1. Once the software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

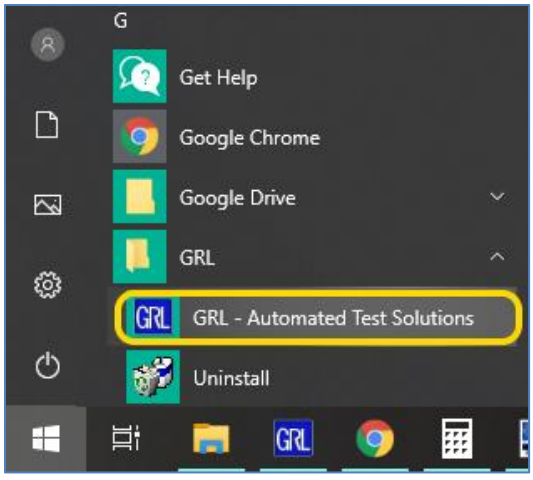


FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

2. From the Application→Rx Test Solution drop-down menu, select 'Anritsu PCIe CEM 5.0 Rx Test' to start the PCIe CEM 5.0 Rx Test Application. If the selection is grayed out, it means that your license has expired.

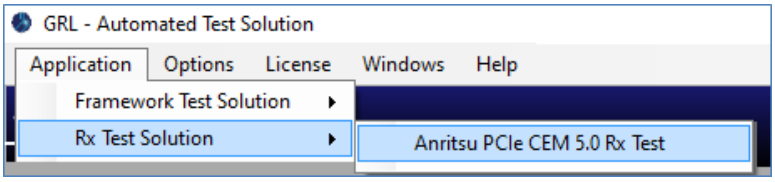


FIGURE 2. START PCIE CEM 5.0 RX TEST APPLICATION

3. To enable license, go to License→License Details.

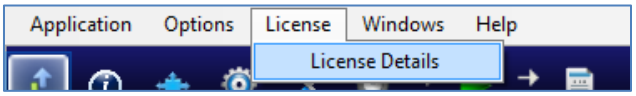


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

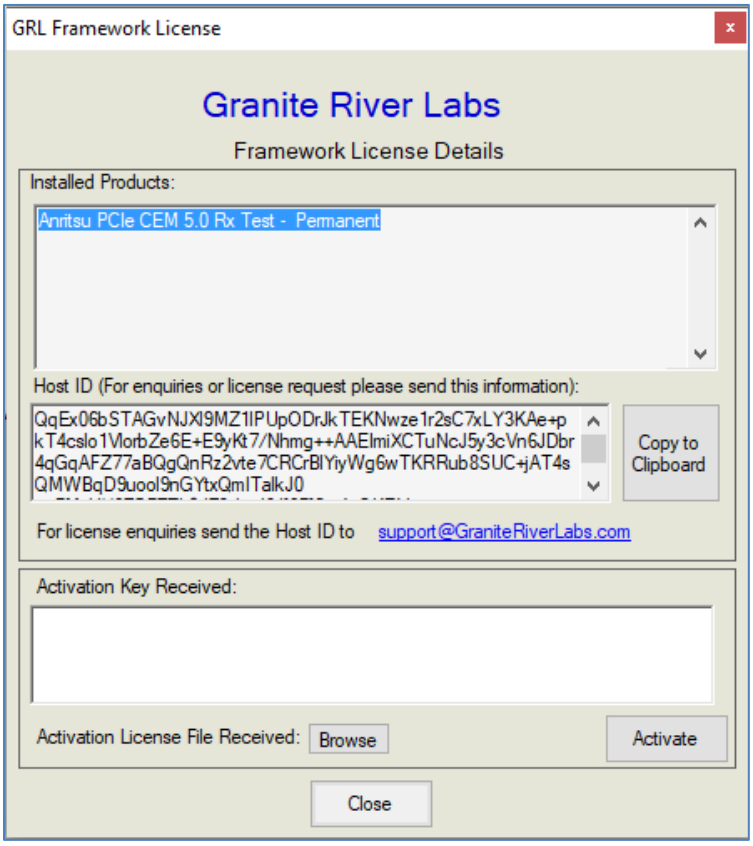


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select "Activate".

- If you do not have an Activation Key, select “Close” to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

4. Select the Equipment Setup icon  on the PCIe CEM 5.0 Rx Test Application menu.
5. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC. The BERT and MX183000A software can be connected using connection string formats similar to the following examples:
   - BERT: “TCPIP0::192.168.0.14::5001::SOCKET” or “192.168.0.14:5001”
   - MX183000A: “TCPIP0::192.168.0.14::5000::SOCKET” or “192.168.0.14:5000”

   Note the IP addresses listed above are only examples and should be changed according to the actual network connection being used.
6. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.
7. On the Equipment Setup page of the GRL PCIe CEM 5.0 Rx Test Application, type in the address of each connected instrument into the ‘Address’ field.

   *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”.)*

   If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

   *(Note: If the GRL software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as “TCPIP0::192.168.0.4::5025::SOCKET”.)*
8. Then select the “lightning” button () for each connected instrument.

   The “lightning” button should turn green () once the software has successfully established connection with each instrument.

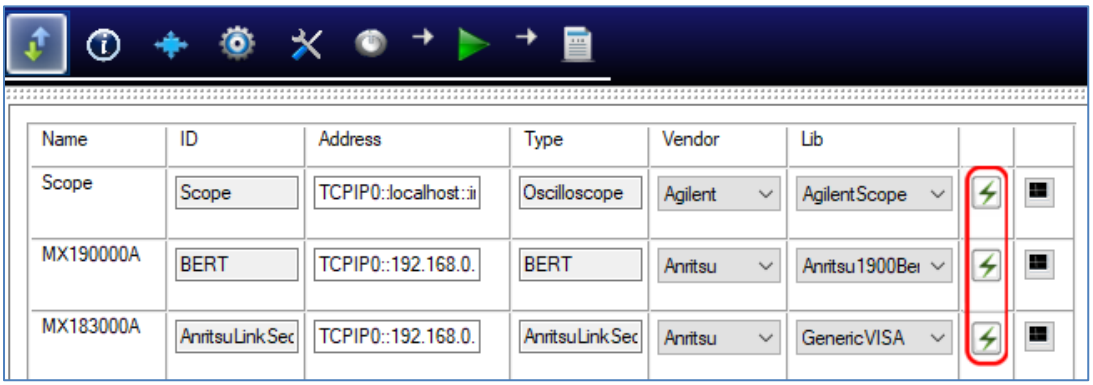


FIGURE 5. CONNECT INSTRUMENTS WITH GRL SOFTWARE

Note: Additional information for connecting supported vendor oscilloscopes (Keysight and Tektronix) to the PC is provided in the Appendix of this document.

3.3 Pre-Configure Software Before Calibration/Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced measurement setup.

3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

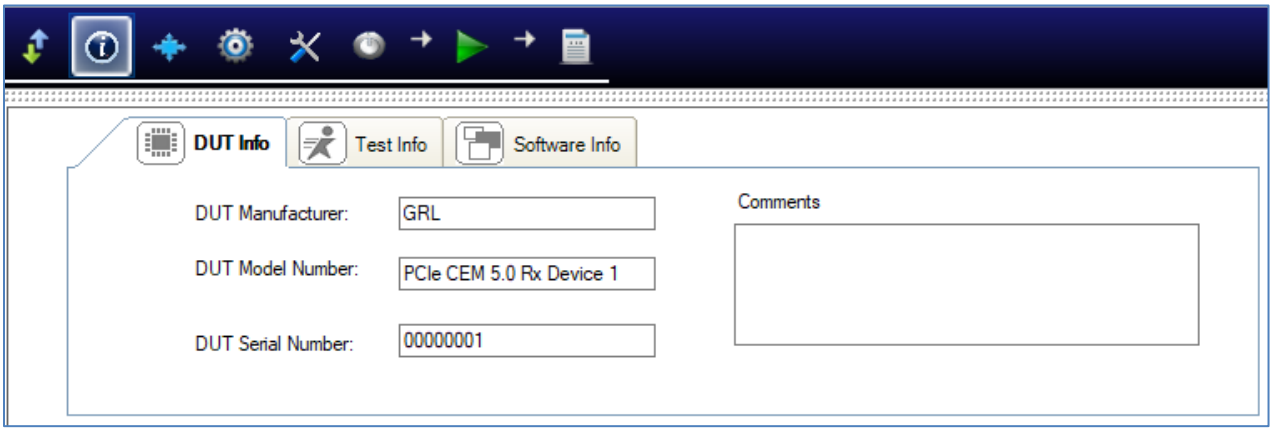


FIGURE 6. SESSION INFO PAGE

4 Calibrating Using GRL-PCIE5-CEM-RXA Software

The GRL-PCIE5-CEM-RXA test solution supports automated Rx calibration using the SigTest and Seasim signal quality and stress tolerance analysis application for PCIe Gen 5 system boards and add-in cards. To perform calibration, the GRL-PCIE5-CEM-RXA software is run from the PC or oscilloscope to enable automation control for each step of calibration and signal quality test sequence.

Calibration for the PCIe CEM 5.0 electrical specification will basically be performed at two physical test points: TP3 and TP2 (for the Long Channel). Test Point 3 (TP3) is a physical test point for calibration without the effect of a channel. An adjustable CEM connector will be used along with the calibration channel for testing the receiver. This will need to adjust the eye amplitude to specification values when measuring eye height/eye width. TP2 is a physical test point that will affect the eye opening due to trace length.

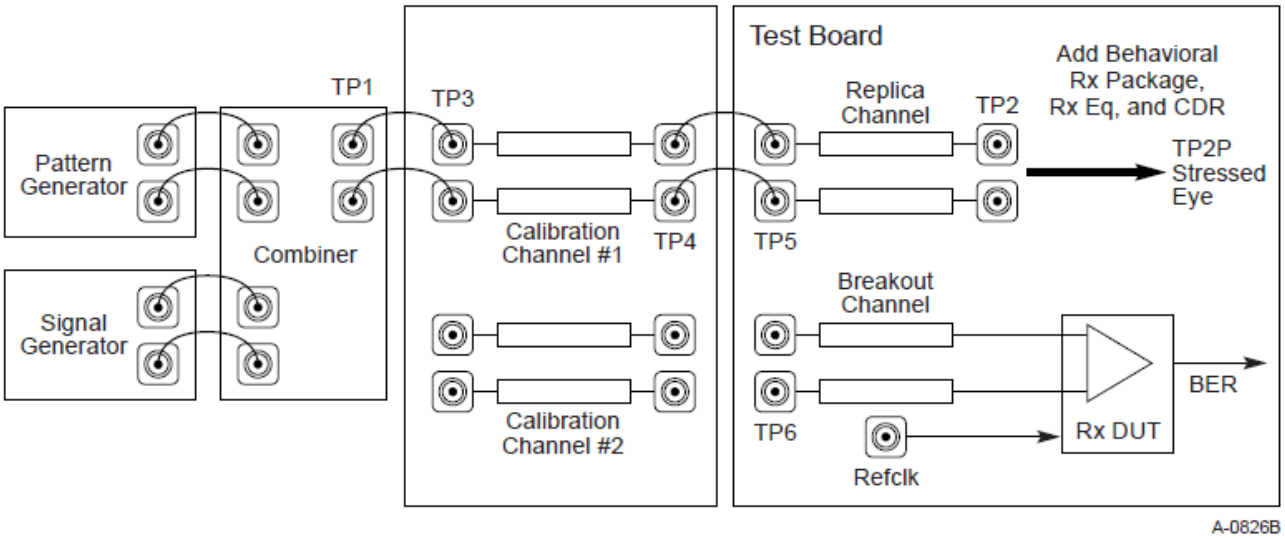


Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

FIGURE 7. RX CALIBRATION DIAGRAM FROM PHY TEST SPECIFICATION

For the Long Channel TP2 calibration, a PCI-SIG compliance load board (CLB) test fixture will be used for the host system board or a PCI-SIG compliance base board (CBB) test fixture for the add-in card. The board will be connected between the BERT noise generator output and the oscilloscope which will validate the test pattern of the signal and measure for stress tolerance to final stressed eye compliance. Post processing analysis of the signal is performed at the TP2P test point using the Seasim or SigTest application to simulate the stressed eye opening after applying Rx Behavioral package, Rx CTLE and DFE (if required). When calibration is completed, the GRL software will generate a test report detailing all results obtained from the calibration.

4.1 Set Up Automated Rx Calibration for TP3

Once pre-configuration has been completed from previous section, continue with the following calibration setup at TP3 (output of the BERT generator) using a GRL automation control enabled oscilloscope and Anritsu MP1900A BERT.

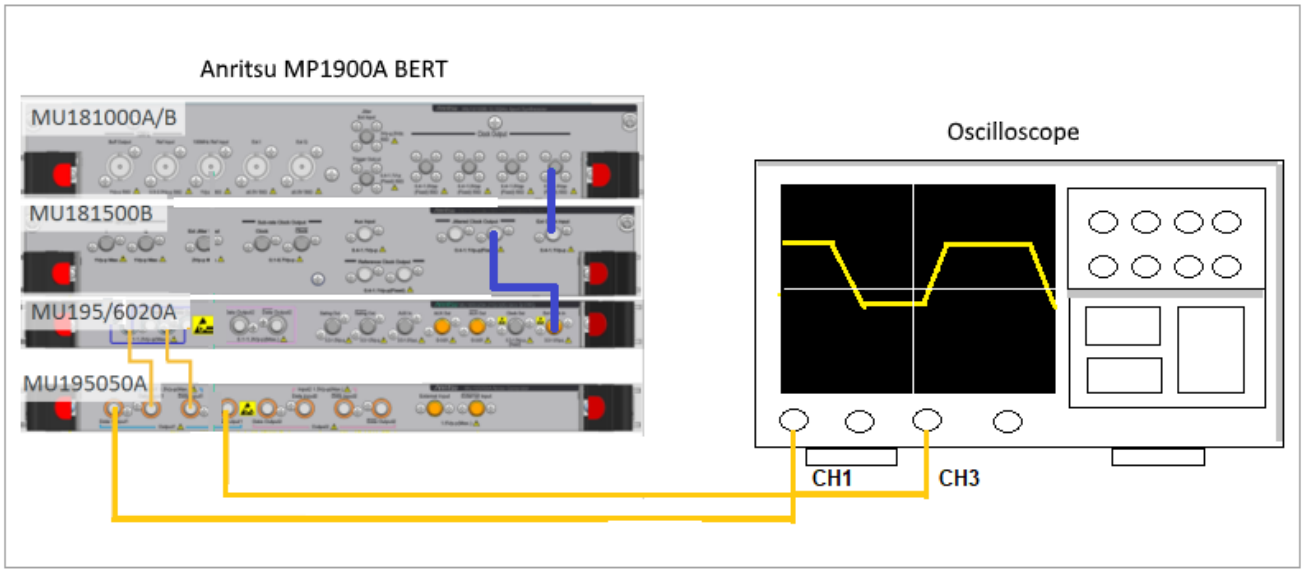


FIGURE 8. RECOMMENDED SETUP FOR TP3 RX CALIBRATION

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 3 on the oscilloscope.

4.1.1 TP3 Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following TP3 calibration setup.

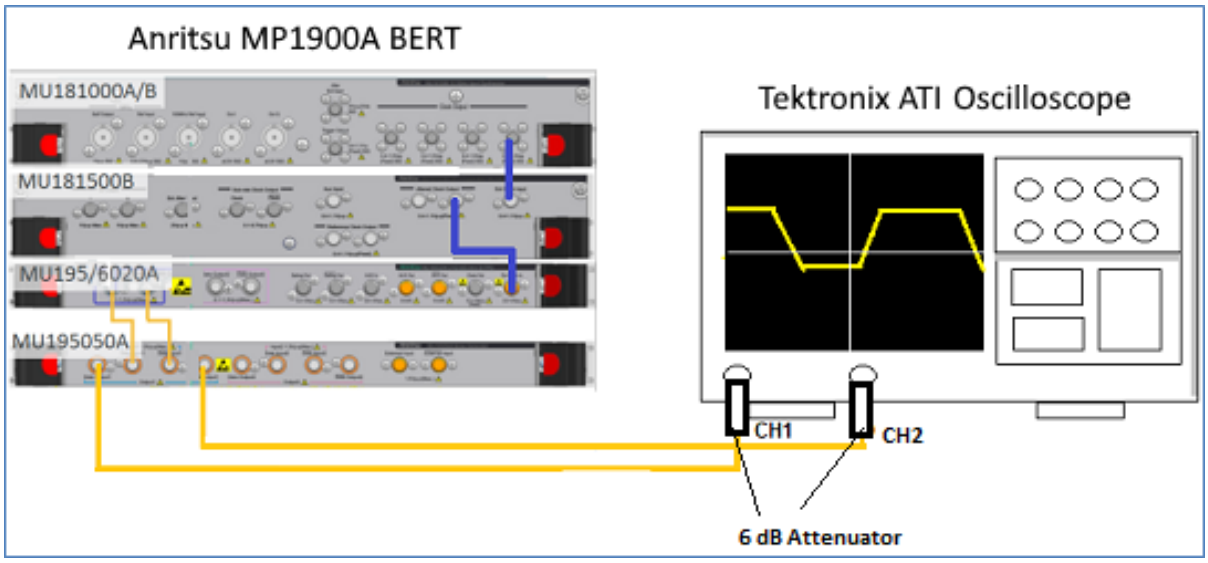


FIGURE 9. RECOMMENDED SETUP FOR TP3 RX CALIBRATION USING TEKTRONIX ATI SCOPE

*Note: Make sure that the "Tektronix Scope Type" is set to **Dual ATI** in the Configurations page (see Section 4.6).*

1. Follow back the same connections from step 1 to 3 in Section 4.1 above.
2. Then using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.2 Set Up Automated Rx Calibration for TP2

The next step is to calibrate the TP3-TP2 Channel (output of the Long Channel) with the following calibration setups using a GRL automation control enabled oscilloscope, Anritsu MP1900A BERT, and PCIe Gen 5 System Board or Add-In Card test fixtures. These calibration setups should also comply with insertion loss limits of 34 to 37 dB.

4.2.1 Connect Equipment for System Board Calibration

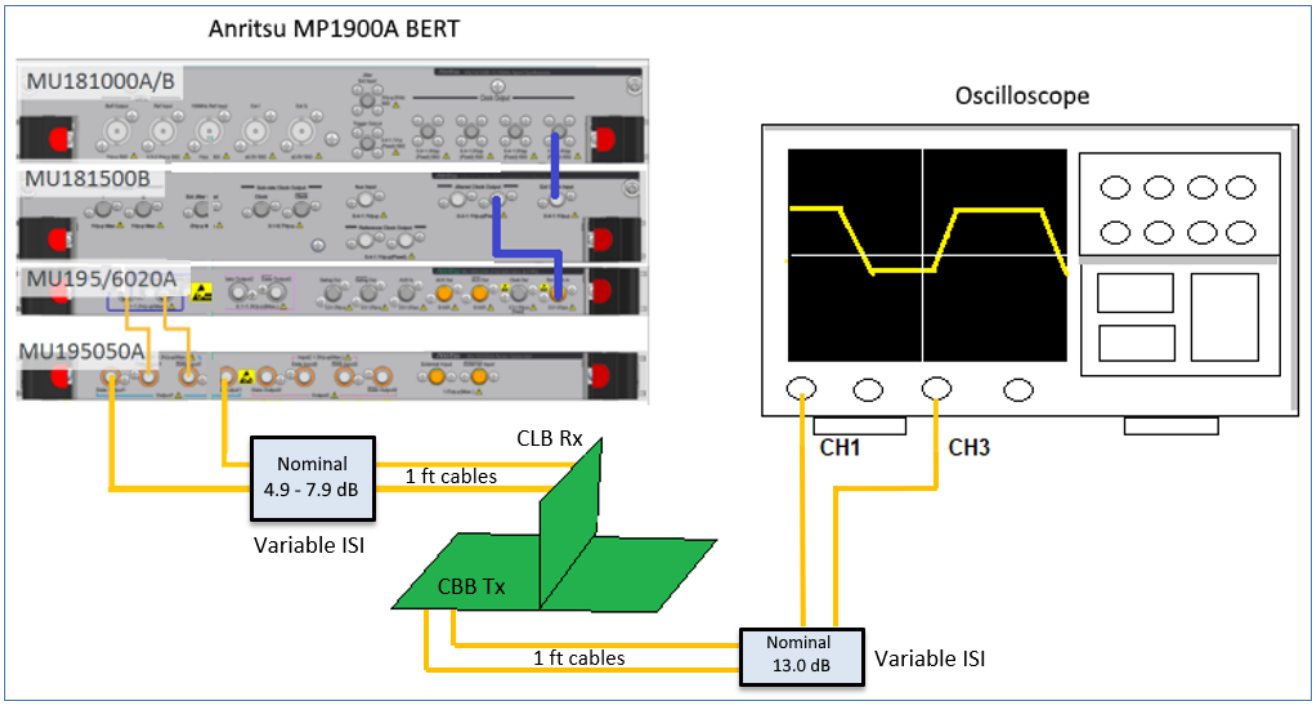


FIGURE 10. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 5 SYSTEM BOARD)

1. Using back the same BERT connections from the TP3 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to Variable ISI (Nominal 4.9 – 7.9 dB).
3. Using 1 ft cables, connect between both the Variable ISI (Nominal 4.9 – 7.9 dB) and the CLB Rx Lane.
4. Using 1 ft cables, connect between both the CBB Tx Lane and Variable ISI (Nominal 13.0 dB).
5. Connect the Variable ISI (Nominal 13.0 dB) to Channels 1 and 3 on the oscilloscope.

4.2.1.1 System Board Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following system board calibration setup.

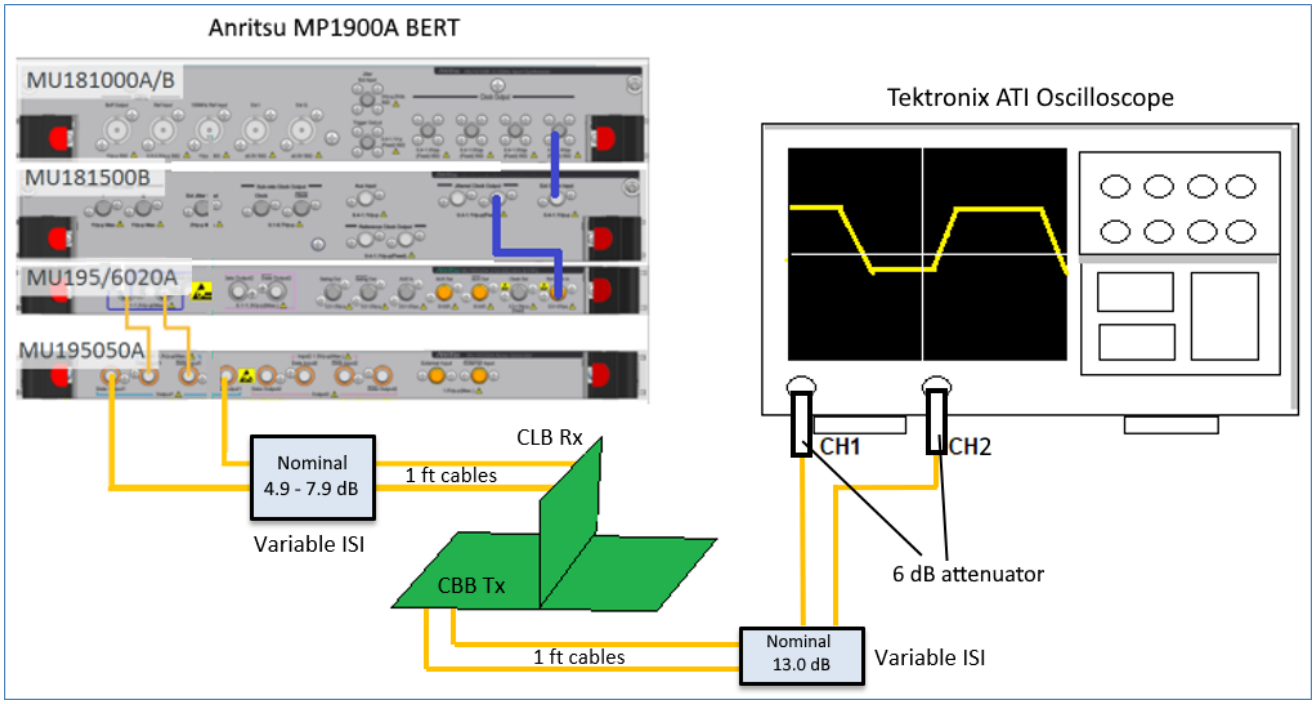


FIGURE 11. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 5 SYSTEM BOARD) USING TEKTRONIX ATI SCOPE

*Note: Make sure that the "Tektronix Scope Type" is set to **Dual ATI** in the Configurations page (see Section 4.6).*

1. Follow back the same connections from step 1 to 4 in Section 4.2.1 above.
2. Then connect the Variable ISI (Nominal 13.0 dB) to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.2.2 Connect Equipment for Add-In Card Calibration

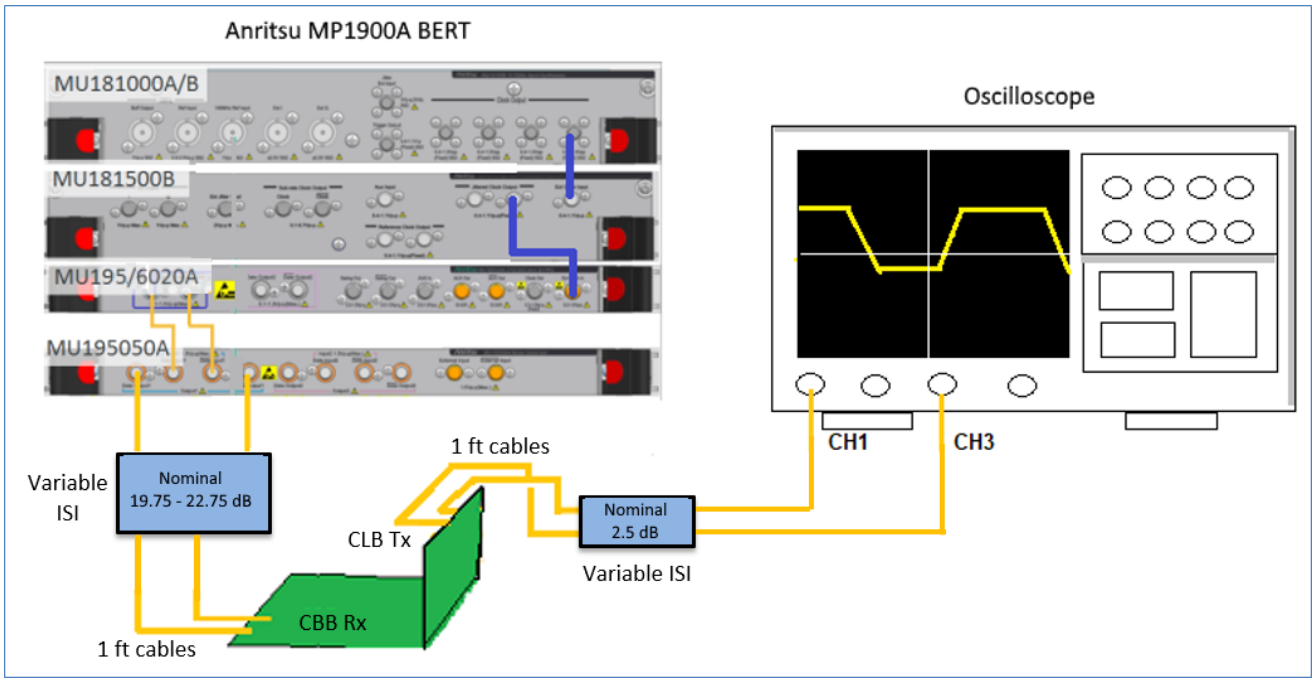


FIGURE 12. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 5 ADD-IN CARD)

1. Using back the same BERT connections from the TP3 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to Variable ISI (Nominal 19.75 – 22.75 dB).
3. Using 1 ft cables, connect between both the Variable ISI (Nominal 19.75 – 22.75 dB) and the CBB Rx Lane.
4. Using 1 ft cables, connect between both the CLB Tx Lane and Variable ISI (Nominal 2.5 dB).
5. Connect the Variable ISI (Nominal 2.5 dB) to Channels 1 and 3 on the oscilloscope.

4.2.2.1 Add-In Card Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following add-in card calibration setup.

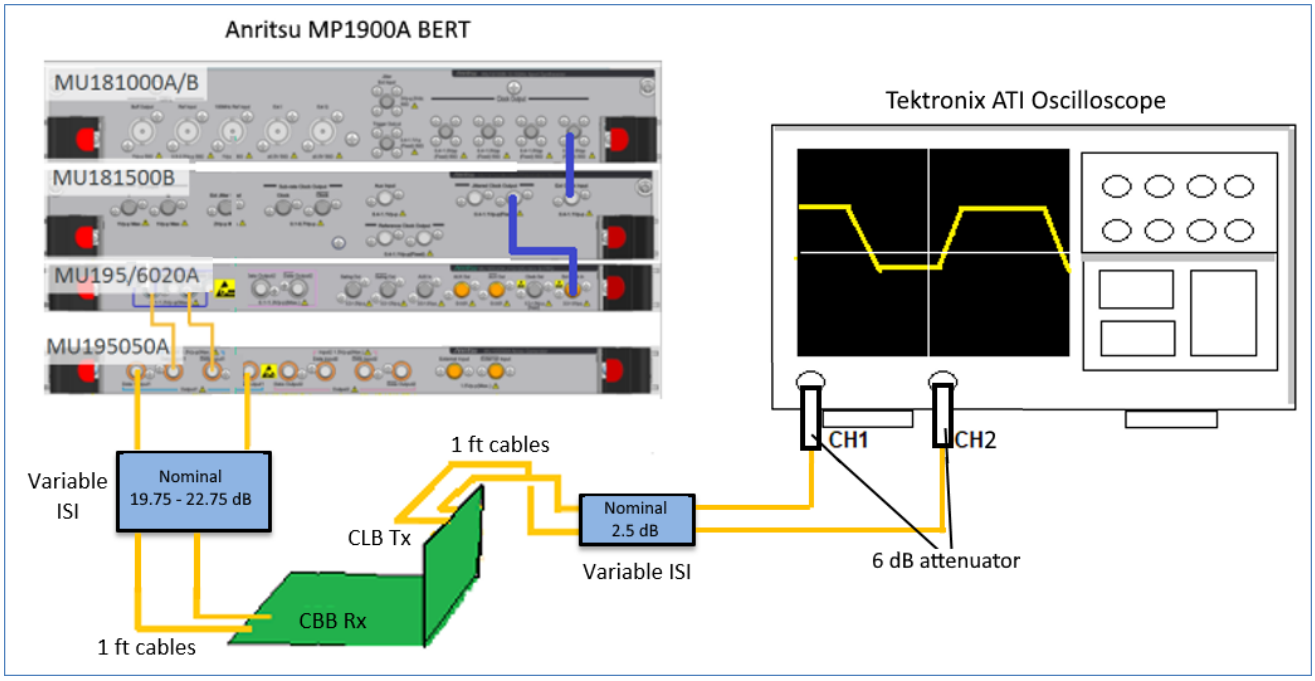


FIGURE 13. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 5 ADD-IN CARD) USING TEKTRONIX ATI SCOPE

*Note: Make sure that the "Tektronix Scope Type" is set to **Dual ATI** in the Configurations page (see Section 4.6).*

1. Follow back the same connections from step 1 to 4 in Section 4.2.2 above.
2. Then connect the Variable ISI (Nominal 2.5 dB) to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.3 Set Measurement Conditions

Select  from the GRL PCIe CEM 5.0 Rx Test Application menu to access the **Conditions** page to set the conditions for calibration and testing. The GRL software will perform calibration and testing for selected defined SJ frequencies.

Recommended procedure:

- *Step 1*: When calibrating, select all conditions that may be used for testing, and perform the calibration.

- *Step 2*: Once calibration is completed and ready for testing, re-select the necessary test conditions. For example, if required to test for a single SJ frequency, then select only the required SJ frequency for testing.

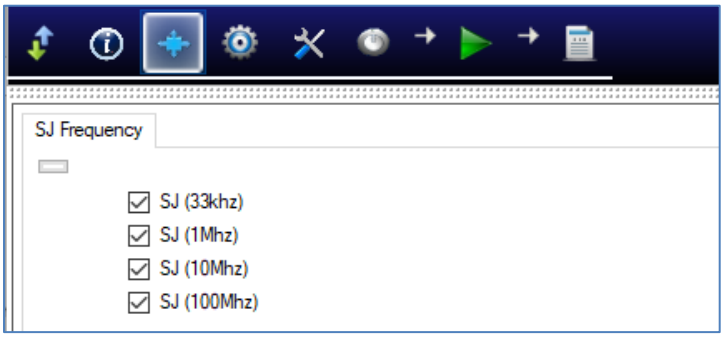


FIGURE 14. SELECT TEST CONDITION

4.4 Set Up Calibration Requirements

After setting up the physical equipment, select  from the GRL PCIe CEM 5.0 Rx Test Application menu to access the Setup Configuration page.

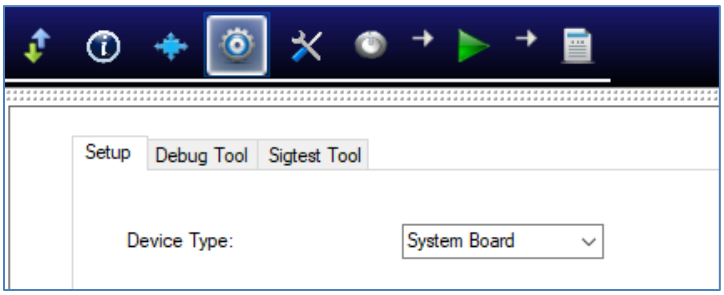


FIGURE 15. SET UP CALIBRATION REQUIREMENTS

4.4.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the calibration device.

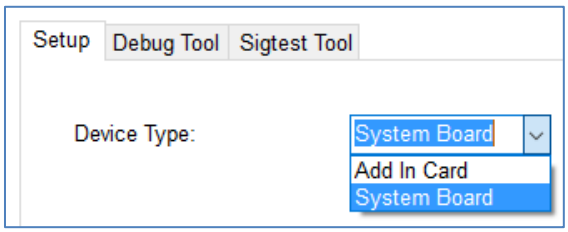


FIGURE 16. SELECT DEVICE FOR CALIBRATION

4.5 Select PCIe CEM 5.0 Rx Calibration

After selecting the device to be calibrated, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 5.0 based receiver calibration to be performed. Select the check box(s) of the desired Rx calibration.

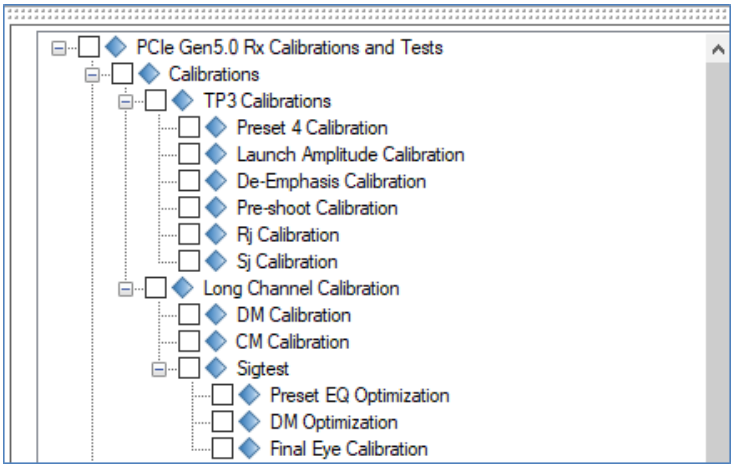


FIGURE 17. SELECT RX CALIBRATION

4.5.1 Select to Perform TP3 Calibration

Under 'TP3 Calibrations', select to calibrate for initial Tx equalization preset, BERT de-emphasis and pre-shoot (which form a linear curve fit), launch amplitude, random jitter (RJ), and sinusoidal jitter (SJ) (for PCIe Gen 5 frequencies as per PCIe CEM 5.0 Rx specs and forms a linear curve fit for each SJ frequency).

The GRL software will automatically run the selected calibration when initiated.

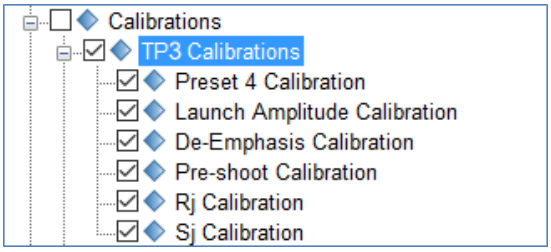


FIGURE 18. SELECT TP3 CALIBRATION

4.5.2 Select to Perform Long Channel TP2 Calibration

Under 'Long Channel Calibration', select to calibrate for differential mode (DM), common mode (CM), and SigTest or Seasim eye calibration parameters to achieve calibrated eye height and width to produce a final stressed eye diagram.

*Note that the list for SigTest eye calibration (for preset equalization (EQ) optimization, DM optimization, and final eye calibration) or Seasim eye calibration (for preset EQ optimization and final eye calibration) can be toggled using the **Configurations** page "Eye Calibration Method" parameter. See Section 4.6 for more details.*

The GRL software will automatically run the selected calibration when initiated.

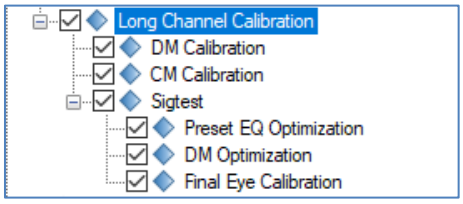


FIGURE 19. SELECT LONG CHANNEL TP2 CALIBRATION (WITH SIGTEST)

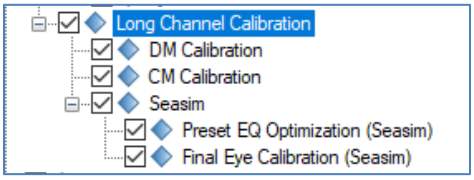


FIGURE 20. SELECT LONG CHANNEL TP2 CALIBRATION (WITH SEASIM)

4.6 Configure Calibration Parameters

After selecting the desired calibration, select  from the menu to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

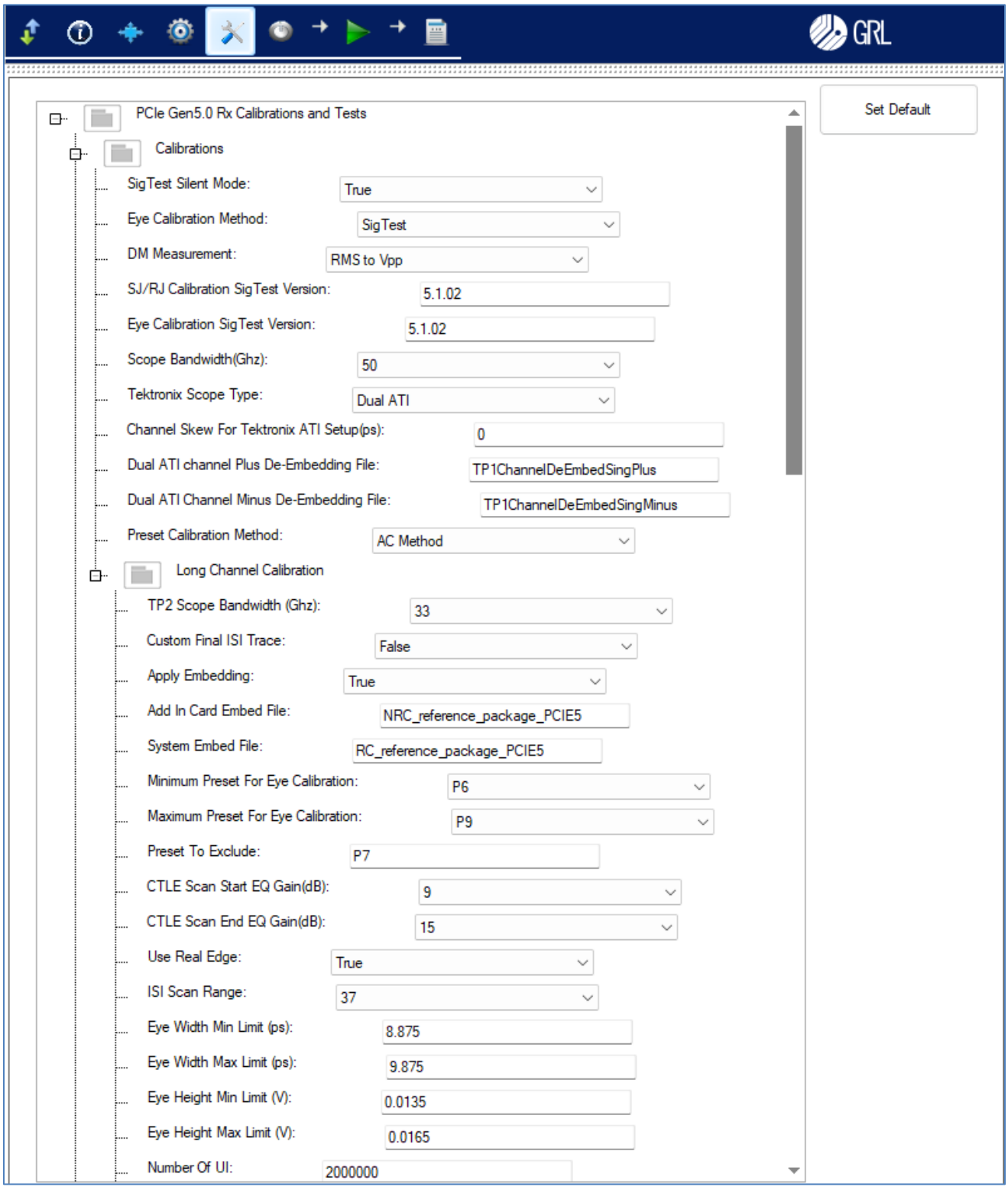


FIGURE 21. CALIBRATION PARAMETERS CONFIGURATION PAGE

TABLE 4. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
SigTest Silent Mode	Select 'True' to enable running the SigTest in silent mode during calibration.
Eye Calibration Method	Select either the SigTest or Seasim application to be used for final stressed eye calibration and post processing signal quality testing. Make sure that the SigTest or Seasim application is already installed in the test controller system. *Note this SigTest or Seasim selection will cause the calibration list to change accordingly.*
DM Measurement	Select the unit for measuring differential mode (DM).
SJ/RJ Calibration SigTest Version	If the SigTest method is selected to be applied during calibration of SJ or RJ, enter the Version number of the SigTest to be used. Make sure that the SigTest application is already installed in the test controller system.
Eye Calibration SigTest Version	If the SigTest method is selected to be applied during eye calibration, enter the Version number of the SigTest to be used. Make sure that the SigTest application is already installed in the test controller system.
Scope Bandwidth (GHz)	Select the appropriate bandwidth of the Scope being used for measurements.
Tektronix Scope Type	If the Tektronix Scope is to be used for measurements, select either the Single-shot based Scope or the Tektronix' owned Dual Asynchronous Time Interleaving (Dual ATI) based Scope.
Channel Skew For Tektronix ATI Setup (ps)	If the Tektronix ATI based Scope is to be used for measurements, enter the channel skew or timing to perform alignment of the Scope channels.
Dual ATI Channel Plus / Minus De-Embedding File	If the Tektronix ATI based Scope is to be used for measurements, specify the file name for de-embedding on the respective Scope channel.
Preset Calibration Method	Select the "AC Method" or "DC Method" to be used for preset calibration.
TP2 Scope Bandwidth (GHz)	Select the bandwidth of the Scope to be used for TP2 measurements.
Custom Final ISI Trace	Select 'True' to enable generating custom ISI trace for the final ISI calibration.
Apply Embedding	Select 'True' to embed the add-in card or system board DUT for calibration.
Add-In Card / System Embed File	Specify the file name for the embedded add-in card or system board.
Minimum & Maximum Preset for Eye Calibration	Select the range of presets to be applied for stressed eye calibration.
Preset to Exclude	Specify the preset that is not used for calibration.

CTLE Scan Start & End EQ Gain (dB)	Select the optimized CTLE Equalization Gain setting index to be used based on the CTLE model to measure the Eye area.
Use Real Edge	Select 'True' to use Real Edge connection for test setup on the Oscilloscope. *Note: This setting is only applicable for the Keysight Scope.*
ISI Scan Range	Select the scan range during ISI calibration.
Eye Width & Eye Height Min / Max Limit	Enter the limits for maximum and minimum eye calibration values.
Number Of UI	Enter the number of unit interval (UI) samples to acquire during calibration.
Final Eye Convergence	Select either a Strict or Loose method to be applied in the calculation for the final calibrated eye.
Brute Force Method	Select 'True' to enable DM Optimization SJ to continue scanning until all SJ ranges are included. The GRL-PCIE5-CEM-RXA software will then select the DM with Eye Height closest to 0.015 V.
If the SigTest method is selected:	
Parallel SigTest Run	Select 'True' to enable running the SigTest in parallel mode with the Long Channel TP2 calibration.
Maximum Thread Spawn	Set the maximum process threads to generate for checking the Rx device functionality during Long Channel TP2 calibration.
SigTest N Acquisition	Enter the number of measurements to acquire when running SigTest over the Long Channel TP2 calibration.
Eye Width/Height SigTest N Acquisition	Enter the number of measurements to acquire when running SigTest for the Eye calibration.
DM Maximum / Minimum Limit	Enter the maximum and minimum limits for DM.
DM Optimization SJ Sweep / Amplitude	Select the SJ scan range or amplitude for DM optimization calibration.
DM Optimization Target	Select the Eye Width or Eye Height to prioritize as a target during DM optimization calibration
DM Fine Tune	Select 'True' to fine tune DM in smaller steps to find the lowest DM value possible with Eye Height and Eye Width still in range.
If the Seasim method is selected:	
Seasim Template	Enter the Seasim template file to be used.
Final Eye Amplitude Cal On First Pass	Select 'True' to enable calibration for final eye amplitude to be performed upon the first successful calibration run.
Intrinsic Noise	Set the intrinsic noise/jitter (if required) to be used in the Seasim calculation.
PW RJ & PW DDJ	Enter the pulse width random jitter or deterministic jitter.

4.7 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for the RJ, SJ, DM and CM calibration. To do this, select  from the menu to access the Calibration page. By default, the calibration target values are those defined in the specification. To change the values, un-select the 'Use Default Value' checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

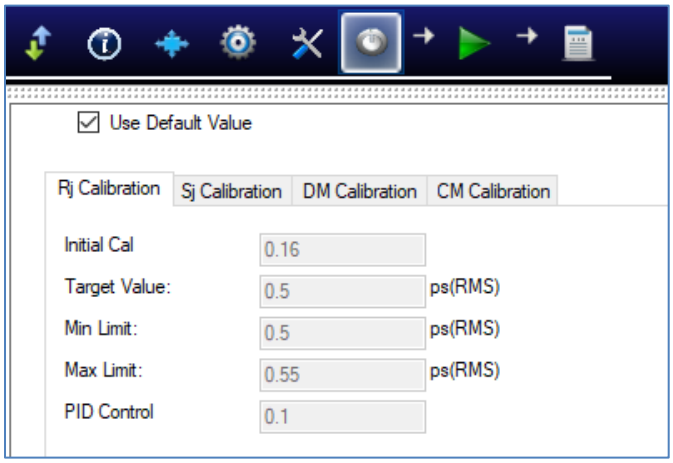


FIGURE 22. CALIBRATION TARGET OVERWRITE PAGE

4.8 Run Automation Calibration

Once calibration have been selected and set up from the previous sections, the calibration are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE5-CEM-RXA software automatically runs the selected calibration when initiated.

Before running the calibration, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration exist, the software will *skip* those calibration.
- **Replace if Result Exists** – If results from previous calibration exist, the software will *replace* those calibration with new results.

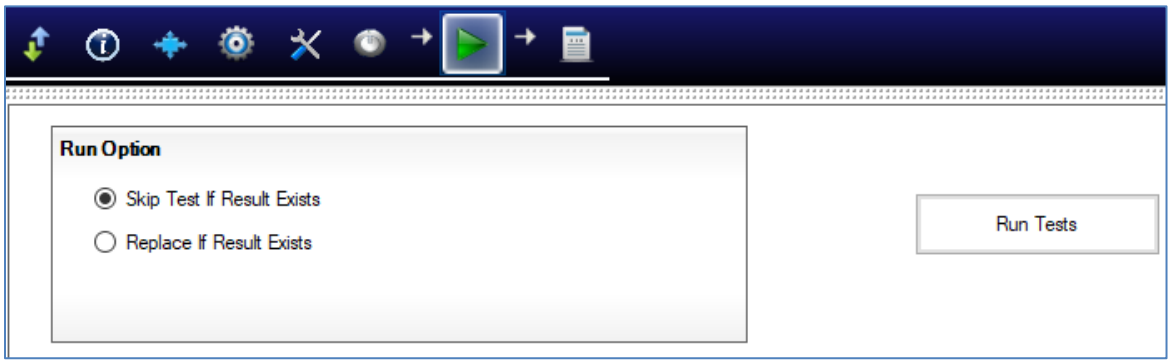


FIGURE 23. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration. The connection diagram for the calibration being run will initially appear to allow the user to make sure that the calibration environment has been properly set up before calibration can proceed. Below shows an example of the connection diagram pop-up for the system board Rx TP3 calibration.

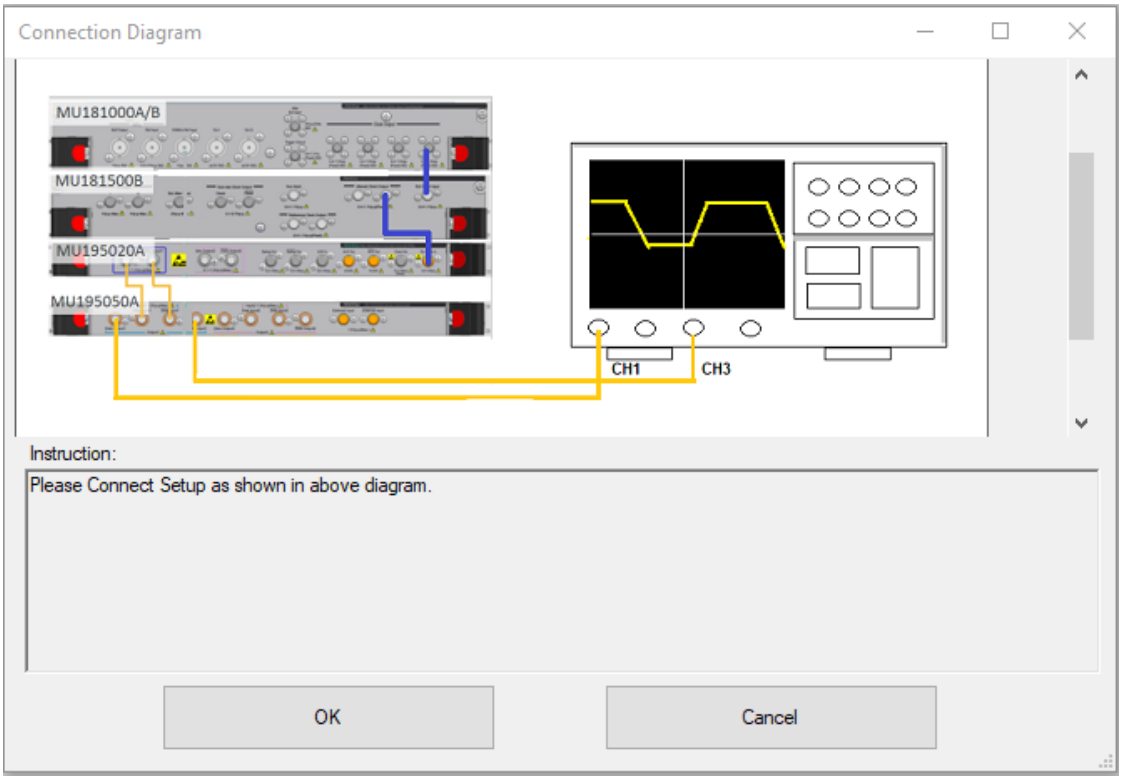


FIGURE 24. EXAMPLE CONNECTION POP-UP DIAGRAM FOR RX TP3 CALIBRATION

5 Testing Using GRL-PCIE5-CEM-RXA Software

The GRL-PCIE5-CEM-RXA test solution supports automated Rx compliance testing as well as optional SJ margin search testing for PCIe Gen 5 system board and add-in card DUT's. Rx compliance testing includes Tx preset test, initial Tx equalization test, Tx link equalization response test, and Rx link equalization test performed at 32.0 GT/s. The GRL software will initially run through link training with the DUT to prepare it for Loopback mode. Once the DUT is ready for next transition state, the software will start to initiate loopback on the DUT and then measuring the Bit Error Ratio (BER) using the calibration stressed signals. The Rx path is tested with worst case eye to ensure a BER of less than 1E-12 can be achieved.

When testing is completed, the GRL software will generate a test report detailing all results obtained from the test runs.

5.1 Overview of DUT Tx Preset Test

Note: This only applies for the add-in card DUT and is not required for the system board DUT.

The PCIe Gen 5 add-in card DUT will be tested for Tx preset compliance as defined by the PHY Test Specification at 32.0 GT/s. This will first ensure the DUT is able to generate the correct Tx equalization values for each of the total 11 presets before being tested for Tx equalization.

Note: This test requires the DUT to be in the polling.compliance state. No Variable ISI channel will be used in the setup.

5.1.1 Add-In Card Tx Preset Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 5.0 (for 32.0 GT/s) CBB with no power applied.
- Connect the compliance toggle outputs (MMPX connectors J5 and J85) on the CBB main board to the Rx lane 0 (MMPX connectors J18 and J2) on the CBB.
- Apply 50-ohm terminations on all Tx lanes other than the Tx lane under test.
- Connect the Tx lane under test to the input of the oscilloscope. Make sure that the CBB is supplying SSC enabled clock (-0.5% down-spread) for this test.

Once the CBB is powered on, set the CBB compliance toggle to initially place the DUT in the 32 GT/s test state and capture the following:

- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 31.25$ ps = 62.5 µs)

Save the captured waveform for the initial preset value, using a compliance pattern of 64 ones and 64 zeros. Then, repeat the test for all 11 presets at 32.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 32.0 GT/s.

5.2 Overview of DUT Initial Tx Equalization Test

Note: This only applies for the add-in card DUT and is not required for the system board DUT.

The PCIe Gen 5 add-in card DUT will be tested for initial Tx equalization as defined by the PHY Test Specification at 32.0 GT/s. This will ensure the DUT is able to use the correct Tx equalization preset as required during the initial stage of testing.

5.2.1 Add-In Card Initial Tx Equalization Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 5.0 (for 32.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Keep additional Tx lanes other than the Tx lane under test unterminated. Make sure that the CBB is supplying SSC enabled clock (-0.5% down-spread) for this test.

Once the CBB is powered on, the DUT should start link training and negotiation to 32.0 GT/s while requesting P0 as the initial preset for the DUT. *Note that Tx equalization adjustments will not be required in phase 3. Ensure that the Tx equalization preset for the DUT is maintained when changing to 32.0 GT/s.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 31.25$ ps = 62.5 µs)

Save the captured waveform for preset P0. Then, repeat the test with presets from P0 to P9 at 32.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 32.0 GT/s.

5.3 Overview of DUT Tx Link Equalization Response Test

The PCIe Gen 5 system board or add-in card DUT will be tested for Tx link equalization response as defined by the PHY Test Specification at 32.0 GT/s. This will ensure the DUT can accurately

respond to commands to adjust the transmitter equalization values during link training for DUT loopback.

5.3.1 System Board Tx Link Equalization Response Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 5.0 (for 32.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the BERT signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.

Note the setup will not include any Variable ISI channel.

Once the system board DUT is powered on, it should start link training and negotiation to 32.0 GT/s. Send a command from the BERT to the DUT to set the Tx equalization to the following:

- preset 0 (preshoot to 0.0 dB and de-emphasis to -6.0 dB)

Ensure that this Tx equalization transition is able to complete within a 1 microsecond response timeframe. Record the cursors reported by the DUT for that preset.

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 31.25$ ps = 62.5 µs)

Save the captured waveform for preset 0. Then, repeat the test with presets from P1 to P9.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 32.0 GT/s as well as able to complete within a 1 microsecond response timeframe.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

5.3.2 Add-In Card Tx Link Equalization Response Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 5.0 (for 32.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.

- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.

Note the setup will not include any Variable ISI channel.

Once the CBB is powered on, the DUT should start link training and negotiation to 32.0 GT/s. *(Note: An initial preset other than the following presets should be used.)* Send a command from the BERT to the DUT to set the Tx equalization to preset 0. *Ensure that this Tx equalization transition is able to complete within a 1 microsecond response timeframe. Record the cursors reported by the DUT for that preset.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 31.25$ ps = 62.5 µs)

Save the captured waveform for preset 0. Then, repeat the test with presets from P1 to P9.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 32.0 GT/s as well as able to complete within a 1 microsecond response timeframe.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

5.4 Overview of DUT Rx Link Equalization Test

The PCIe Gen 5 system board or add-in card DUT will be tested for Rx link equalization as defined by the PHY Test Specification at 32.0 GT/s. This will ensure the DUT can successfully send commands to adjust the transmitter equalization of its link partner as required.

5.4.1 System Board Rx Link Equalization Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 5.0 (for 32.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.
- Connect the CLB 100 MHz clock output from the system board DUT to the BERT synthesizer (that has passed PCIe 5.0 base specification PLL compliance or equivalent for the respective data rate).
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.

Adjust the Tx equalization (EQ) of the BERT to align with the initial Tx EQ preset at 32.0 GT/s requested by the system board DUT.

Once the system board DUT is powered on, it should start link training and equalization sequence by the BERT at 32.0 GT/s, which should eventually place the DUT in the loopback state. The

transmitted pattern to be used for the Bit Error Rate (BER) measurement is the MCP modified compliance pattern.

The test is considered as successful if detected no more than one error in 4E12 bits transmitted (125 seconds).

5.4.2 Add-In Card Rx Link Equalization Test at 32.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 5.0 (for 32.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the signal source.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.

Set the BERT to initially transmit with preset P5. *(Note this is required only if the DUT does not request any preset to be transmitted by the BERT.)*

Once the CBB is powered on, the DUT should start link training and equalization sequence by the BERT, which should eventually place the DUT in the loopback state. The transmitted pattern to be used for the Bit Error Rate (BER) measurement is the MCP modified compliance pattern.

The test is considered as successful if detected no more than one error in 4E12 bits transmitted (125 seconds).

5.4.3 Link Training

During link training process, the DUT basically goes through multiple states via the status state machine (SSM) method to enter Loopback mode as shown below.

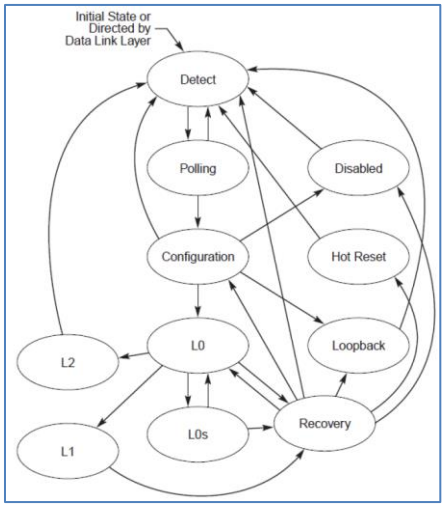


FIGURE 25. MAIN STATE DIAGRAM FOR LINK TRAINING AND STATUS STATE MACHINE (FROM PHY TEST SPECIFICATION)

Below is a loopback training sequence example from PHY Test Specification:

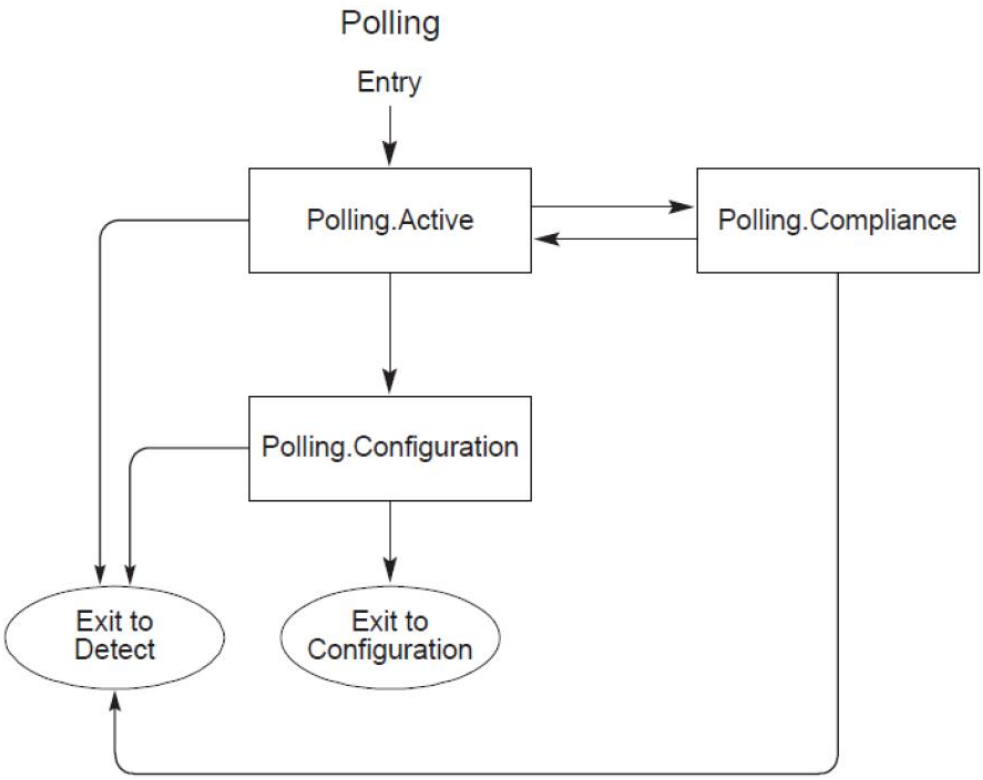


FIGURE 26. POLLING SUBSTATE MACHINE (FROM PHY TEST SPECIFICATION)

1. Enable the DUT to enter the Polling.Active state by sending TS1 with PAD (K23.7).
2. The DUT will go into the Polling.Configuration state after sending more than 1024 TS1 and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The DUT will next enter the Configuration state after 8 consecutive TS2 with PAD have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Start speed negotiation by sending TS1 at 2.5 GT/s advertising the supported speeds. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
5. The DUT will finally switch to the Loopback mode after having two consecutive TS1 at the requested speed with Loopback bit asserted.

5.5 Set Up Automated DUT TxRx Link Equalization Test

Once calibration has been completed from Section 4, continue with the following setup to perform initial link equalization (EQ) tests to prepare the DUT for the final stage of Rx compliance testing. The setup requires the Anritsu MP1900A BERT (including the MU195040A SI Error Detector), PCIe Gen 5 System Board or Add-In Card DUT, PCIe5 Re-Driver, and oscilloscope to be used.

5.5.1 Connect Equipment for System Board TxRx Link EQ Testing

The following link EQ test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen 5 System Board DUT.

***Note**: Use logical Lane 0 for the following test setup.*

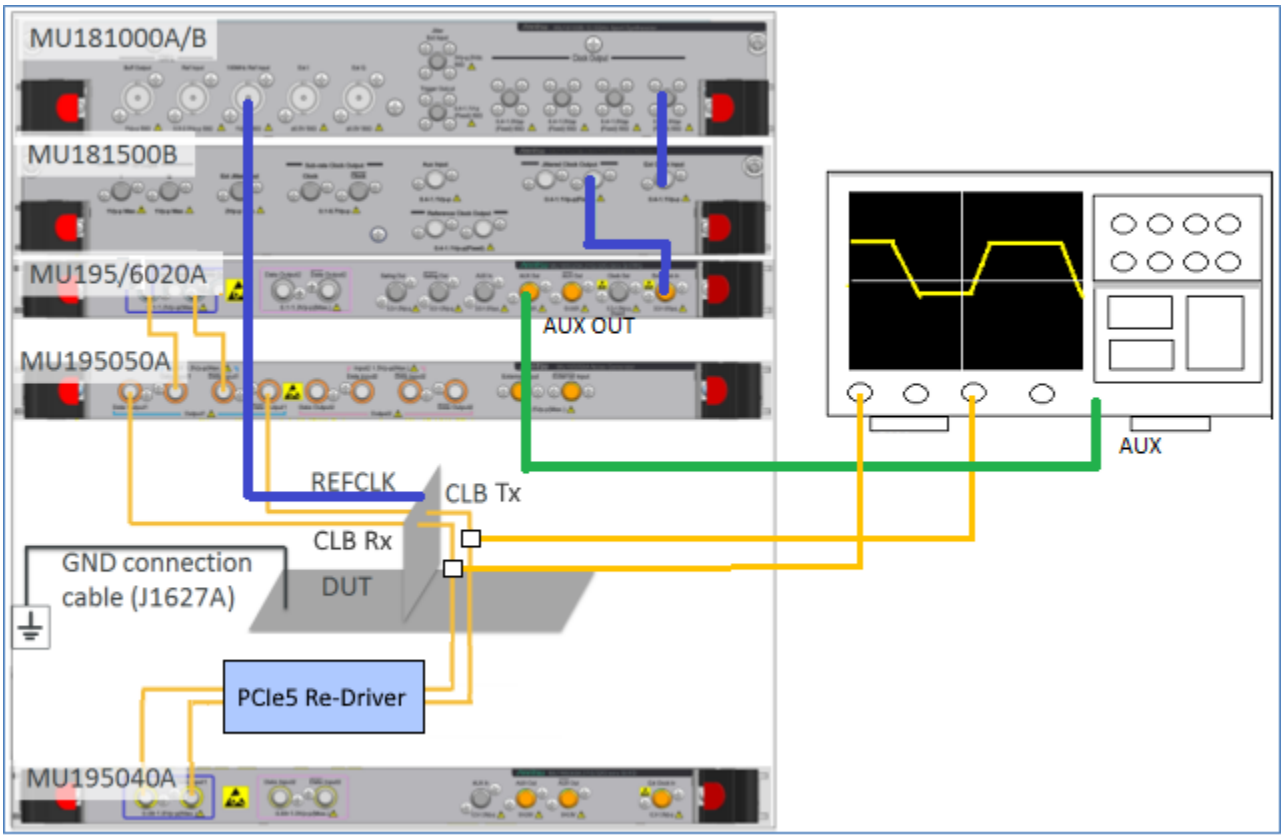


FIGURE 27. RECOMMENDED SETUP FOR DUT TXRX LINK EQ TESTING (PCIE GEN 5 SYSTEM BOARD)

***Note**: Before starting the System Board TxRx Link EQ Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Appendix B or C for details.*

1. Using back the same BERT connections from the Long Channel system board calibration, remove all Variable ISI channels and connect the Ref Clk of the CLB to the 100 MHz Ref Input on the MU181000A/B with a BNC cable.

2. Using a SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
3. Using coaxial cables, connect the CLB Tx Lane to the Power Splitter IN (or the pick-off tee IN) port.
4. Using phase matched cables, connect Channels 1 and 3 on the oscilloscope to the Power Splitter OUT (or the pick-off tee PICK OFF) port.
5. Using coaxial cables, connect the other OUT port of the Power Splitter (or the pick-off tee OUT) to the PCIe5 Re-Driver and then to the MU195040A data inputs for loopback error detection.
6. Using the J1627A GND connection cable, connect the CLB to ground.

5.5.2 Connect Equipment for Add-In Card TxRx Link EQ Testing

The following link EQ test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen 5 Add-In Card DUT.

***Note**: Use logical Lane 0 for the following test setup.*

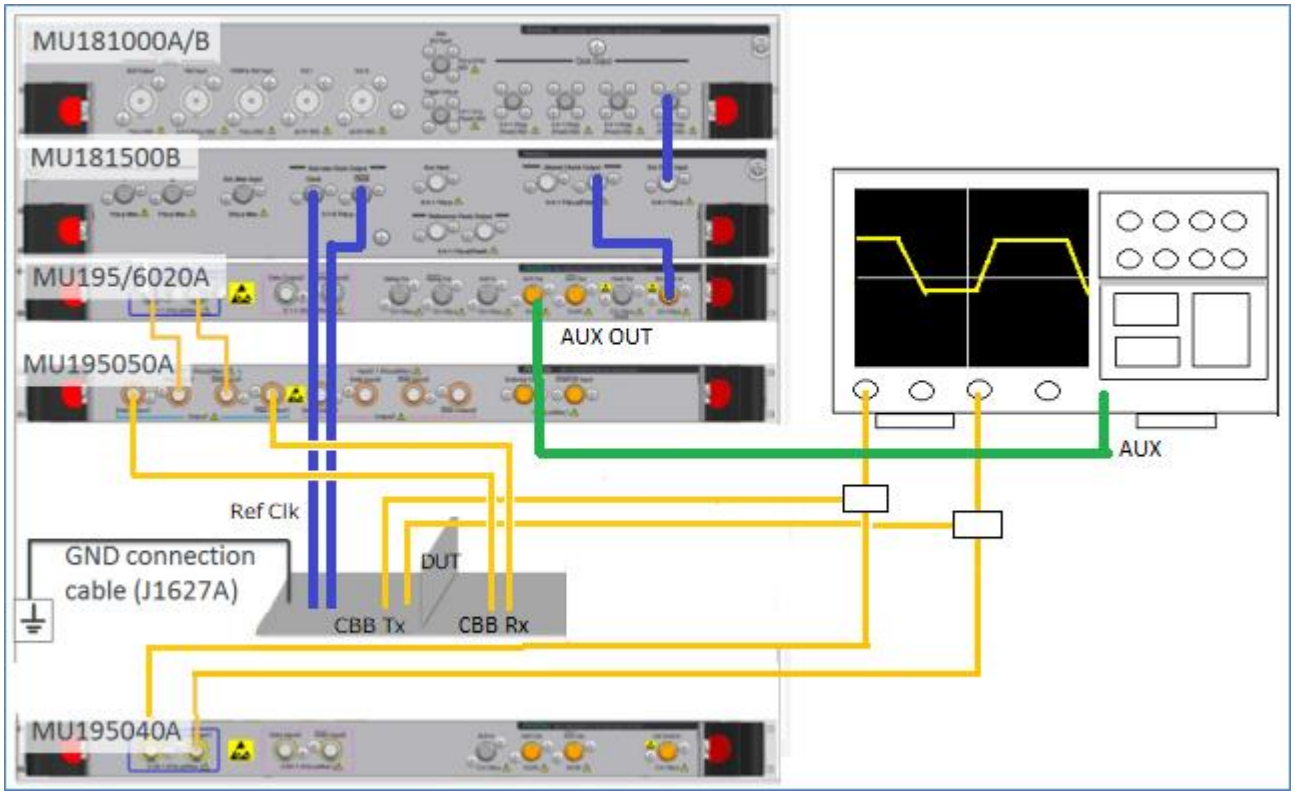


FIGURE 28. RECOMMENDED SETUP FOR DUT TXRX LINK EQ TESTING (PCIE GEN 5 ADD-IN CARD)

1. Using back the same BERT connections from the Long Channel add-in card calibration, remove all Variable ISI channels.

2. Using coaxial cables, connect the MU181500B sub-rate clock outputs to the Ref Clk+/- of the CBB.
3. Using a SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
4. Using phase matched cables, connect Channels 1 and 3 on the oscilloscope to the Power Splitter OUT (or the pick-off tee PICK OFF) port.
5. Using coaxial cables, connect the CBB Tx Lane to the Power Splitter IN (or the pick-off tee IN) port.
6. Using coaxial cables, connect the other OUT port of the Power Splitter (or the pick-off tee OUT) to the MU195040A data inputs for loopback error detection.
7. Using the J1627A GND connection cable, connect the CBB to ground.

5.6 Set Up Automated DUT Rx Compliance Test

After link EQ testing has successfully completed from previous section, proceed with testing for DUT Rx compliance with the following setup.

5.6.1 Connect Equipment for System Board Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen 5 System Board DUT.

***Note**: Use logical Lane 0 for the following test setup.*

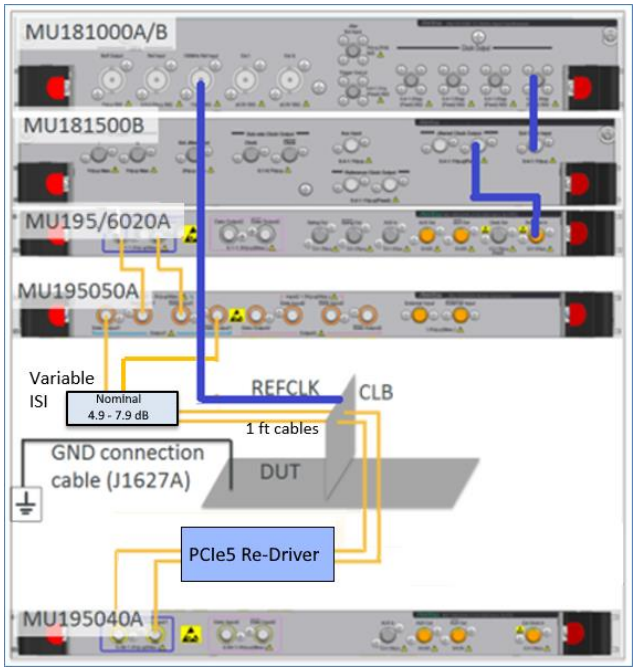


FIGURE 29. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIE GEN 5 SYSTEM BOARD)

***Note**: Before starting the System Board Rx Compliance Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Appendix B or C for details.*

1. Using the same setup from the system board link EQ test, remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to Variable ISI (Nominal 4.9 – 7.9 dB).
3. Using 1 ft cables, connect between both the Variable ISI and CLB Rx Lane.
4. Using coaxial cables, connect the CLB Tx Lane to the PCIe5 Re-Driver and then to the MU195040A data inputs for loopback error detection.

5.6.2 Connect Equipment for Add-In Card Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen 5 Add-In Card DUT.

***Note**: Use logical Lane 0 for the following test setup.*

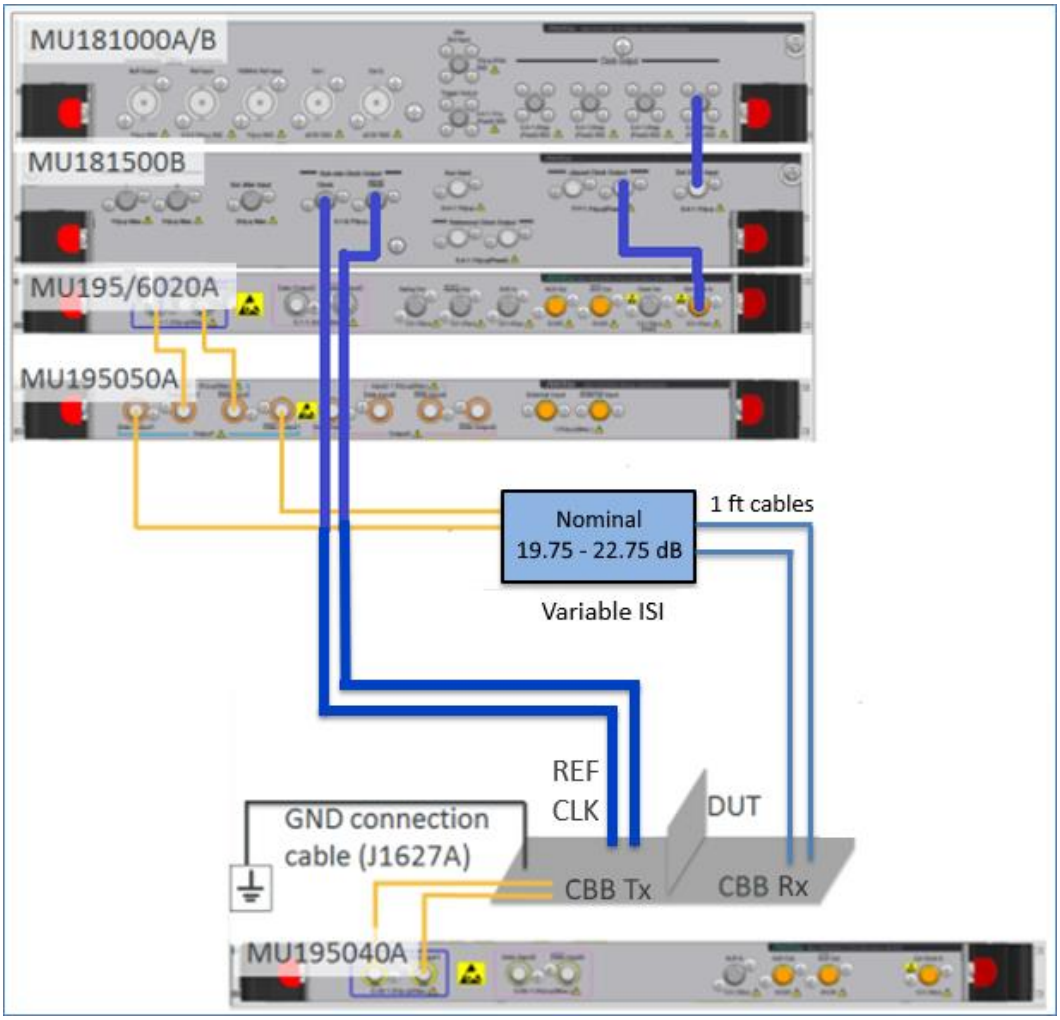


FIGURE 30. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIE GEN 5 ADD-IN CARD)

1. Using the same setup from the add-in card link EQ test, remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to Variable ISI (Nominal 19.75 – 22.75 dB).
3. Connect the Variable ISI to the CBB Rx Lane with the 1 ft cables.
4. Using coaxial cables, connect the CBB Tx Lane directly to the MU195040A data inputs for loopback error detection.

5.7 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL PCIe CEM 5.0 Rx Test Application menu to access the Setup Configuration page.

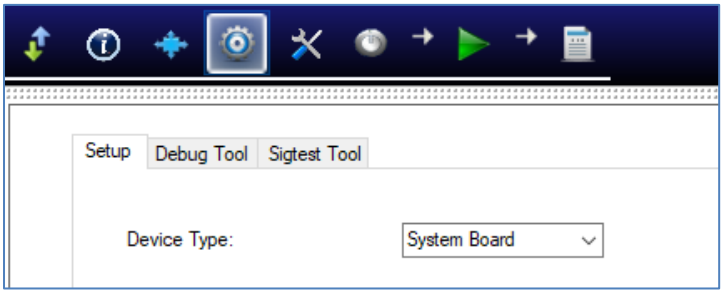


FIGURE 31. SET UP TEST REQUIREMENTS

5.7.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the DUT.

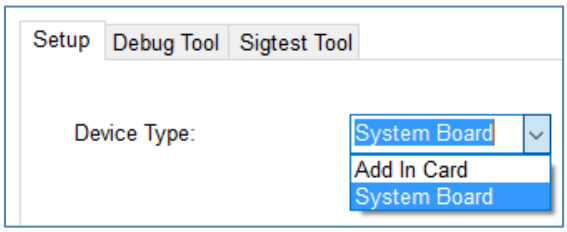


FIGURE 32. SELECT DUT TYPE

5.8 Select PCIe CEM 5.0 Rx Tests

After selecting the DUT type, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 5.0 Rx tests to be run. Select the check box(s) for the required Rx tests.

Note: When running tests for the first time or changing anything in the setup, it is suggested to perform calibration first. If calibration is not completed, attempting to run the Rx tests will throw errors.

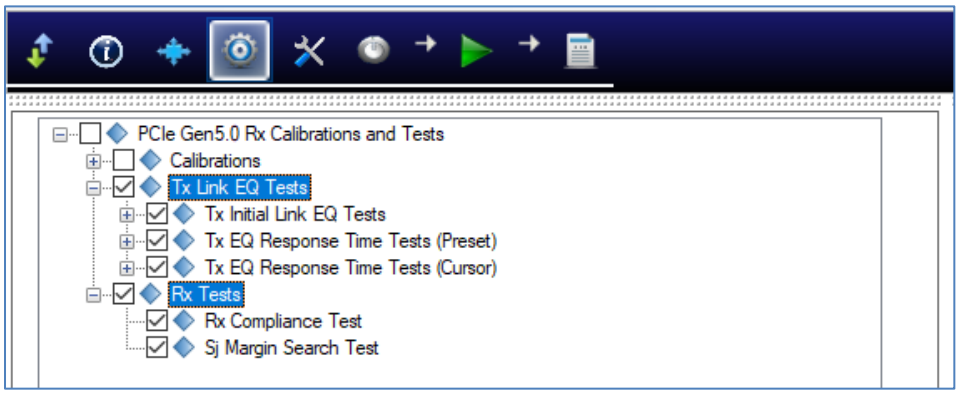


FIGURE 33. SELECT RX TESTS

5.8.1 Select to Run DUT Link Training and Rx Compliance Test

Select the 'Tx Link EQ Tests' group and 'Rx Compliance Test' to prepare and test the DUT for compliance with the PCIe CEM 5.0 Rx specifications. The GRL software will automatically run the link equalization test sequence when initiated. *Note the 'Tx Initial Link EQ' test is only available when Add-in Card is selected as the DUT in the Setup Configuration page.*

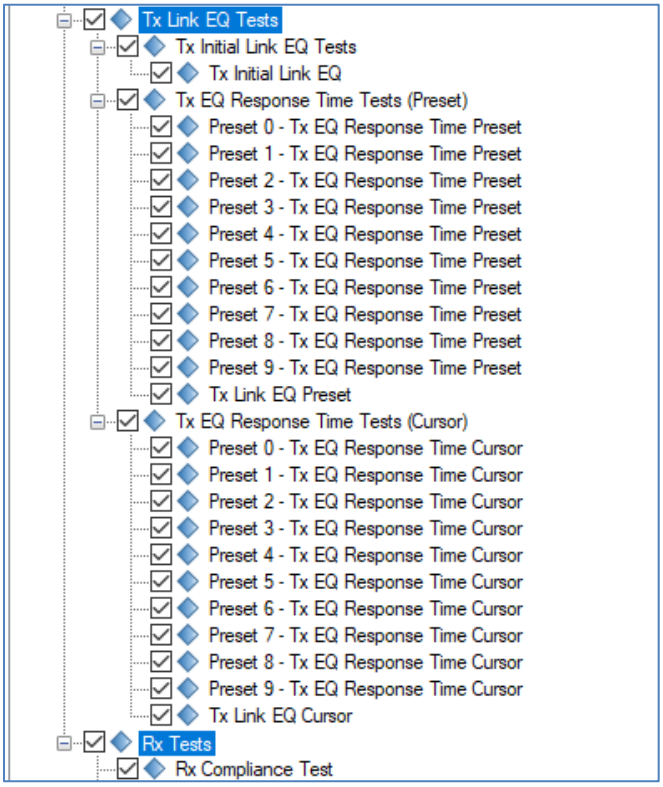


FIGURE 34. SELECT DUT TX LINK EQ AND RX COMPLIANCE TESTS

5.8.2 Select to Run SJ Margin Search Test

Select 'Sj Margin Search Test' to perform an optional test to conduct a SJ margin search for jitter tolerance. The GRL software will automatically run the selected test when initiated.

FIGURE 35. SELECT SJ MARGIN SEARCH TEST

5.9 Configure Test Parameters

After selecting the desired tests, select  from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.

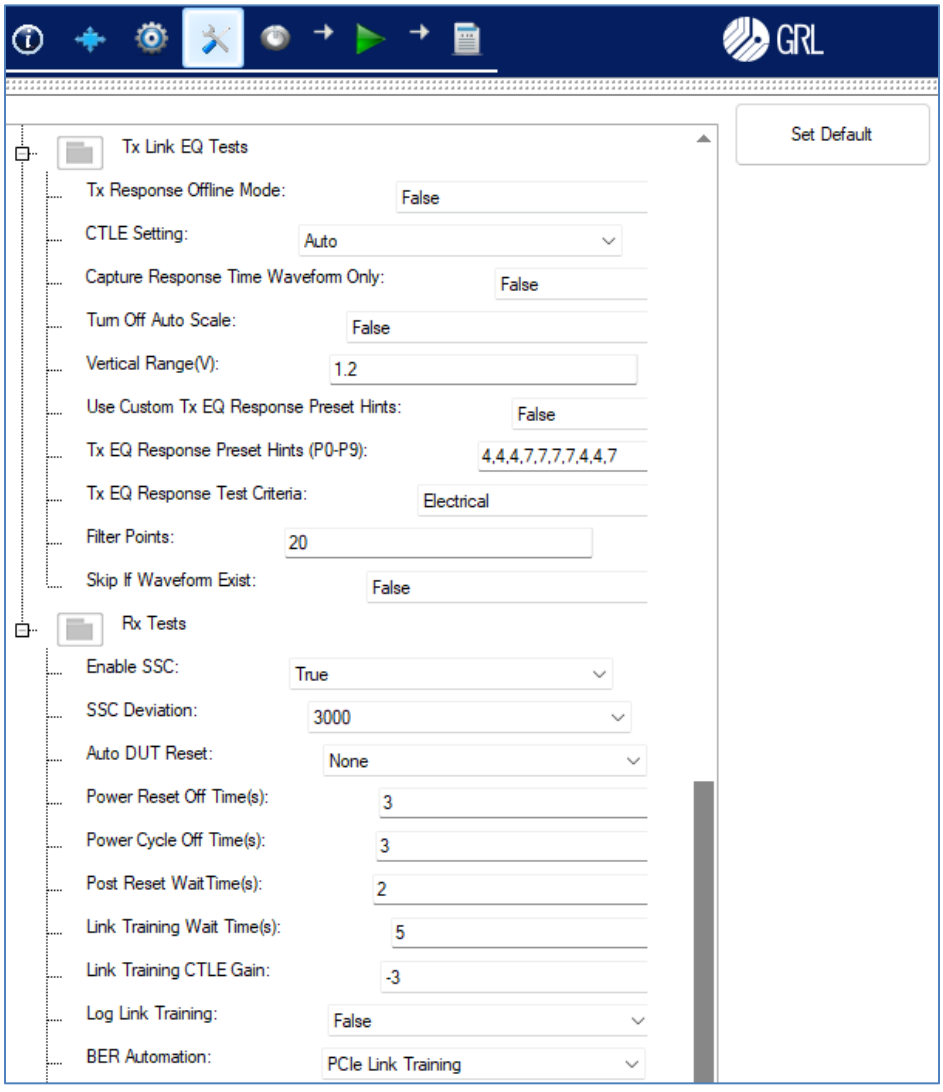


FIGURE 36. TEST PARAMETERS CONFIGURATION PAGE

TABLE 5. TEST PARAMETERS DESCRIPTION

Parameter	Description
Tx Response Offline Mode	Select 'True' to enable running Tx link equalization response tests in offline mode using appropriate offline PCIe compliant waveforms.
CTLE Setting	Select the CTLE method or gain setting index to be used when decoding PCIe compliant waveforms to verify Tx equalization change during link equalization response tests.
Capture Response Time Waveform Only	Select 'True' to enable capturing waveform data for time response verification only when running Tx link equalization response tests.
Turn Off Auto Scale	Select 'True' to disable auto scaling during Tx link equalization response tests.
Vertical Range (V)	Set the vertical range of the Scope to easily detect a change to the voltage level when running Tx link equalization response tests.
Use Custom Tx EQ Response Preset Hints	Select 'True' to enable custom preset hints to be used when running Tx link equalization response tests.
Tx EQ Response Preset Hints (P0-P9)	If 'True' is selected from the '**Use Custom Tx EQ Response Preset Hints**' field, specify the custom preset hints for Preset 0 to Preset 9.
Tx EQ Response Test Criteria	Select to enable the Tx link equalization response negotiation to occur in either the 'Electrical' level only or simultaneously in both the 'Electrical and Protocol' level.
Filter Points	Set the number of points that need to be captured.
Skip If Waveform Exist	Select 'True' to skip the Tx link equalization response tests if there are existing waveforms.
Enable SSC	Select 'True' to enable Spread Spectrum Clock (SSC) capabilities for receiver testing (if supported by the DUT).
SSC Deviation	If 'True' is selected from the '**Enable SSC**' field, select the Deviation values for SSC.
Auto DUT Reset	Select which controller device connected with the GRL software to be used to perform auto reset for the DUT as required during test runs.
Power Reset Off Time (s)	Set the duration in seconds to reset the power for the system under test when internal power reset mechanism is used.
Power Cycle Off Time (s)	Set the duration in seconds to cycle the power for the system under test when internal power cycle mechanism is used.
Post Reset Wait Time (s)	Set the delay/buffer in seconds after power is reset for the system under test.
Link Training Wait Time (s)	Set the delay/buffer in seconds before initiation of each link training step.

Link Training CTLE Gain	Select the CTLE gain for the BERT error detector.
Log Link Training	Select 'True' to enable logging for the link training steps.
BER Automation	Select 'PCIe Link Training' to run BER automation tests using Anritsu PCIe Link Sequencer software loopback method, or select 'Manual' to run BER automation tests manually.
Prompt Before Link EQ Training	Select 'True' to enable a prompt to come up prior to start running Rx link equalization tests.
Ignore Failed Link Training	Select 'True' to ignore tests that have failed when running the PCIe loopback link training sequence.
Compliance BER Measurement Time (s)	Set the duration in seconds to complete the Rx compliance testing to measure Bit Error Ratio (BER).
Maximum Compliance Error	Set the maximum error count for error checking during Rx compliance test runs.
Margin Test Measurement Time (s)	Set the duration in seconds to complete the Rx SJ margin search testing.
Margin Test Max Steps	Set the maximum number of steps for stepping through margins during the SJ margin search test.
Margin Test Step Size (%)	Set the step size in percentage for stepping through margins during the SJ margin search test.
Maximum Margin Test Error	Set the maximum error count for error checking during the SJ margin search test.
Loopback Mode	Select 'Recovery' (recommended) or 'Configuration' to be used as the link training method for placing the DUT in the loopback state.
Default Link Training Sequence	Select 'Yes' to enable the default sequence for link training to be used.
Retrain When SJ Frequency Changed	Select 'True' to re-send link training sequence when there is a change in the SJ frequency.
Margin Search Live Plot	Select 'True' to enable a graphical margin plot that updates as the margin test is performed to indicate progress of the test results.
Apply CM	Select 'Yes' to integrate the common mode component in a specific test.
PPG Start Preset	Select the preset co-efficient to be used at the start of link training.
DUT Initial Preset	Select the initial preset co-efficient for the DUT to be applied during Rx compliance test runs.
PPG Final Preset	Select the preset co-efficient to be used after link training is successful for the final BER test. If 'Auto' is selected, a negotiated preset will be applied during the final BER test.

DUT Final Preset	Select the preset co-efficient for the DUT to be applied during the final BER test.

5.10 Enable Loopback BER Test

To set up the GRL software to automate loopback testing for error detection, go to the Equipment Setup page and type in the VISA address that connects to the Anritsu MX183000A High-Speed Serial Data Test Software.

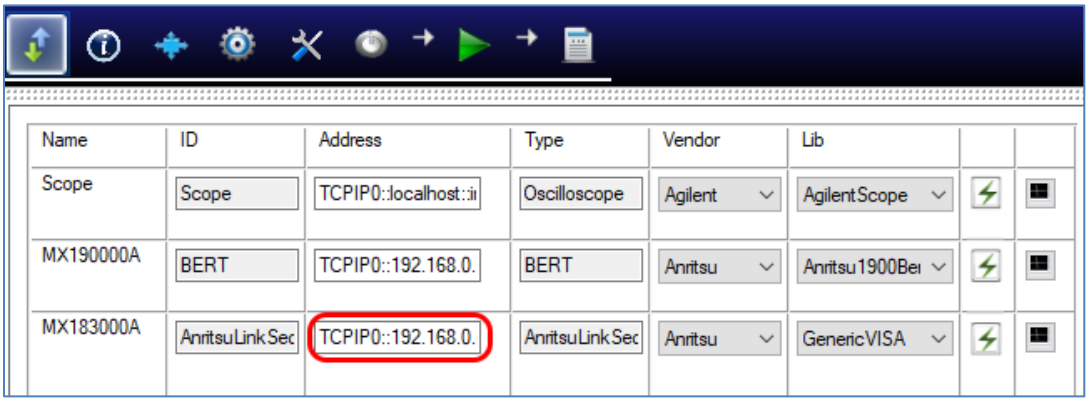


FIGURE 37. CONNECT EQUIPMENT FOR LOOPBACK BER TEST

On the Configurations page, select the BER Automation test method as 'PCIe Link Training' to enable the Anritsu PCIe Link Sequencer software loopback mode. Additional configurations can also be made through this page.

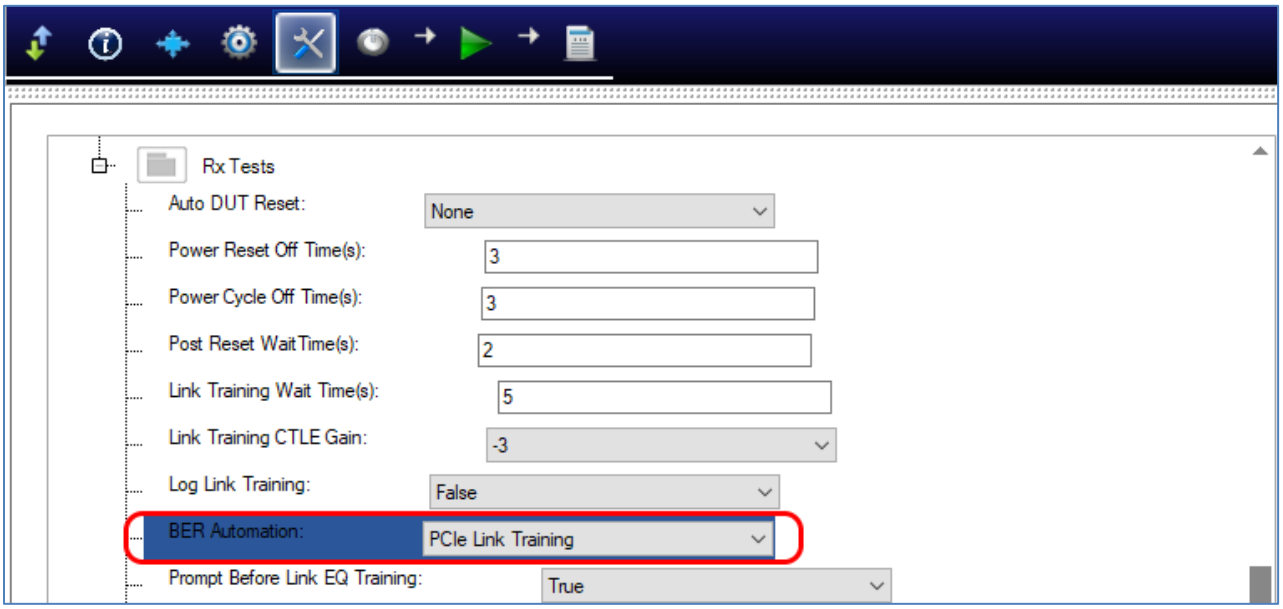


FIGURE 38. SELECT BER LOOPBACK TEST METHOD

5.11 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE5-CEM-RXA software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

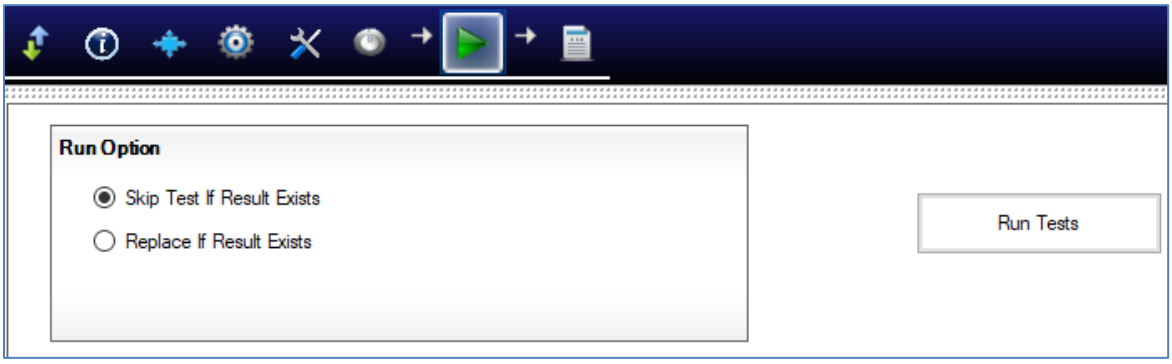


FIGURE 39. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed. Below shows an example of the connection diagram pop-up for the system board DUT Rx compliance test.

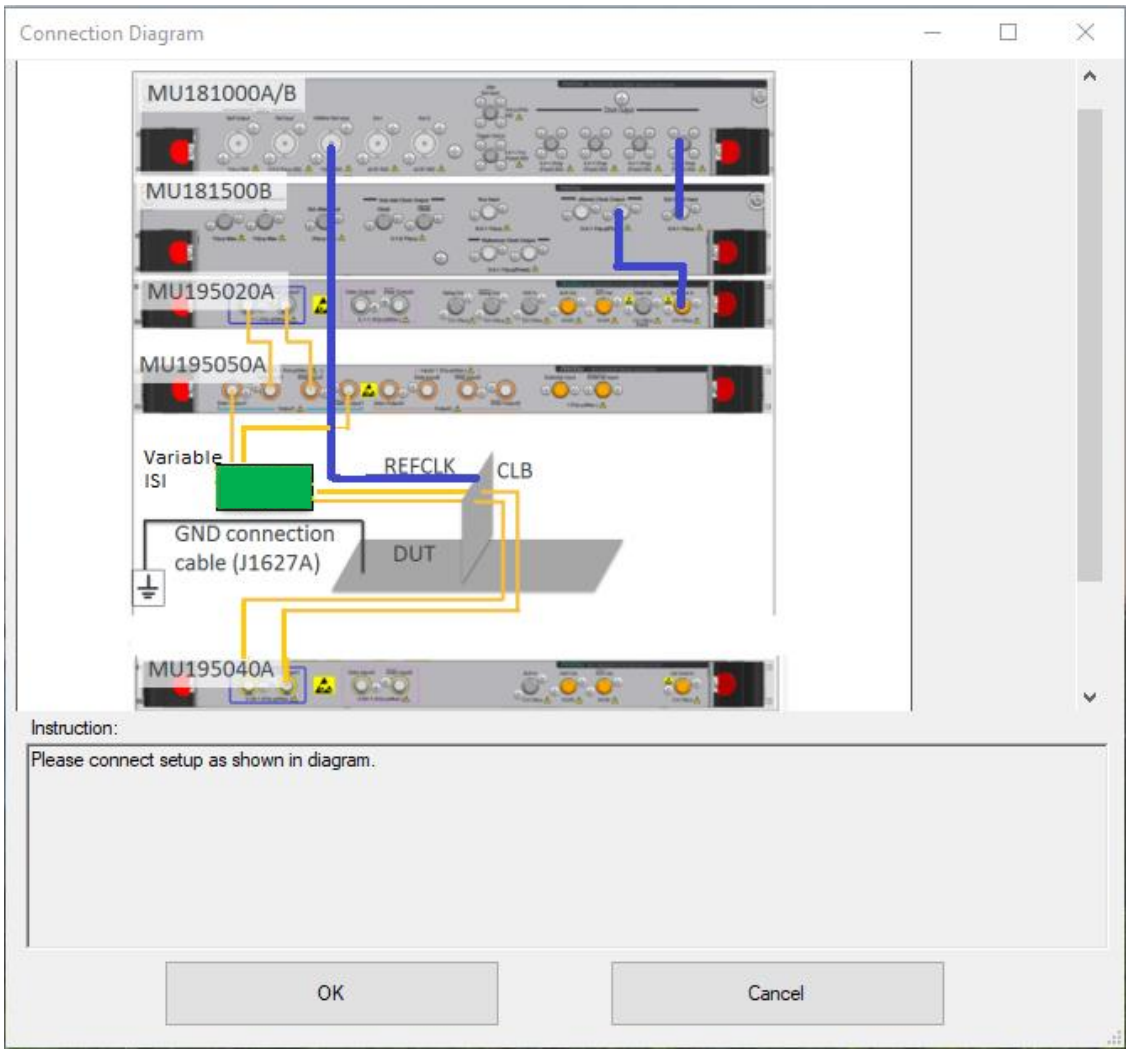


FIGURE 40. EXAMPLE CONNECTION POP-UP DIAGRAM FOR RX COMPLIANCE TEST

6 Interpreting GRL-PCIE5-CEM-RXA Test Report

When all calibration and test runs have completed from the previous section, the GRL-PCIE5-CEM-RXA software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

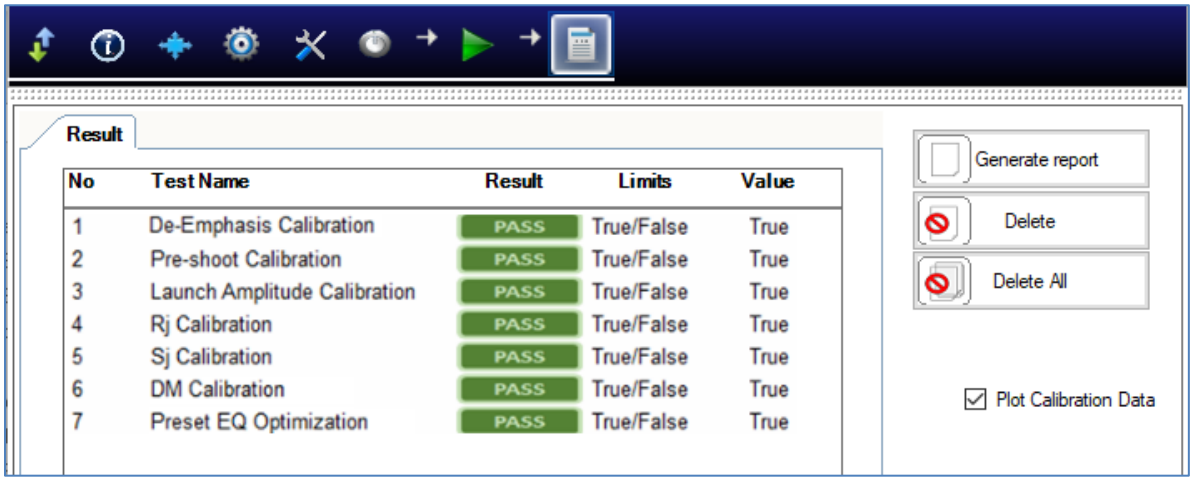


FIGURE 41. TEST REPORT PAGE

6.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

6.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.

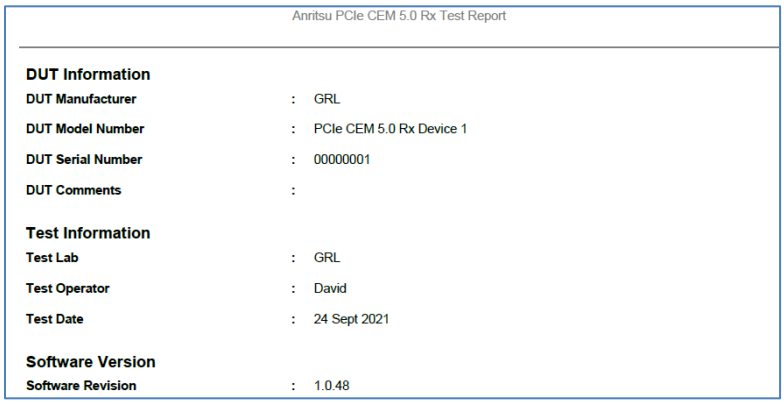


FIGURE 42. TEST SESSION INFORMATION EXAMPLE

6.1.2 Test Summary Table

This table provides an overall view of all the calibration and tests performed along with their conditions and results.

Anritsu PCIe CEM 5.0 Rx Test Report

No	TestName	Limits	Value	Results	SJ Frequency
1	Preset 4 Calibration	N/A	N/A	Pass	
2	Launch Amplitude Calibration	N/A	N/A	Pass	
3	De-Emphasis Calibration	N/A	N/A	Pass	
4	Pre-shoot Calibration	N/A	N/A	Pass	
5	Rj Calibration	N/A	N/A	Pass	
6	Sj Calibration	N/A	N/A	Pass	SJ_33khz
7	Sj Calibration	N/A	N/A	Pass	SJ_1Mhz
8	Sj Calibration	N/A	N/A	Pass	SJ_10Mhz
9	Sj Calibration	N/A	N/A	Pass	SJ_100Mhz
10	DM Calibration	N/A	N/A	Pass	
11	CM Calibration	N/A	N/A	Pass	
12	Preset EQ Optimization	N/A	N/A	Pass	
13	DM Optimization	N/A	N/A	Pass	
14	Final Eye Calibration	N/A	N/A	Pass	

Rx Compliance Test

Sj Frequency	SJ_100Mhz
Result	PASS(1)

**Note: In the example above, the number "(1)" next to "PASS" indicates the number of errors detected along with the pass/fail status.*

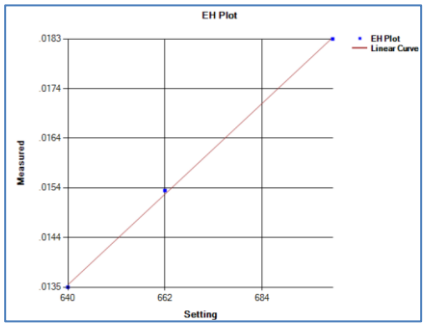
FIGURE 43. TEST SUMMARY TABLE EXAMPLE

6.1.3 Test Results

This portion displays the results in detail along with supporting data points and screenshots for each calibration/test run.

14. Final Eye Calibration

Pass/Fail Stats	:	Pass
EH Limits	:	13.50 mV <= EH <= 16.50 mV
EW Limits	:	8.88 ps <= EW <= 9.88 ps
Cal Parameter 1	:	EH
EH Settings	:	662.0000
EH Measured Value	:	15.3657 m
Cal Parameter 2	:	EW
EW Settings	:	128.0000 m
EW Measured Value	:	9.3951
Final DM Value	:	28.0392 mV
Final DM Settings	:	5.50000E+001 mV
SigTest Version	:	
Test completed time	:	31 May 2021 19:25:06 PM



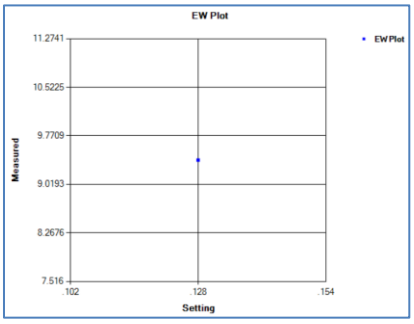


FIGURE 44. TEST RESULTS EXAMPLE

6.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

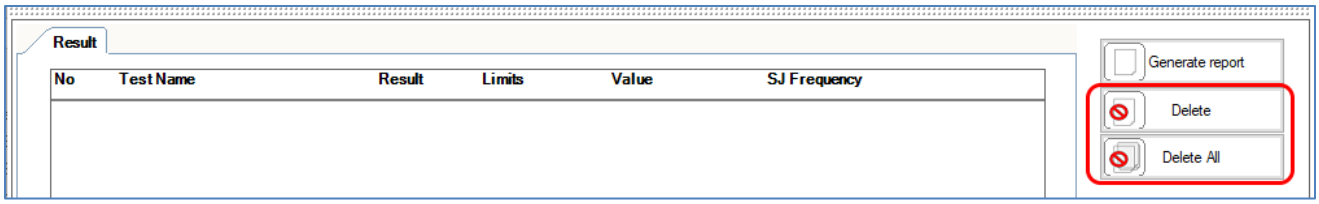


FIGURE 45. DELETE TEST RESULTS

7 Saving and Loading GRL-PCIE5-CEM-RXA Test Sessions

The usage model for the GRL-PCIE5-CEM-RXA software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To ***create a new test session*** and return the application back to the default configuration, select Options → 'New Session'.

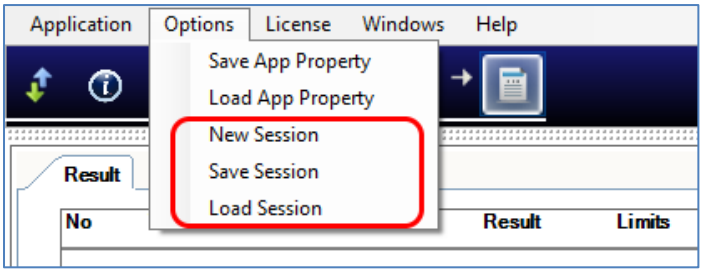


FIGURE 46. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

8 Appendix A: Method of Implementation (MOI) for Manual PCIe CEM 5.0 Receiver Measurements

This section describes how to manually perform PCIe CEM 5.0 Rx calibration and DUT compliance testing based on Anritsu's recommended test procedure using the MP1900A BERT.

The following steps give a general overview for testing the PCIe CEM 5.0 receiver.

i) Calibrate for the following components:
   - Channel Loss measurement with a vector network analyzer (VNA)
   - Eye Amplitude, Preset, SJ and RJ measurements with MP1900A BERT and high-performance real-time oscilloscope
   - DM Amplitude and Eye Height/Eye Width measurements with MP1900A BERT and high-performance real-time oscilloscope

ii) Perform link training sequence for BER loopback testing:
   - Enable DUT loopback mode for error detection with MP1900A BERT
   - Troubleshoot in the case of link training failure

iii) Test for DUT Rx compliance to target specifications:
   - BER compliance checking for <1E-12 with stressed eye
   - SJ marginal testing (optional)

Note: Existing PCI-SIG Compliance Load Boards (CLB's) and Compliance Base Boards (CBB's) will be used as test fixtures for system host and device DUT's respectively.

8.1 Perform Calibration

This section describes how to calibrate for the stressed test signal before testing the receiver for compliance.

Calibration is initially performed for Channel Loss, followed by Eye Amplitude and Presets, RJ and SJ, and DM-SI. The final step is to determine the Eye Width (EW) and Eye Height (EH).

The main equipment required for calibration consists of the MP1900A BERT, high performance real-time oscilloscope, and vector network analyzer. The SigTest application will also be used to ensure signal quality compliance.

8.1.1 Calibration Settings

Configure the following settings to be applied for PCIe Gen 5 based Rx calibration.

TABLE 6. CALIBRATION SETTINGS

Component	Setting	PCIe Gen 5
Variable ISI Board	Insertion Loss (dB)	34-37 [a]
SigTest	CTLE Gain (dB)	9-15 [b]
MP1900A BERT	Tx Emphasis Preset	P5, P6, P8, P9
	Amplitude (mV)	550 *(800 mVpp-diff at output of Noise Module)*
	RJ (mUIpp)	180
	SJ @100 MHz (UIpp)	0.1
	DM-I (mV)	27
	CM-I (mVpp)	170.0

[a] The insertion loss measures in between 34 to 37 dB for all configurations using different variable ISI pairs that provide the correct amount of insertion loss being measured.

[b] The CTLE range from 9 dB to 15 dB in 1 dB step sizes is run for every waveform. (Note that this is a subset of allowed CTLE range. This subset is used to reduce calibration time.)

The following table shows the calibration targets to achieve:

TABLE 7. CALIBRATION TARGETS

Setting	PCIe Gen 5
Amplitude (mV)	800
RJ (psrms)	0.5
SJ @100 MHz (mUIpp)	100 (at TP3)
DM-I (mVpp)	10 (at TP2)
CM-I (mVpp)	150
EH (mV)	*13.5 to 16.5*
EW (ps)	*8.875 to 9.875*

8.1.2 Calibration Process

Calibration for the PCIe CEM 5.0 electrical specification will basically be performed at two physical test points: TP3 and TP2 (for the Long Channel). Test Point 3 (TP3) is a physical test point for calibration without the effect of a channel. An adjustable CEM connector will be used along with the calibration channel for testing the receiver. This will need to adjust the eye amplitude to

specification values when measuring eye height/eye width. TP2 is a physical test point that will affect the eye opening due to trace length.

For the Long Channel TP2 calibration, an existing PCI-SIG CBB test fixture will be used as the host system board or PCI-SIG CLB test fixture for the add-in card device. The board will be connected between the BERT noise generator output and the oscilloscope which will validate the test pattern of the signal and measure for stress tolerance to final stressed eye compliance.

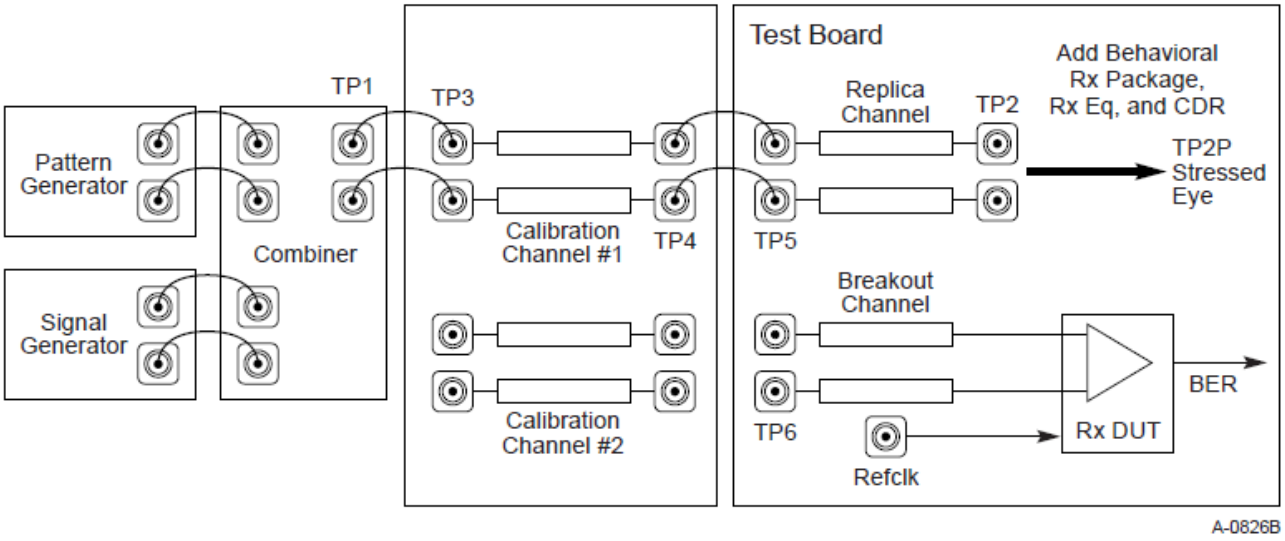


Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

FIGURE 47. PHY TEST SPECIFICATION RX CALIBRATION DIAGRAM FOR PCIE GEN 5

8.1.3 Channel Loss Calibration

The following connection diagram shows the channel loss calibration setup for PCIe Gen 5 using a 4-port (differential) vector network analyzer (VNA) and a compliant CLB/CBB test fixture for the add-in card and system board.

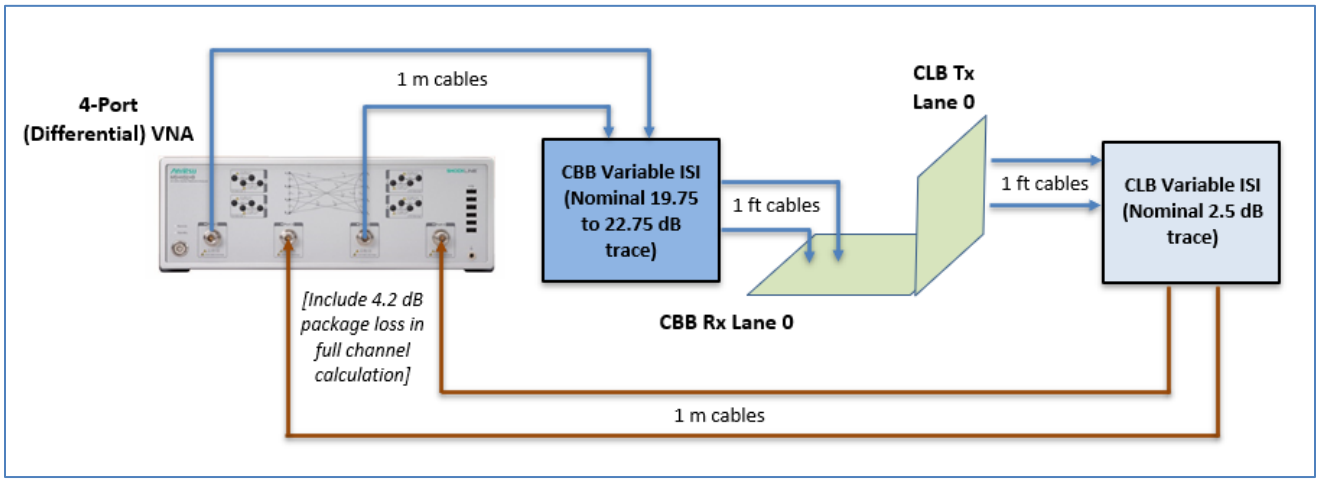


FIGURE 48. CONNECTION DIAGRAM FOR CHANNEL LOSS CALIBRATION (ADD-IN CARD)

***Note**: For the Add-In Card CEM Rx calibration, a 9.5 dB add-in card budget and 19.75 to 22.75 dB system budget shall be used in the intended 34 to 37 dB pad-to-pad loss range.*

1. Using 1 ft cables, connect between both the CBB Rx Lane 0 and CBB Variable ISI (Nominal 19.75 to 22.75 dB trace) and between both the CLB Tx Lane 0 and the CLB Variable ISI (Nominal 2.5 dB trace).
2. Using 1 m cables, connect between both the VNA Ports 1 & 3 and the CBB Variable ISI and between both the CLB Variable ISI and the VNA Ports 2 & 4.

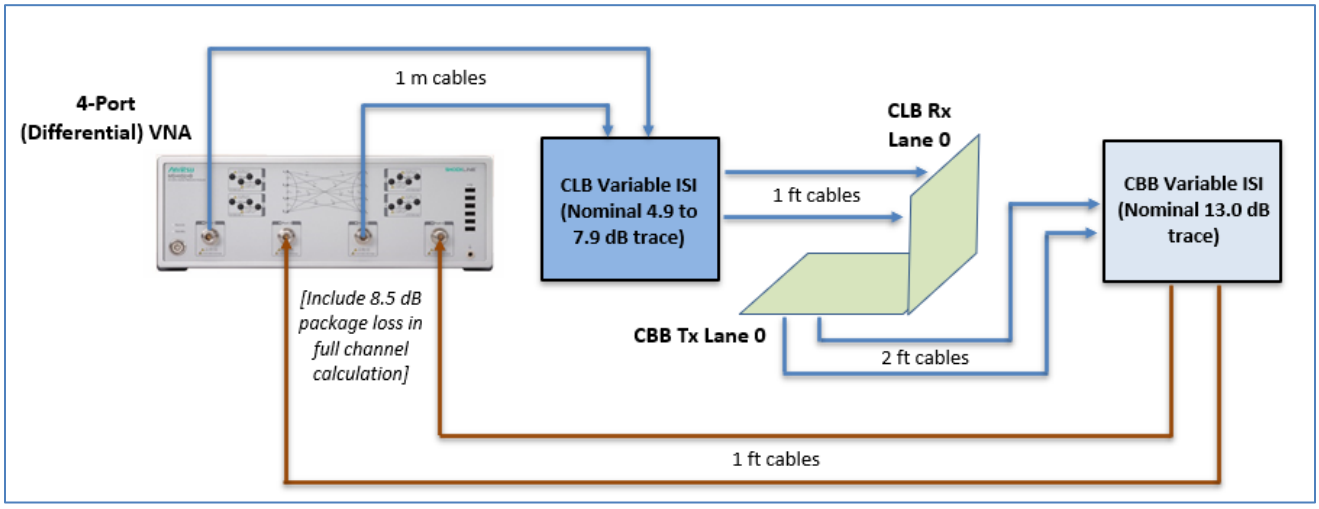


FIGURE 49. CONNECTION DIAGRAM FOR CHANNEL LOSS CALIBRATION (SYSTEM BOARD)

***Note**: For the System Board CEM Rx calibration, a 26.5 dB system budget and 7.5 to 10.5 dB add-in card budget shall be used in the intended 34 to 37 dB pad-to-pad loss range.*

1. Using 1 ft cables, connect between both the CLB Rx Lane 0 and CLB Variable ISI (Nominal 4.9 to 7.9 dB trace).
2. Using 2 ft cables, connect between both the CBB Tx Lane 0 and the CBB Variable ISI (Nominal 13.0 dB trace).
3. Using 1 m cables, connect between both the VNA Ports 1 & 3 and the CLB Variable ISI and between both the CBB Variable ISI and the VNA Ports 2 & 4.

8.1.4 Amplitude, Preset, SJ and RJ Calibration Setup

The following connection diagram shows the calibration setup for amplitude, preset, SJ, and RJ at TP3 without any channel effect. The MP1900A BERT is directly connected to a digital oscilloscope supporting ≥ 50 GHz bandwidth and ≥ 128 GS/s sampling rate.

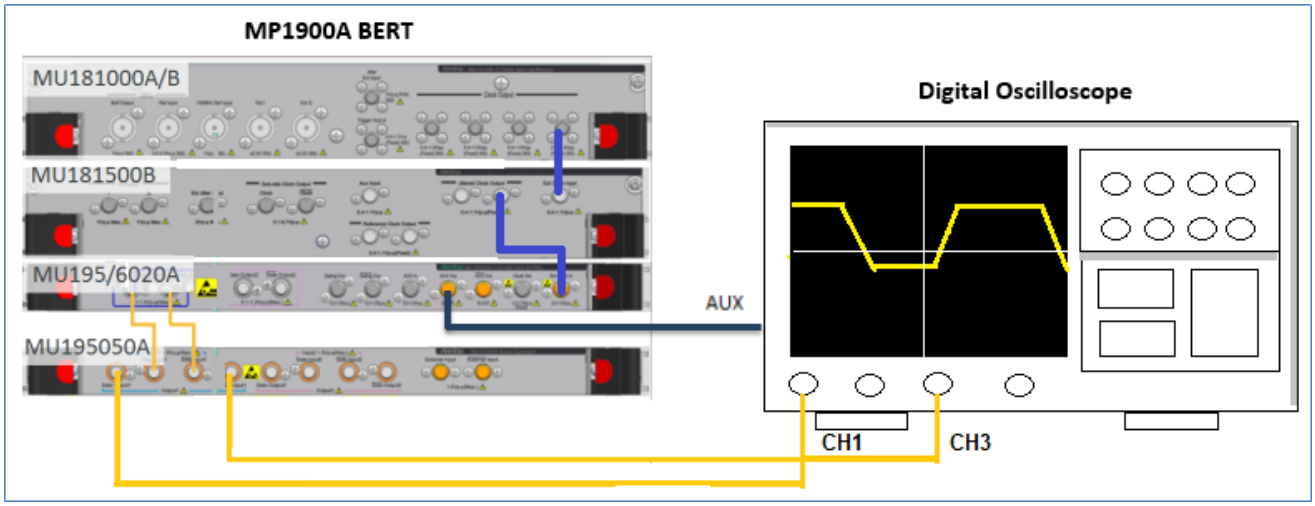


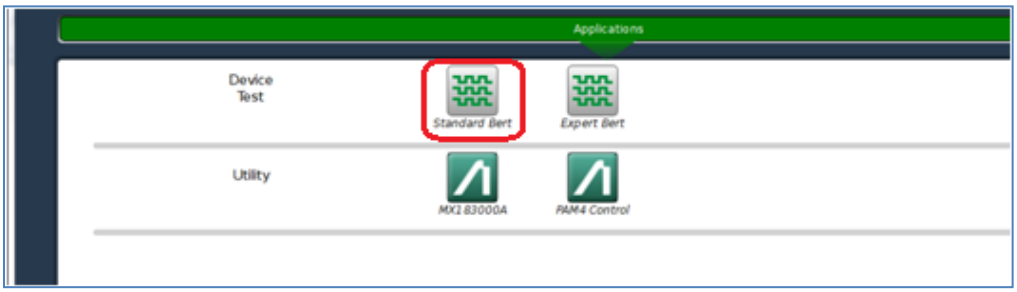
FIGURE 50. CONNECTION DIAGRAM FOR AMPLITUDE, PRESET, SJ AND RJ CALIBRATION

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to the digital Scope channels.
5. Using a SMA cable, connect the MU195020A/MU196020A Aux output to the digital Scope for pattern sync triggering.

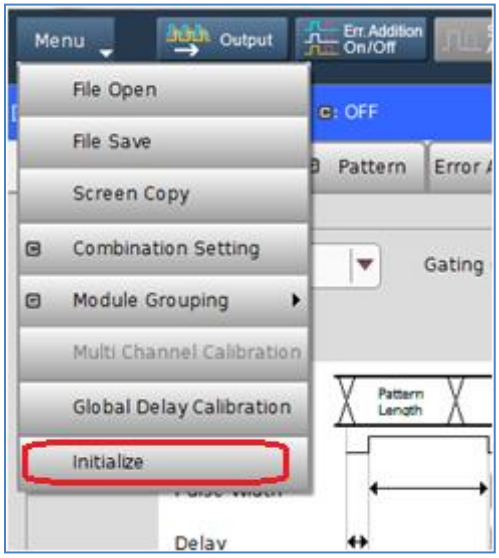
8.1.5 Anritsu Standard BERT Device Test Application (MX190000A) Startup

To adjust the calibration parameters when measuring on the Scope, use the MX190000A Standard test application on the MP1900A BERT.

1. On the BERT's Applications screen, select the MX190000A Standard Bert application for SI (if using SI-PPG) or Standard Bert application for SI and PAM4 (if using PAM4-PPG).



2. In the drop-down Menu, select 'Initialize' to start using the application.

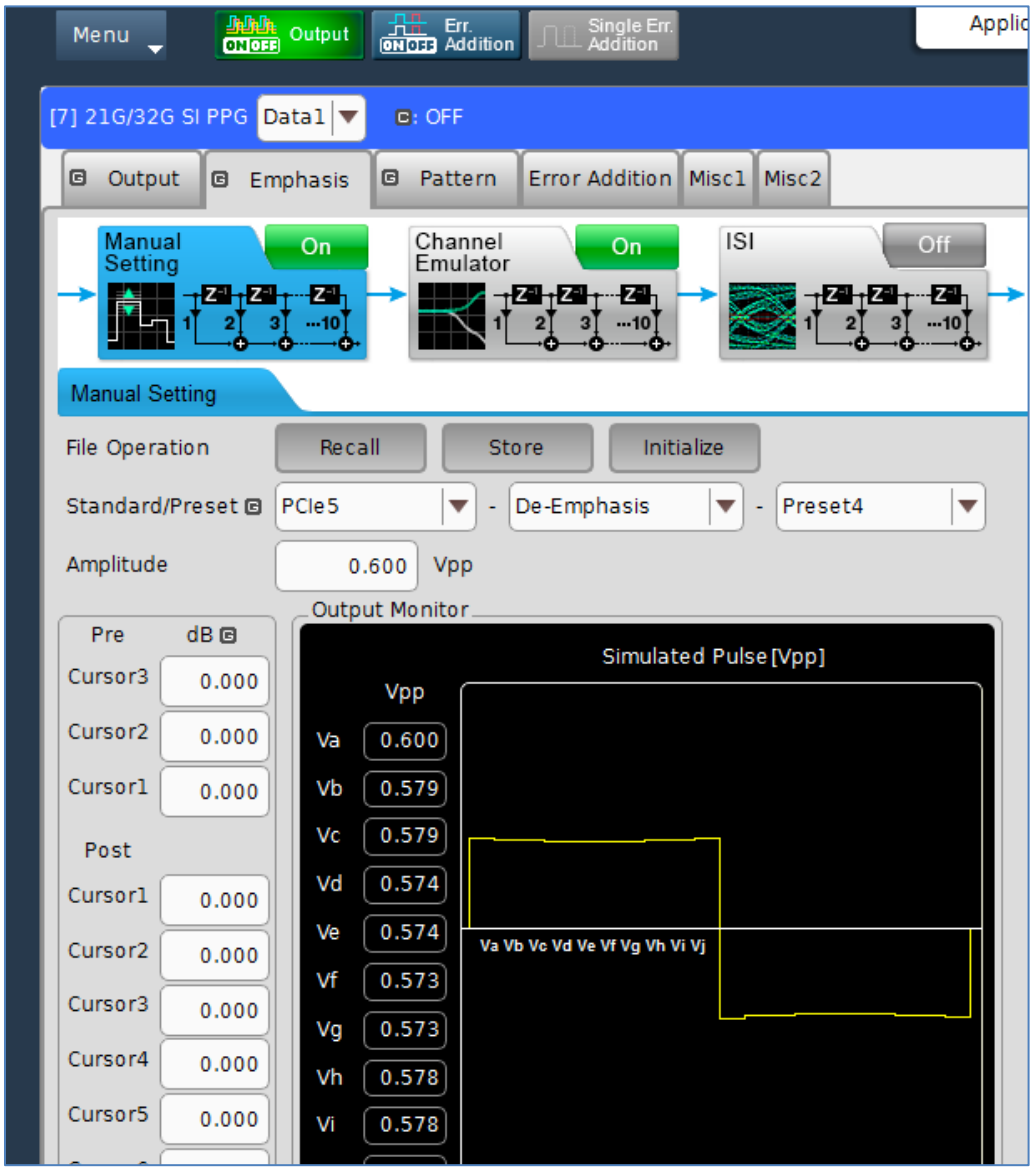


8.1.6 Amplitude Calibration Adjustment

Adjust the Amplitude with Scope markers to 800 mVpp(diff) using the following configuration.

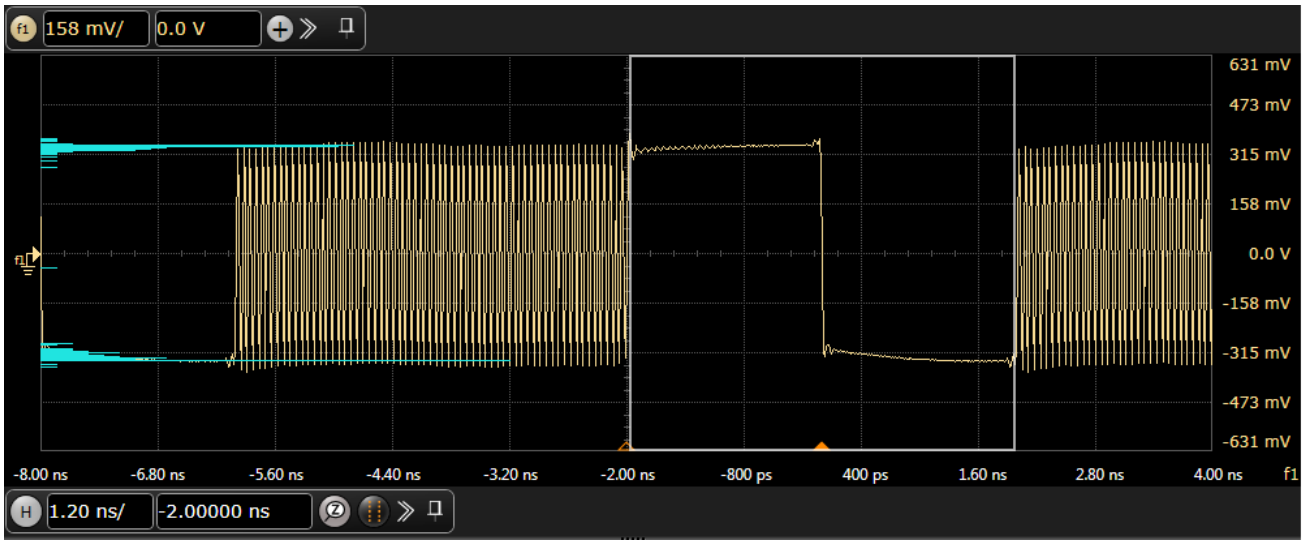
a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF, Manual Setting pane- Standard/Preset: PCIe5, De-Emphasis, Preset 4
- Select the Pattern tab- Test Pattern: Using Preset 4, with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 32.0 GT/s
- Select the Misc1 tab- Aux Output: Pattern Sync



b) Scope Settings:

- Averaging: 256 points
- Horizontal Scale: 100 ns/div
- Bandwidth: 50 GHz
- Sampling Rate: 128 GS/s



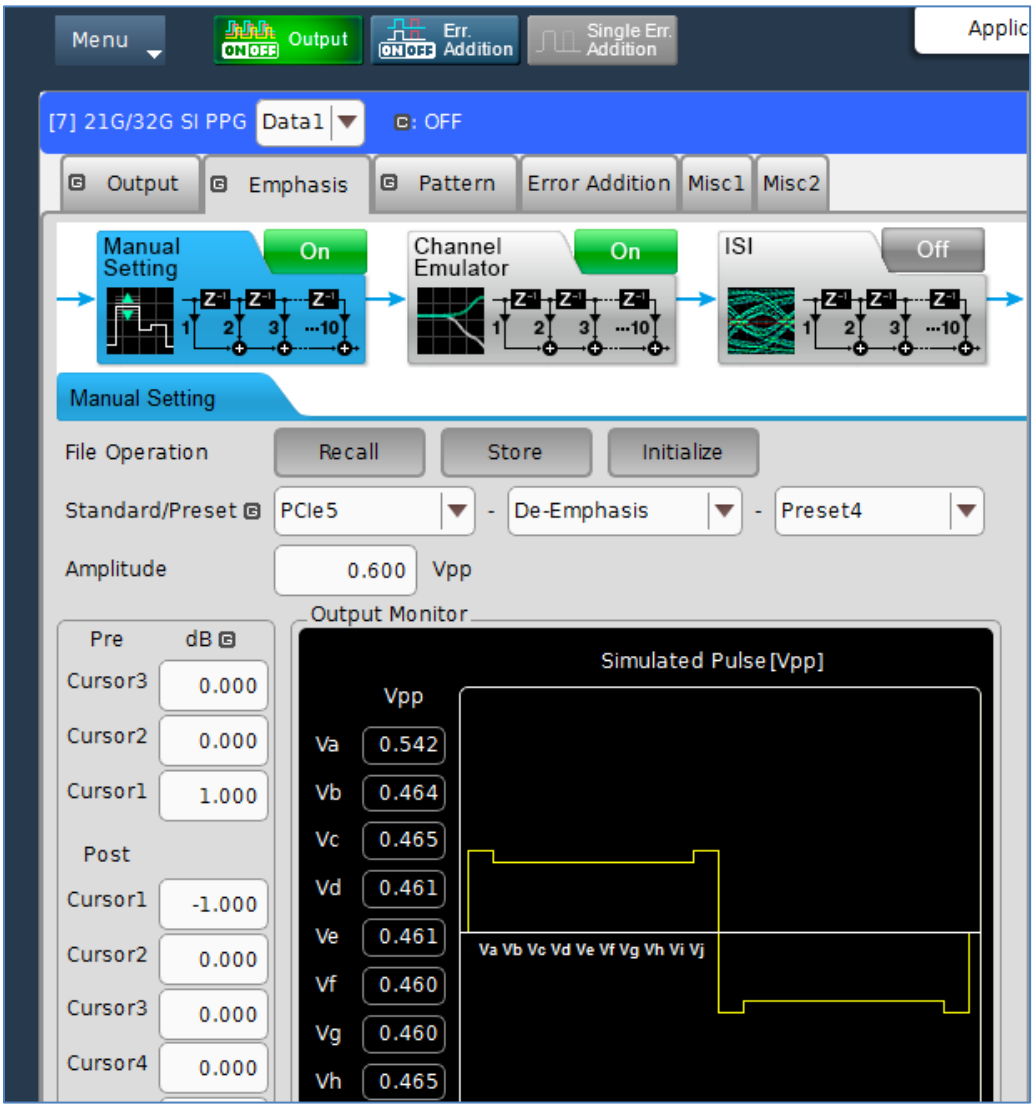
8.1.7 Preset Calibration Adjustment

Adjust the Pre and Post Cursor1 of Presets 0 to 9 with Scope markers using the following configuration.

Preset 4 Calibration:

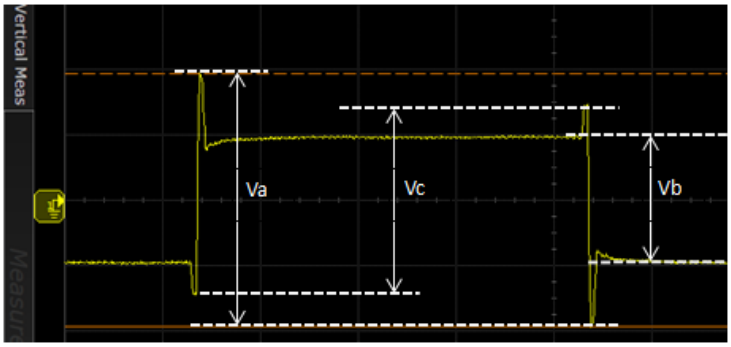
a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: ON
- Select the Pattern tab- Test Pattern: Using Preset 4, with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 32.0 GT/s
- Select the Misc1 tab- Aux Output: Pattern Sync



b) Scope Settings:

- Averaging: 256 points
- Horizontal Scale: 1 ns/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥128 GS/s



De-emphasis = $20\log_{10}(Vb/Va)$

Preshoot = $20\log_{10}(Vc/Vb)$

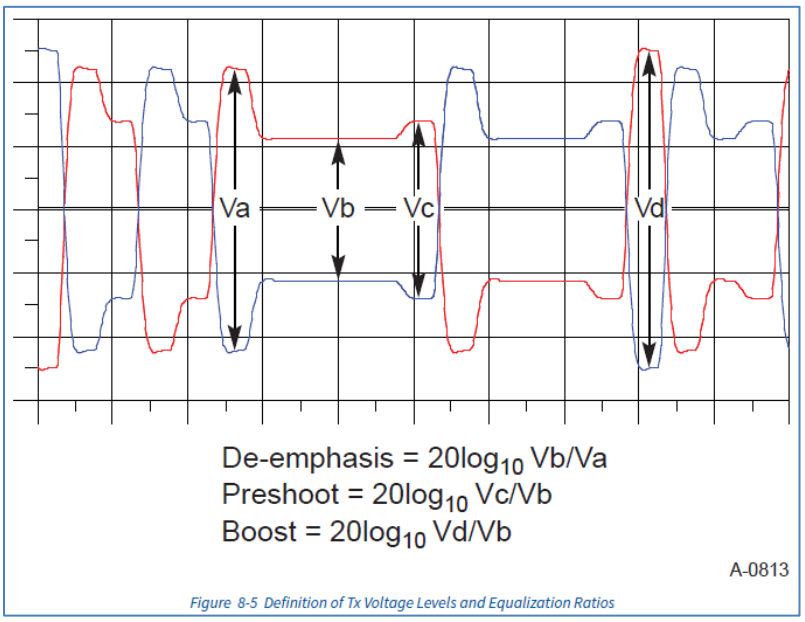


Figure 8-5 Definition of Tx Voltage Levels and Equalization Ratios

Other Presets Calibration (De-Emphasis and Preshoot):

a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF, Manual Setting pane- Standard/Preset: PCIe5, De-Emphasis, Preset 4
- Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen5_P0
- Select the Misc1 tab- Aux Output: Pattern Sync

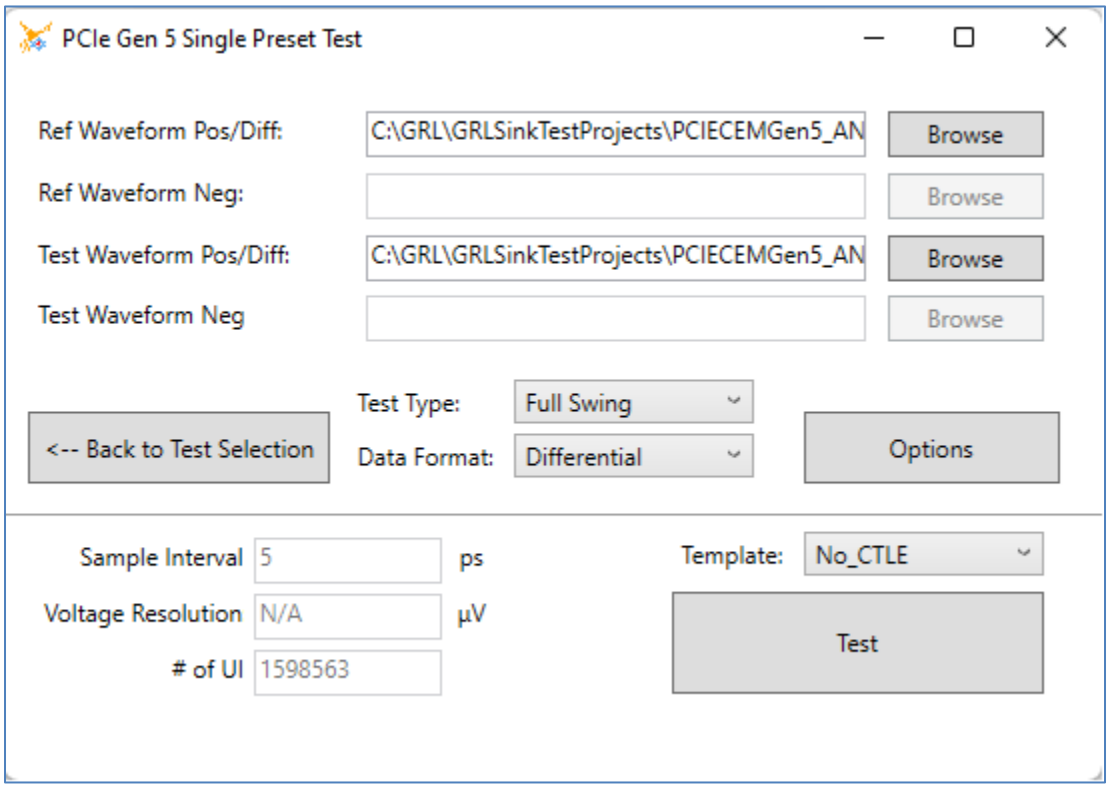
b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 10 µs/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥128 GS/s

c) SigTest Settings:

- Select Technology as ‘PCIe’
- Select Generation as “5_0”
- Select Test as “Preset_TestAC_SingleRun”

- Click “Confirm”
- Browse to the saved waveform file:
    - “Ref Waveform” is the Preset 4 waveform.
    - Test Waveform is the new waveform saved to measure Preshoot/De-Emphasis
- Select Template as “No_CTLE”
- Run Test



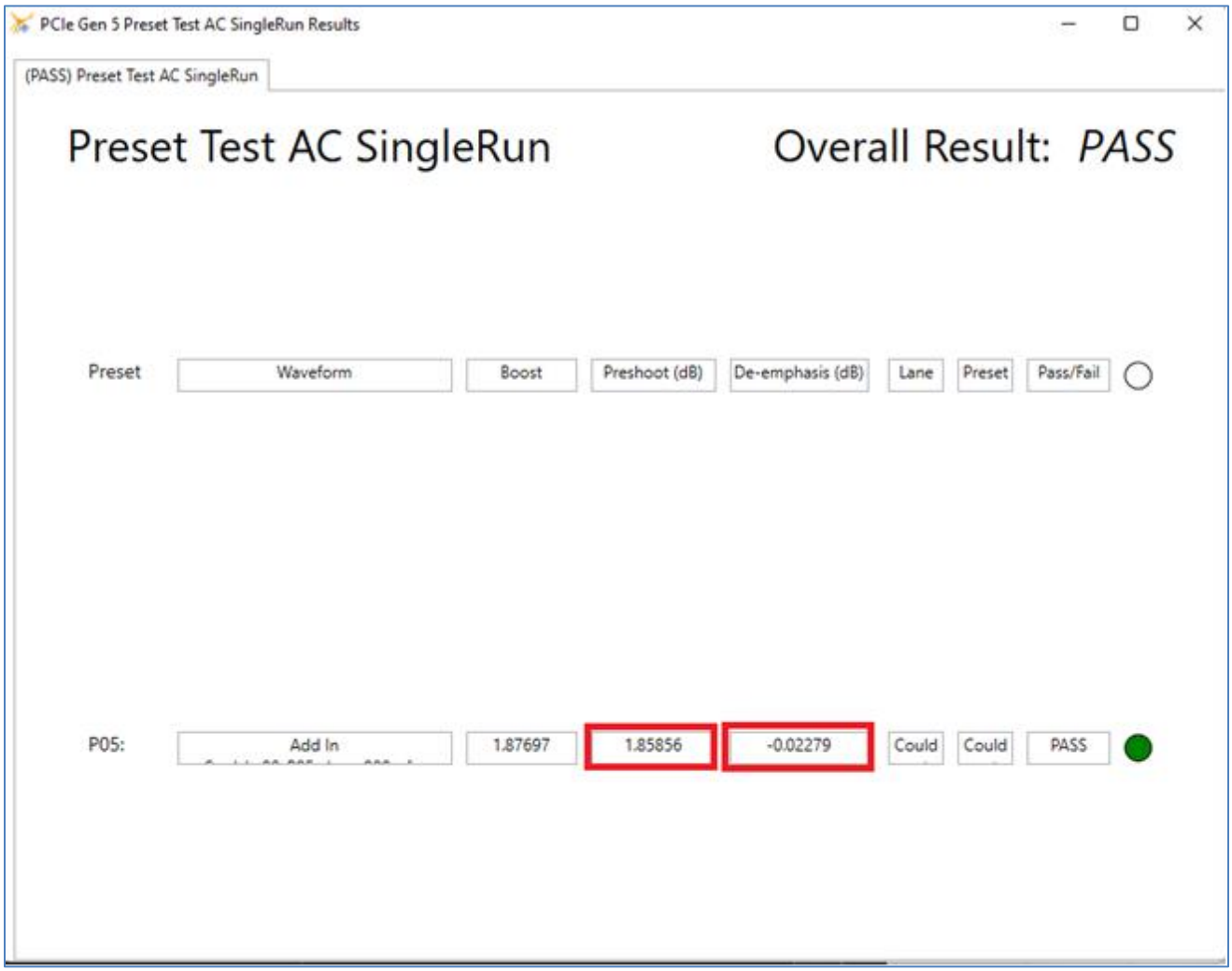


Table 8-1 Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Notes:

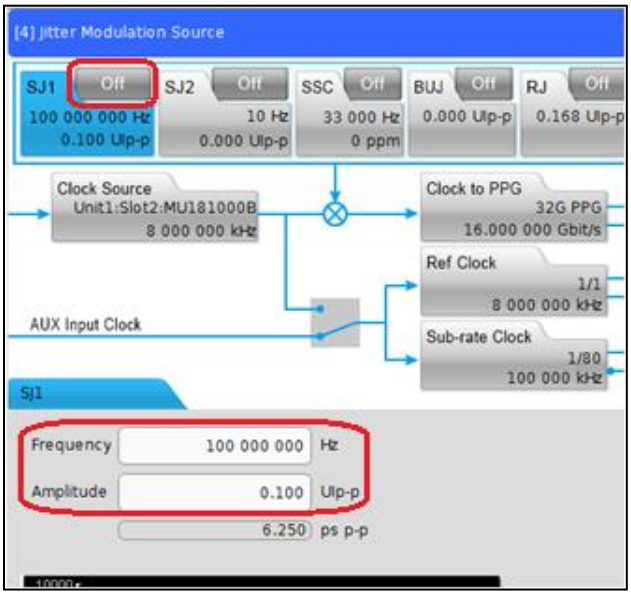
1. Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

8.1.8 SJ Calibration

Capture three waveforms for both TJ(Base) and TJ(Jittered) and analyze SJ using SigTest. Set up the following parameters.

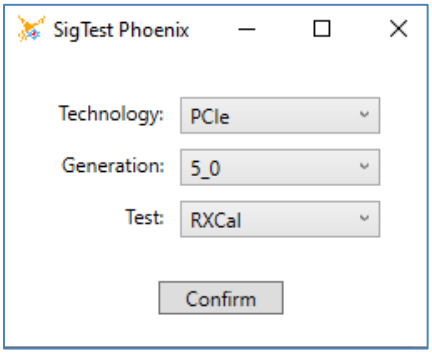
a) BERT Settings:

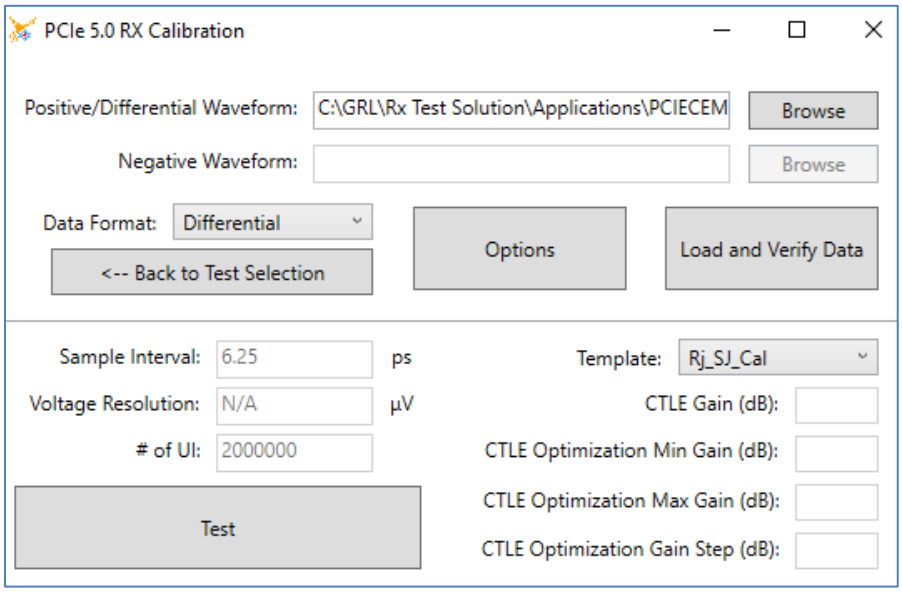
- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen5_P0
- Select Jitter Modulation Source- SJ1: ON
- SJ1 Frequency and Amplitude: 100 MHz, 0.000 UIpp, Measure Total Jitter as TJ(Base)
- SJ1 Frequency and Amplitude: 100 MHz, 0.100 UIpp, Measure Total Jitter as TJ(Jittered)



b) Scope Settings:
   - Averaging: OFF
   - Horizontal Scale: 10 µs/div
   - Bandwidth: 50 GHz
   - Sampling Rate: ≥128 GS/s

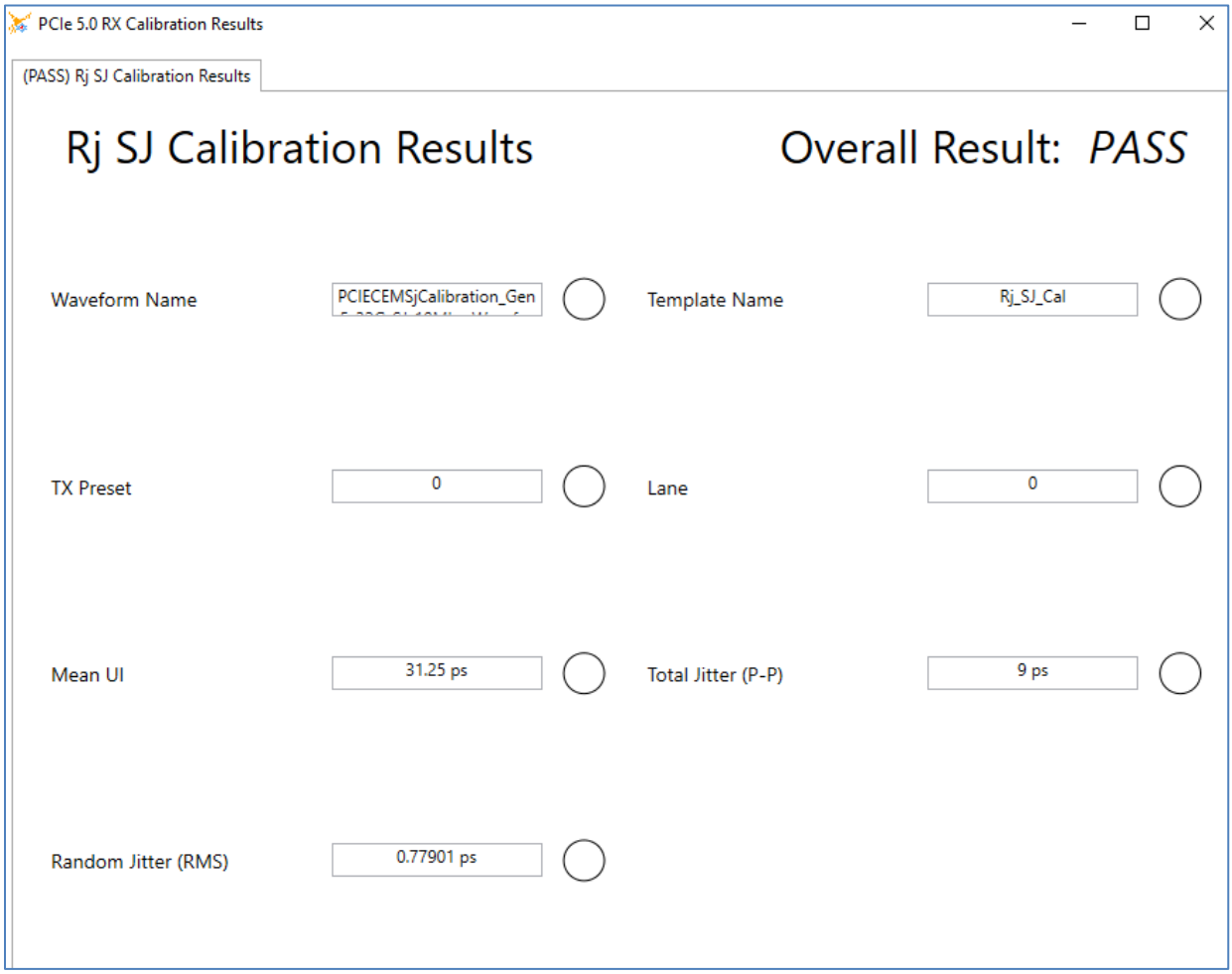
c) SigTest Settings:
   - Select Technology as 'PCIe'
   - Select Generation as "5_0"
   - Select Test as "RXCal"
   - Click "Confirm"
   - Browse to the saved waveform file
   - Select Template as "Rj_SJ_Cal"
   - Run Test





d) SigTest Results:

- Read 'Total Jitter (P-P)' value



- Calculate SJ by subtracting the average value of the three TJ(Jittered) and TJ(Base) waveforms.
- Adjust SJ until SJ = 3.125ps.

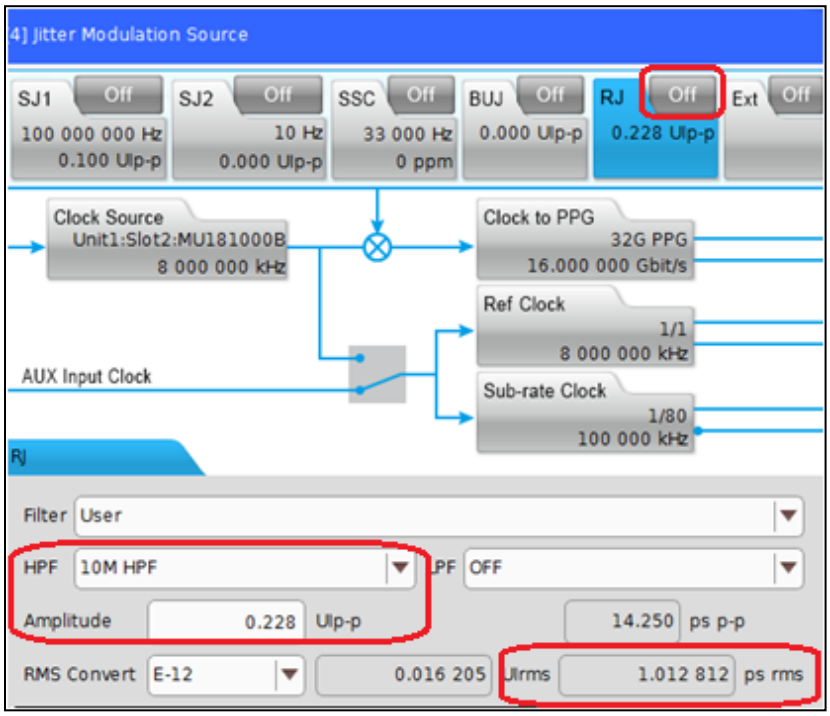
8.1.9 RJ Calibration

Capture the waveform on the Scope and analyze RJ using SigTest. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: Toggle_1bit

- Select Jitter Modulation Source- RJ: ON
- RJ HPF and Amplitude: 10 MHz, 0.228 UIpp

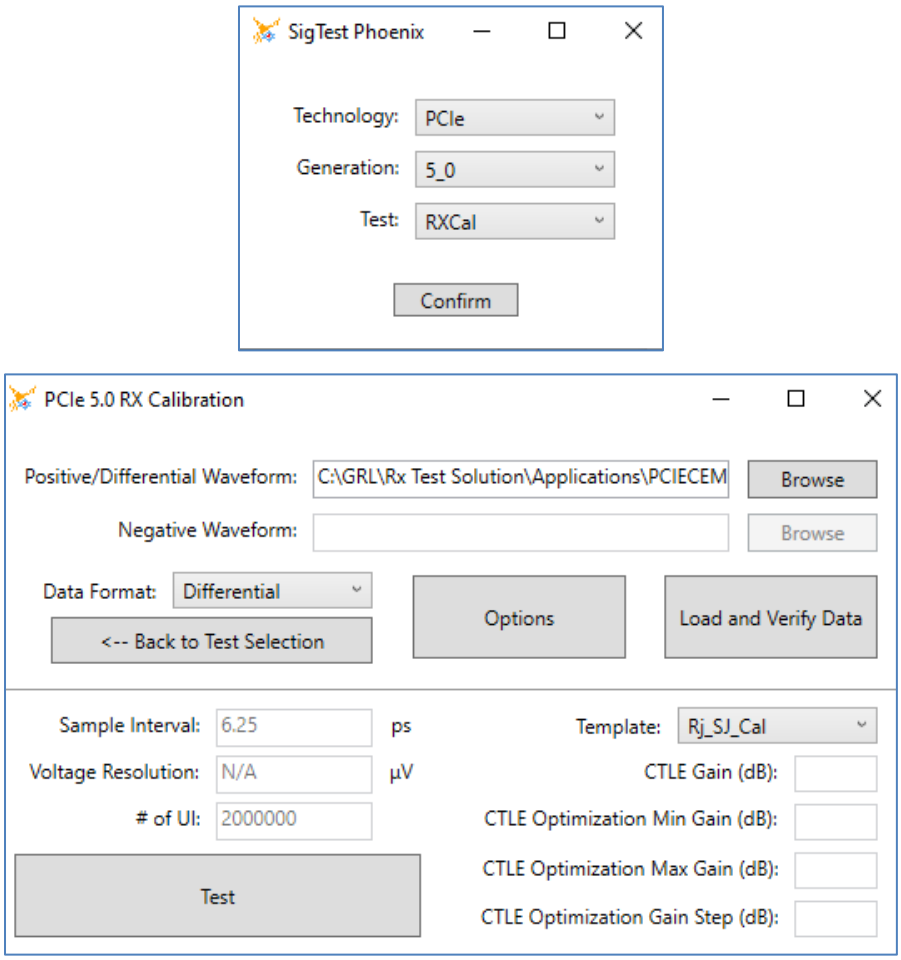


b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 10 µs/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥ 128 GS/s

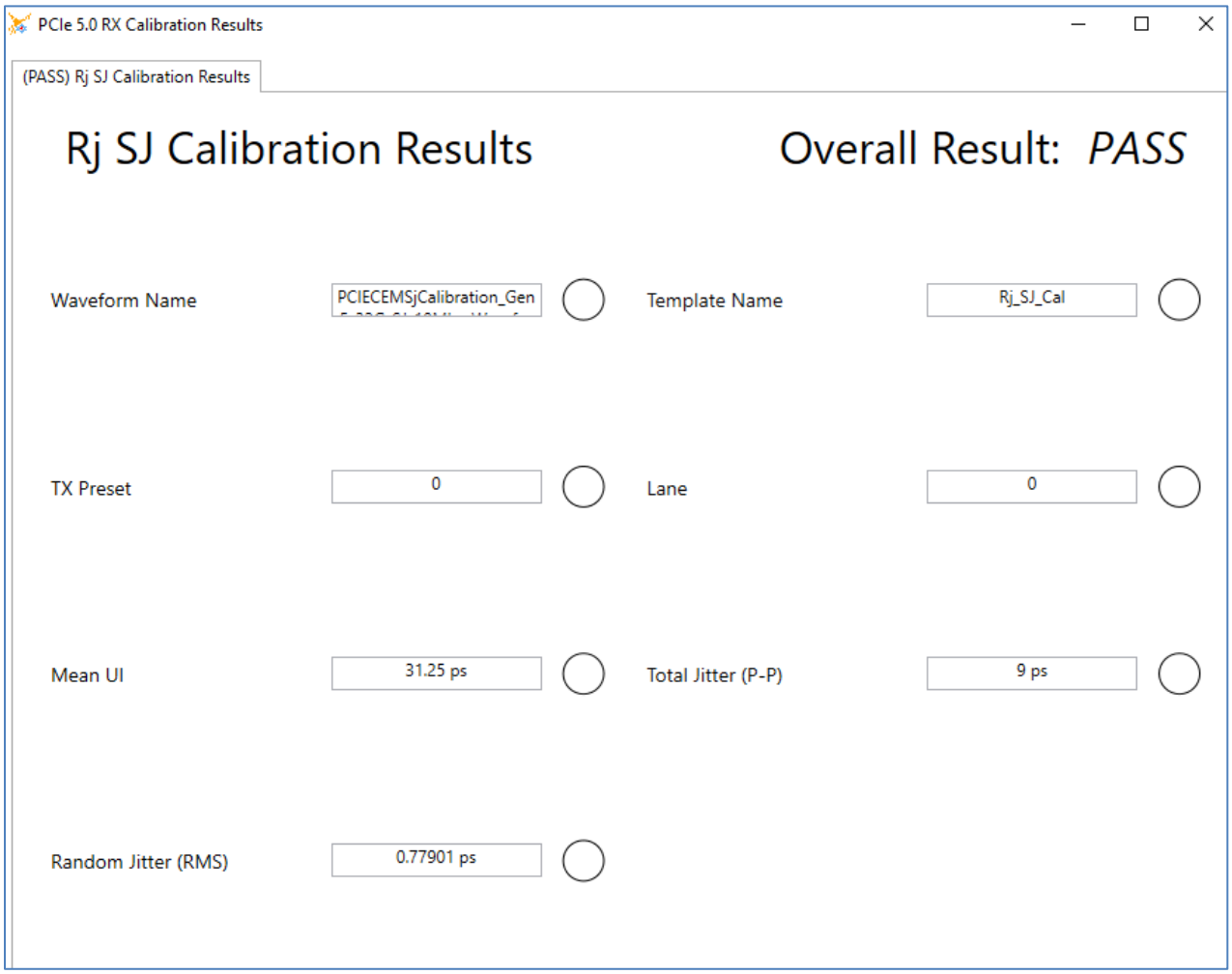
c) SigTest Settings:

- Select Technology as 'PCIe'
- Select Generation as "5_0"
- Select Test as "RXCal"
- Click "Confirm"
- Browse to the saved waveform file
- Select Template as "Rj_SJ_Cal"
- Run Test



d) SigTest Results:

- Read ‘Random Jitter (RMS)’ value
- Adjust RJ until RJ = 0.5 ps (RMS)


PCIe 5.0 RX Calibration Results
(PASS) Rj SJ Calibration Results
Rj SJ Calibration Results
Overall Result: PASS
Waveform Name
PCIECEMSjCalibration_Gen
Template Name
Rj_SJ_Cal
TX Preset
0
Lane
0
Mean UI
31.25 ps
Total Jitter (P-P)
9 ps
Random Jitter (RMS)
0.77901 ps

8.1.10 DM & CM Amplitude and Eye Height/Eye Width Calibration Setup

The following connection diagrams show the calibration setups at TP2 for DM amplitude (DM-I), CM amplitude (CM-I) and Eye Height (EH)/Eye Width (EW) for PCIe Gen 5. The CLB/CBB test fixture is connected in between the MP1900A BERT and a digital oscilloscope.

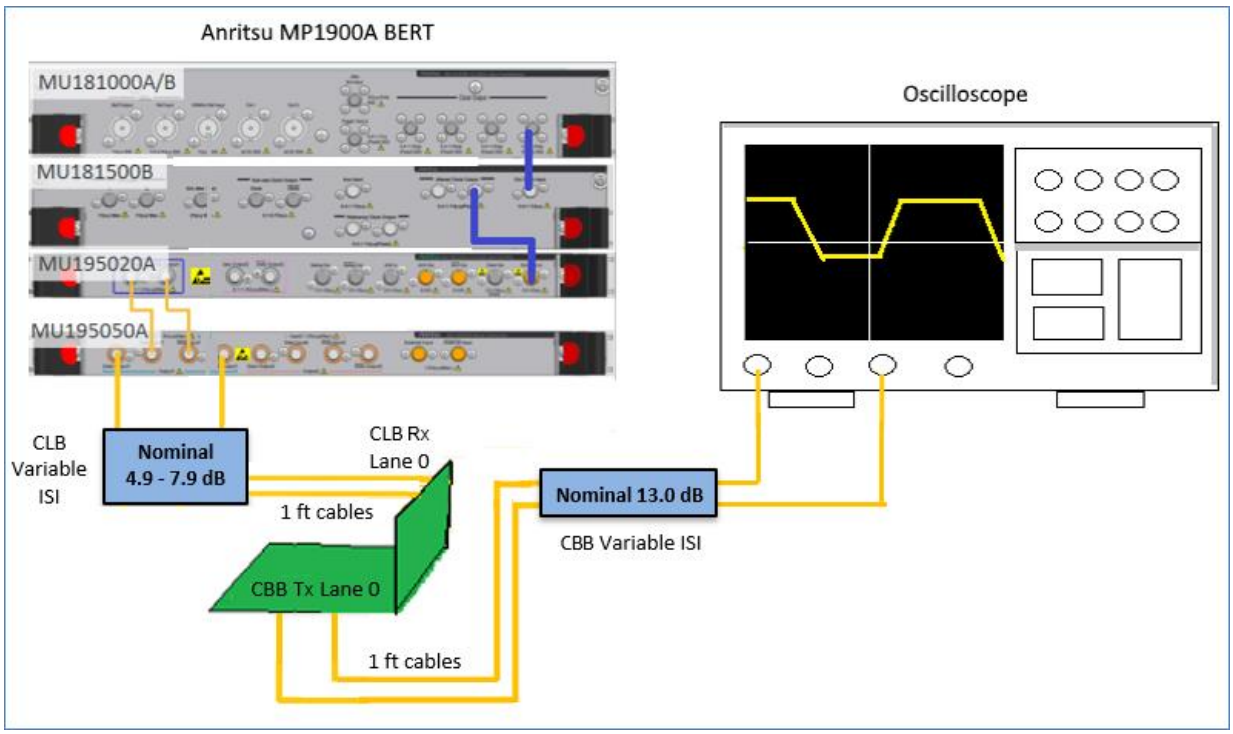


FIGURE 51. CONNECTION DIAGRAM FOR PCIE GEN 5 DM-I, CM-I AND EH/EW TP2 CALIBRATION (FOR SYSTEM BOARD)

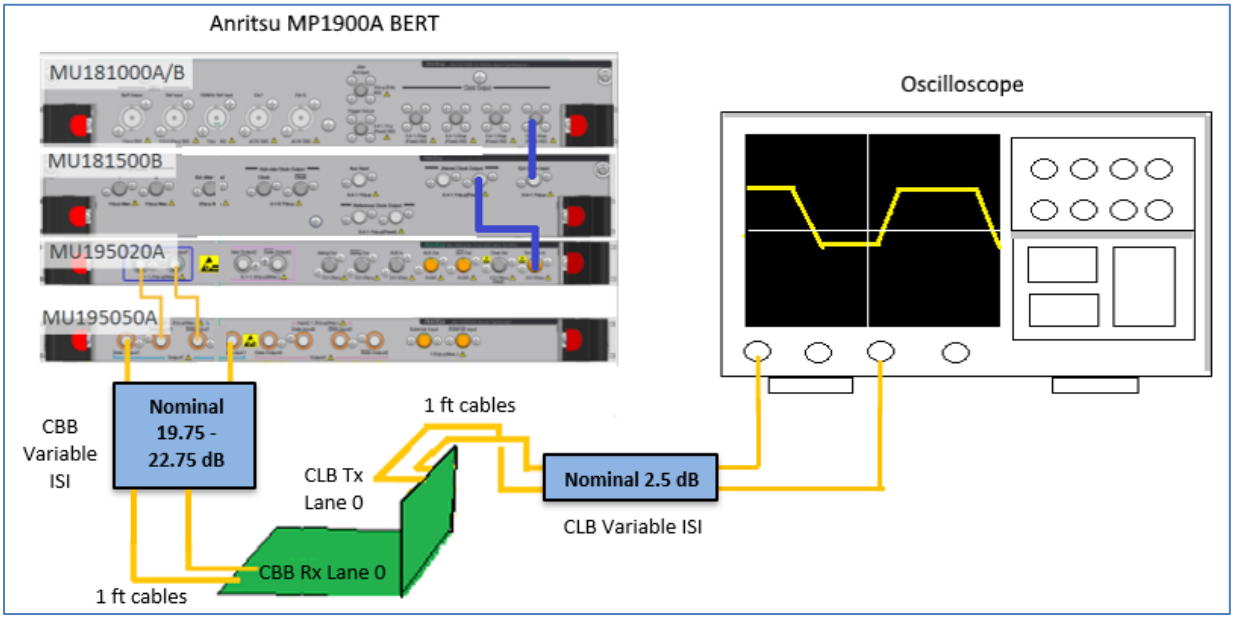


FIGURE 52. CONNECTION DIAGRAM FOR PCIE GEN 5 DM-I, CM-I AND EH/EW TP2 CALIBRATION (FOR ADD-IN CARD)

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. For System Board calibration:
   a) Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 4.9 – 7.9 dB) of the CLB.
   b) Using 1 ft cables, connect between both the CLB Rx Lane 0 and CLB Variable ISI and between both the CBB Tx Lane 0 and the CBB Variable ISI (Nominal 13.0 dB).
5. For Add-In Card calibration:
   a) Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 19.75 – 22.75 dB) of the CBB.
   b) Using 1 ft cables, connect between both the CBB Rx Lane 0 and CBB Variable ISI and between both the CLB Tx Lane 0 and the CLB Variable ISI (Nominal 2.5 dB).

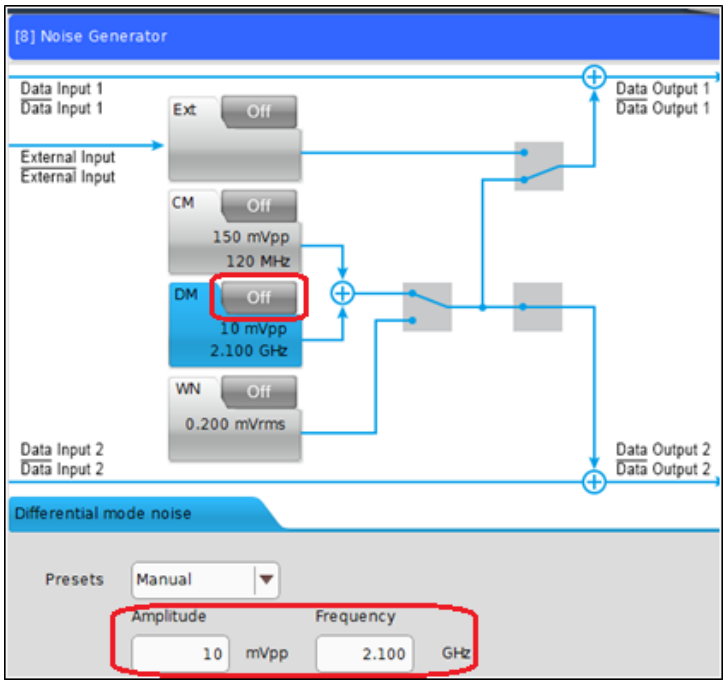
[Note: DM-I and CM-I should be calibrated with no reference package embedding applied.]

6. Connect the CLB Variable ISI (for add-in card) or the CBB Variable ISI (for system board) to the digital Scope channels.

8.1.11 DM-I Calibration Adjustment

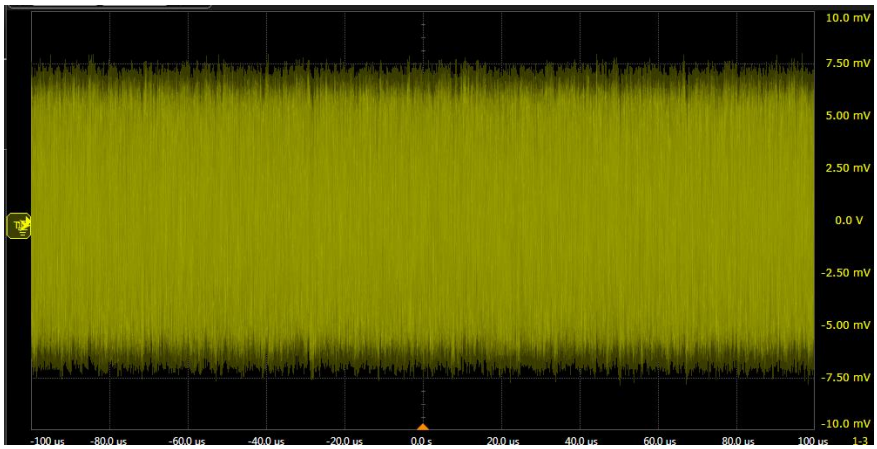
Adjust the DM Amplitude using the Scope RMS function with the following configuration. Compute V_{Diff} = (RMS * 2)/0.707.

a) BERT Settings:
   - Loss Channel
   - General Output: ON
   - Select SI-PPG and Emphasis tab
   - PPG Data Output: OFF
   - Select Noise Generator- DM: ON
   - Differential mode noise Amplitude and Frequency: 10 mVpp and 2.1 GHz



b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 5 ns/div
- Bandwidth: 8 GHz



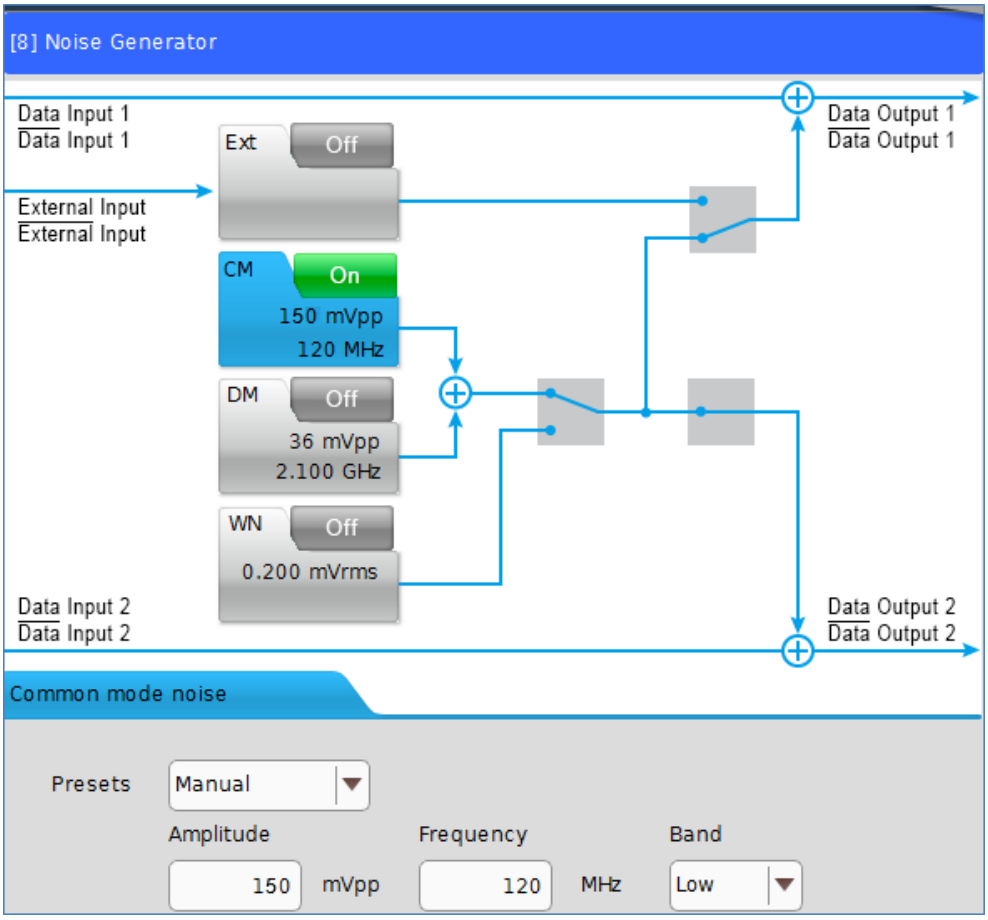
8.1.12 CM-I Calibration Adjustment

Adjust the CM Amplitude using the Scope RMS function with the following configuration. Compute Vpp = RMS/0.707.

a) BERT Settings:

- Loss Channel

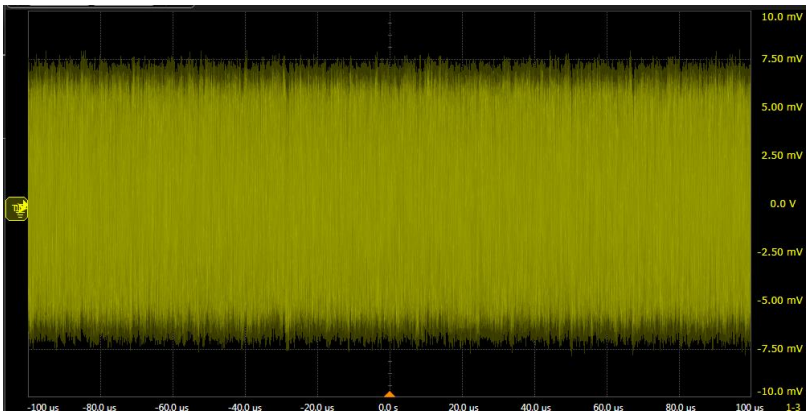
- General Output: ON
- Select SI-PPG and Emphasis tab
- PPG Data Output: OFF
- Select Noise Generator- CM: ON
- Common mode noise Amplitude and Frequency: 150 mVpp and 120 MHz



b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 12.5 µs/div
- Bandwidth: 8 GHz

Measure RMS on (CH1+CH3)/2 and calculate Vpp = RMS/0.707.



8.1.13 EH/EW Calibration Adjustment

The following Eye Height/Eye Width calibration procedure applies for PCIe Gen 5:

Set ISI Trace to 37 dB (physical loss of 25.5 to 28.5 dB for the System Board and 29.8 to 32.8 dB for the Add-In Card).

The goal is to calibrate final eye to achieve the following targets:

- Eye Width: 8.875 to 9.875 ps
- Eye Height: 13.5 to 16.5 mV

Capture seven waveforms for each condition on the Scope and analyze Eye Height/Eye Width using SigTest. Set up the following parameters.

a) BERT Settings:
   - General Output: ON
   - Select SI-PPG and Emphasis tab- Emphasis Function: ON
   - Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen5_P0
   - Set all Jitter, Noise, and Amplitude values.
   - Save seven waveforms and read in SigTest.
   - Determine the Optimized Preset and CTLE as follows:
     - Start Preset 5 on BERT and capture seven waveforms.
     - Measure all the seven waveforms for all CTLE's ranging from -5.0 to -15 dB using SigTest and repeat measurements for P5, P6, P8 and P9. For each CTLE and Preset combination, calculate EW/EH through averaging after filtering the outliers (see below):
       - The waveform is considered an outlier if the Eye Width is < 1.0 ps or deviates from the median by 2.0 ps.
       - The waveform is considered an outlier if the Eye Height is < 1.0 mV or deviates from the median by 5.0 mV.

- Determine which CTLE and Preset combination provides the largest Eye Area (Eye Width * Eye Height) and record these values.

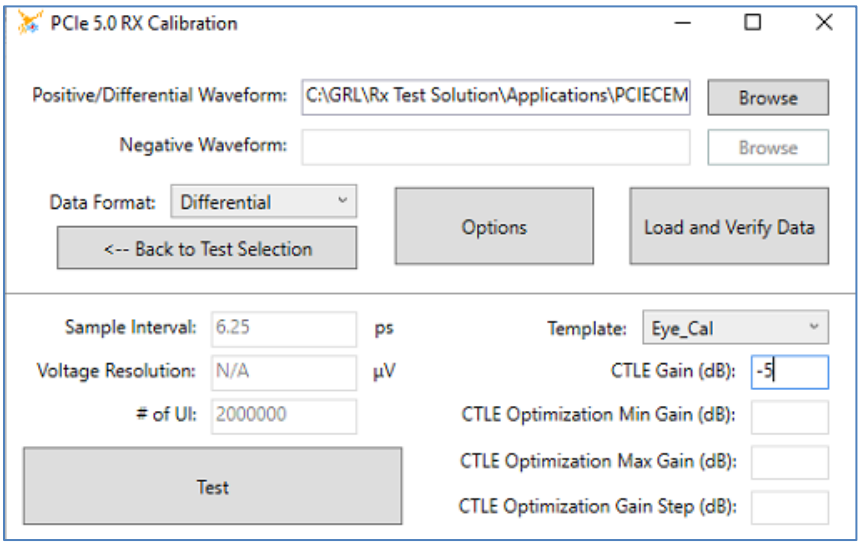
- Using the Optimized Preset and CTLE, save at least 10 waveforms and obtain the average value.
- Adjust the Eye Height/Eye Width to target specification values by scanning through:
  - SJ: 1 to 5 pspp
  - DM: 5 to 30 mV at TP2
  - VSwing : 720 mV to 800 mV (To be adjusted only if unable to achieve target values with SJ/DM combination)
- If the target values cannot be achieved, reduce ISI by 0.5 dB and repeat the steps from "Determine the Optimized Preset and CTLE as follows:…" until the total ISI loss is 34 dB.

b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 6.25 µs/div (2M UI)
- Bandwidth: 33 GHz
- Sampling Rate: ≥128 GS/s

c) SigTest Settings:

- Select Technology as 'PCIe'
- Select Generation as "5_0"
- Select Test as "RXCal"
- Click "Confirm"
- Browse to the saved waveform file
- Select Template as "Eye_Cal"
- Set CTLE Gain, for example: -5
- Run Test

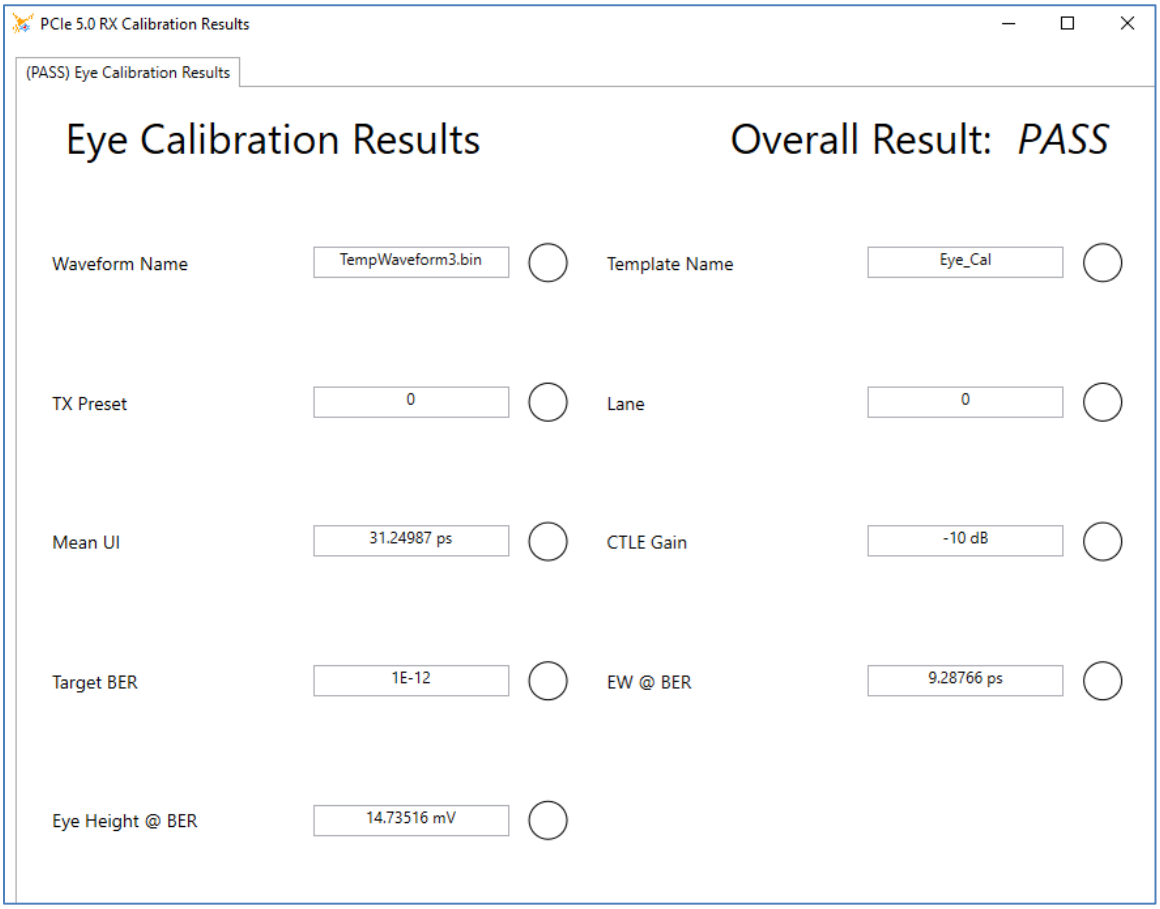


d) SigTest Results:

The Eye Height @BER and Eye Width @BER must fall within the following target values:

Target Minimum Eye Width: 9.375 +0.5/-0.5 ps

Target Extrapolated Eye Height: 15 +1.5/-1.5 mV



For final eye calibration, adjust Voltage Swing, SJ, and DM Amplitude until the target Eye Width and Eye Height are achieved and then save at least 10 waveforms.

8.2 Perform Initial Tx Equalization & Tx Link Equalization Response Tests

This section describes how to set up the DUT to perform initial Tx equalization (EQ) testing (for the add-in card only) and Tx link EQ response testing (for both the system board and add-in card). This is to ensure that the DUT will be able to apply the correct Tx EQ preset as required along the test.

To perform the initial Tx EQ & Tx link EQ response tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to reference clock with the DUT fixture. After data is processed, the signals will be separated to flow through two different directions- one part of the signal will be sent back through the test fixture to the stress signal generator for error detection while the other part will be sent to the oscilloscope for waveforms to be captured and analyzed for target EQ values.

Note: *Refer to Sections 5.2 and 5.3 for more details on test setup requirements for the DUT.*

8.2.1 Equipment Setup for Add-in Card DUT Initial Tx EQ / Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform initial Tx EQ / Tx link EQ response test for the PCIe Gen 5 add-in card DUT. This setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CBB test fixture for the DUT.

Note*: Use logical Lane 0 for the following test setup.*

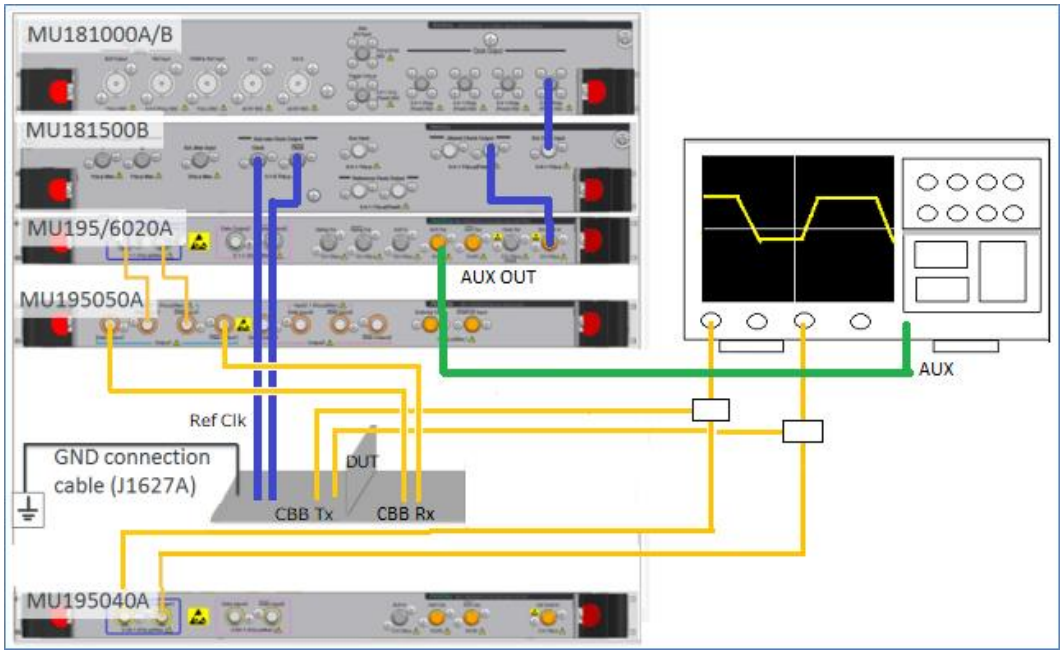


FIGURE 53. CONNECTION DIAGRAM FOR PCIE GEN 5 ADD-IN CARD DUT INITIAL TX EQ / TX LINK EQ RESPONSE TEST

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to Rx Lane 0 of the CBB.
5. Using coaxial cables, connect the MU181500B sub-rate clock outputs (100 MHz reference clock) to the REF CLK INJ of the CBB.
6. Using a SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
7. Using phase matched cables, connect Channels 1 and 3 on the oscilloscope to the Power Splitter OUT (or the pick-off tee PICK OFF) port.
8. Using coaxial cables, connect the CBB Tx Lane 0 to the Power Splitter IN (or the pick-off tee IN) port.
9. Using coaxial cables, connect the other OUT port of the Power Splitter (or the pick-off tee OUT) to the MU195040A data inputs for loopback error detection.
10. Using the J1627A GND connection cable, connect the CBB to ground.

8.2.2 Equipment Setup for System Board DUT Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform Tx link EQ response test for the PCIe Gen 5 system board DUT. This setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CLB test fixture for the DUT.

***Note**: Use logical Lane 0 for the following test setup.*

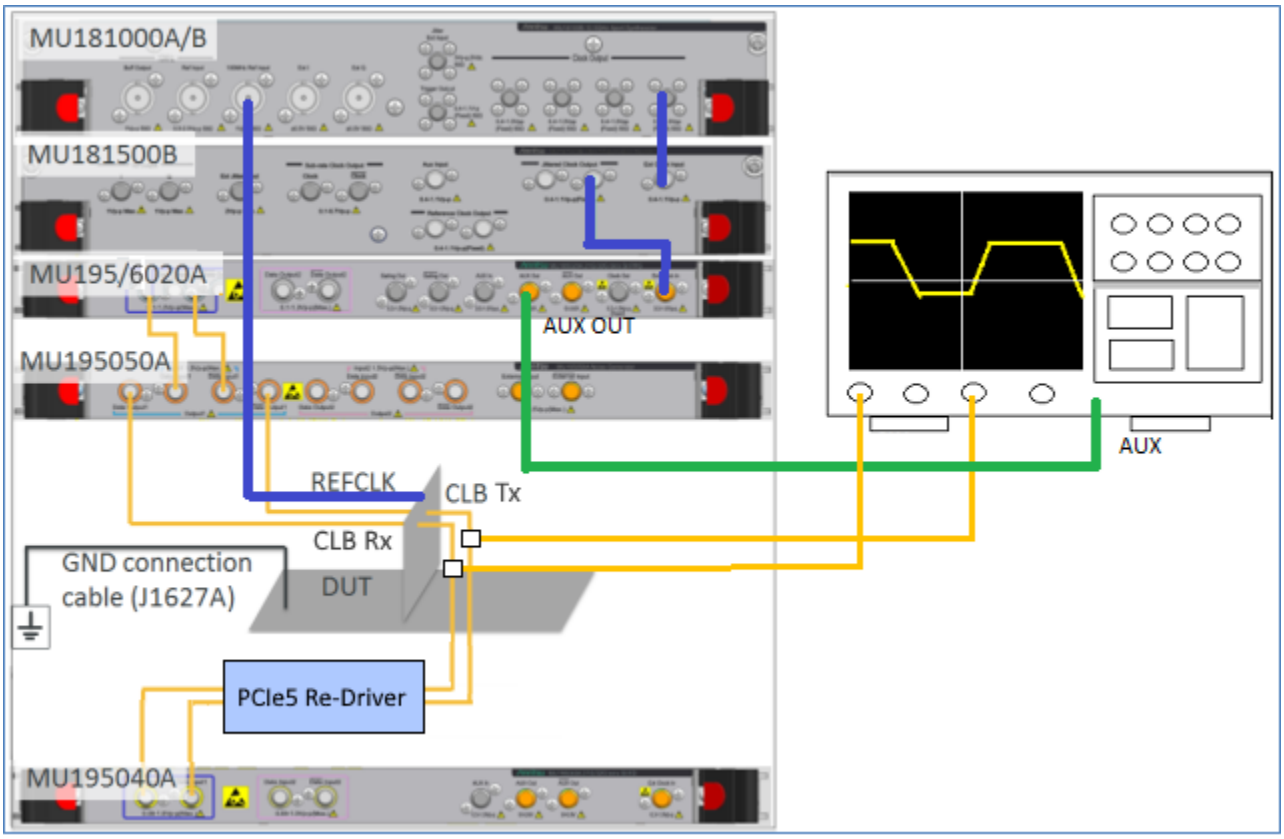


FIGURE 54. CONNECTION DIAGRAM FOR PCIE GEN 5 SYSTEM BOARD DUT TX LINK EQ RESPONSE TEST

***Note**: Before starting the System Board DUT Tx Link EQ Response Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Appendix B or C for details.*

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to Rx Lane 0 of the CLB.
5. Using a BNC cable, connect the CLB 100 MHz clock output from the system board DUT to the 100 MHz reference clock input on the MU181000A/B.
6. Using a SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
7. Using coaxial cables, connect the CLB Tx Lane 0 to the Power Splitter IN (or the pick-off tee IN) port.

8. Using phase matched cables, connect Channels 1 and 3 on the oscilloscope to the Power Splitter OUT (or the pick-off tee PICK OFF) port.
9. Using coaxial cables, connect the other OUT port of the Power Splitter (or the pick-off tee OUT) to the PCIe5 Re-Driver and then to the MU195040A data inputs for loopback error detection.
10. Using the J1627A GND connection cable, connect the CLB to ground.

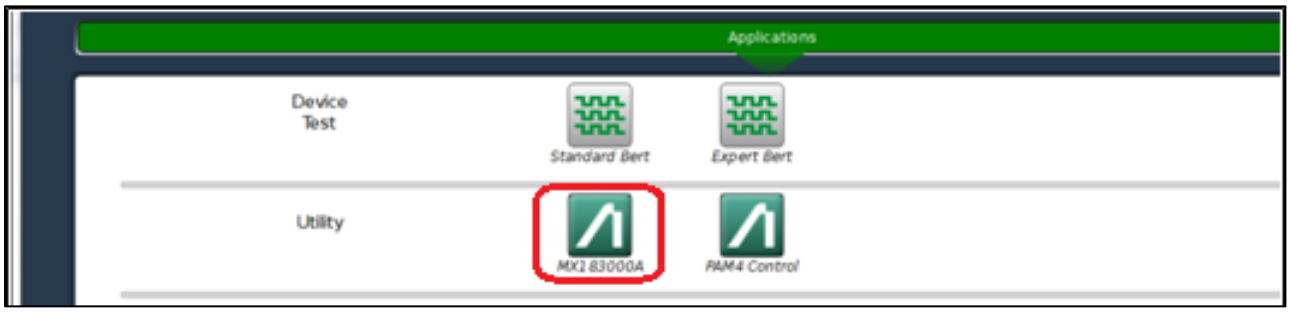
8.2.3 Initial Tx EQ Startup and Testing

Prior to starting this test, take note of the following:

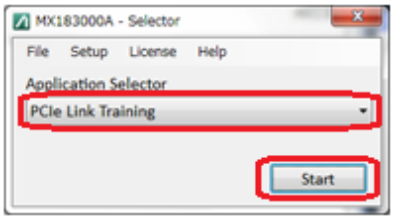
- This test uses AC fit methodology defined in the *PCIe CEM 5.0 Specification* for preset testing at 32 GT/s. Testing at lower data rates uses Vb based methodology defined in respective *PCIe Base Specifications*.
- To account for measurement noise, a tolerance of ±1.0 dB is used for measured preshoot and de-emphasis that are defined as 0.0 dB in the *PCI Express Base Specification*.
- Due to measurement sensitivity having more impact on higher boost preset, a tolerance of ±1.5 dB is used for P10 preshoot.
- The designs are expected to not support any preshoot or de-emphasis on presets that define 0.0 dB for preshoot or de-emphasis. The allowed tolerance is to account for measurement noise only.

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the initial Tx EQ test. The oscilloscope will also be used to capture waveforms for post processing analysis.

1. Configure the oscilloscope as follows:
   - Averaging: OFF
   - Horizontal Scale: 6.25 µs/div (2M UI)
   - Max Bandwidth: 33 GHz
   - Sampling Rate: ≥ 128 GS/s
   - Trigger: 0 V, Channel 1
2. Set Preset 0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.



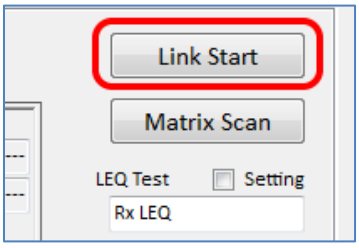
4. In the MX183000A – Selector pop-up, select ‘PCIe Link Training’ and then ‘Start’.



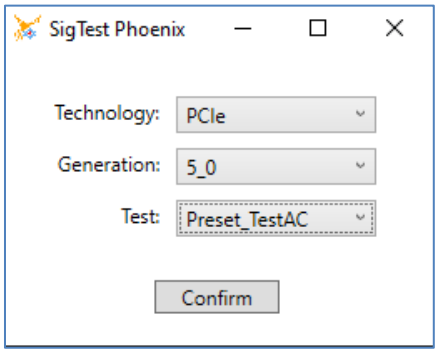
5. In the next window, select the network address of the MX190000A BERT application followed by ‘Connect’ to link up with the MX190000A.

6. In the MX183000A – PCIe Link Training window, select the Link Training tab. Select the “Setting” check box on the right of the screen.
7. When the LEQ Test pane appears, select the Initial Tx LEQ tab. Set the “DUT Initial Preset (Preset Hint Tx)” to Preset 0 (P0). Then select “Apply”.
8. Press the Power Reset button on the CBB test fixture to reset the DUT.

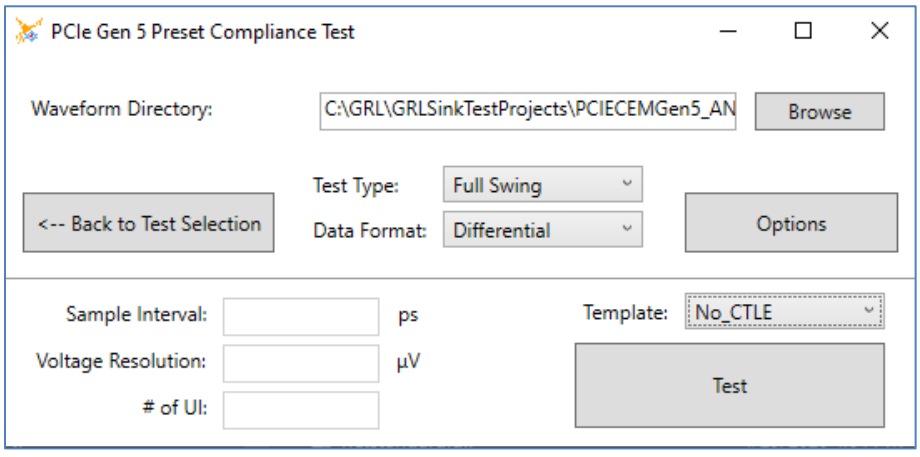
9. In the MX183000A – PCIe Link Training window, select 'Link Start' in the Link Training tab.

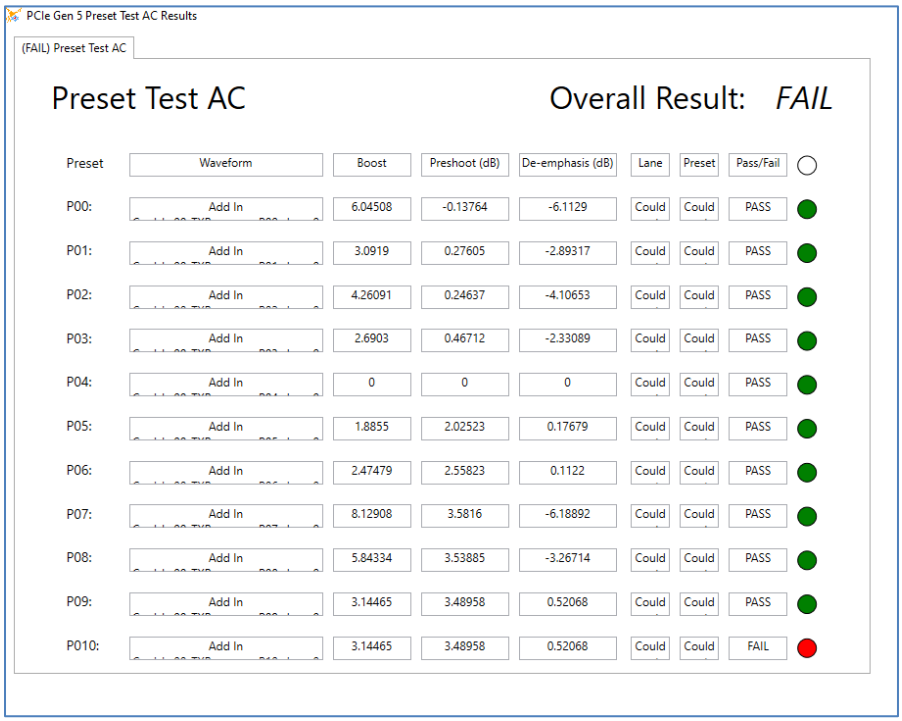


10. On the Scope, capture the Preset 0 waveforms and save to a file labeled as either *"Add In Card_Ln00_TXResponse_P0X_d_acq000"* (for the add-in card where P0X represents the Preset Number) or *"System Board_TXResponse_P0_d_acq000"* (for the system board). For example if using a add-in card DUT, the Preset 0 waveform should be saved as *"Add In Card_Ln00_TXResponse_P00_d_acq000"*. If using a system board DUT, the Preset 0 waveform should be saved as *"System Board_TXResponse_P0_d_acq000"*.
11. Repeat steps 1 to 9 to capture all waveforms for all Presets (up to Preset 9). All waveforms must be saved to same file directory.
12. Launch SigTest and select the PCIe Gen5 Preset Test as shown in the following example.



13. Browse to select the directory of the saved waveform file to be tested and select "No_CTLE" at the Template drop-down field. Then select the "Test" button at the bottom to start the test run. All preset numbers must turn green once the test completes to indicate a Pass.





Preset	Waveform	Boost	Preshoot (dB)	De-emphasis (dB)	Lane	Preset	Pass/Fail
P00:	Add In	6.04508	-0.13764	-6.1129	Could	Could	PASS
P01:	Add In	3.0919	0.27605	-2.89317	Could	Could	PASS
P02:	Add In	4.26091	0.24637	-4.10653	Could	Could	PASS
P03:	Add In	2.6903	0.46712	-2.33089	Could	Could	PASS
P04:	Add In	0	0	0	Could	Could	PASS
P05:	Add In	1.8855	2.02523	0.17679	Could	Could	PASS
P06:	Add In	2.47479	2.55823	0.1122	Could	Could	PASS
P07:	Add In	8.12908	3.5816	-6.18892	Could	Could	PASS
P08:	Add In	5.84334	3.53885	-3.26714	Could	Could	PASS
P09:	Add In	3.14465	3.48958	0.52068	Could	Could	PASS
P010:	Add In	3.14465	3.48958	0.52068	Could	Could	FAIL

8.2.4 Tx Link EQ Time Response (with Presets/Cursors) Startup and Testing

Prior to starting this test, take note of the following:

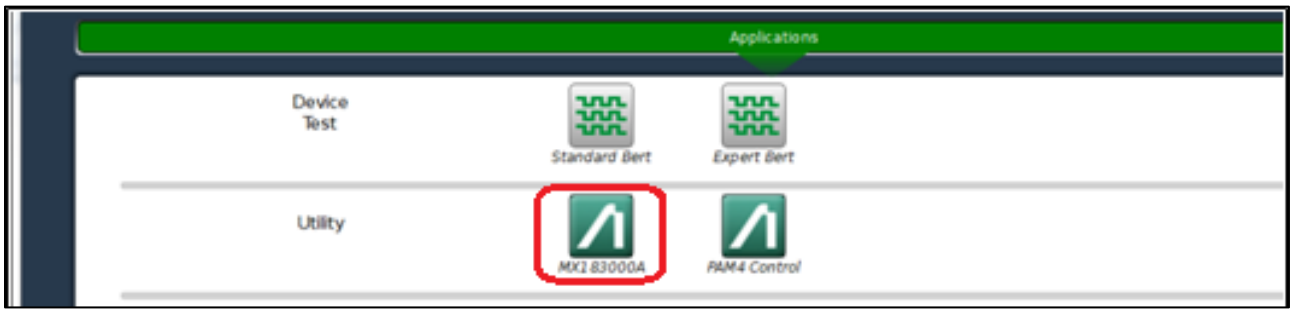
- This test uses AC fit methodology defined in the *PCIe CEM 5.0 Specification* for preset testing at 32 GT/s. Testing at lower data rates uses Vb based methodology defined in respective *PCIe Base Specifications*.
- To account for measurement noise, a tolerance of ±1.0 dB is used for measured preshoot and de-emphasis that are defined as 0.0 dB in the *PCI Express Base Specification*.
- Due to measurement sensitivity having more impact on higher boost preset, a tolerance of ±1.5 dB is used for P10 preshoot.
- The designs are expected to not support any preshoot or de-emphasis on presets that define 0.0 dB for preshoot or de-emphasis. The allowed tolerance is to account for measurement noise only.

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the Tx link EQ time response test with presets or cursors. The oscilloscope will also be used to capture waveforms for post processing analysis.

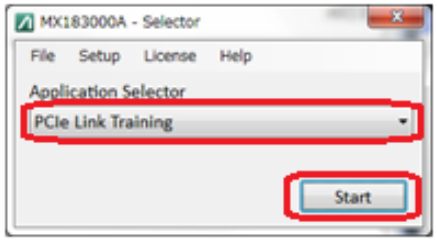
1. Configure the oscilloscope as follows:
    - Averaging: OFF
    - Horizontal Scale: 6.25 µs/div (2M UI)
    - Max Bandwidth: 33 GHz

- Sampling Rate: ≥ 128 GS/s
- Trigger: -350 mV, Anritsu AUX channel

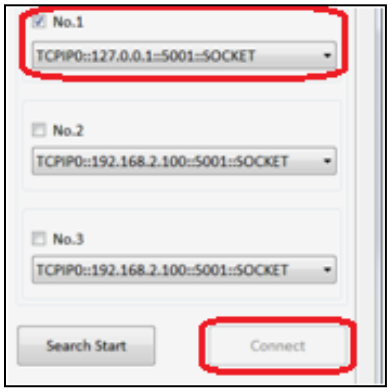
2. Set Preset 0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.



4. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



4. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.

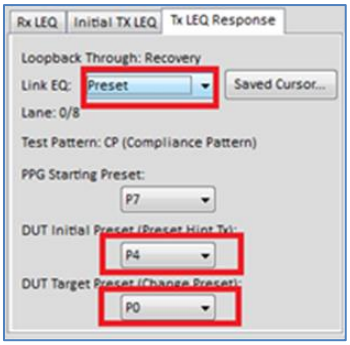


5. In the MX183000A – PCIe Link Training window, select the Link Training tab. Select the "Setting" check box on the right of the screen.
6. When the LEQ Test pane appears, select the Tx LEQ Response tab. Set the "DUT Initial Preset (Preset Hint Tx)" to Preset 4 (P4) and the "DUT Target Preset (Change Preset)" to P0.

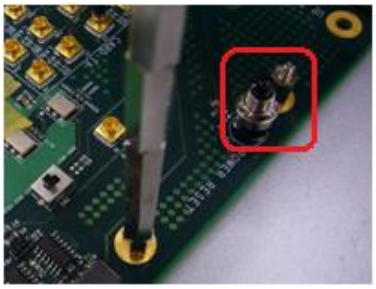
   Note: Use the following "DUT Initial Preset (Preset Hint Tx)" and "DUT Target Preset (Change Preset)" combinations for this step:

Preset # to be Tested	DUT Initial Preset (Preset Hint Tx)	DUT Target Preset (Change Preset)
P0	P4	P0
P1	P4	P1
P2	P4	P2
P3	P7	P3
P4	P7	P4
P5	P7	P5
P6	P7	P6
P7	P4	P7
P8	P4	P8
P9	P7	P9

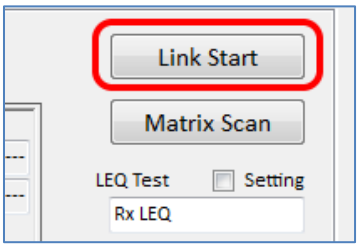
Set Link EQ to “Preset” if testing for Tx Response Preset or “Cursor” if testing for Tx Response Cursor.



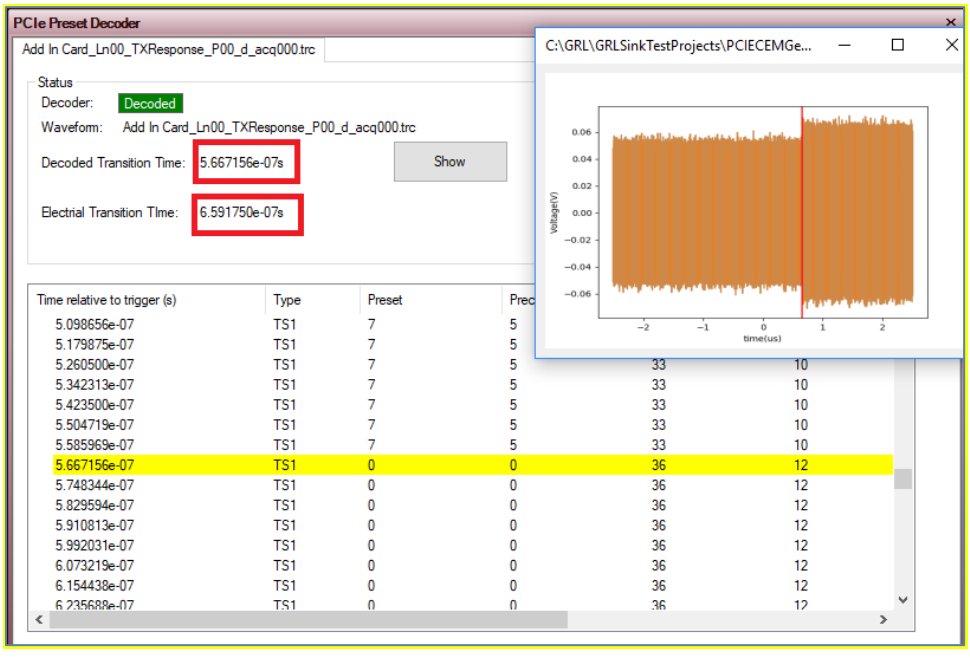
7. Press the Power Reset button on the CBB test fixture to reset the DUT.



8. In the MX183000A – PCIe Link Training window, select ‘Link Start’ in the Link Training tab.



9. On the Scope, capture the Preset 0 waveforms and save to a file labeled as either *"Add In Card_Ln00_TXResponse_P0X_d_acq000"* (for the add-in card where P0X represents the Preset Number) or *"System Board_TXResponse_P0_d_acq000"* (for the system board). For example if using a add-in card DUT, the Preset 0 waveform should be saved as *"Add In Card_Ln00_TXResponse_P00_d_acq000"*. If using a system board DUT, the Preset 0 waveform should be saved as *"System Board_TXResponse_P0_d_acq000"*.
10. Repeat steps 1 to 8 for each Preset change.
11. Repeat steps 1 to 9 for each Cursor change.
12. Perform post processing analysis for each waveform to locate the transition time between the preset/cursor change.
13. On the GRL software, go to the Setup Configuration page and select the Debug Tool tab. Select either the "Tx Response Preset" or "Tx Response Cursor" button depending on which is being tested. In the Select Waveforms pop-up window, select all the waveforms that were previously captured and click "OK".
14. In the PCIe Preset Decoder screen, verify that the Electrical transition time is showing < 1 µs to pass the test. *Note: The Decoded transition time serves as an informative value only and is not required for compliance.*



8.3 Perform Rx Link EQ Test

This section describes how to set up the DUT for loopback testing to measure the Bit Error Rate (BER) using the link equalization test method.

To perform link training loopback tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to reference clock with the DUT fixture. After data is processed, the signals will be sent back through the test fixture to the stress signal generator for error detection. To enable this loopback mode, the error detector on the stress signal generator will run link training procedure on the DUT. When the DUT enters loopback state, the error detector will proceed to measure BER of the loopback signals.

Note: *Refer to Section 5.5 to set up the DUT for link equalization testing to verify initially that the DUT is ready for link training and loopback.*

8.3.1 Equipment Setup for Add-in Card DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 5 add-in card DUT. This setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CBB test fixture for the DUT.

Note*: Use logical Lane 0 for the following test setup.*

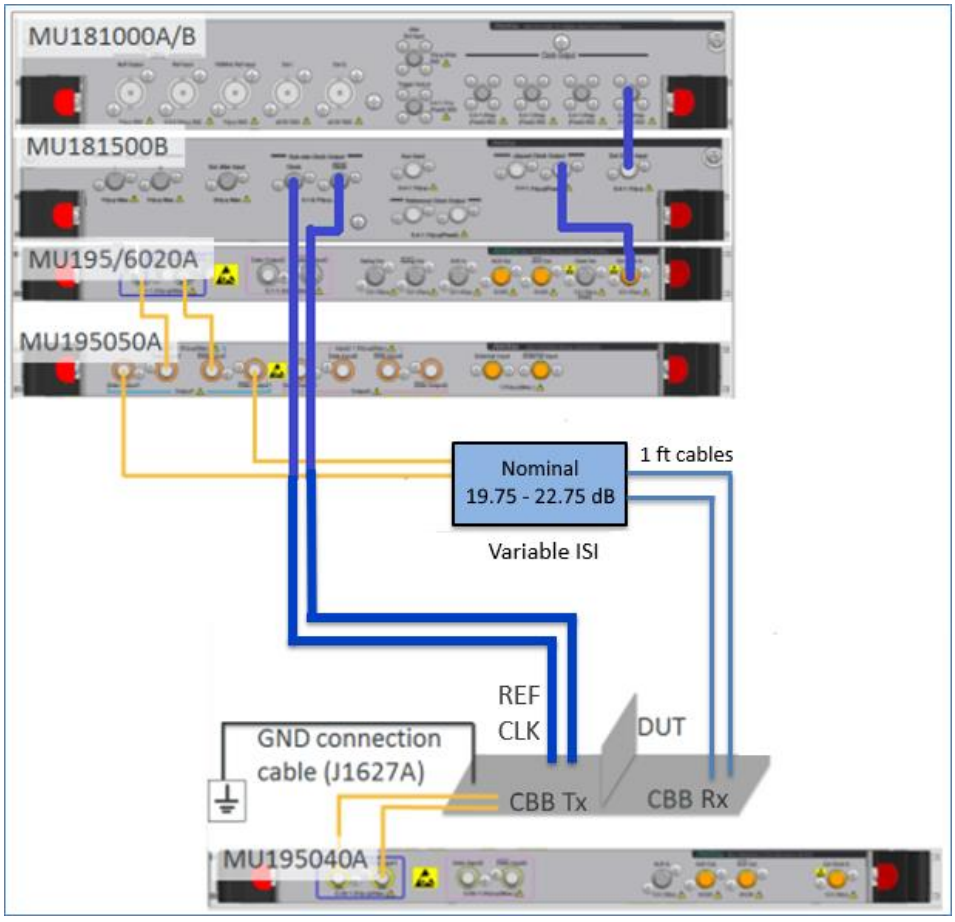


FIGURE 55. CONNECTION DIAGRAM FOR PCIE GEN 5 ADD-IN CARD DUT LOOPBACK TEST

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 19.75 – 22.75 dB).
5. Using 1 ft cables, connect between both the CBB Rx Lane 0 and Variable ISI.
6. Using coaxial cables, connect the MU181500B sub-rate clock outputs (100 MHz reference clock) to the REF CLK INJ of the CBB.
7. Using coaxial cables, connect the CBB Tx Lane 0 to the MU195040A data inputs for loopback error detection.
8. Using the J1627A GND connection cable, connect the CBB to ground.

8.3.2 Equipment Setup for System Board DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 5 system board DUT. This setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CLB test fixture for the DUT.

***Note**: Use logical Lane 0 for the following test setup.*

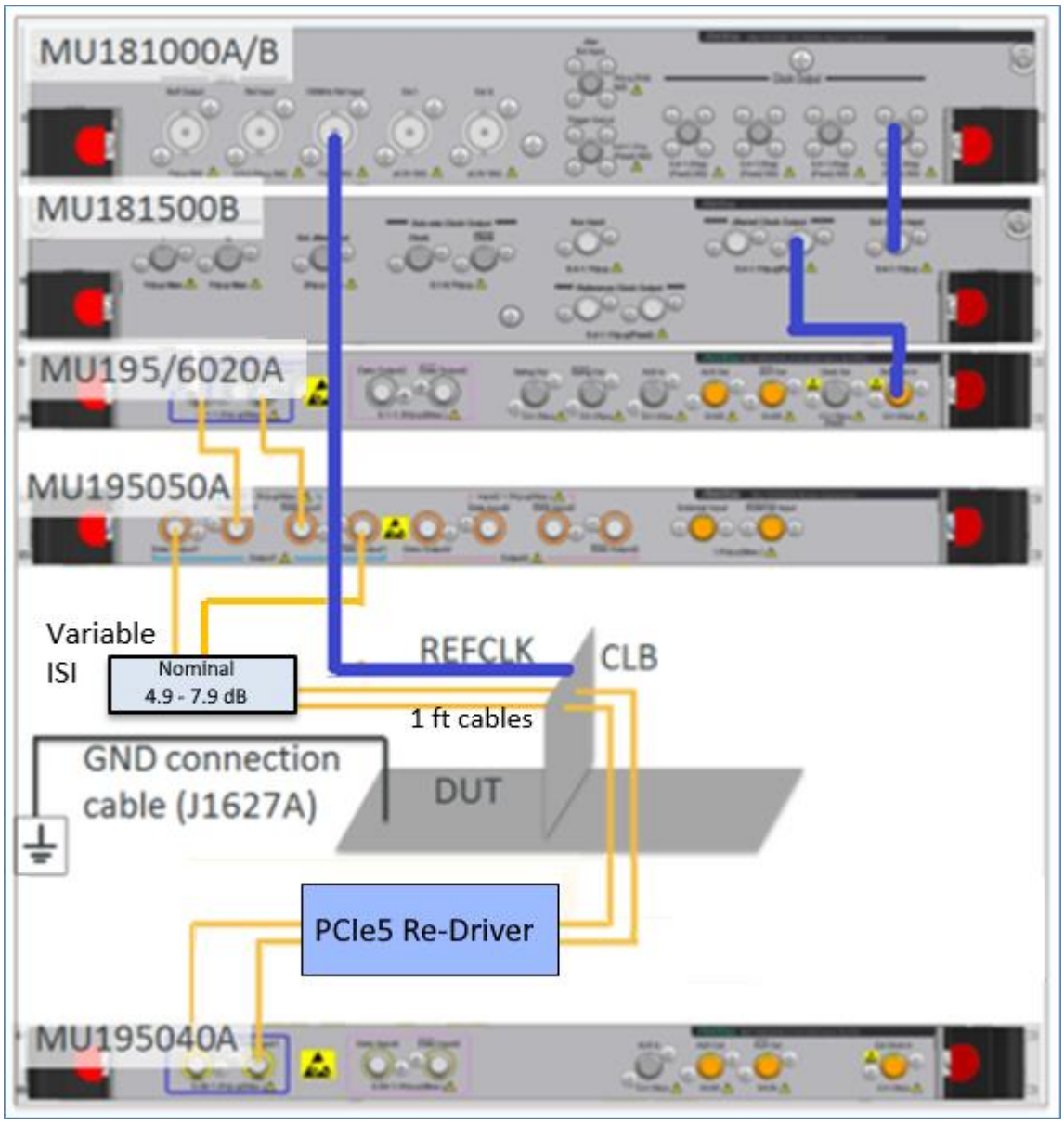


FIGURE 56. CONNECTION DIAGRAM FOR PCIE GEN 5 SYSTEM BOARD DUT LOOPBACK TEST

***Note**: Before starting the System Board DUT Loopback Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Appendix B or C for details.*

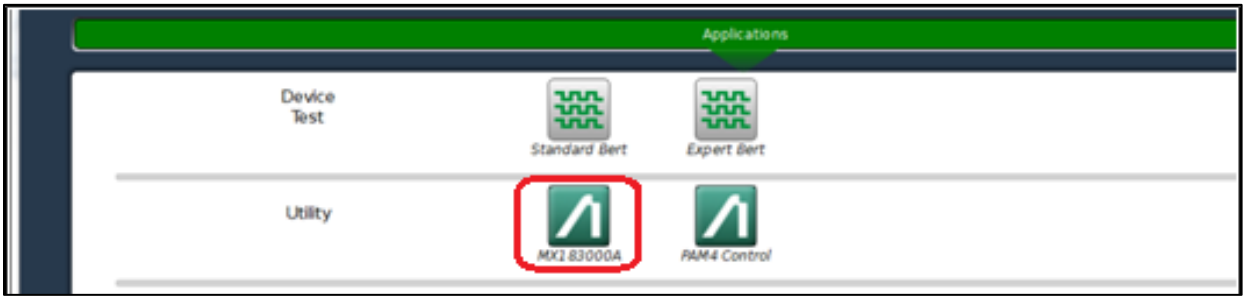
1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 4.9 – 7.9 dB).

5. Using 1 ft cables, connect between both the CLB Rx Lane 0 and Variable ISI.
6. Using a BNC cable, connect the CLB 100 MHz clock output from the system board DUT to the 100 MHz reference clock input on the MU181000A/B.
7. Using coaxial cables, connect the CLB Tx Lane 0 to the PCIe5 Re-Driver and then to the MU195040A data inputs for loopback error detection.
8. Using the J1627A GND connection cable, connect the CLB to ground.

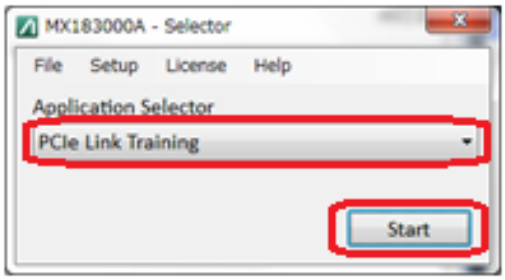
8.3.3 Link Training Initialization and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform link training.

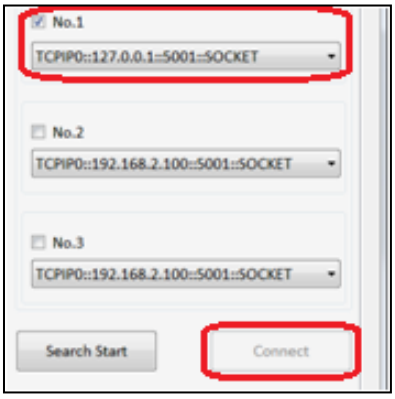
1. Enable all calibrated stresses on the BERT.
2. On the BERT's Applications screen, select the MX183000A Utility application.



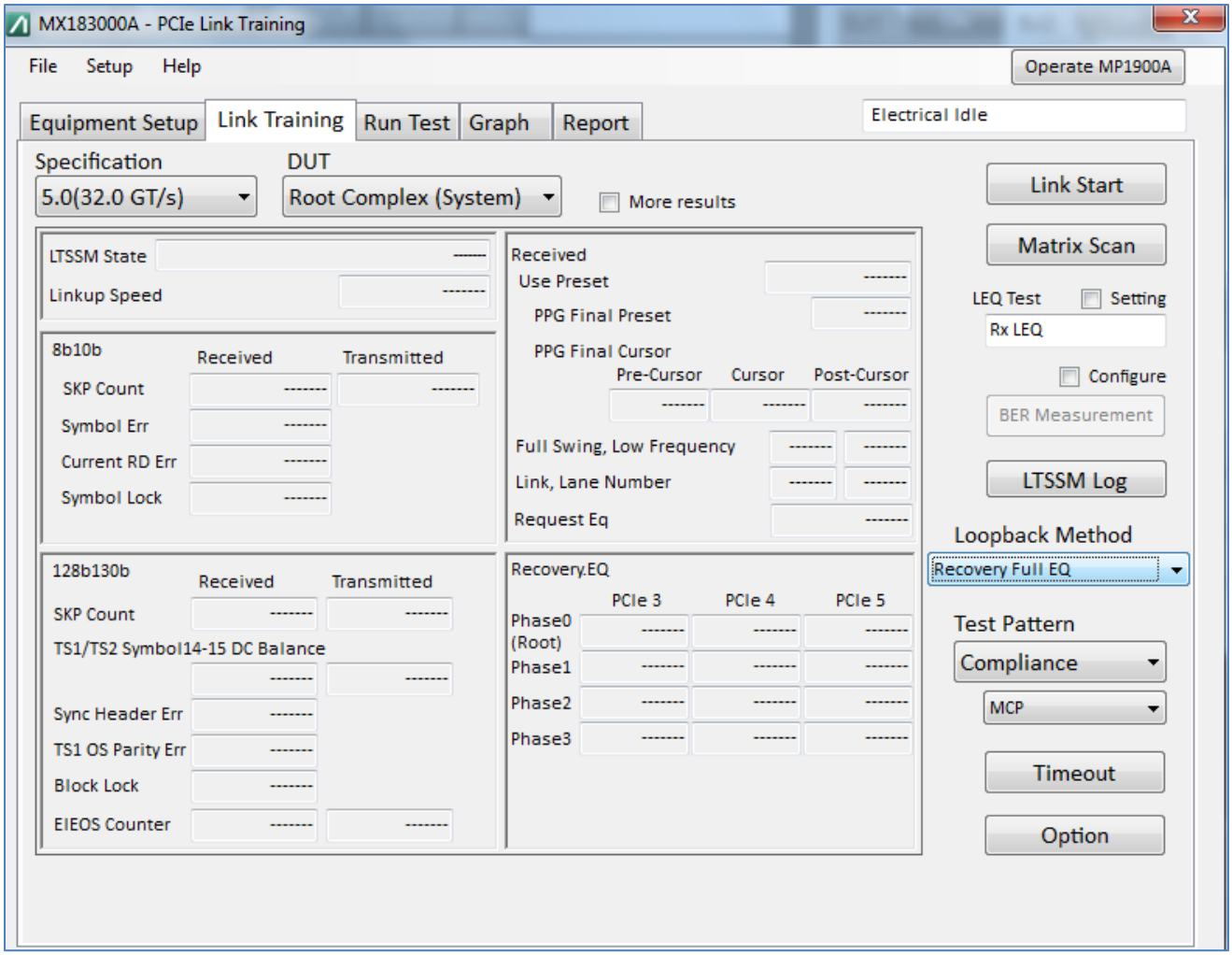
3. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



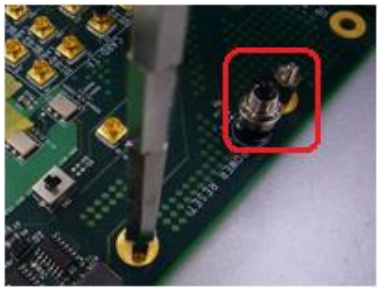
4. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.



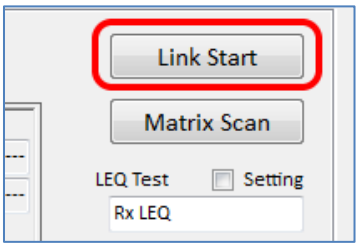
5. In the MX183000A – PCIe Link Training window, select the Link Training tab. Select 'Recovery Full EQ' under the Loopback Method drop-down field. The Recovery mode is a recommended setting for the DUT loopback state.



6. Press the Power Reset button on the CBB test fixture to reset the DUT.



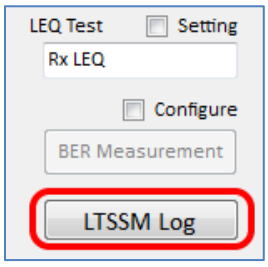
7. In the MX183000A – PCIe Link Training window, select 'Link Start' in the Link Training tab.



8. If the LTSSM (Link Training and Status State Machine) State shows 'Loopback.Active.Master', it means link training is successful.

   If 'Detect.Quiet' is shown instead, it means link training has failed.

9. Select 'LTSSM Log' to generate a log of the link training results.



   If the link training is successful, the log will show the DUT enter a Loopback Active state.

   If the link training has failed, the log will show Detect and Polling states.

8.3.4 Link Training Failure Troubleshooting

If the link training has been unsuccessful, perform troubleshooting for any of the following cases that may have been encountered during testing.

a) The LTSSM state for link training is repeated at 2.5 GT/s:

- Check that the instruments and fixtures have been properly connected.
- Ensure sufficient power supply to the DUT.
- Press the Power Reset button on the CBB or reboot the DUT.
- Connect the MU195050A noise generator data outputs directly to the MU195040A SI error detector data inputs, and try to run link training by selecting 'Configuration' under the Loopback through field in the Link Training tab.

b) The DUT enters the 32 GT/s LTSSM state, but the Loopback Active state is not shown.

- Set all Jitter and Noise to OFF on the BERT.
- Remove the ISI channel and connect data signals to the DUT directly.
- Press the Power Reset button on the CBB or reboot the DUT.
- Ensure the PPG Output setting is ON.

- Change to other Preset values, for example:
  - P5, P6, P8 and P9 are recommended for PCIe Gen 5.
- Ensure the correct EIEOS pattern revision of the DUT is being used.

If link training still fails, restart both the MX190000A and MX183000A applications.

8.4 Perform DUT Rx Compliance Testing

This section describes how to test the DUT to meet PCIe CEM 5.0 Rx electrical compliance specs. The Rx path is tested with worst case stressed eye to ensure a BER of no more than 1 error in 4E12 bits transmitted can be achieved. An optional jitter tolerance test is also described here.

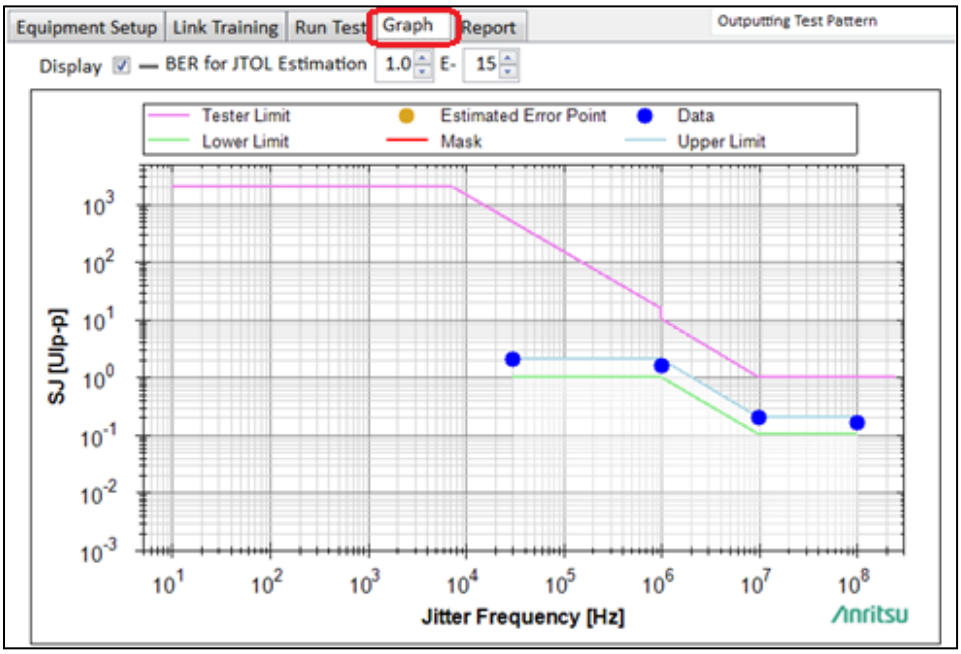
The Rx compliance test can be performed once the DUT has passed the link training loopback tests (as described in the previous section).

1. Enable all calibrated stresses on the BERT.
2. In the same link training window from the previous test, the LTSSM State will show 'Loopback.Active.Master' to indicate link training has been successful. From there, select 'BER Measurement' to start the error detection process for the DUT.
3. Run the test for 125 seconds for the PCIe Gen 5 DUT with maximum of one error at a single preset.

8.4.1 Jitter Tolerance Testing (Optional)

The DUT can be additionally tested for jitter tolerance after it has passed Rx compliance testing. The optional jitter tolerance test is basically carried out to search for SJ margins and measure the BER.

1. Continuing from the same Rx compliance test window, select the Run Test tab. Select 'Run Test' to start running measurements for jitter tolerance.
2. When completed, select the Graph tab to view a data plot from the measurement results.


Equipment Setup
Link Training
Run Test
Graph
Report
Outputting Test Pattern
Display
BER for JTOL Estimation
1.0
E-
15
Tester Limit
Lower Limit
Estimated Error Point
Mask
Data
Upper Limit
SJ [UIp-p]
Jitter Frequency [Hz]
Anritsu

9 Appendix B: Return Path Optimization Using Anritsu J1890A PCIe5 Re-Driver Set

It is important to optimize the Return Path (DUT Tx to BERT Error Detector) when testing for Receiver Link Equalization with PCIe Gen5 (32 GT/s), as described below.

9.1 Requirements for Using an External Driver (J1890A)

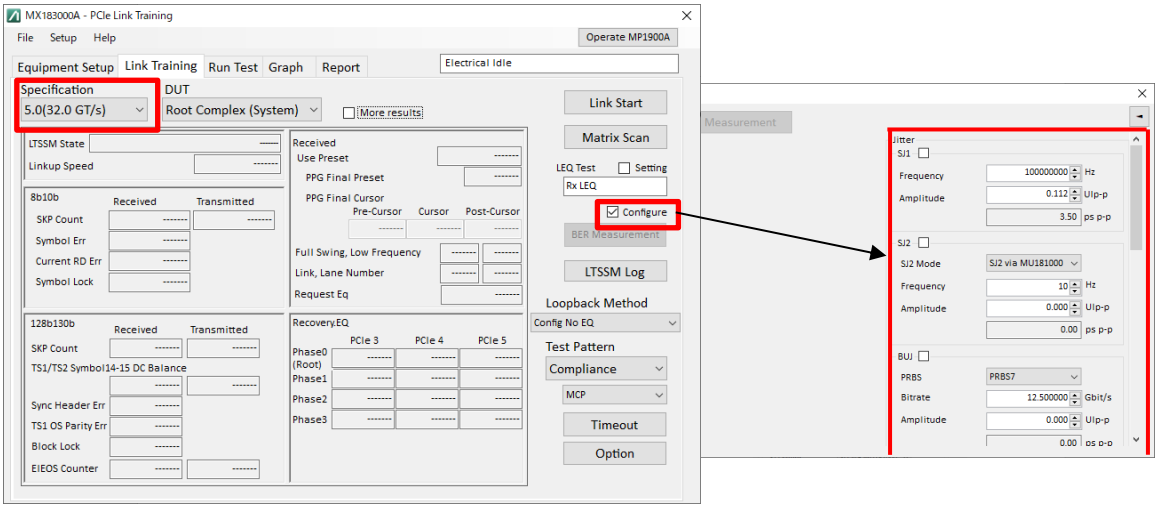
When testing the System Board, connect the J1890A PCIe5 Re-Driver Set between the DUT Tx and BERT Error Detector. Refer to Section 9.3 for information on how to set up the J1890A PCIe5 Re-Driver Set.

***Note**: While it is not necessary to use a Re-Driver for the Add-In Card Rx Link EQ Test, the same method of optimizing the Return Path should apply when testing the System Board or Add-In Card.*

9.2 Return Path Optimization Procedure

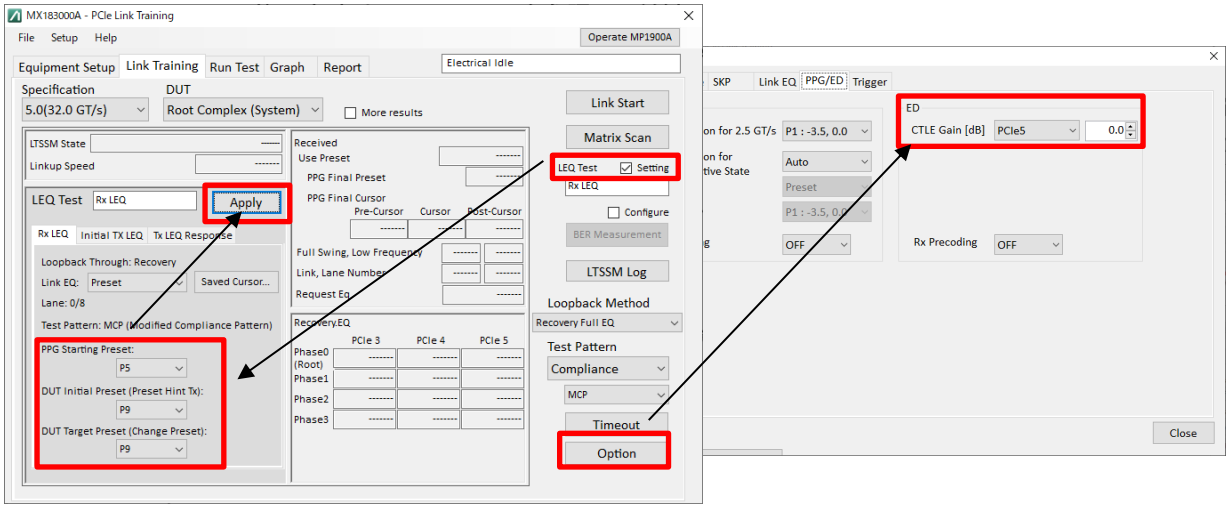
Follow the steps below to optimize the Return Path.

1. Connect the equipment as shown in the System TxRx Link EQ Test setups in Section 5.5.1 & 5.6.1 or Section 8.2.2 & 8.3.2 respectively.
2. Start the MX183000A, set the 'Specification' to 'Gen5', and then turn off all stresses as follows:
   - SJ
   - RJ
   - DMI
   - CMI

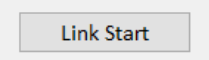


3. Select the 'LEQ Test Setting' checkbox in the MX183000A Main Window and set the following:
   i) Set 'PPG Starting Preset' to 'P5'

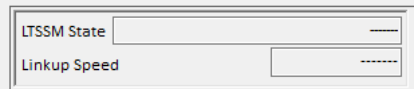
ii) Set ‘DUT Initial Preset (Preset Hint Tx)’ to ‘P9’
iii) Set ‘DUT Target Preset (Change Preset)’ to ‘P9’
iv) Click on ‘Apply’
v) From the ‘Option’ button, set ‘CTLE Gain’ to ‘0.0 dB’ on the ‘PPG / ED’ tab.



4. Execute ‘Link Start’ of MX183000A.



5. Establish Loopback.



i) If the ‘Linkup Speed’ is not ’32.0 Gbps’ and the ‘LTSSM State’ is not ‘Loopback.Active.Lead’, reduce the CTLE setting of step 3 v) by 3 dB, re-execute Link Training, and confirm whether Loopback is established through the LTSSM State displayed.
ii) If Loopback cannot be established even if CTLE is set to -12 dB, set the Preset setting of steps 3 ii) / 3 iii) to ‘P8’, set CTLE to ‘0 dB’, and check the Loopback status according to step 5 i).
iii) If Loopback cannot be established even with Preset P8, redo step 5 ii) with P7, P6, ... P0.
iv) Check the Preset and CTLE settings for which Loopback was established in steps 5 i) to 5 iii).
v) If Loopback cannot be established up to step 5 iv), remove ISI from the measurement system and execute steps 5 i) to 5 iv).

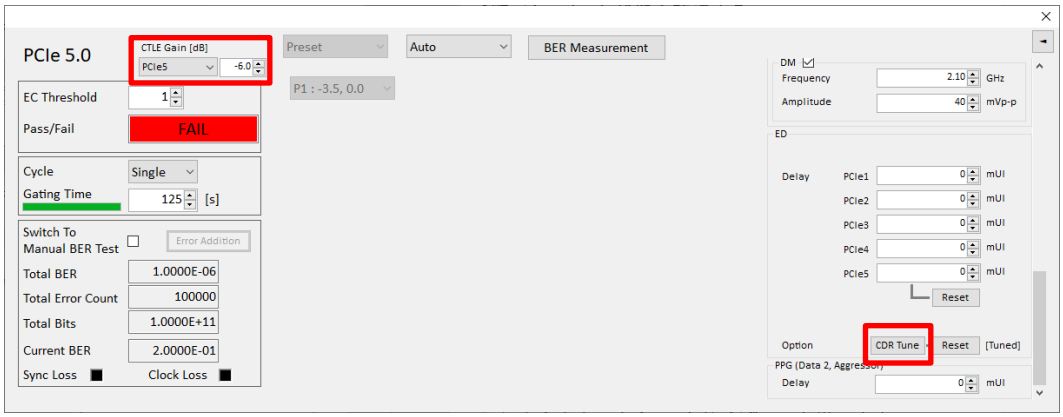
Note: If Loopback cannot be established by the procedure up to this point, the measurement environment may be incorrect (cable connection error, etc.) or it may be a DUT problem, so review the measurement environment again.

6. BER optimization:

Perform Link Training with Preset and CTLE settings specified in step 5 to measure BER.

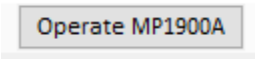
i) Adjust CTLE to locate the setting that gives the best BER.

ii) Execute ‘CDR Tune’.



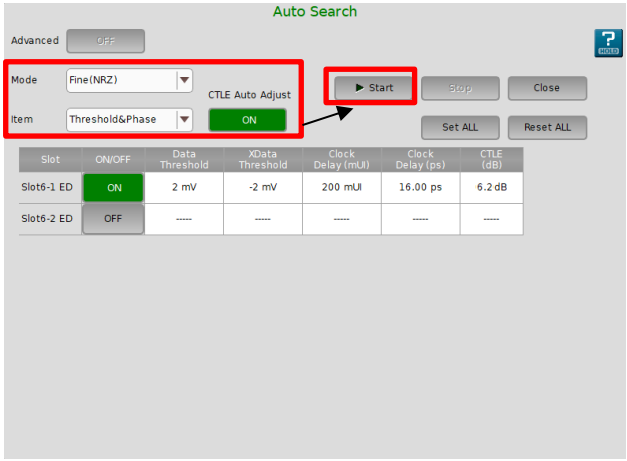
iii) Execute ‘Auto Search’:

- Click on the ‘Operate MP1900A’ button to switch to the MP1900A User Interface.



- Click on the ‘Auto Search’ button.

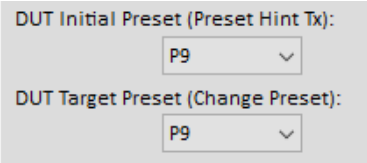
- Execute ‘Auto Search’ using the following settings:
  - Mode: Fine(NRZ)
  - Item: Threshold&Phase
  - CTLE Auto Adjust：ON



7. Error Detector (ED) setup for Return Path optimization:

   In the procedure up to step 6, ED setting parameters for optimizing the Return Path are determined. Each parameter is as follows:

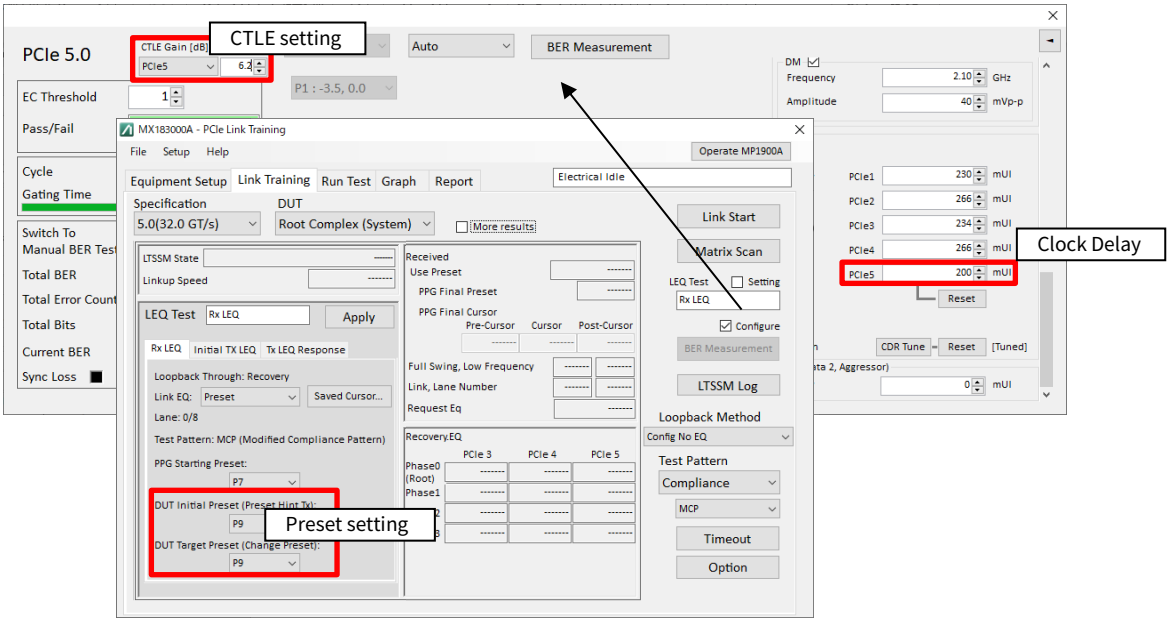
   - Preset setting confirmed in step 5:
     - DUT Initial Preset (Preset Hint Tx)
     - DUT Target Preset (Change Preset)



   - CTLE and Phase settings confirmed in step 6.

Slot	ON/OFF	Data Threshold	XData Threshold	Clock Delay (mUI)	Clock Delay (ps)	CTLE (dB)
Slot6-1 ED	ON	2 mV	-2 mV	200 mUI	16.00 ps	6.2 dB

By applying the above settings to the following parameters of MX183000A, optimization of Return Path is completed.



9.3 J1890A PCIe5 Re-Driver Set Setup & Configuration

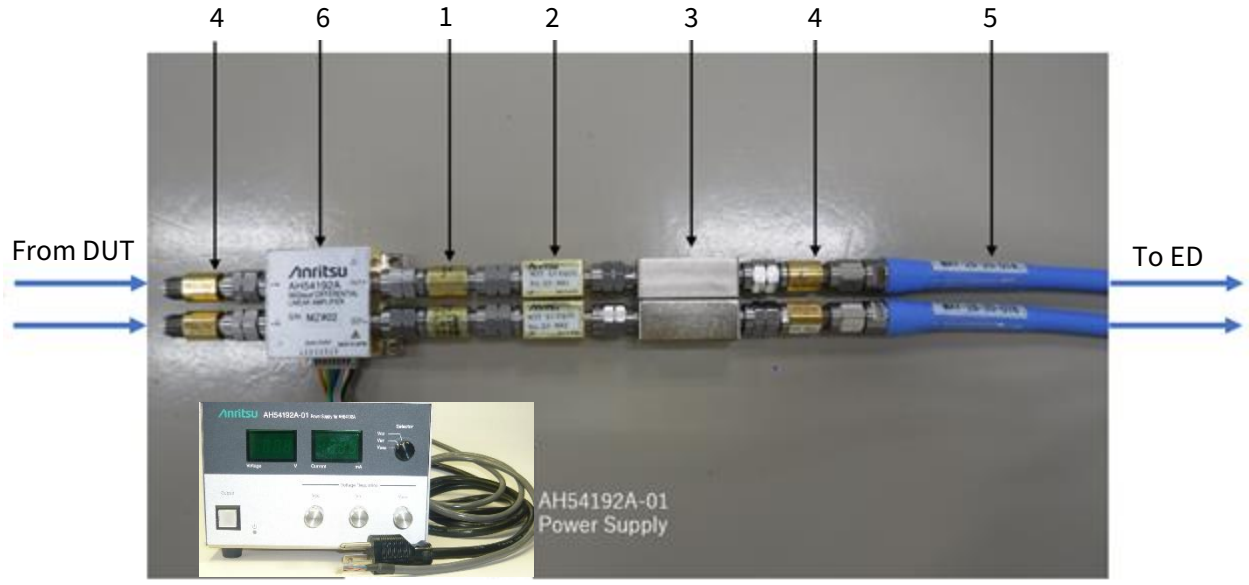
9.3.1 Configuration of Re-Driver

No.	Model	Name	Qty.	Appearance/Label
	J1890A [a]:	PCIe5 Re-Driver Set	—	
1	41VA-3	Fixed Attenuator	2	Labelled 41VA-3
2	J1877A	Passive Low Frequency Equalizer 3.5 dB	2	Labelled 1877A
3	J1645A	Passive Equalizer 3 dB (V-connector)	2	Labelled REQ-M05-F0.0-28.0-S3.0-V-ITI-R
4	34VKF50A	Precision Adapter	4	Labelled 34VKF50A
5	J1820A	Electrical Length Specified Coaxial Cable (0.4 m, K-connector)	2	0.4-m Cable
6	AH54192A [a]	56 Gbaud Differential Linear Amplifier	1	Labelled AH54192A Supplied as a set with dedicated power supply AH54192A-01

[a] *The J1890A and AH54192A are packaged separately. Check the contents of both boxes.*

9.3.2 Connections

Refer to the following picture for the appearance of each part and displayed labels.



9.3.3 Setting of Power Supply AH54192A-01

The following table lists the power supply specifications of AH54192A-01.

There are three types of supply voltages. Set each voltage with the following typ. settings:

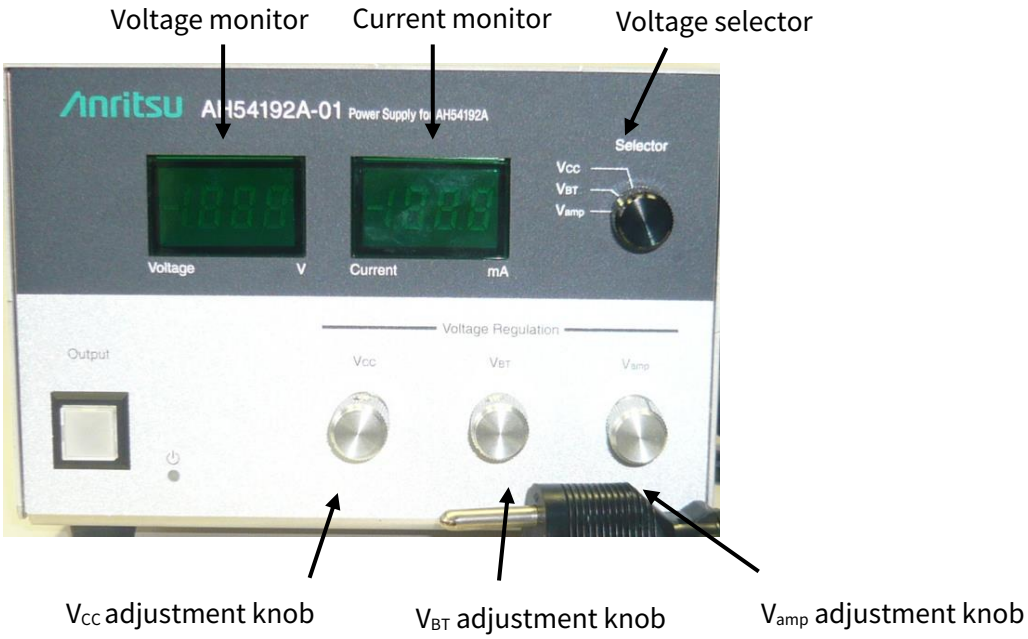
- V_{CC}: Core voltage of AH54192A
- V_{amp}: Gain setting of output signal
- V_{BT}: Output current adjustment

The electrical characteristics of the AH54192A are guaranteed.

Power Supplies

Items	Conditions	Units	Specifications		
			min.	typ.	max.
Supply Voltage	V_{BT}	V		+4.2	+4.4
	V_{CC}			+3	
	V_{amp}			+3	
Supply Current	I_{BT} (×2)	mA		160	180
	I_{CC}			65	75
	I_{amp}			10	20
Power Consumption		W		0.9	

9.3.4 Voltage Setup Steps of AH54192A-01



1. Remove the dedicated DC power cable with the AH54192A.
2. While checking the voltage monitor, switch between V_{CC}/V_{amp}/V_{BT} with the voltage selector and adjust each to the typ. value.
3. Turn off the power and connect the dedicated DC power cable to the AH54192A.

10 Appendix C: Return Path Optimization Using G0430A PCIe5 Re-Driver Set

It is important to optimize the Return Path (DUT Tx to BERT Error Detector) when testing for Receiver Link Equalization with PCIe Gen5 (32 GT/s), as described below.

10.1 Requirements for Using an External Driver (G0430A)

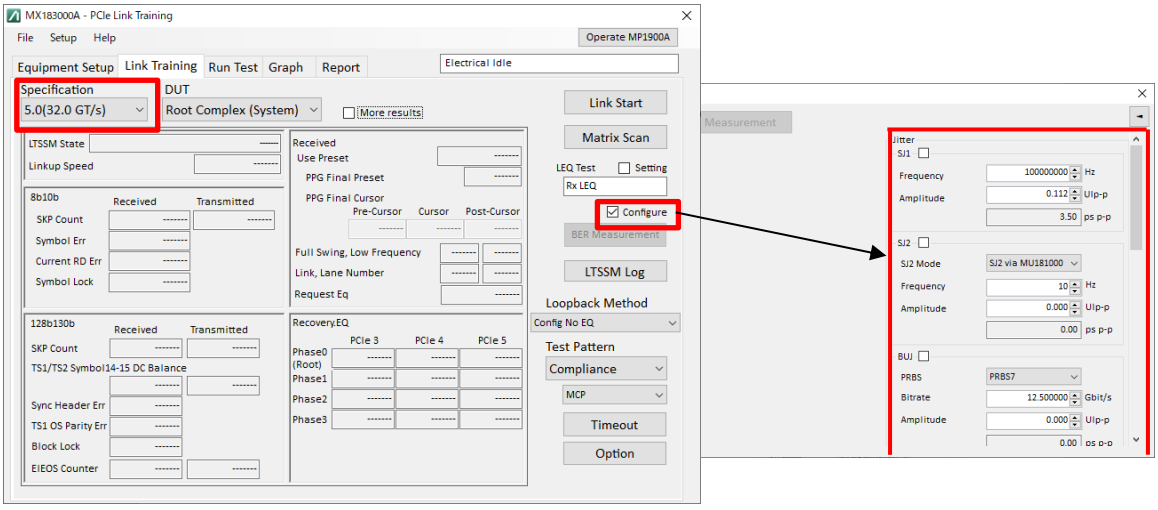
When testing the System Board, connect a G0430A Re-Driver between the DUT Tx and BERT Error Detector. Refer to Section 10.3 for information on how to set up the G0430A Re-Driver.

***Note**: While it is not necessary to use a Re-Driver for the Add-In Card Rx Link EQ Test, the same method of optimizing the Return Path should apply when testing the System Board or Add-In Card.*

10.2 Return Path Optimization Procedure

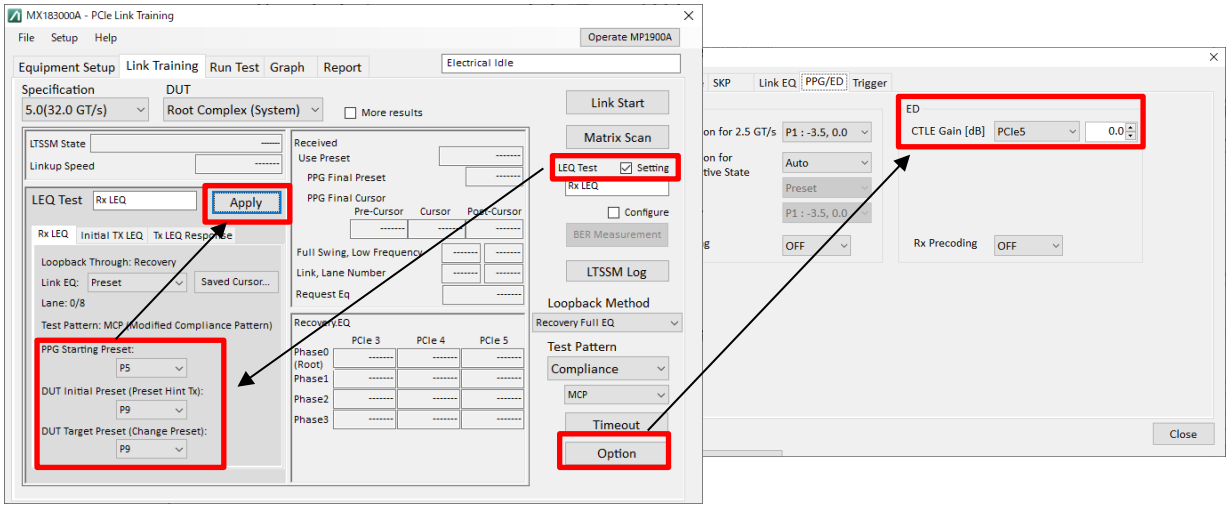
Follow the steps below to optimize the Return Path.

1. Connect the equipment as shown in the System TxRx Link EQ Test setups in Section 5.5.1 & 5.6.1 or Section 8.2.2 & 8.3.2 respectively.
2. Start the MX183000A, set the 'Specification' to '5.0(32.0 GT/s)', and then turn off all stresses as follows:
   - SJ
   - RJ
   - DM
   - CM



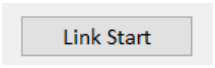
3. In the MX183000A main screen, select the 'Setting' check box for **LEQ Test**, and follow the steps below:

a) Set ‘PPG Starting Preset’ to ‘P5’
b) Set ‘DUT Initial Preset (Preset Hint Tx)’ to ‘P9’
c) Set ‘DUT Target Preset (Change Preset)’ to ‘P9’
d) Click **Apply**
e) Click **Option**, and then on the ‘PPG / ED’ tab of the **Option** dialog box, set ‘CTLE Gain’ to ‘0.0’ dB.



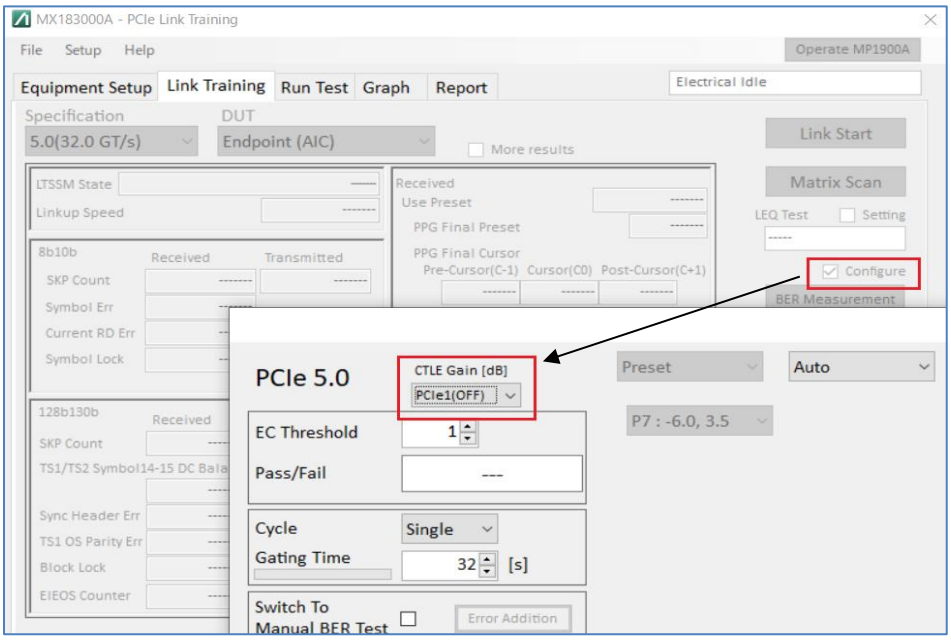
4. Turn the G0430A Re-Driver on and load the channel control parameters as shown in the Section 10.4 table using the *‘MAEQ-39904_EQ_P0.txt’* preset file.

5. Click **Link Start**.



6. Establish Loopback.

a) If the ‘Linkup Speed’ is not ‘32.0 Gbps’ and the ‘LTSSM State’ is not ‘Loopback.Active.Lead’, increase the preset file number of the re-driver, for example at intervals of four, EQ_P0 → EQ_P4 → … → EQ_P20. Each time the preset file number set to the re-driver changes, make sure that the LTSSM is in the Loopback state displayed.
b) If Loopback cannot be established despite the preset file number is set to EQ_P20, set the Preset values in steps 3b and 3c to P8, set the preset file number of the re-driver to EQ_P0, and then retry to check the Loopback state according to step 6a.
c) If Loopback cannot be established even with Preset P8, redo step 6b with the Preset values set to P7, P6, … P0.
d) If Loopback cannot be established, set CTLE Gain to OFF (Step 3e) and redo steps 3 to 6.



e) If Loopback is established according to steps 6a to 6d, check the Preset values of the MX183000A and the preset file number of the re-driver.

f) If Loopback cannot be established up to step 6e, remove ISI from the measuring system and retry steps 6a to 6e.

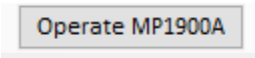
Note: If Loopback cannot be established by the steps above, the measurement environment may be incorrect (cable connection error, etc.) or there may be a problem with the DUT, so review the measurement environment again.

7. BER optimization:

   Perform Link Training with the Preset values, CTLE Gain Setting and the preset file number of the re-driver as specified in step 6 to measure BER.

   a) Optimize EQ to find the setting that gives the optimal BER.
   b) Set the EQ confirmed in step 6.
   c) Run 'Auto Search':

      i) Click **Operate MP1900A** to switch over to the MP1900A User Interface.

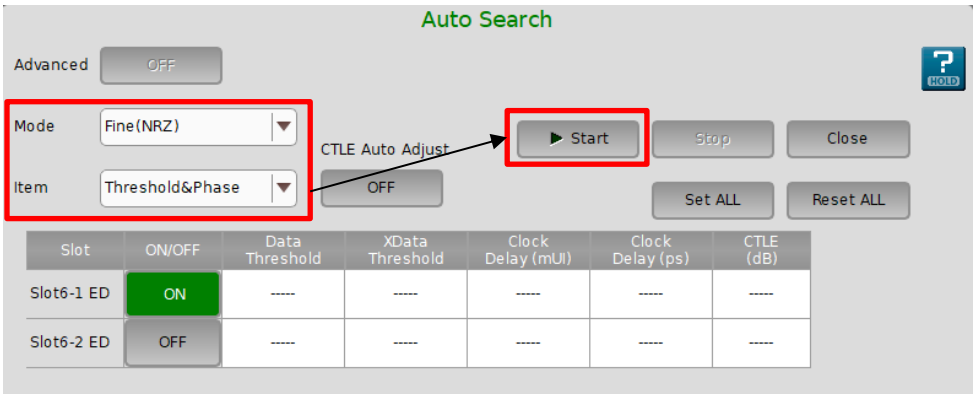


      ii) Click **Auto Search**.

      iii) Set as below and click **Start**:

      - Mode: Fine(NRZ)

- Item: Threshold&Phase
- CTLE Auto Adjust: OFF (if CTLE Gain Setting is ON)



d) Wait until Auto Search is completed, and then check BER.

e) Increase the preset file number of the re-driver by 1 or 2 at a time, and then check the BER again. If the optimal preset BER numbers are detected in succession, repeat until you find the preset number at which the BER deteriorates. If an error-free condition is achieved with multiple preset file numbers, use the preset file with the middle number of a series of preset file numbers as the optimum setting.

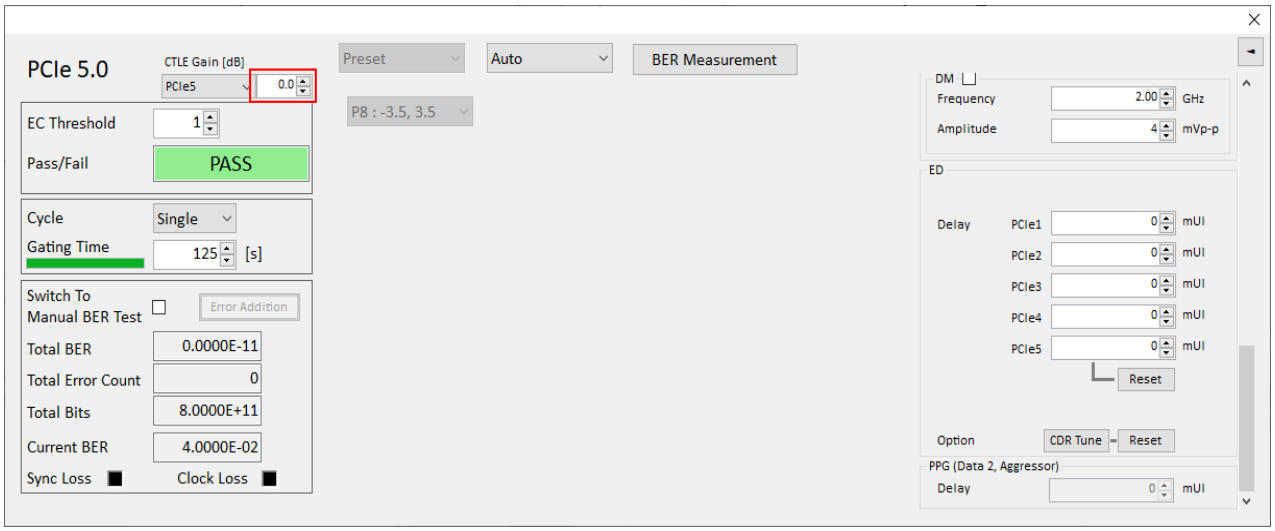
f) Click the **Auto Search** button in step 7c and check the BER again.

When an error-free condition is achieved with the steps so far, then optimization of Return Path is completed successfully. Then, proceed to step 8.

Otherwise, follow steps 7g to 7j as below.

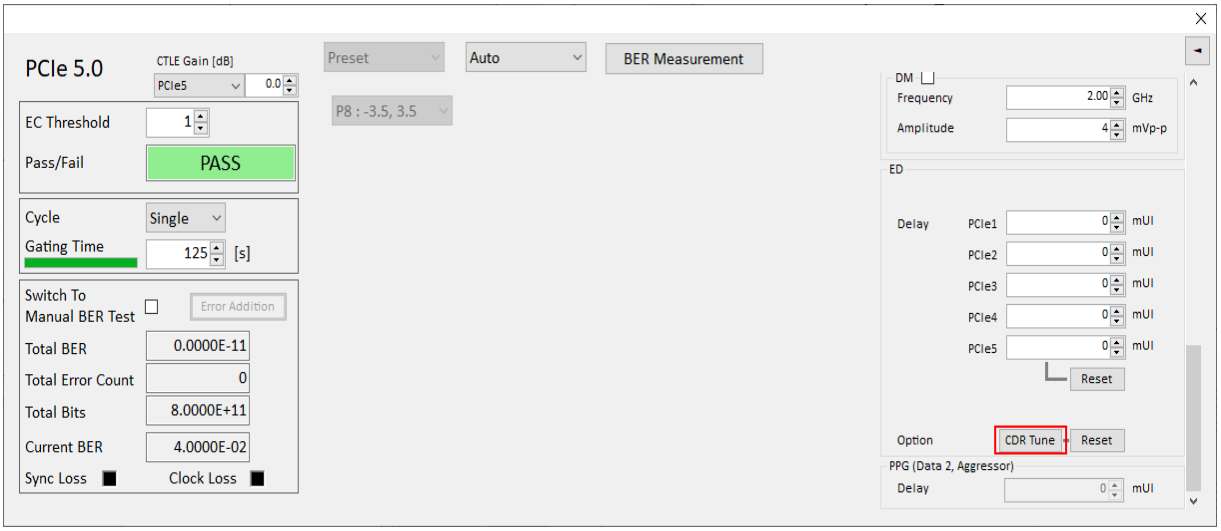
g) CTLE adjustment:

Adjust the CTLE Gain value or set CTLE Gain to OFF to minimize Total BER.



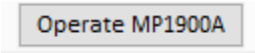
h) Run CDR Tune:

Click **CDR-Tune** to check BER.



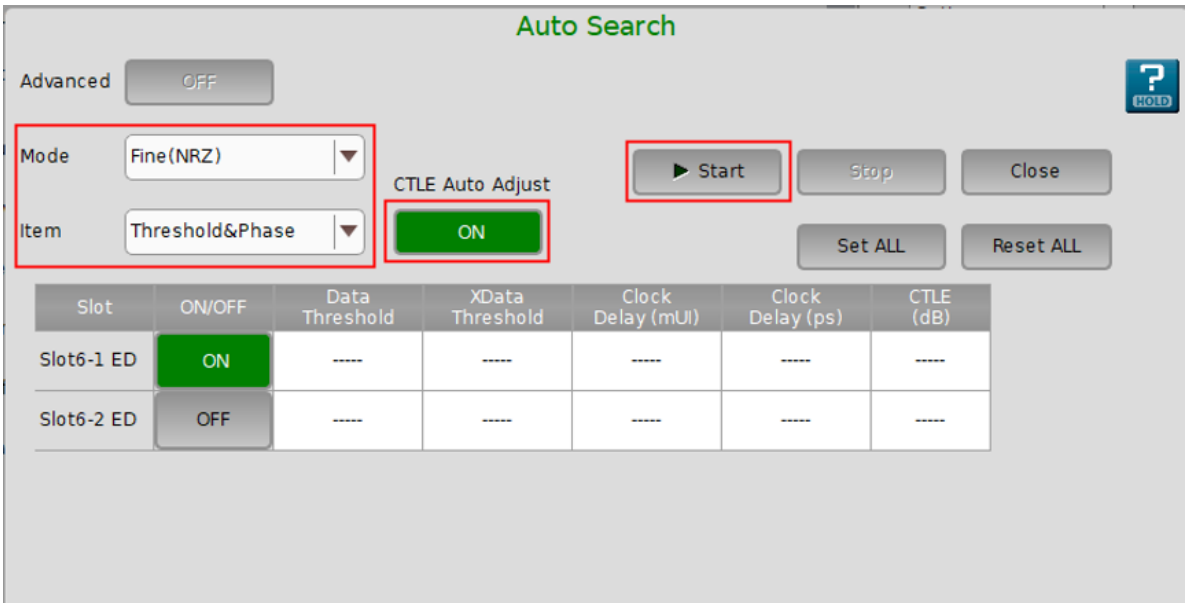
i) Run Auto Search:

- Click **Operate MP1900A** to switch over to the MP1900A User Interface.



- Click **Auto Search**.

- Set as below and click **Start**:
  - Mode: Fine(NRZ)
  - Item: Threshold&Phase
  - CTLE Auto Adjust: ON (if CTLE Gain Setting is ON)



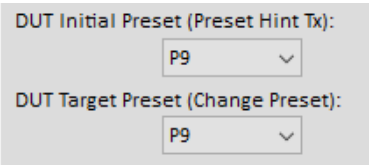
j) Wait until Auto Search is completed, and then check the BER.

With the steps so far, if an error is still detected, it is confirmed that there is an error in the Rx of the DUT.

8. Confirm the setting parameters for optimization:

   These parameters for optimization are determined according to the procedure above (steps 1 to 7), as shown below:

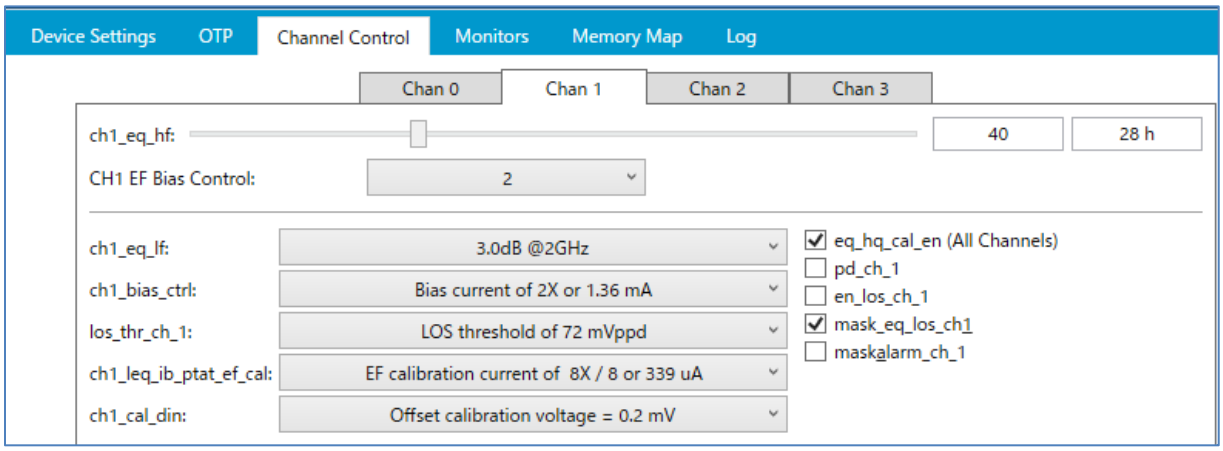
   - Preset setting confirmed in step 6:
     - DUT Initial Preset (Preset Hint Tx)
     - DUT Target Preset (Change Preset)



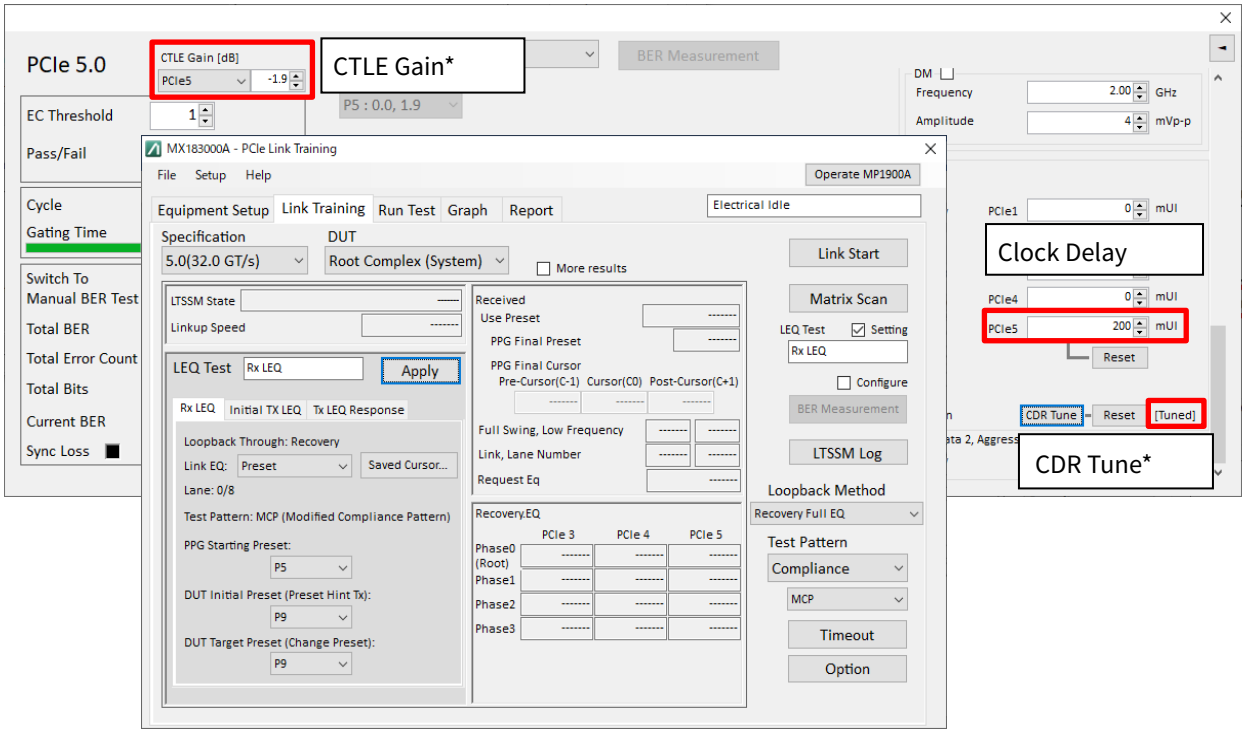
   - Threshold, Phase, and G0430A settings confirmed in step 7.

     CTLE setting is effective only when step 7i is followed.

Slot	ON/OFF	Data Threshold	XData Threshold	Clock Delay (mUI)	Clock Delay (ps)	CTLE (dB)
Slot6-1 ED	ON	0 mV	0 mV	200 mUI	48.96 ps	-1.9 dB



Now, the Return Path is successfully optimized.



* Only when steps 7g to 7j are followed

10.3 G0430A PCIe5 Re-Driver Setup & Configuration

10.3.1 Configuration of Re-Driver

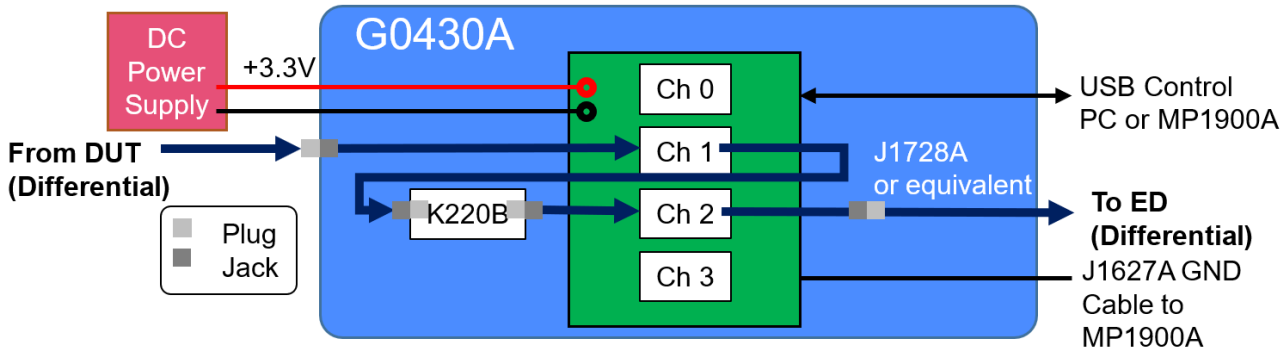
No.	Name	Qty.	Remarks
1	MAEQ-39904B EVM board	1	Linear Equalizer EVM board
2	Mini USB cable	1	Cable
3	USB flash drive	1	The following files are stored: • GUI software • Operation manual • Preset files • Test report
4	2.92 mm Carlisle cable	2	Cable
5	K220B	2	Precision Adapter DC to 40 GHz, 50 Ω
6	DC cable	1	A pair of black and red cords
7	GND connection cable	1	Cable
8	ASB-316.5E	7	Posts
9	3NPS6Ni+SW+WBS	7	Screws
10	+3.3 V label	1	For MAEQ-39904B EVM board Red Terminal

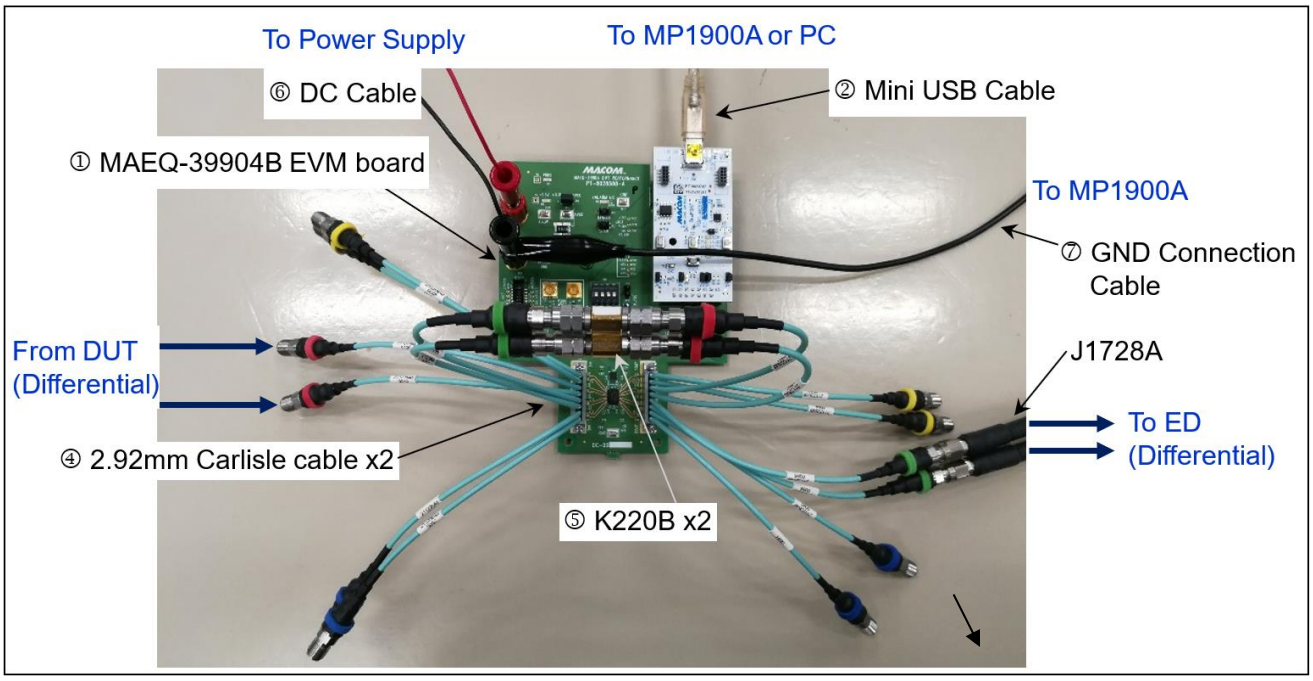
To use the G0430A re-driver, the following required components should be prepared by the customer.

Model	Name	Qty.	Remarks
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K Connector)	2	J1728A or equivalent
N/A	DC Power Supply	1	Single power supply (+3.3 V, 1.5 A)

10.3.2 Connection Diagram

Refer to the following figure for connecting each part of the re-driver. After completing all connections, turn the DC power ON to +3.3 V. Unused channels (Ch0 and Ch3) do not need to be terminated.





10.3.3 Operation Guide

The following procedure will prepare the re-driver for operation.

1. Install the GUI software to a Host PC or the MP1900A.

Note:

The GUI software works only on Windows 10.

If the operating system on the MP1900A is Windows 7, install the GUI software on an external PC installed with Windows 10.

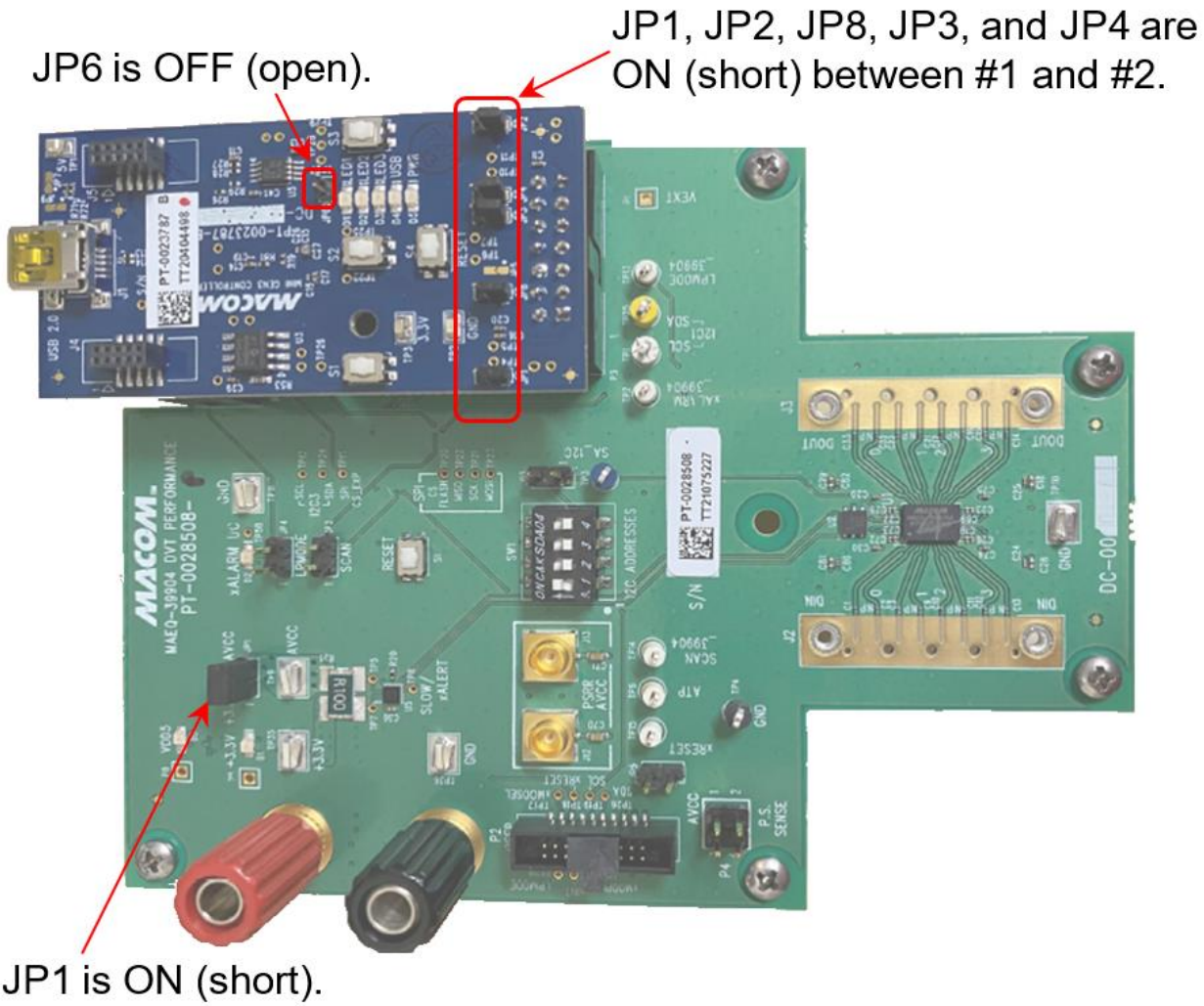
The GUI software is stored on the USB flash drive.

Folder name: \EVM Kit Zip File\EVM Setup vx.x.x

(where x.x.x represents the software version)

Executable file: setup.exe

2. Verify jumpers are present in the positions shown in the following Figure and Table.



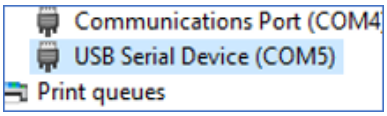
Board	Jumper	Setting	Description
Main Board (Green)	JP1	ON	3.3 V to AVCC
Controller (Blue)	JP1, JP2, JP8, JP3, JP4	1-2, ON	Micro-controller programming setup
	JP6	OFF	Do not use.

3. Connect the device under test (hereafter, DUT) outputs to the MAEQ-39904B Ch1 inputs with the Carlisle connector cables.
4. Connect between the MAEQ-39904B Ch2 outputs and the MP1900A Error Detector inputs using 2.92 mm Carlisle connector cables.
5. Make sure the necessary hardware connections for the G0430A re-driver are in place, and launch the User Control software by going to Start → All Programs → MACOM Technology Solutions.

6. Make sure the software is active, and then click **Connect**.

   The device will be recognized and displayed in the upper-right corner of the window.

   When the **Bad COM Port Settings** dialog box is displayed, open the Device Manager, expand **Ports (COM & LPT)**, and check the number displayed after USB Serial Device.



   Change the Port setting for the software from **Auto** to the USB Serial Device number (for example, **COM5**).

   Also, check that I²C Display is set to **7-Bit**.

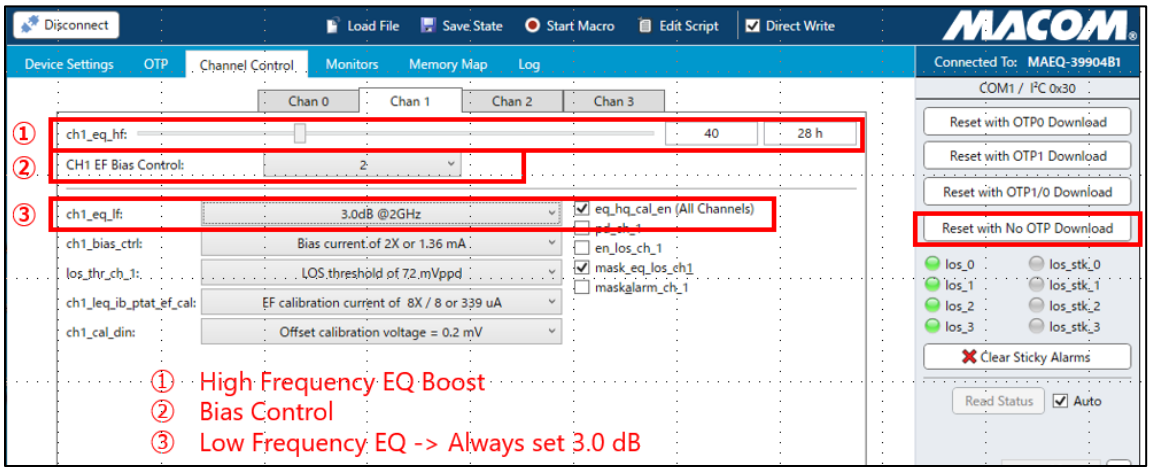
7. On the right side of the **Channel Control** tab, click **Reset with No OTP Download** to reset the device.

   The Channel Control tab helps you control the settings for each of the four channels individually.

   The high frequency boost can be controlled using the slide bar or by inputting a decimal number between 1 to 127 (① in the following figure).

   Channel control also allows control over the settings such as, low frequency boost, bias control and disabling the channel (② and ③ in the following figure).

   On the individual channel tab, each of the four channels can be configured differently.



10.4 EQ Setting Optimization

Refer to the following preset table for optimizing EQ setting.

Set No.	ch1_eq_hf	CH1 EQ Bias Control	ch1_eq_lf (dB)	ch2_eq_hf	CH2 EQ Bias Control	ch2_eq_lf (dB)
0	28	2	3.0	7F	3	3.0
1	20	2	3.0	7F	3	3.0
2	18	2	3.0	7F	3	3.0
3	10	1	3.0	7F	3	3.0
4	8	1	3.0	7F	3	3.0
5	1	1	3.0	7F	3	3.0
6	1	1	3.0	78	3	3.0
7	1	1	3.0	70	3	3.0
8	1	1	3.0	68	3	3.0
9	1	1	3.0	60	3	3.0
10	1	1	3.0	58	3	3.0
11	1	1	3.0	50	2	3.0
12	1	1	3.0	48	2	3.0
13	1	1	3.0	40	2	3.0
14	1	1	3.0	38	2	3.0
15	1	1	3.0	30	2	3.0
16	1	1	3.0	28	2	3.0
17	1	1	3.0	20	2	3.0
18	1	1	3.0	18	2	3.0

Set No.	ch1_eq_hf	CH1 EQ Bias Control	ch1_eq_lf (dB)	ch2_eq_hf	CH2 EQ Bias Control	ch2_eq_lf (dB)
19	1	1	3.0	10	1	3.0
20	1	1	3.0	1	1	3.0

11 Appendix D: SigTest Tool Tab

The SigTest Tool allows the user to manually perform SigTest verification tests for the DUT using appropriate offline PCIe compliant SigTest template and waveform files. This function is used for debugging purposes.

1. Select  from the GRL PCIe CEM 5.0 Rx Test Application menu to access the Setup Configuration page.

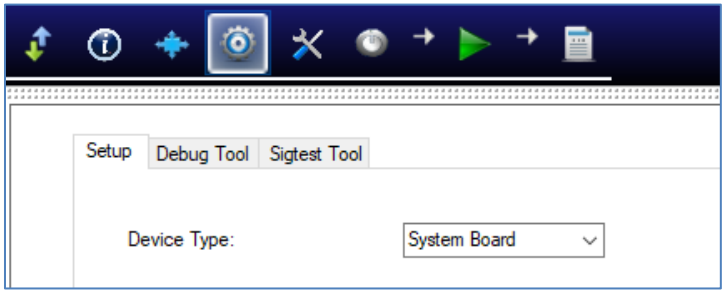


FIGURE 57. SETUP CONFIGURATION PAGE

2. Select the **SigTest Tool** tab.

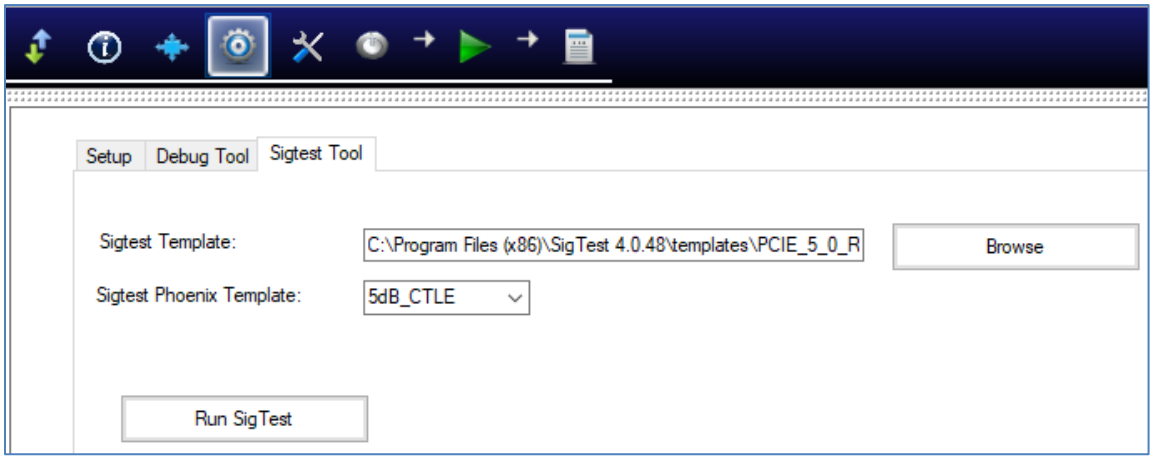


FIGURE 58. PERFORM SIGTEST DEBUGGING

3. Select the Rx Calibration template file from the 'SigTest Phoenix Template' drop-down menu. The SigTest Phoenix with the selected Rx Calibration template file will be used to analyze the captured waveforms.
4. Then select the 'Run SigTest' button to perform SigTest using a selected saved offline waveform file. When selected, the GRL software will automatically run the SigTest for the waveform as shown in below example.

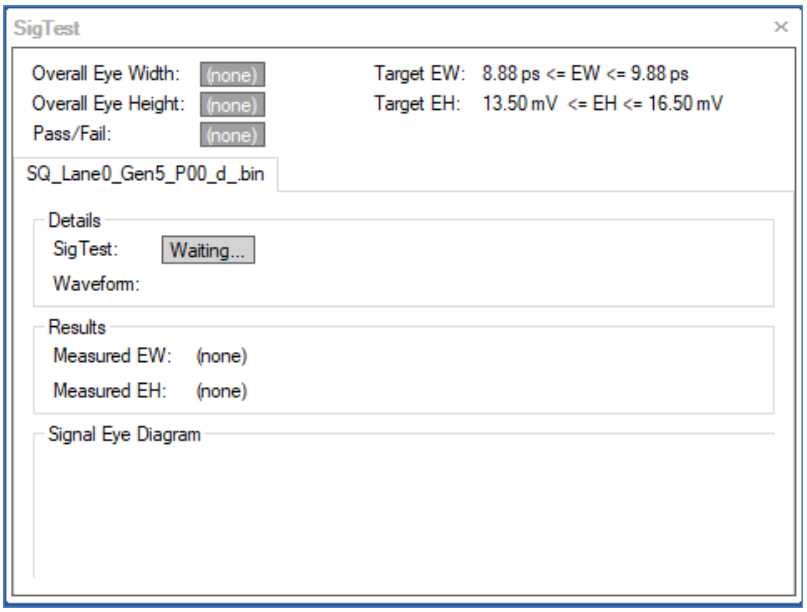


FIGURE 59. RUNNING OFFLINE SIGTEST VERIFICATION

5. Once test is completed, the results will be displayed like in the following example.

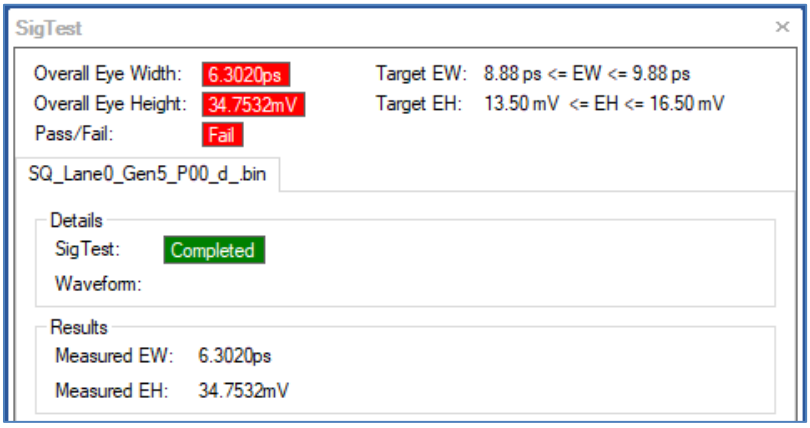


FIGURE 60. VIEWING SIGTEST ANALYSIS RESULTS

12 Appendix E: Debug Tool Tab

The Debug Tool allows the user to manually perform Tx link equalization time response tests with presets and cursors for the DUT using appropriate offline PCIe compliant waveforms. This function is used for debugging purposes.

1. Select  from the GRL PCIe CEM 5.0 Rx Test Application menu to access the Setup Configuration page.

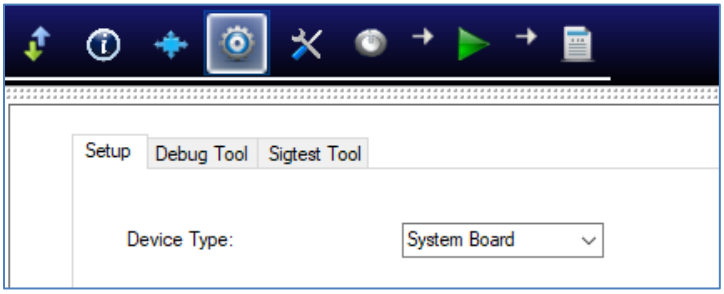


FIGURE 61. SETUP CONFIGURATION PAGE

2. Select the **Debug Tool** tab.

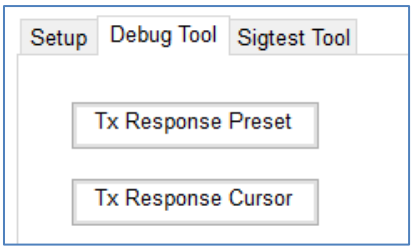


FIGURE 62. PERFORM TX LINK EQ TIME RESPONSE OFFLINE TESTS DEBUGGING

3. Select the 'Tx Response Preset' or 'Tx Response Cursor' button to initiate the respective Tx link EQ time response test. The Select Waveforms pop-up will appear as below.

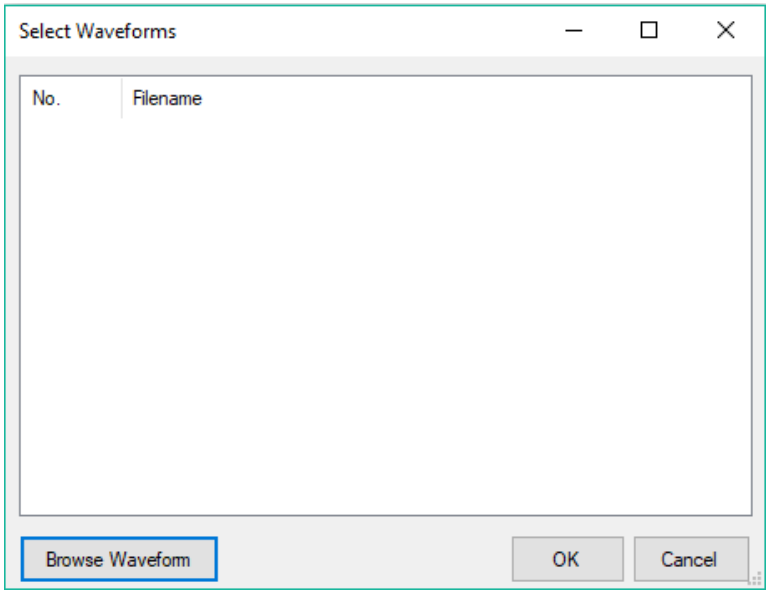


FIGURE 63. INITIATE TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST

4. Select the 'Browse Waveform' button to go to the specific offline waveform file directory and select the waveform file to be used. When selected, the GRL software will automatically run the Tx link EQ time response preset/cursor test for the waveform as shown in below example.

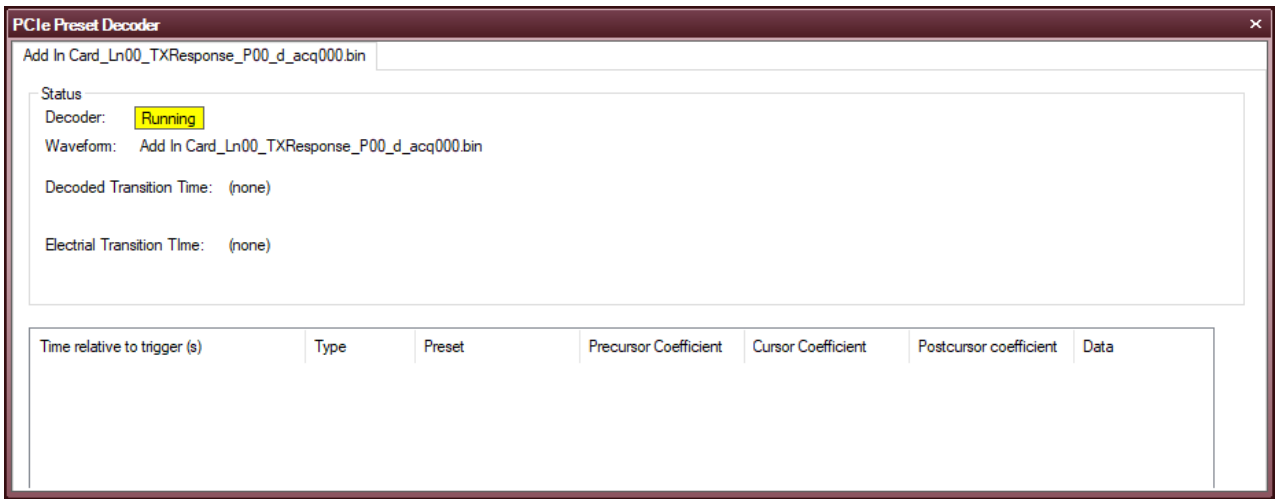


FIGURE 64. RUNNING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST

5. Once test is completed, the results will be displayed like in the following example. A detailed list of the entire requested equalization change can be viewed at the bottom of the window. To quickly determine at which point the Tx equalization change starts to happen in the DUT, select the 'Show' button which will display the row highlighted in yellow.

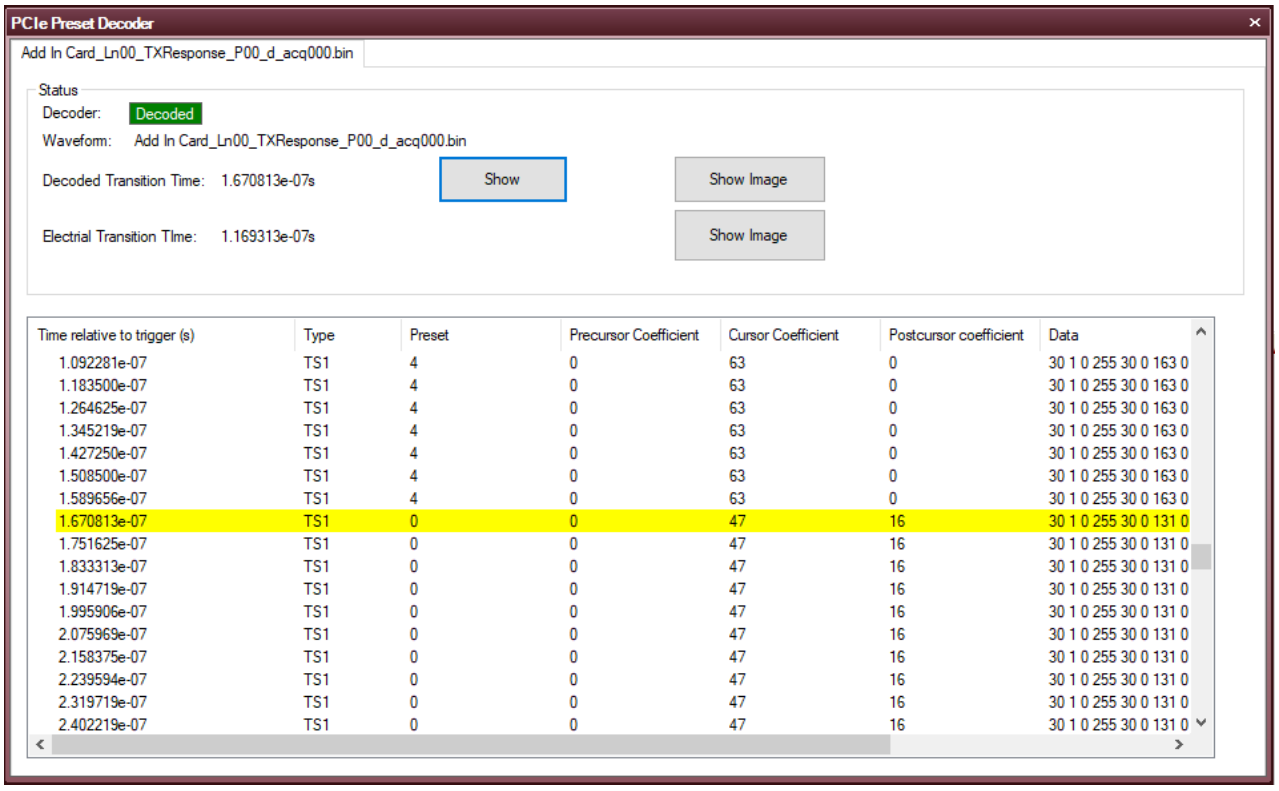


FIGURE 65. VIEWING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST RESULTS

6. For further analysis of the test results, respective traces for the decoded and electrical transition times can be viewed by selecting the 'Show Image' button for each category. An example is shown below.

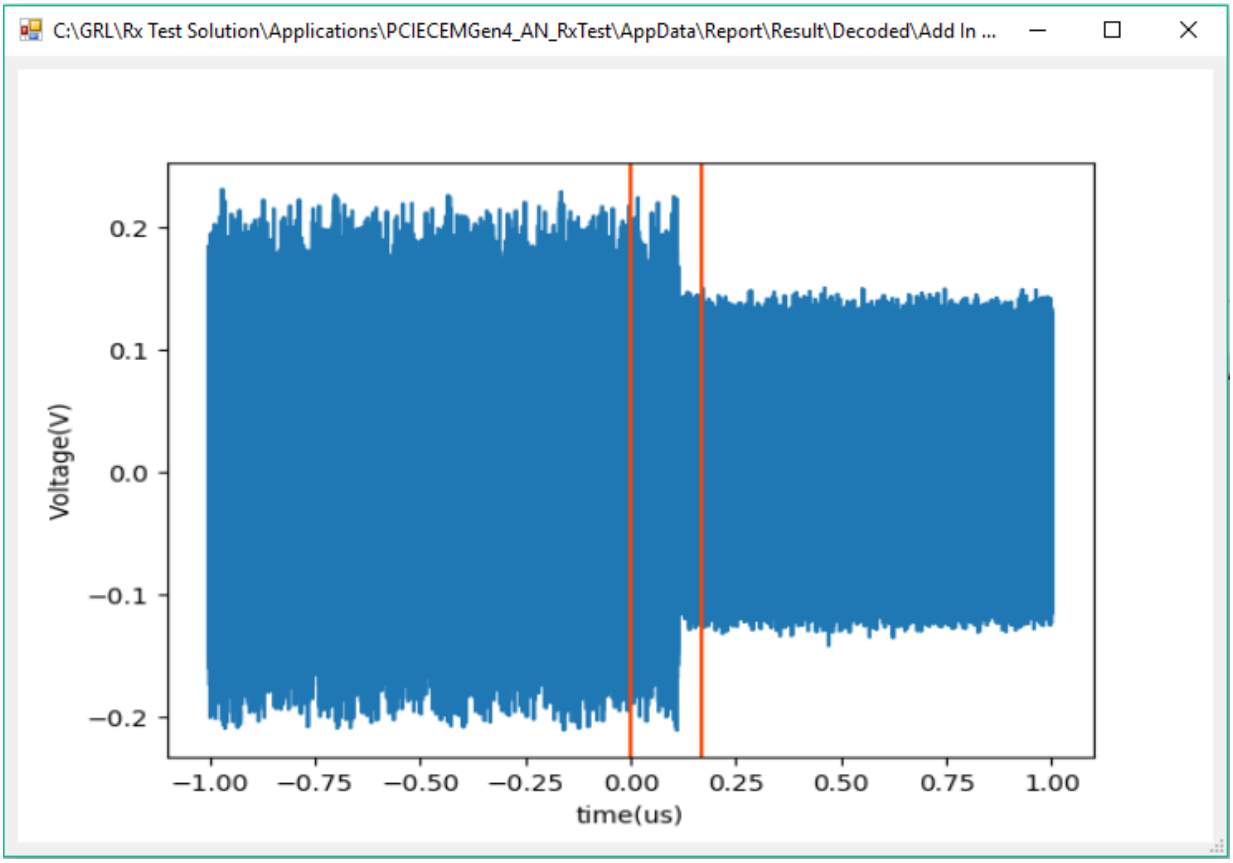


FIGURE 66. VIEWING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST TRACE FOR TRANSITION TIME

Note: The Decoded transition time serves as an informative value only and is not required for compliance.

13 Appendix F: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

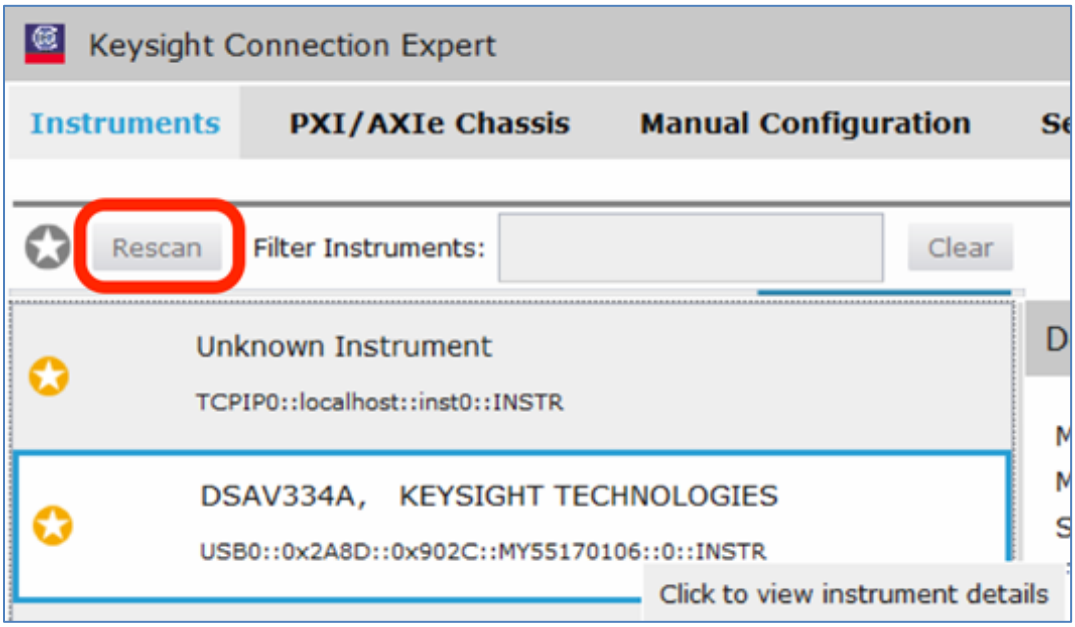


FIGURE 67. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

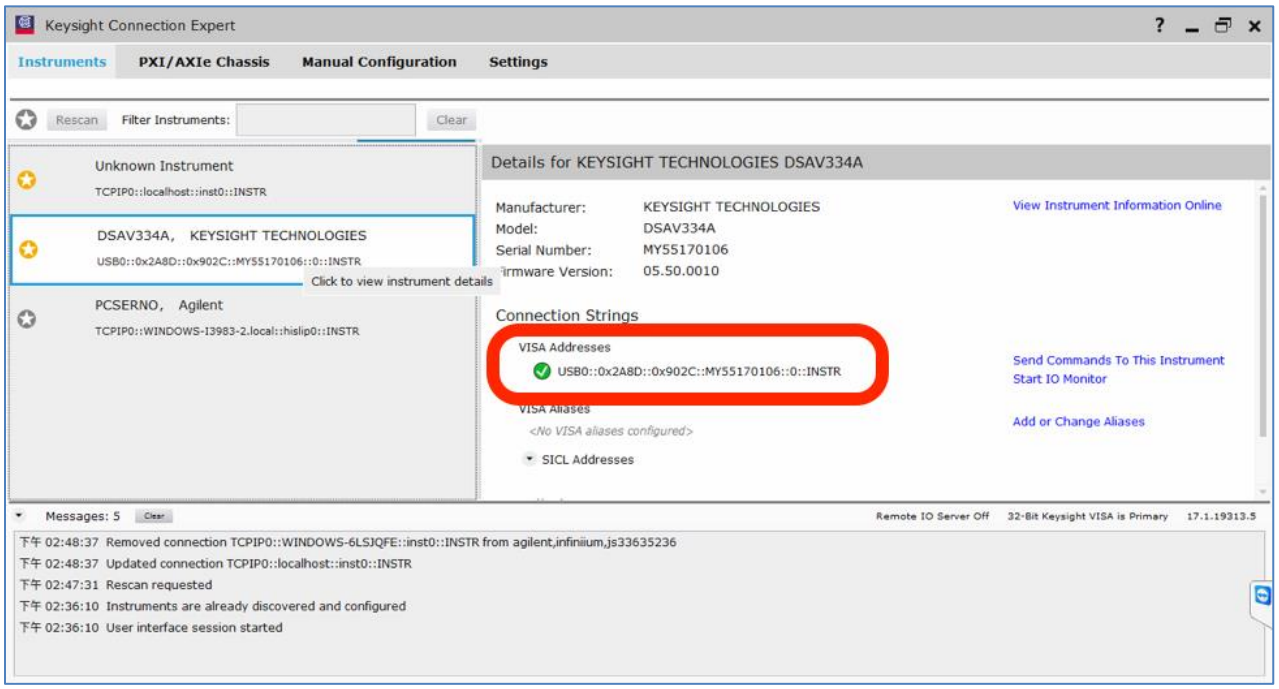


FIGURE 68. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe CEM 5.0 Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

   If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".

14 Appendix G: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

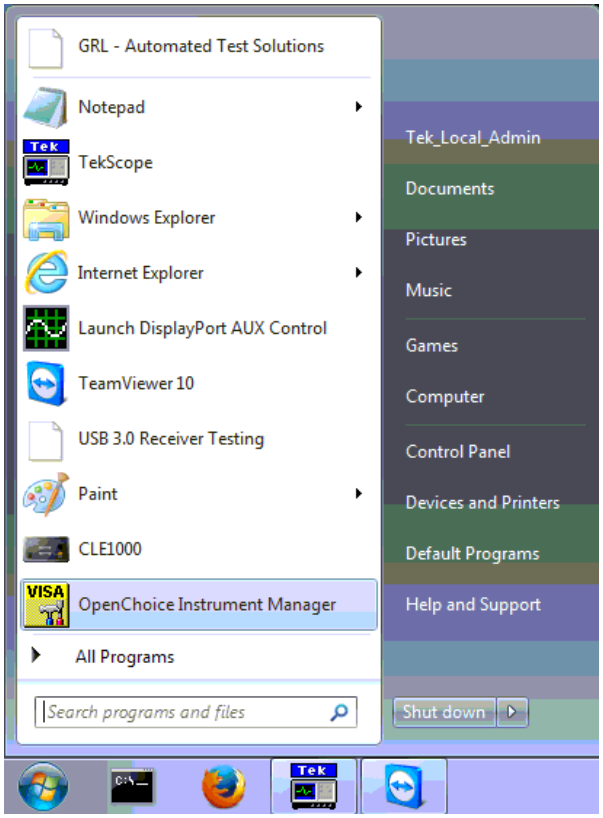


FIGURE 69. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
   a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
   b) “Search Criteria”: Select to configure the instrument search function.
   c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
   d) “Properties”: Select to display and view the selected instrument properties.

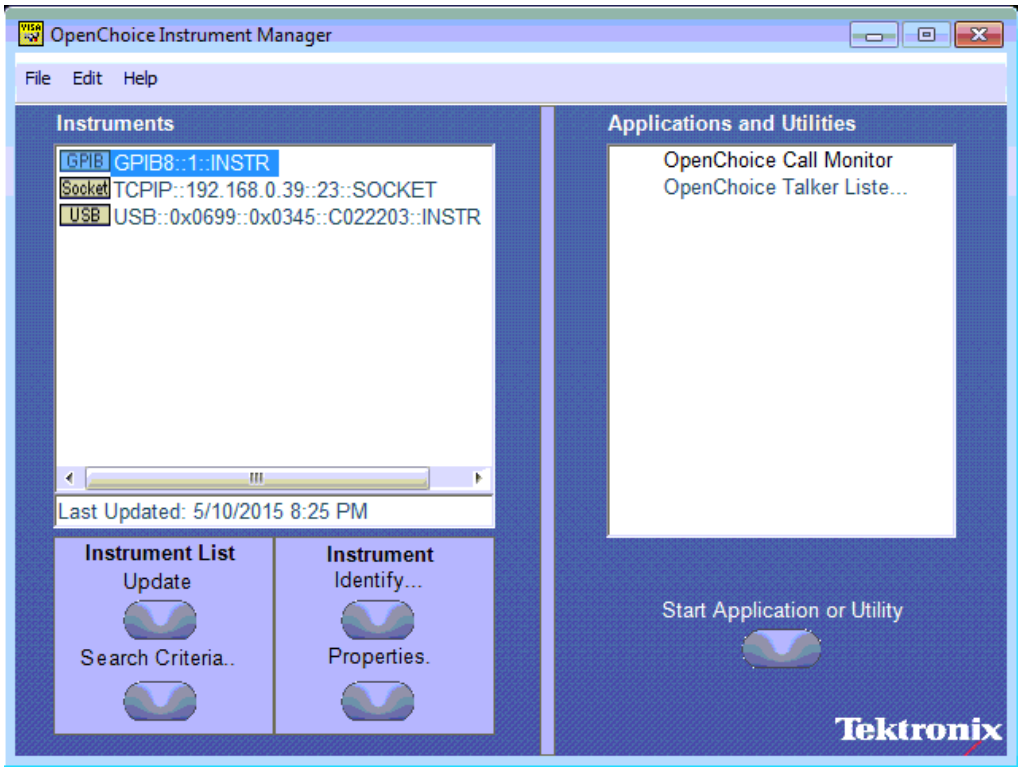


FIGURE 70. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe CEM 5.0 Rx Test Application, type in the Scope address into the ‘Address’ field. If the GRL PCIe CEM 5.0 Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to ***omit*** the Port number from the address.

END_OF_DOCUMENT