Granite River Labs
PCI Express® 5.0 Base Specification (Version 1.0)
Receiver Test Method of Implementation (MOI)
for Anritsu 32Gbps Physical Layer Test Suite
Using Anritsu MP1900A BERT,
High Performance Real-Time Oscilloscope,
and GRL-PCIE5-BASE-RXA Calibration and Test Software

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Questions regarding this document in the GRL may be forwarded to:

Granite River Labs 3500 Thomas Road, Suite A, Santa Clara, CA 95054

Phone: 408-627-7608 Fax: 408-912-1810

E-mail: info@graniteriverlabs.com

http://www.graniteriverlabs.com

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Revision Record

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4.1	10/2020	Added V-K adapter (for PAM4 PPG) to Equipment Requirements	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com

1 Introduction

This User Guide & MOI describes the procedures for receiver (Rx) calibration and jitter tolerance testing based on the PCIe Base 5.0 (ASIC) Specification (for 32 GT/s), using the GRL-PCIE5-BASE-RXA PCIe 5.0 Base Specification Receiver Calibration and Test Software to automate the Anritsu BERT Model (MP1900A) and a high performance real-time oscilloscope to calibrate the stressed eye opening and test receiver conformance and jitter tolerance. The GRL-PCIE5-BASE-RXA software uses Seasim statistical data eye simulator to establish the calibrated test channel DDJ. The final calibrated eye diagram uses the Seasim software to achieve the final stressed eye calibration.

The BERT and appropriate accessories provide the necessary test patterns with jitter, ISI, and crosstalk. Additionally, the BERT is used to add the required transmitter (Tx) equalization. The receiver jitter tolerance test includes various Differential Mode Sinusoidal Interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver eye opening has been calibrated, the receiver jitter tolerance and margin testing can then be performed on the device under test (DUT). The BERT is used to transmit a modified compliance pattern to the receiver DUT and monitors that the loopback pattern conforms to a Bit Error Ratio (BER) that is less than 10^{-12} with a confidence level of 95%.

In summary, this User Guide & MOI basically describes using the GRL-PCIE5-BASE-RXA software to:

1. Calibrate the stressed eye at the receiver of the DUT.
    - This includes calibrating Voltage Swing, Random Jitter (RJ), Sinusoidal Jitter (SJ), Insertion Loss (ISI), Differential Mode Noise, Common Mode Noise, Tx Equalization and Eye Height & Width.
2. Test the receiver using Bit Error Ratio (BER) as a metric. The receiver path is tested with worst case eye to ensure a BER of less than 10^{-12} can be achieved.

Note: Important information detailing method of implementation using automation, oscilloscope and cable calibration, as well as other setup information are included in Appendixes of this document. It is highly recommended to thoroughly review these information prior to performing any testing or data collection.

The GRL-PCIE5-BASE-RXA software is designed to work with the Anritsu BERT as a signal source and error detector for automation of the PCIe Gen 5.0 Base Receiver calibration and testing. Details on how to set up and configure the GRL software are provided in this document.

1.1 Glossary

SJ	Sinusoidal Jitter
ISI	Inter Symbol Interference
RJ	Random Jitter
CTLE	Continuous Time Linear Equalization
DFE	Decision Feedback Equalization
CDR	Clock / Data Recovery
BER	Bit Error Rate
BERT	Bit Error Rate Tester
EH	Eye Height
EW	Eye Width
DPP	Digital Pre-emphasis Processor
Upstream	Reference to Host Test Setup (Calibrated with Device Channel)
Downstream	Reference to Device Test Setup (Calibrated with Host Channel)
DUT	Device Under Test

1.2 Reference Documents

[1] PCI Express® Base Specification Rev. 5.0; Version 1.0; May, 2019
[2] PCI Express Card Electromechanical Specification, Revision 4.0
[3] PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
[4] PCI Express Mini Card Electromechanical Specification, Revision 2.1
[5] PCI Express OCuLink Specification, Revision 1.0
[6] PCI Express M.2 Specification, Revision 1.1
[7] PCI Express External Cabling Specification, Revision 2.0
[8] PCI Express ExpressModule Electromechanical Specification, Revision 1.0
[9] PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0
[10] PCI Hot-Plug Specification, Revision 1.1
[11] PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0
[12] PCI Code and ID Assignment Specification, Revision 1.9 (or later)
[13] PCI Firmware Specification, Revision 3.2
[14] Advanced Configuration and Power Interface Specification, Revision 6.2
[15] Unified Extensible Firmware Interface (UEFI) Specification Version 2.7 Errata A
[16] Guidelines for 64-bit Global Identifier (EUI-64) Registration Authority
[17] Multi-Root I/O Virtualization and Sharing Specification, Revision 1.0

The most current versions of above documents and ECNs are available to PCI-SIG Working Group members at: http://www.pcisig.com/specifications/pciexpress/.

2 Resource Requirements

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS AND ACCESSORIES

Equipment	Qty.	Description	Key Specification Requirement
Keysight/Tektronix Oscilloscope	1	High Performance Real-time Oscilloscope [a]	≥ 50 GHz bandwidth with Windows 7+ OS [b]
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator • MU195040A 21G/32G bit/s SI Error Detector • MU195050A Noise Generator	
ISI Generator	1	PCIe Gen 5 Base Spec compliant Fixed or Variable ISI Channel [c]	
V(m) - K(f) Adapter	*2*	*34VKF50A Coaxial Adapter, only required if using a PAM4 Pulse Pattern Generator*	
Computer	1	Laptop or desktop (Windows 7+ OS) for automation control	

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

[c] The Artek CLE Model Series is supported for variable ISI generation. Refer to Appendix of this document for the Artek CLE Series driver installation procedure.

Note: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table below is a recommended list. Please also refer to the respective manufacturer for detailed cabling recommendations related to PCI Express.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable	Qty.	Key Specification Requirement
Anritsu J1508A BNC to SMA cable pair	1 pair	For MU181000A/B to MU181500B
Anritsu J1624A SMA-SMA cable	3	30cm
Anritsu J1625A SMA-SMA cable	4	100cm
Anritsu J1551A or Huber Suhner 0130-314-00 K-K phase matched cable pair	3 pairs	3ft
Anritsu J1746A K-K cable set	1	For MU195050A output connections
Rosenberger L71-456-102 or Rosenberger RNA 0111 603841, phase matched SMA-SMP adapters	2 pairs	

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Source
GRL-PCIE5-BASE-RXA	Granite River Labs PCIe® 5.0 (32 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com Included with Node Locked License to single oscilloscope or PC OS
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-PCIE5-BASE-RXA software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
Seasim	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software at TP2P) – www.pcisig.com

3 Setting Up GRL-PCIE5-BASE-RXA Software

3.1 Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL-PCIE5-BASE-RXA PCIe 5.0 Base Receiver Test software at 32 GT/s. It also helps you familiarize yourself with the basic operation of the software.

The GRL software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the software, follow the procedure in the following section.

3.1.1 Download and Set Up GRL-PCIE5-BASE-RXA Software

Install, launch and set up the GRL-PCIE5-BASE-RXA software:

1. If the GRL-PCIE5-BASE-RXA software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The zip file contains:
   a) **PCIe5_0_BaseANPatternFilesInstallationxxxxxxxxxSetup.exe** – Run this on the Anritsu Signal Quality Analyzer to install the test pattern setup files.
   b) **PCIEGen5ANBaseSpecTestApplicationxxxxxxxxxSetup.exe** – Run this on the controller PC or oscilloscope to install the GRL-PCIE5-BASE-RXA application.
   c) **PCIe5_0_BaseANRxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.
4. Launch and set up the software as follows:
   a) Open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

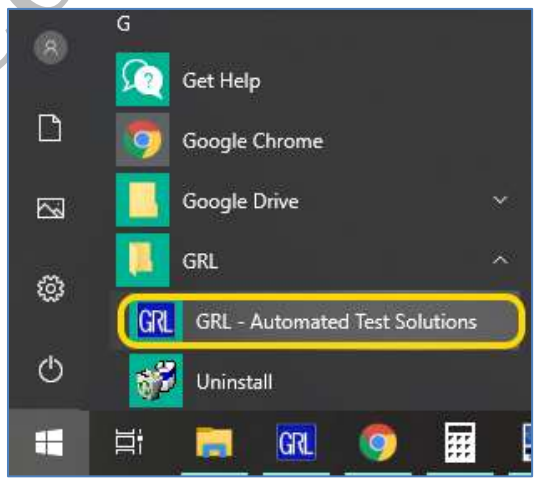

FIGURE 1. LAUNCHING GRL FRAMEWORK

b) From the Application→Rx Test Solution drop-down menu, select "Anritsu PCIe 5.0 Base Rx Test" to start the PCIe 5.0 Base Rx Test Application. If the selection is grayed out, it means that your license has expired.

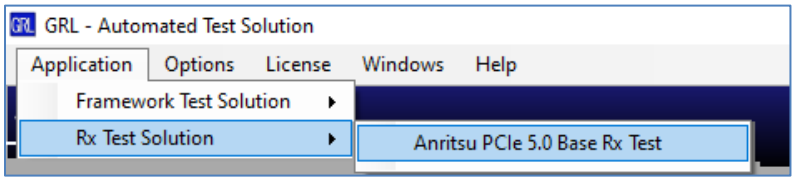

FIGURE 2. LAUNCHING PCIE 5.0 BASE RX TEST APPLICATION

i) To enable license, go to License→License Details.

FIGURE 3. LICENSE DETAILS

ii) Review the installed application.

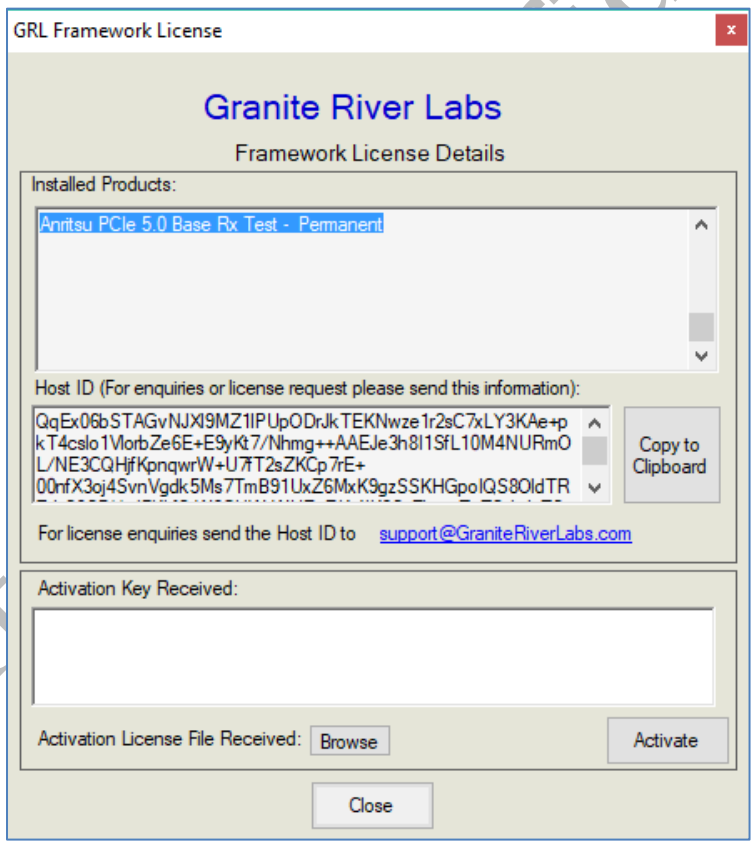

FIGURE 4. INSTALLED APPLICATION

iii) Activate a License:

[1] If you have an Activation Key, enter it in the box provided, and select **Activate**.
[2] If you do not have an Activation Key, select **Close** to use the software for 10 days free of charge.

Note: Once the 10-day trial times out, you will need to request an Activation Key for future usage on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device.

For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.

3.1.2 Connection Configuration

- Connect the Anritsu Signal Quality Analyzer with the controller PC through LAN.
- Connect the Artek ISI Generator (if used) with the controller PC through USB. (*Note: The USB driver software for the ISI Generator must be installed on the PC. The driver is available from the ISI Generator manufacturer. Refer to Appendix of this MOI for driver installation information.)*
- Connect the oscilloscope with the controller PC through either GPIB, USB or LAN. *(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the controller PC is provided in the Appendix of this MOI.)*

3.1.3 Launch and Set Up GRL-PCIE5-BASE-RXA Software (on the Scope or Controller PC)

1. Launch the GRL Host Application from "Start Menu -> GRL -> GRL – Automated Test Solutions".
2. Select "Application -> Rx Test Solution -> Anritsu PCIe 5.0 Base Rx Test Application".
3. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL-PCIE5-BASE-RXA software.
4. If instruments are connected using LAN, type in the IP address of each instrument into the "Address" field, or if using USB, type in the COM address, and click the "lightning" button ( ).

   The "lightning" button should turn green ( ) once the GRL software has successfully established connection with each instrument.

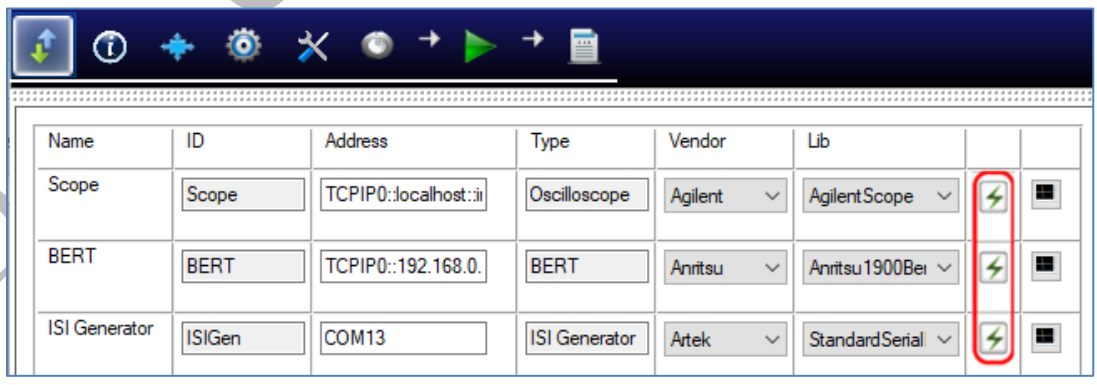

FIGURE 5. GRL-PCIE5-BASE-RXA SOFTWARE INSTRUMENT ADDRESSING

5. *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR.)* If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address. The "lightning" button should turn green if successfully connected to the instrument.

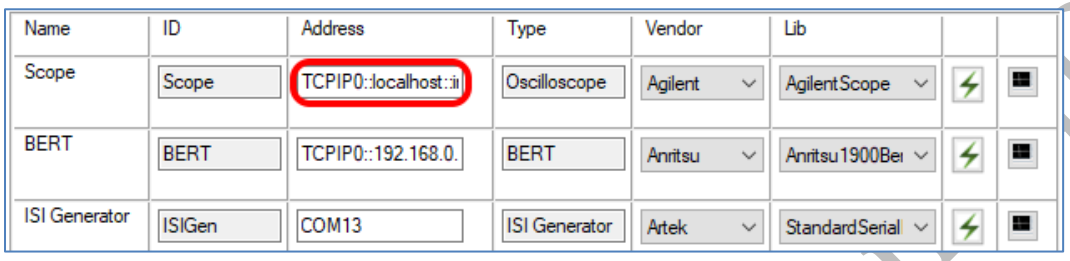

FIGURE 6. GRL-PCIE5-BASE-RXA SOFTWARE SCOPE IP ADDRESSING

3.2 Configuring the GRL-PCIE5-BASE-RXA Software Before Calibration

3.2.1 Session Info

This section ( ) allows information to be entered by the user for defining a specific test. The information provided will also be included in the test report.

The fields under the **DUT Info** and **Test Info** tabs are defined by the user.

The **Software Info** tab is automatically populated.

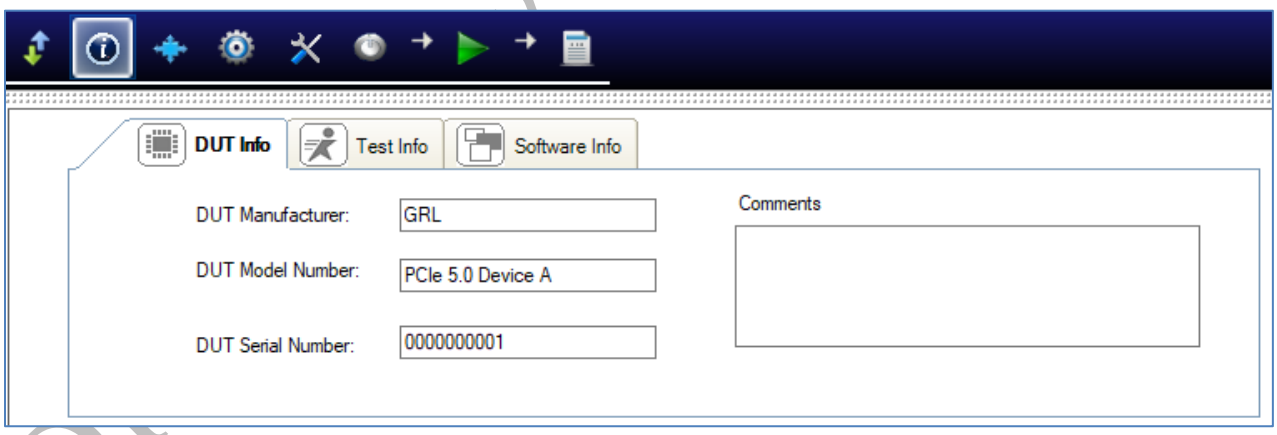

FIGURE 7. SESSION INFO

3.2.2 Conditions for Testing and Calibration

This section ( ) allows conditions required for testing and calibration to be set.

During calibration, the GRL software will calibrate for the selected default or user defined SJ frequency values.

Recommended procedure:

1. When calibrating: Select conditions for calibration and perform desired calibration.
2. When testing: Re-select desired conditions for testing. For example, it may be only necessary to test range A at a specific SJ frequency. The user would select the appropriate SJ frequency for testing.

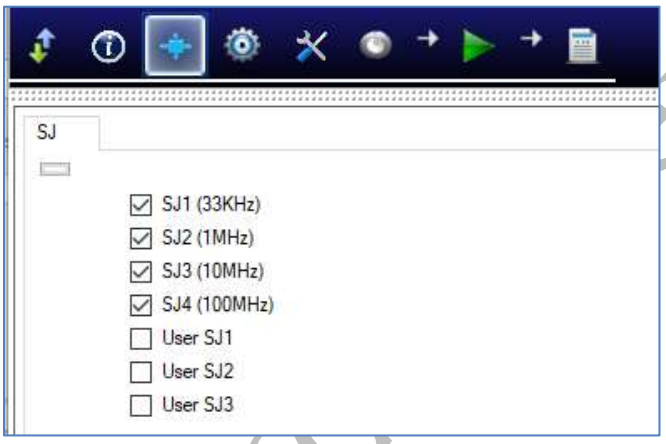

FIGURE 8. CONDITIONS FOR TESTING AND CALIBRATION

3.2.3 Setup Configuration

This section ( ) allows parameters to be configured for calibration and testing.

3.2.3.1 User SJ Frequencies Setting

Set custom SJ frequencies to test for condition setup on the Conditions page.

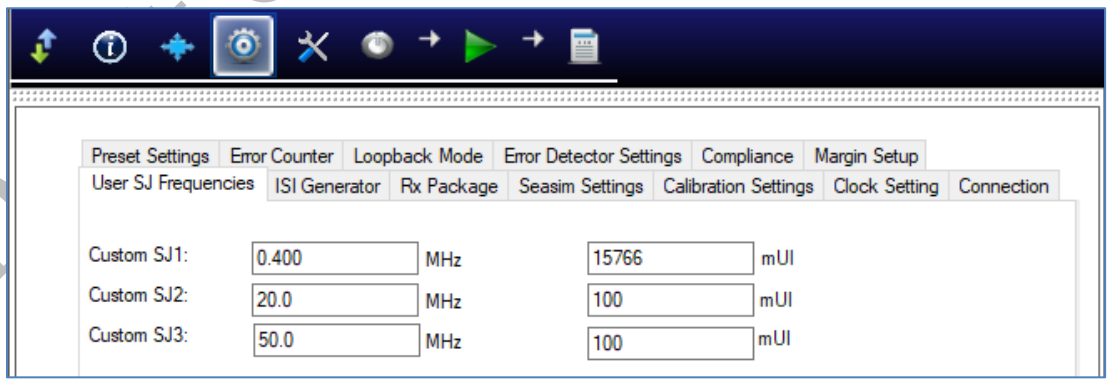

FIGURE 9. USER SJ FREQUENCIES SETTING

3.2.3.2 ISI Generator Setup

Select the type of supported ISI generators to be used:

- "None": This is the recommended method which is used to provide 20 to 27.5 dB physical channel Insertion Loss for calibration and testing. A PCIe 5.0 CEM Fixture can be used in the setup for this method.
- "Artek": This is provided as an Option. The Artek CLE1000-H2 ISI channel and an additional ISI board can be used in the setup for ISI automation. *(Also see Appendix for more information on installing the Artek CLE Series.)*
- "PCIe ISI Board": This is provided as an Option which can be used to measure Insertion Loss when a Vector Network Analyzer is not available.

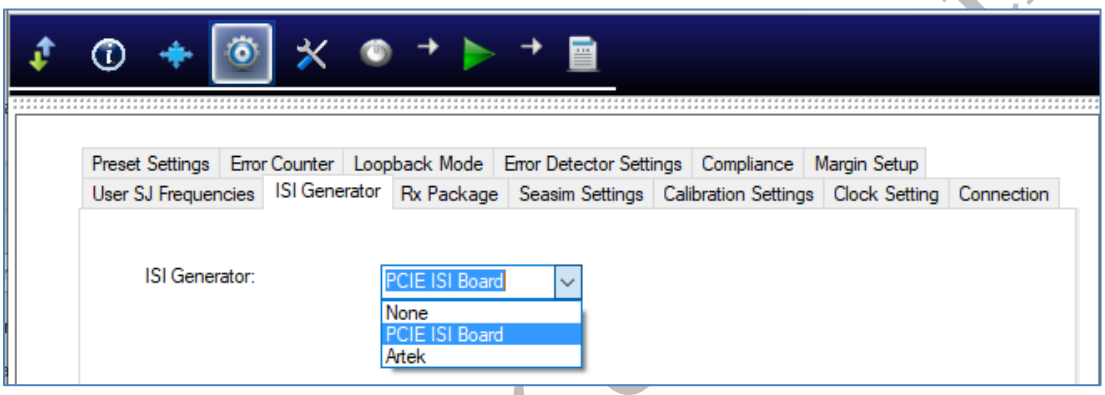

FIGURE 10. ISI GENERATOR SETUP

3.2.3.3 Rx Package Settings

Set up user-defined Rx Behavioral package to be applied during post processing analysis for the Eye Height and Eye Width Calibration.

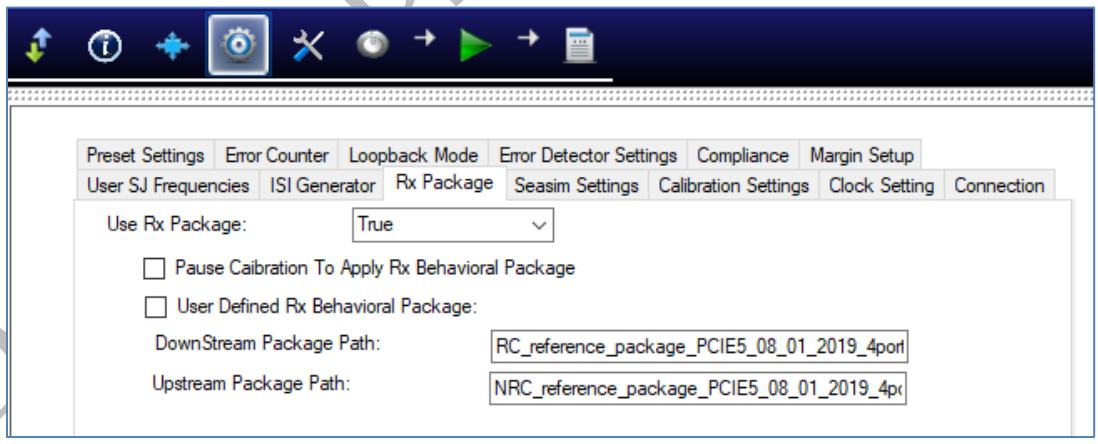

FIGURE 11. RX PACKAGE SETTINGS

3.2.3.4 Seasim Settings

Set the intrinsic noise and jitter (if required) to be used in the Seasim calculation.

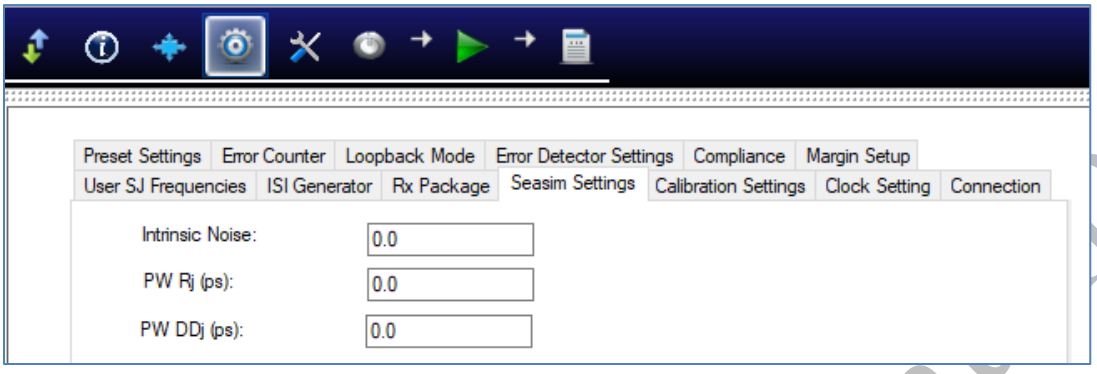

FIGURE 12. SEASIM SETTINGS

3.2.3.5 DM and CM Calibration Settings

Specify or use the default frequency values for Differential Mode (DM) and Common Mode (CM) calibration.

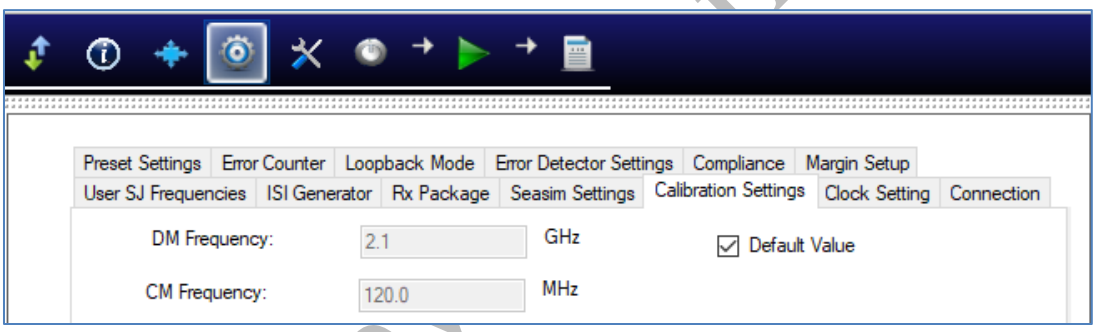

FIGURE 13. DM AND CM CALIBRATION SETTINGS

3.2.3.6 Clock Setup

Select the checkbox to enable Spread Spectrum Clock (SSC) capabilities for calibration and receiver testing (if supported by the DUT) for informative purpose. Set the Frequency and Deviation values for SSC.

Select the type of Rx Reference Clock architecture/mode to be used when testing the Rx DUT (depending on which clock mode is supported by the DUT). For the Common Clock (CC) Refclk mode, a single Refclk source is applied for both the BERT signal generator and the DUT along with SSC and SJ mask. For the Independent Refclk (IR) mode, or in this case "Separate" Refclk mode, two Refclk sources are applied for both the BERT signal generator and the DUT along with independent SSC and SJ mask.

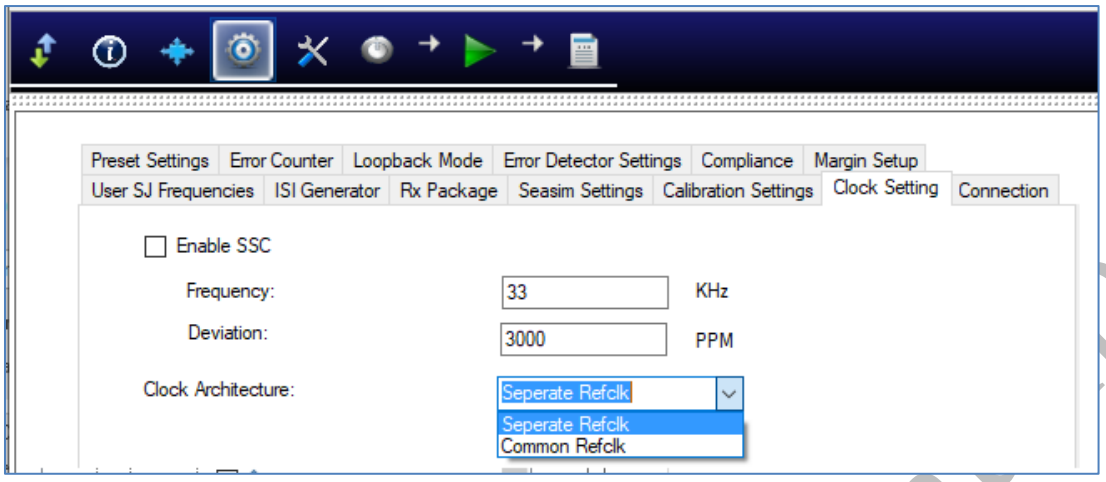

FIGURE 14. SSC AND REF CLK SETUP

3.2.3.7 Connection Setup

Set to use Real Edge connection for test setup on the Oscilloscope. *Note: This setting is only applicable for the Keysight Scope and will be disabled when the Tektronix Scope is used.*

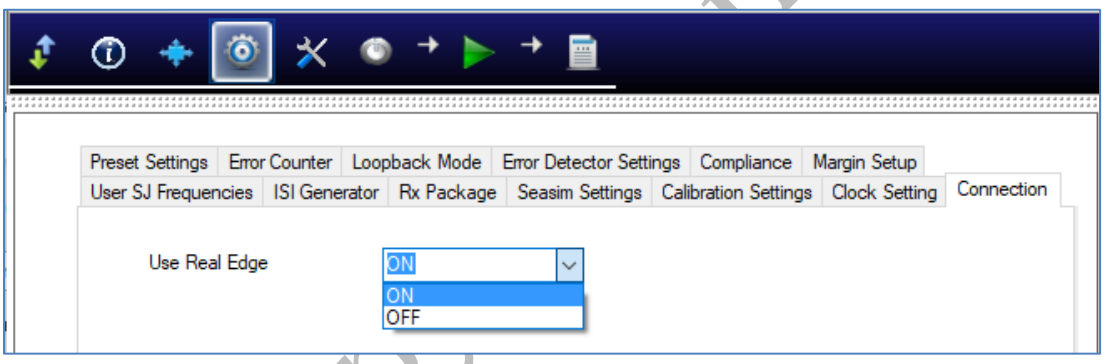

FIGURE 15. CONNECTION SETUP

3.2.3.8 Preset Settings

Select the preset to use, and optionally custom Pre-shoot and De-emphasis settings.

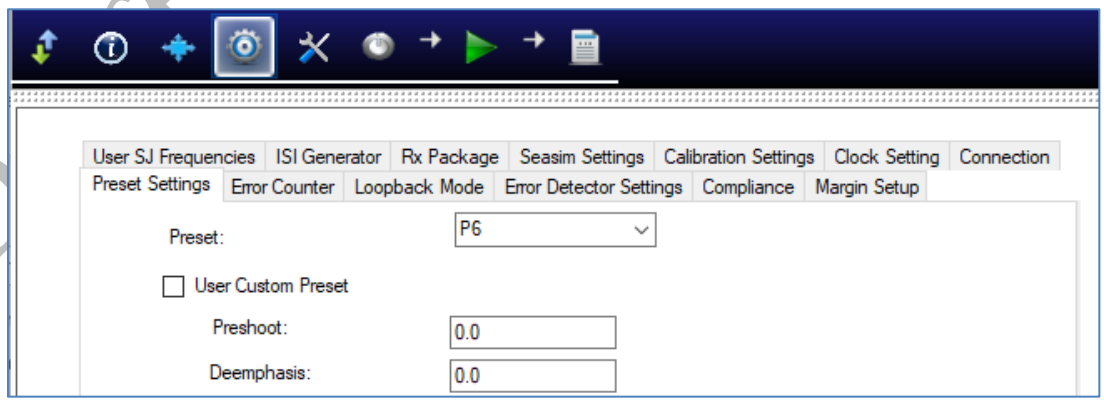

FIGURE 16. PRESET SETTINGS

3.2.3.9 Error Counter Setup

Enable loopback test mode for the Rx base DUT for error detection. If the DUT can be configured to loopback mode, select 'LoopBack', if not select 'Manual'.

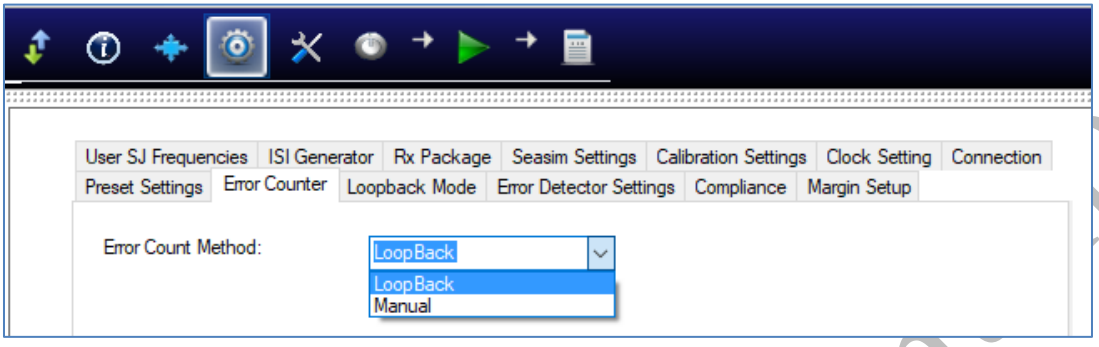

FIGURE 17. BER LOOPBACK TEST METHOD

3.2.3.10 Loopback Mode Setup

If "LoopBack" has been selected from the Error Counter tab, then select "Clock Recovery" in the Clock Recovery Method drop-down on the Loopback Mode tab. *Other options on the Clock Recovery Method drop-down are not yet supported.* Select to apply the default Jitter Tolerance loop bandwidth type or manually define the loop bandwidth values for the clock recovery.

If a Custom Pattern is to be used for error detection analysis, select the checkbox and then select the test pattern type. If the checkbox is not selected, a default test pattern will be used.

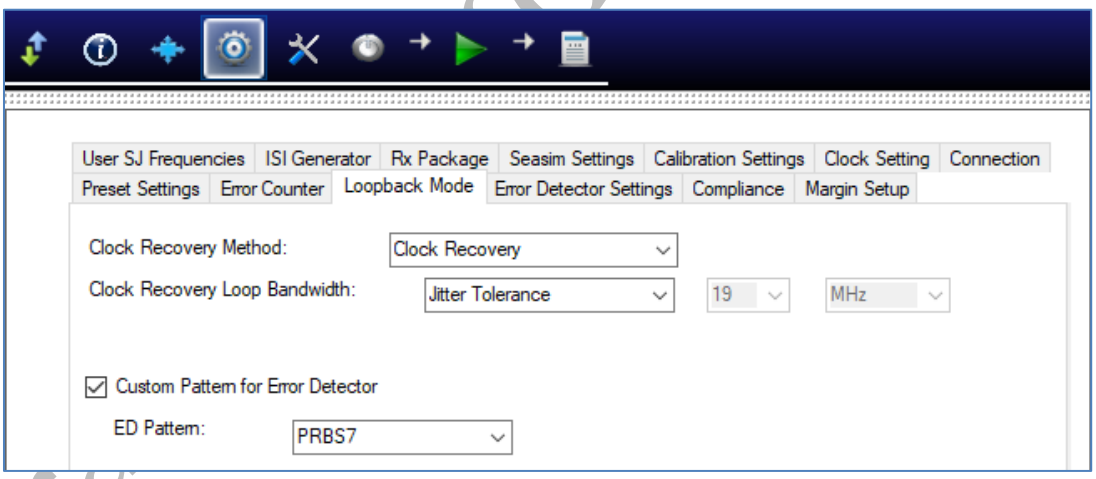

FIGURE 18. LOOPBACK MODE SETUP

3.2.3.11 Error Detector Setup

Enable or disable CTLE and Skip Ordered Set (SKP OS) symbol filtering for BER testing.

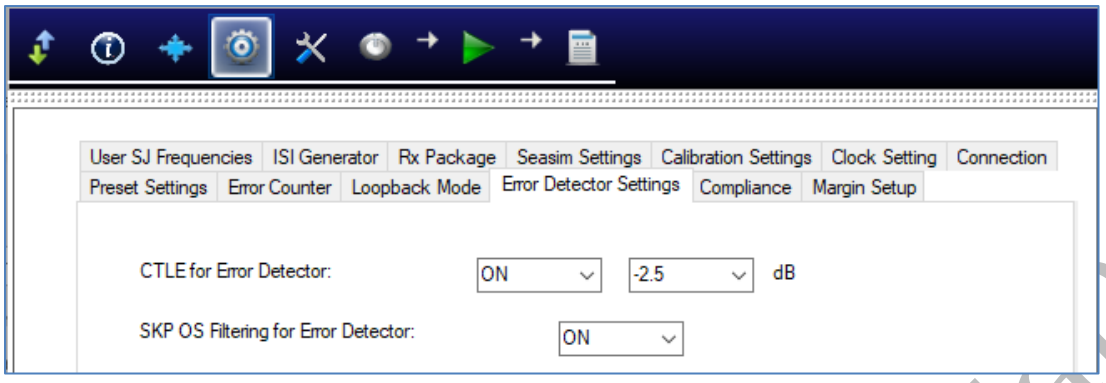

FIGURE 19. BER TEST SETUP

3.2.3.12 Compliance BER Setup

Set the allowable BER and Maximum Error limits to be tested for compliance. By default, these limits are set to Specification, but can be defined by the user. The syntax '1e-12' indicates $1x10^{-12}$, and is the only syntax supported in this field. In normal circumstances, any error count above one constitutes a fail.

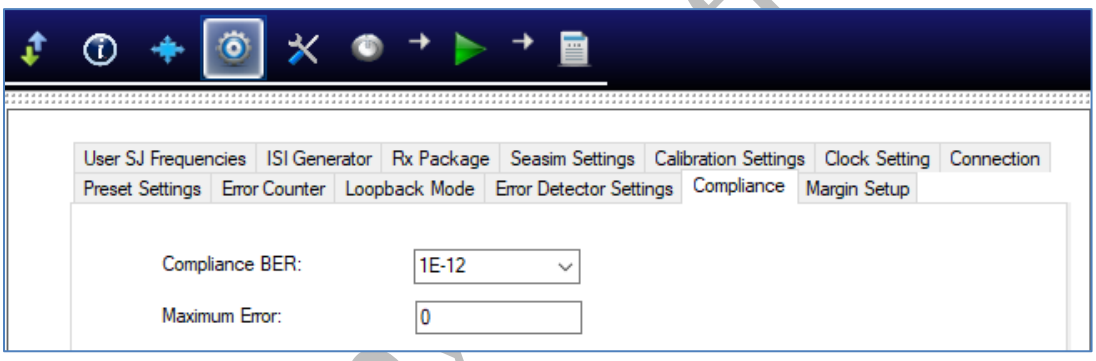

FIGURE 20. COMPLIANCE BER AND MAXIMUM ERRORS SETUP

3.2.3.13 Margin Setup

Select the target BER, step size, and limits to be applied during marginal testing.

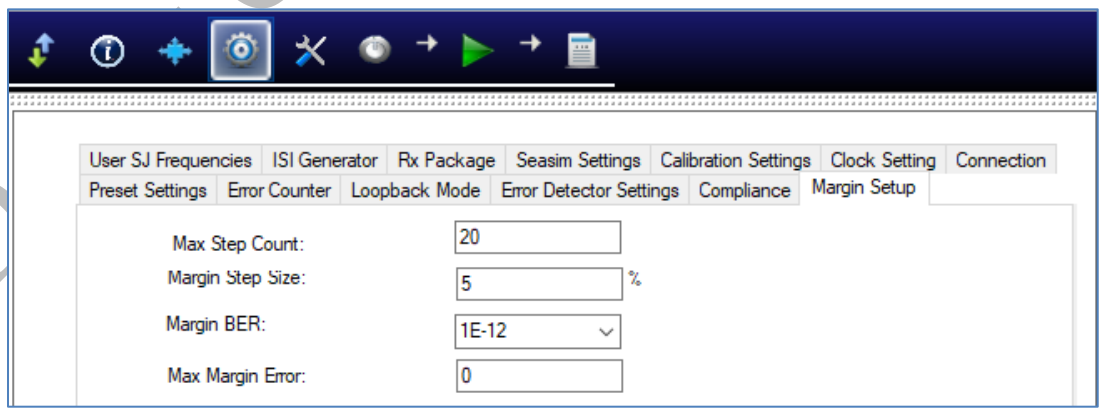

FIGURE 21. MARGIN SEARCH PARAMETERS SETUP

4 Calibrating Using GRL-PCIE5-BASE-RXA Software

Calibration for PCI Express 5.0 Base Specification are performed at two physical test points – TP1 and TP2. TP1 is a physical test point for calibration without the effect of a channel. An adjustable calibration channel is defined that is to be used along with the replica channel for stressed eye calibration. After calibration the signal source will go through the breakout channel to the DUT for Rx compliance testing. TP2 is a physical test point that will affect the eye opening due to trace length. Post processing analysis of the signal is performed at the TP2P test point using the Seasim application to simulate the stressed eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

To calibrate the stressed eye at TP2, the calibration channel shall receive signals with appropriate test patterns generated by the signal source. After calibration the signal source shall be used for testing Rx DUT compliance.

Note: Calibration for the differential voltage swing and Tx equalization of the signal source are performed at the TP3 test point. Overall calibration channel loss shall be determined after the TP3 test point.

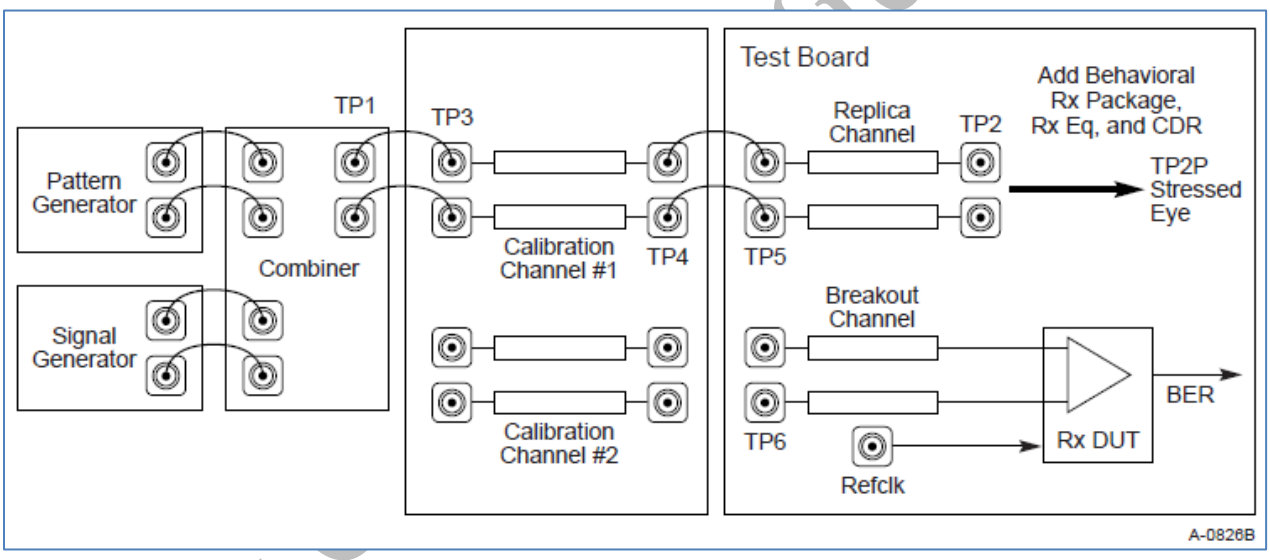

FIGURE 22. RX CALIBRATION/TEST SCHEMATIC OVERVIEW FROM THE PCIE 5.0 BASE SPECIFICATION

4.1 Calibration for TP1 (Output of BERT Generator)

4.1.1 Setup for TP1 Calibration

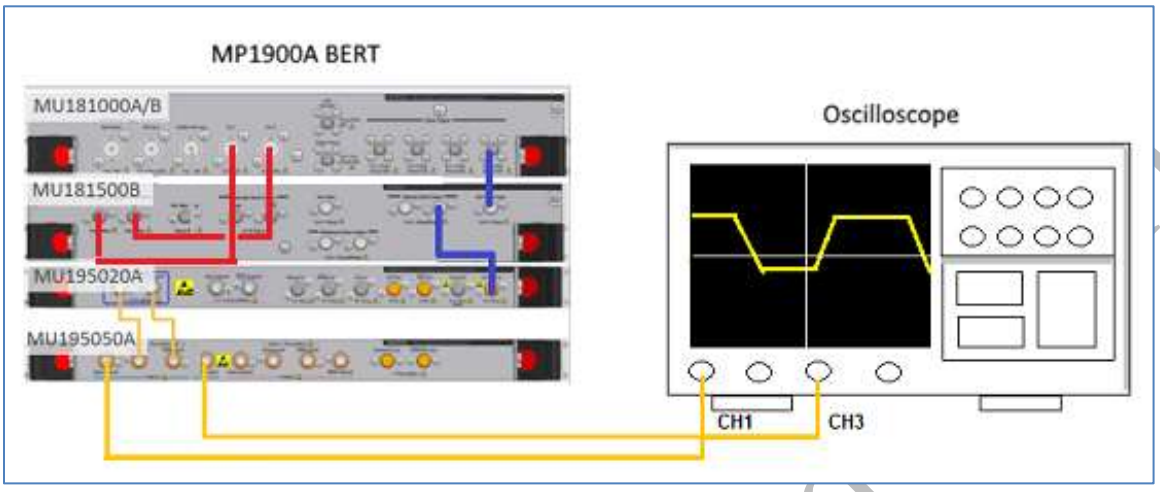

FIGURE 23. TYPICAL SETUP FOR TP1 CALIBRATION

Connection Steps:

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A Ext clock input.
3. Using BNC-SMA cables, connect the MU181000A/B Ext I_Ext Q to the MU181500B I_Q output.
4. Using coaxial cables, connect the MU195020A data outputs to the MU195050A data inputs.
5. Using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 3 on the oscilloscope.

4.1.1.1 TP1 Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following TP1 calibration setup.

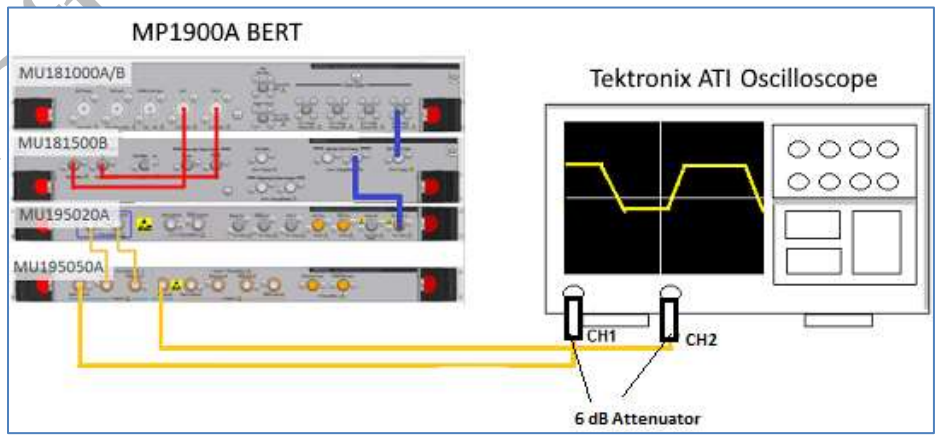

FIGURE 24. RECOMMENDED SETUP FOR TP1 CALIBRATION USING TEKTRONIX ATI SCOPE

*Note: Make sure that the "Tektronix Scope Configuration" is set to **Dual ATI** in the Configurations page (see Section 4.1.3).*

1. Follow back the same connections from step 1 to 4 in Section 4.1.1 above.
2. Then using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.1.2 Select Calibration

The following calibration are defined at TP1 and TP2 Test Points.

Calibration at TP1:

1. Preset 4 Calibration
2. Pre-shoot Calibration
3. De-emphasis Calibration
4. Launch Amplitude Calibration
5. RJ Calibration
6. SJ Calibration
7. SJ Tone Calibration

Calibration at TP2, can be Downstream (for Host) or Upstream (for Device):

8. Downstream or Upstream:
   a. ISI Calibration (CEM Connector Channel + Replica Channel) *[Only applicable if ISI Generator other than "None" is selected from the Setup Configuration menu – see Section 3.2.3.2]*
   b. Common Mode (CM) Sinusoidal Interference Calibration
   c. Differential Mode (DM) Sinusoidal Interference Calibration (Achieves Calibrated Eye Height)
   d. Stressed Jitter Voltage Calibration (Final stressed voltage and jitter eye adjustment with optimized preset to achieve Calibrated Eye Width using the Seasim calibration method)

The GRL-PCIE5-BASE-RXA software automatically calibrates these parameters when initiated. See Appendix for an implementation method with automation for the above calibration.

The test selection panel allows the calibration/tests that need to be performed to be selected. Initially, when starting for the first time or changing anything in the setup, it is suggested to run calibration first. If the calibration is not completed, the Rx DUT tests will throw an error when initiated.

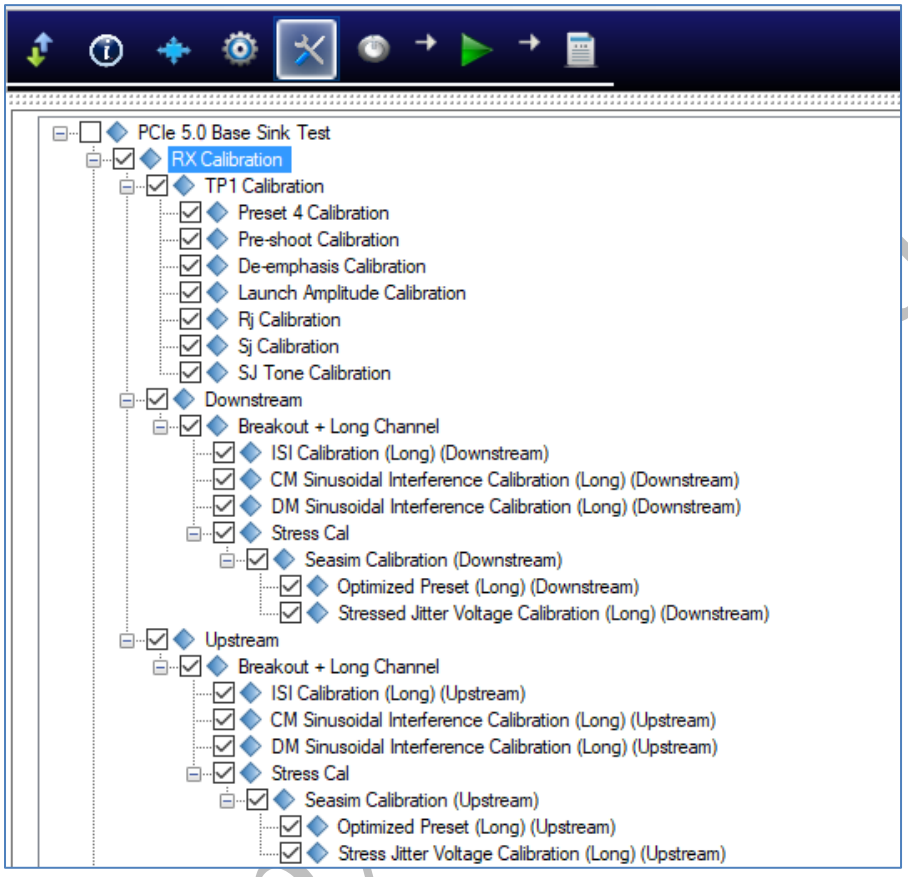

FIGURE 25. CALIBRATION SELECTION

4.1.3 Configure Calibration Parameters

After selecting the desired calibration, the user can select  from the menu to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

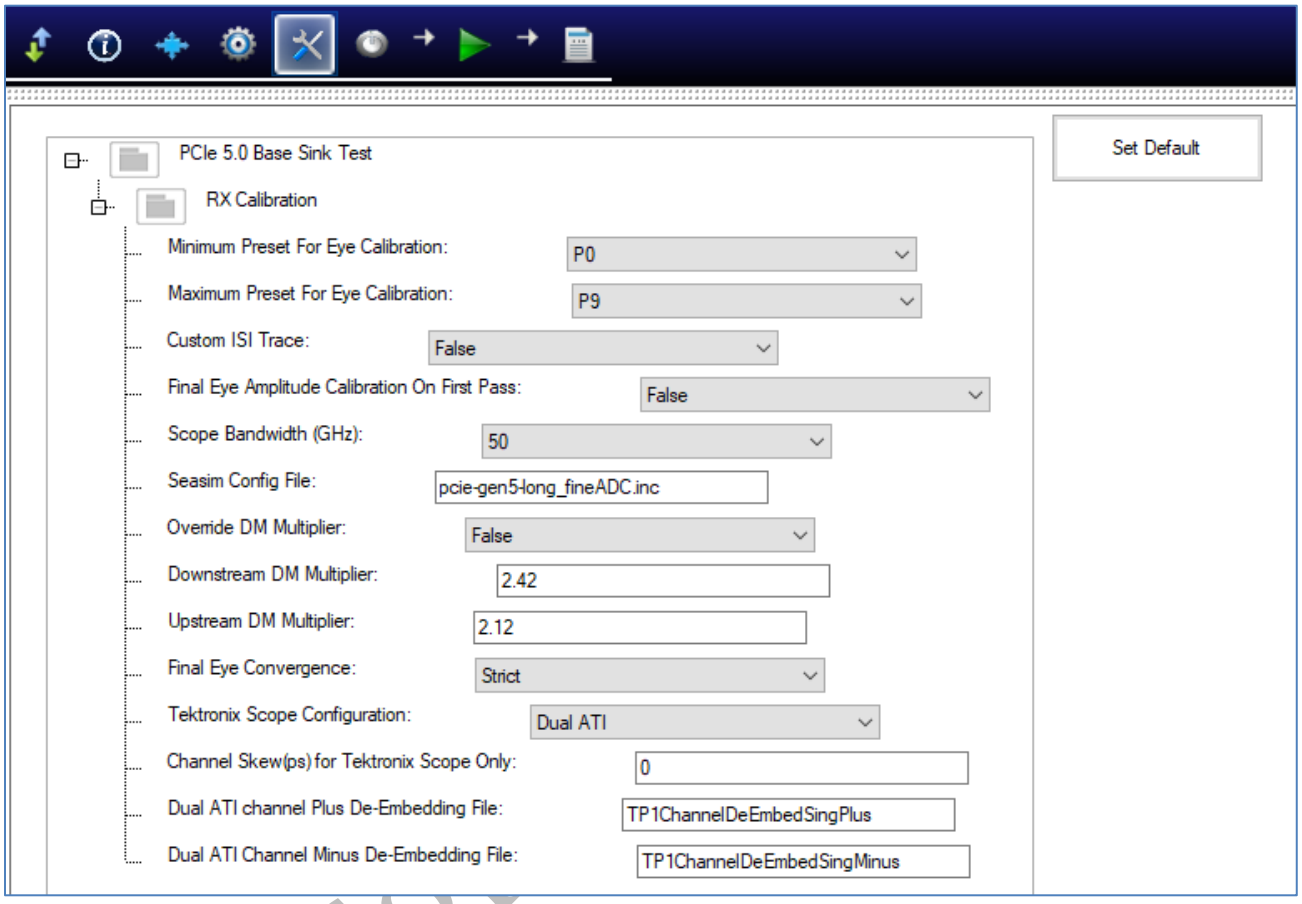

FIGURE 26. CALIBRATION PARAMETERS CONFIGURATION PAGE

TABLE 4. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
Minimum & Maximum Preset for Eye Calibration	Select the range of presets to be applied for stressed eye calibration.
Custom ISI Trace	Select 'True' to enable generating custom ISI trace for ISI calibration.
Final Eye Amplitude Calibration On First Pass	Select 'True' to allow the final stressed voltage/jitter eye to be calibrated over the first attempt of calibration run.
Scope Bandwidth (GHz)	Select the bandwidth supported by the oscilloscope in use.
Seasim Config File	Enter the specific Seasim configuration template file to be used for Seasim measurements.
Override DM Multiplier	Select 'True' to use the upstream/downstream multiplier value for estimation of Differential Mode (DM) at TP2.

Downstream & Upstream DM Multiplier	Enter the multiplier value for conversion of DM at TP2P to TP2 for downstream and upstream devices.
Final Eye Convergence	Select 'Strict' to ensure that final eye width and height from eye calibration converge within specification beyond prediction curve.
Tektronix Scope Configuration	If the Tektronix Scope is to be used for measurements, select either the Single-shot based Scope or the Tektronix' owned Dual Asynchronous Time Interleaving (Dual ATI) based Scope.
Channel Skew (ps) for Tektronix Scope Only	If the Tektronix ATI based Scope is to be used for measurements, enter the channel skew or timing to perform alignment of the Scope channels.
Dual ATI Channel Plus & Minus De-Embedding File	If the Tektronix ATI based Scope is to be used for measurements, specify the file name for de-embedding on the respective Scope channel.

4.1.4 Run Calibration at TP1

Select  from the menu to select the following run options and then start running the selected calibration.

- **Skip Test if Result Exists–** If previous calibration results exist, the GRL software will *skip* the calibration steps that have existing reports.
- **Replace if Result Exists–** If previous calibration results exist, the GRL software will *replace* each step in the calibration with new results.

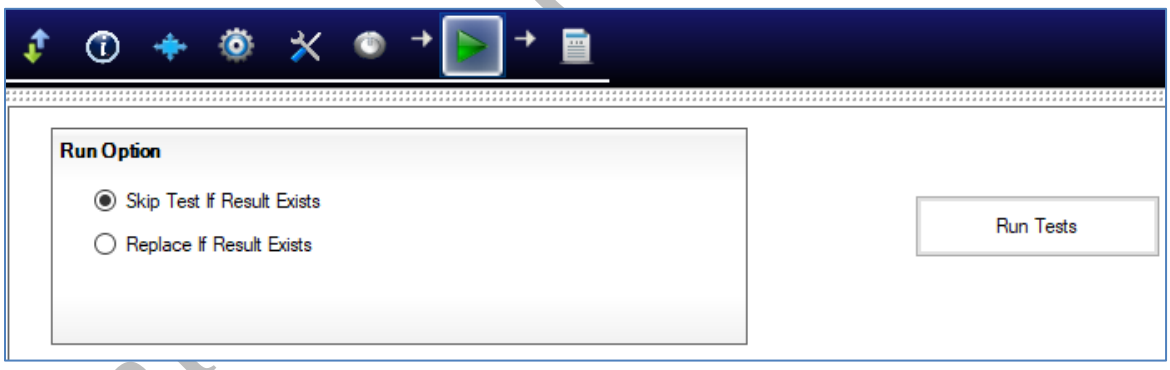

FIGURE 27. RUN TESTS

Select the **Run Tests** button to start running calibration.

When running calibration at TP1, the GRL software will display the connection diagram as a first step to help the user make sure all connections are proper before calibration is performed. Example as below:

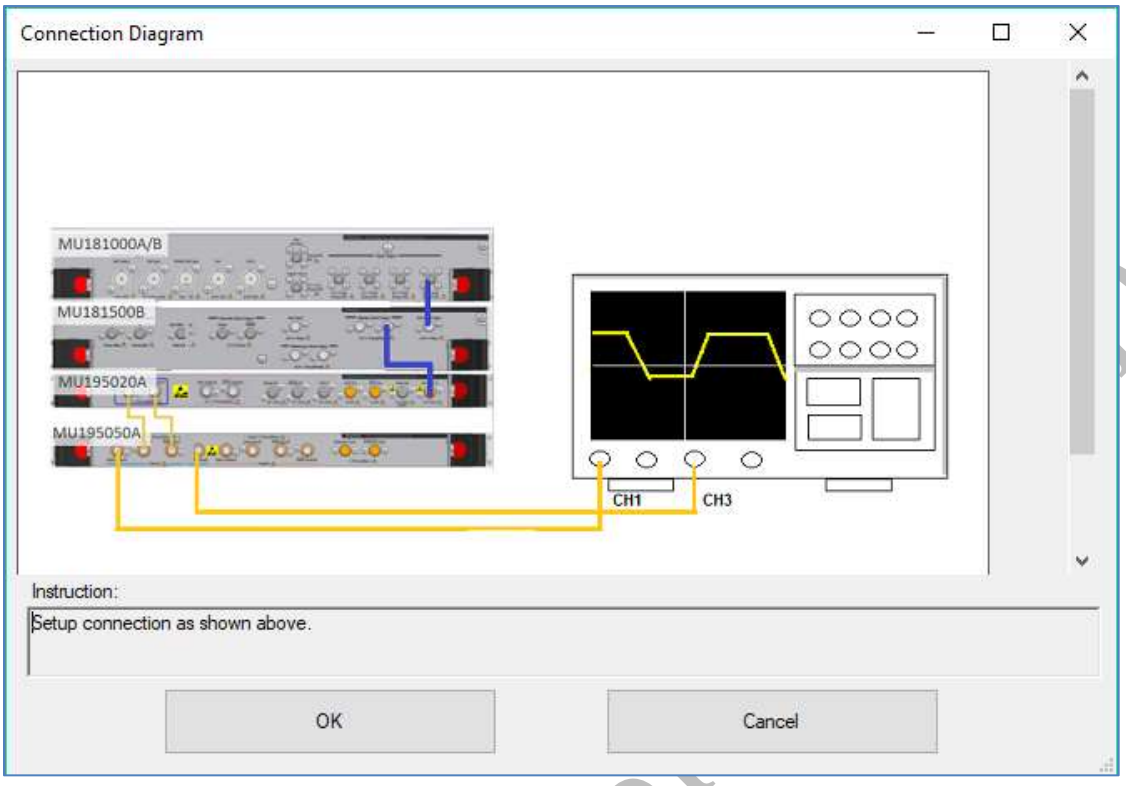

FIGURE 28. TP1 CONNECTION DIAGRAM DIALOG EXAMPLE

4.2 Calibration for TP2 (Output of Long Channel)

4.2.1 Setup for TP2 Calibration

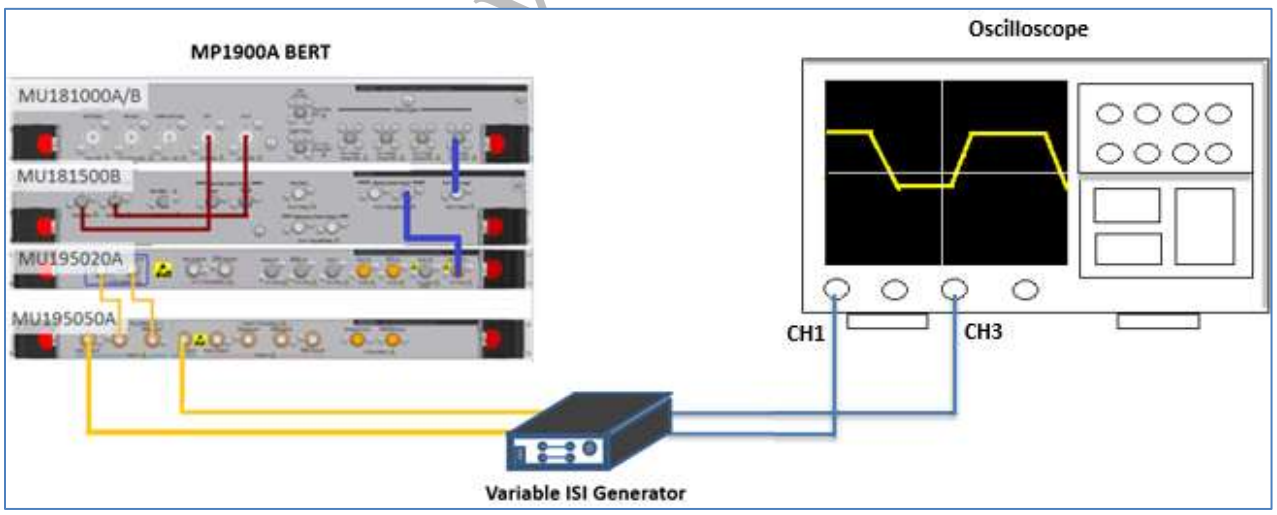

FIGURE 29. TYPICAL SETUP FOR TP2 CALIBRATION

Connection Steps:

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.

2. Connect the MU195050A data outputs to the inputs of the variable ISI generator.
3. Connect the ISI generator outputs to Channels 1 and 3 on the oscilloscope.

4.2.1.1 TP2 Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following TP2 calibration setup.

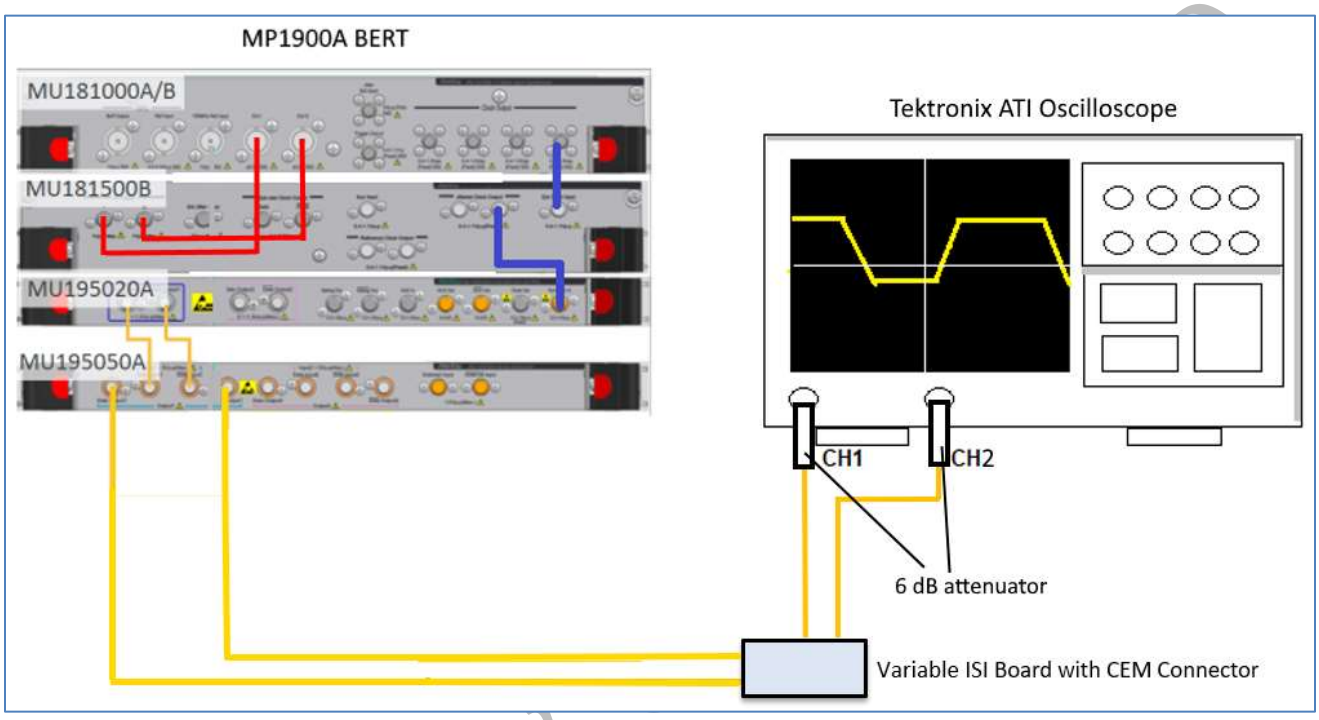

FIGURE 30. RECOMMENDED SETUP FOR TP2 CALIBRATION USING TEKTRONIX ATI SCOPE

*Note: Make sure that the "Tektronix Scope Configuration" is set to **Dual ATI** in the Configurations page (see Section 4.1.3).*

1. Using back the same BERT connections from the TP1 calibration in Section 4.1.1.1, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to the variable ISI board with the CEM connector.
3. Then connect the variable ISI to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.2.2 Run Calibration Steps at TP2

Repeat Section 4.1.2 to complete the selected calibration steps at TP2.

After calibrating the loss profile to be used by adjustment of de-emphasis; ISI measurement, CM Sinusoidal Interference, DM Sinusoidal Interference, Final ISI and SJ adjustments to achieve calibrated eye height and width, the final calibrated stressed Eye diagram is calculated by Seasim, and should look similar to the following example.

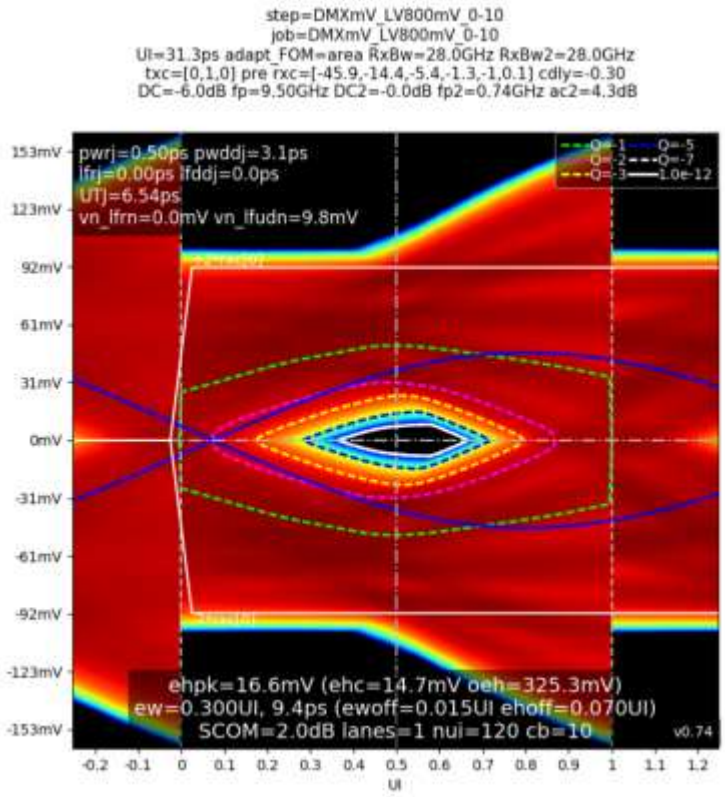

FIGURE 31. FINAL CALIBRATED STRESSED EYE DIAGRAM EXAMPLE

4.3 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for the RJ and CM calibration. To do this, select  from the menu to access the Calibration page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the Use Default Value checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

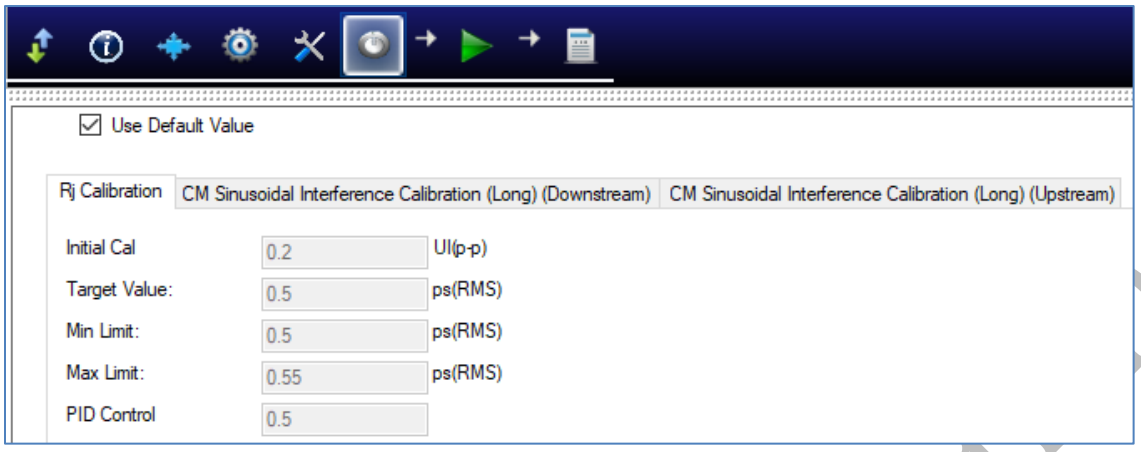

FIGURE 32. CALIBRATION TARGET OVERWRITE PAGE

5 Testing Using GRL-PCIE5-BASE-RXA Software

Once the final stressed eye has been calibrated successfully, receiver stress jitter voltage tolerance and margin testing can then be performed on the device under test (DUT). The DUT should have a Replica Channel of the same Insertion Loss as the Replica Channel used for calibration. The Replica Channel is removed when performing the DUT tests.

The GRL-PCIE5-BASE-RXA software automates the receiver compliance and jitter tolerance testing, at the spec-defined or user-defined jitter frequency steps. The GRL software also supports nested loop testing of multiple parameters to facilitate silicon PVT testing or testing across multiple test conditions. When testing is completed, the results will be logged in an aggregated test report which can be generated into a PDF format.

Receiver device compliance ensures the receiver DUT is able to correctly interpret data from a received signal with valid voltage and timing characteristics by achieving an acceptable bit error ratio (BER) of less than 1E-12. The signal used for verifying receiver tolerance must contain the maximum allowable jitter, noise and signal loss. The stressed receiver tolerance test should include various differential mode sinusoidal interference, minimum transmitter voltage amplitude and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

The receiver DUT can operate in the Common Clock (CC) Refclk and Independent Refclk (IR) clock modes. For the CC clock mode, a single Refclk source is applied for both the BERT signal generator and the DUT along with SSC and SJ mask.

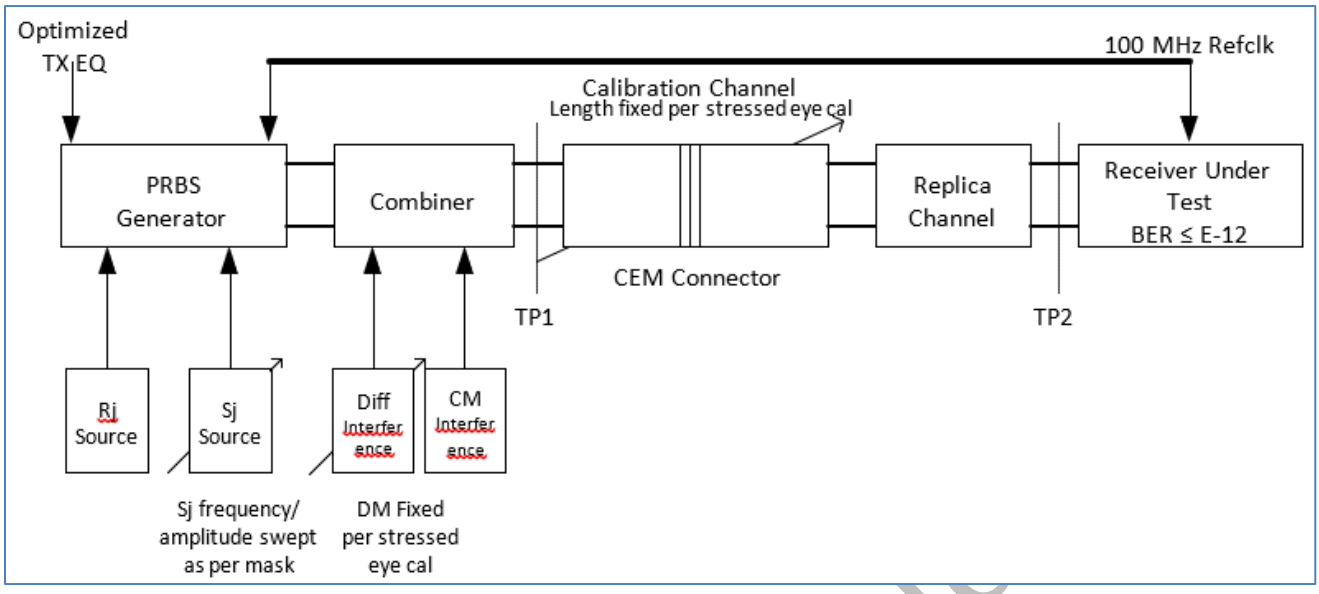

FIGURE 33. RX DUT STRESS JITTER TEST (CC MODE) BLOCK DIAGRAM FROM PCIE GEN 5 BASE SPECIFICATION

For the IR clock mode, two Refclk sources are applied for both the BERT signal generator and the DUT along with independent SSC and SJ mask.

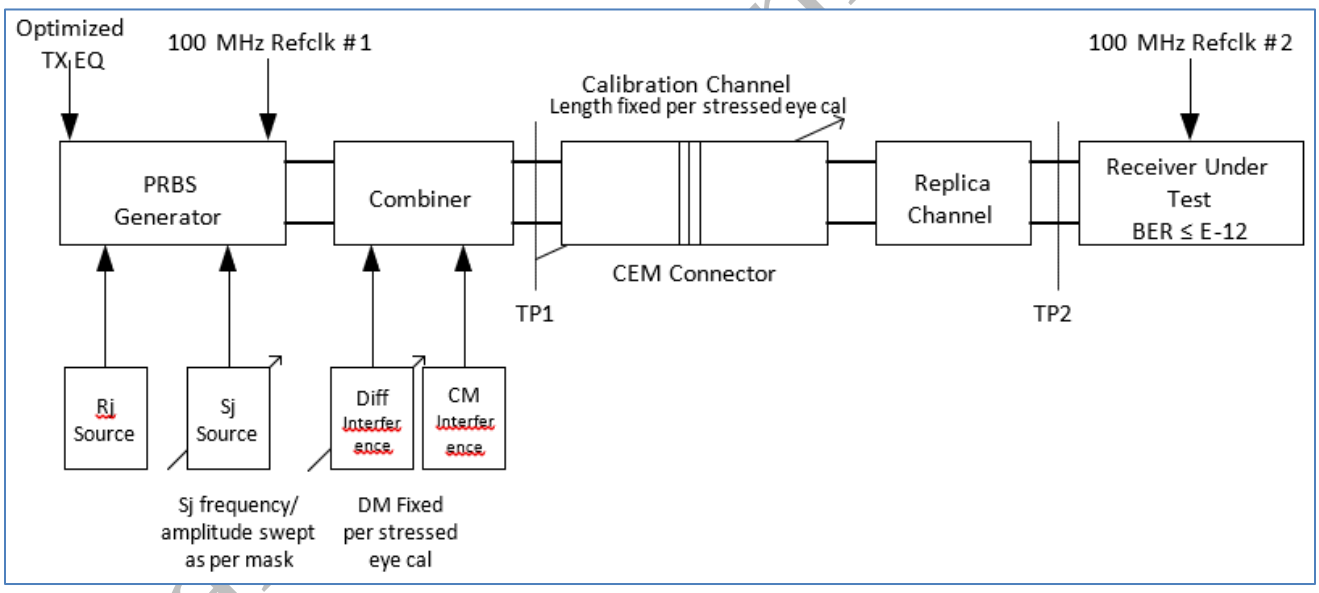

FIGURE 34. RX DUT STRESS JITTER TEST (IR MODE) BLOCK DIAGRAM FROM PCIE GEN 5 BASE SPECIFICATION

Once the stressed receiver tolerance test setup has been calibrated, the BERT will transmit a modified compliance pattern to the receiver and monitors the loopback pattern has a BER that is less than 1E-12.

5.1 Receiver DUT Compliance Test Setup

5.1.1 Test Setup

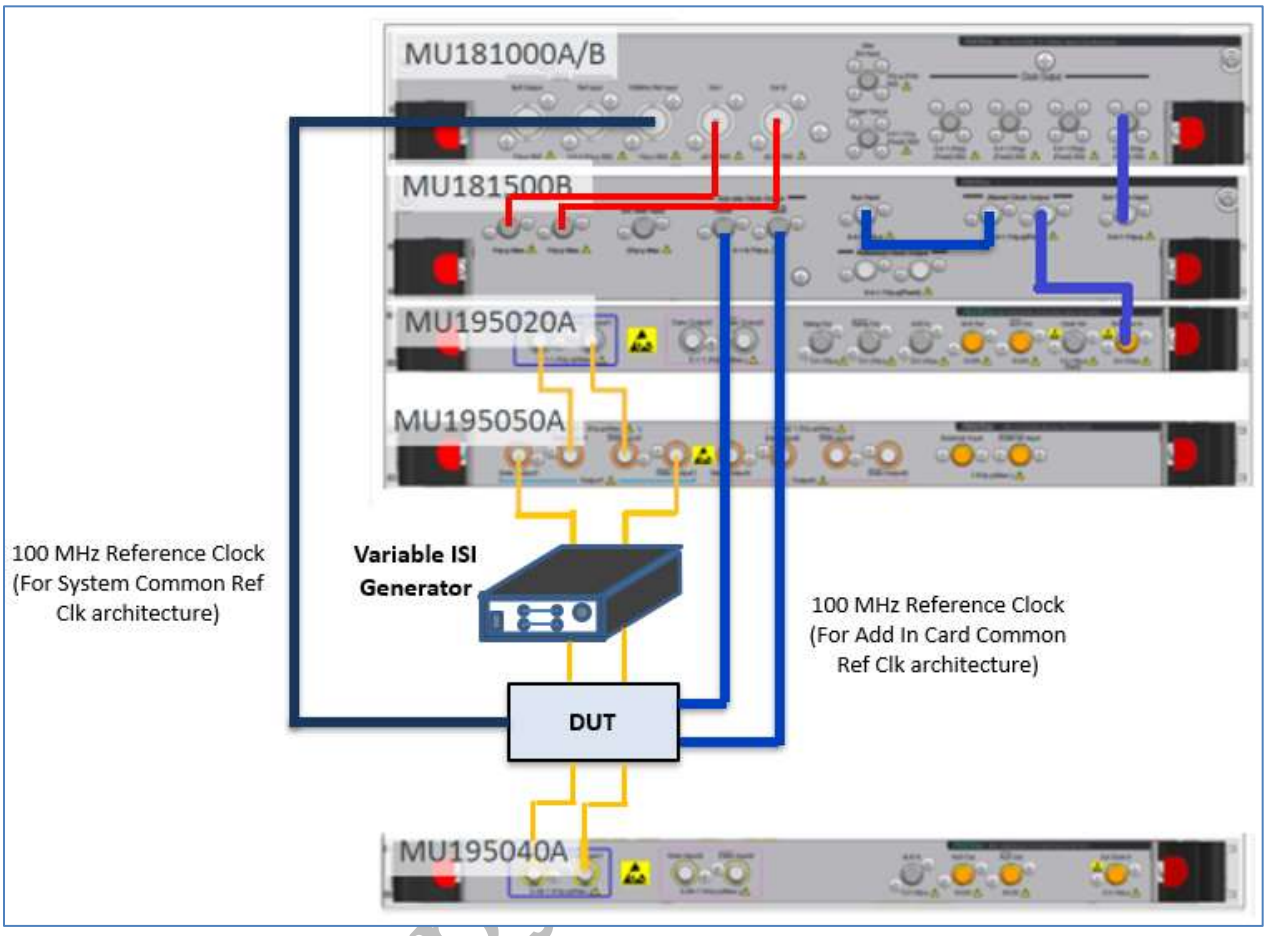

FIGURE 35. TYPICAL RECEIVER DUT TEST SETUP

Connection Steps:

1. Using back the same BERT connections from calibration, remove the oscilloscope connections from the ISI generator.
2. Connect the jittered clock output to the Aux input on the MU181500B using a SMA-SMA short cable.
3. Using phase matched K-K coaxial cables, connect the ISI generator outputs to the DUT Rx inputs.
4. ***If using an Add-in card DUT***, connect the MU181500B sub-rate clock outputs to the Ref Clk+/- of the DUT using coaxial cables.
5. ***If using a System DUT***, connect the Ref Clk of the DUT to the 100 MHz Ref Input on the MU181000A/B with a BNC cable.
6. Using phase matched K-K coaxial cables, connect the DUT Tx outputs to the MU195040A data inputs for loopback error detection.

5.1.2 Receiver Compliance Tests

In the following diagram, **Stress Jitter Voltage** tests are selected if tests at the Compliance Jitter Limits are to be performed.

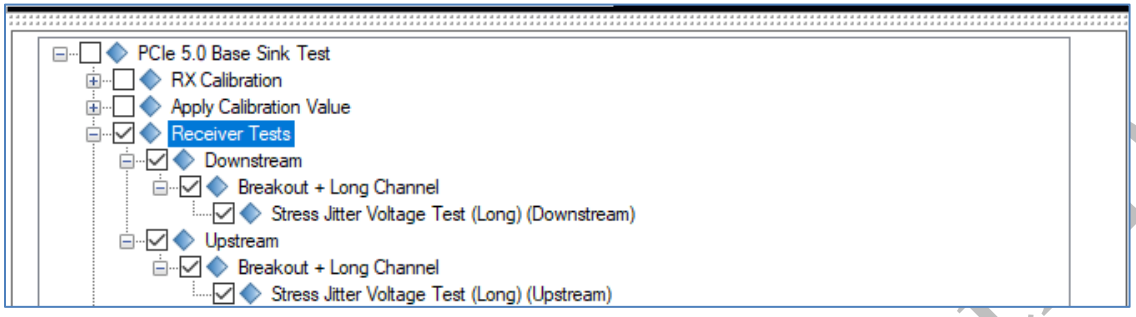

FIGURE 36. SELECTING RECEIVER COMPLIANCE TESTS

Once eye height and eye width have been calibrated, the Rx DUT will be connected to the far end of the calibration channel for testing. Optimization for the transmitter equalization will then be performed (equalization must also be optimized for the Rx DUT as well). SJ will be set to an initial value of 0.1 UI at 100 MHz that allows the receiver CDR to achieve lock which will then be swept over a frequency range of 400 kHz to 100 MHz, while maintaining fixed Tx equalization. The 100 MHz SJ initial tone will then be removed to perform testing for the appropriate swept SJ profile.

Note that an additional SJ tone at 210 MHz shall be present for all testing at 32 GT/s, while having the same amplitude as the 100 MHz SJ to achieve the target eye width minus 0.1 UI. This is not required if the SJ calibration is less than 0.1 UI.

The DUT must achieve a compliance BER of 10E-12 or lower for the entire swept SJ range. The Rx DUT is tested using an SJ mask in the 400 kHz to 100 MHz range and the 33 kHz single tone magnitude of 25 ns pp.

The stress jitter voltage tests are run from the same screen as shown in Figure 27.

5.1.3 Receiver Margin Tests

In the following diagram, **Stress Jitter Voltage Margin** tests are selected if Jitter Margin testing is to be performed.

FIGURE 37. SELECTING RECEIVER MARGIN TESTS

The marginal tests are run from the same screen as shown in Figure 27.

5.1.4 Apply Calibrated Values for Testing

Calibrated values from the stressed jitter voltage calibration can be used in the DUT Rx tests. To apply these values, select **Apply Stress Voltage Param**.

FIGURE 38. SELECTING TO APPLY CALIBRATION VALUES

5.2 Enable Loopback BER Test

To set up the GRL software to automate loopback testing for error detection, go to the Configurations menu and set up the following settings. *Make sure that the Rx DUT is capable of supporting loopback mechanism for BER measurements.*

1. Under the Error Counter tab, select 'LoopBack' to enable loopback test mode for the DUT (refer Section 3.2.3.9).
2. Under the Loopback Mode tab, select 'Clock Recovery' in the Clock Recovery Method field to apply the clock data recovery function to process the modified compliance pattern generated by the DUT (refer Section 3.2.3.10). Then, set the value for the Clock Recovery Loop Bandwidth by selecting 'Manual' or simply use the default 'Jitter Tolerance' values.

   If using a user-defined pattern instead of the default test pattern for error checking, select the 'Custom Pattern for Error Detector' checkbox. Then, select the type of custom test pattern to be used.
3. Under the Error Detector Settings tab, choose to enable or disable CTLE and SKP OS symbol filtering as required in BER testing (refer Section 3.2.3.11).
4. If needed to change the default spec-defined limits for the target BER and maximum error allowed for BER measurements, then select the Compliance tab and define new values (refer Section 3.2.3.12).

6 Interpreting Test Report

The **Report** page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

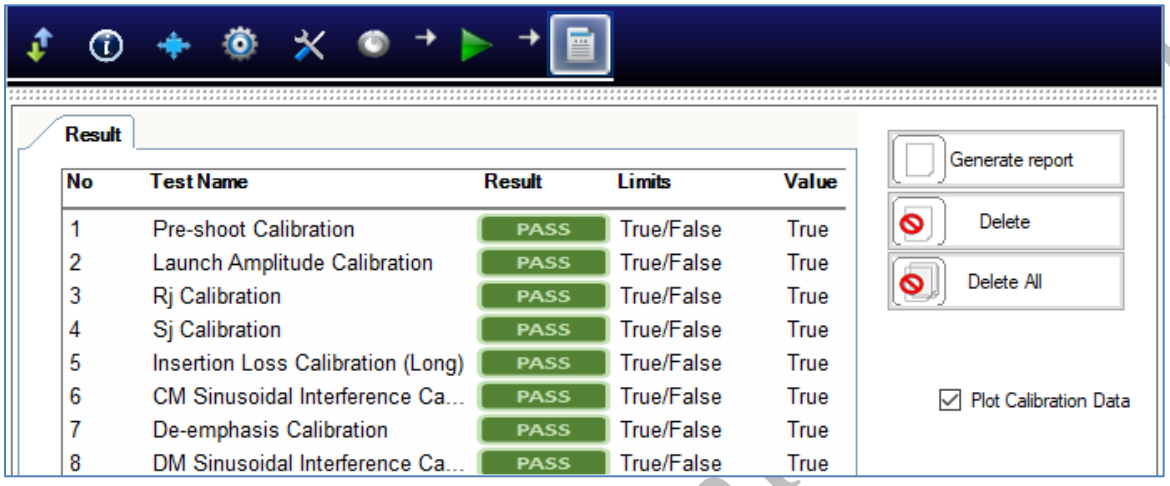

FIGURE 39. REPORT RESULTS PAGE

6.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.

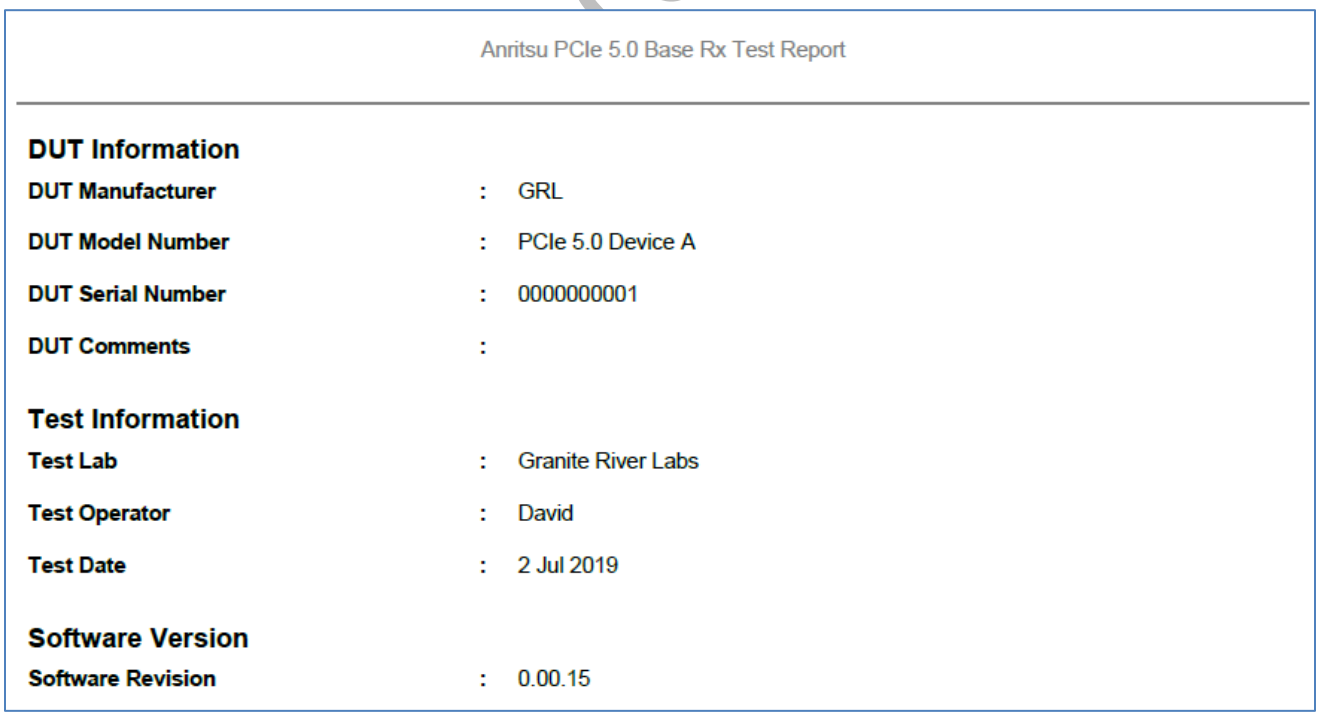

FIGURE 40. DUT INFORMATION

6.2 Summary Table

This portion is populated from the tests performed and its results. This gives an overall view of all the results and its test conditions.

No	TestName	Limits	Value	Results	SJ
1	Pre-shoot Calibration	N/A	N/A	Pass	
2	De-emphasis Calibration	N/A	N/A	Pass	
3	Launch Amplitude Calibration	N/A	N/A	Pass	
4	Rj Calibration	N/A	N/A	Pass	
5	Sj Calibration	N/A	N/A	Pass	SJLF_1
6	Sj Calibration	N/A	N/A	Pass	SJLF_2
7	Sj Calibration	N/A	N/A	Pass	SJLF_3
8	Sj Calibration	N/A	N/A	Pass	SJLF_4
9	SJ Tone Calibration	N/A	N/A	Pass	
10	ISI Calibration (Long) (Downstream)	N/A	N/A	Fail	
11	CM Sinusoidal Interference Calibration (Long) (Downstream)	N/A	N/A	Pass	
12	DM Sinusoidal Interference Calibration (Long) (Downstream)	N/A	N/A	Pass	
13	Stressed Jitter Voltage Calibration (Long) (Downstream)	N/A	N/A	Pass	
14	ISI Calibration (Long) (Upstream)	N/A	N/A	Pass	
15	CM Sinusoidal Interference Calibration (Long) (Upstream)	N/A	N/A	Pass	
16	DM Sinusoidal Interference Calibration (Long) (Upstream)	N/A	N/A	Pass	
17	Stress Jitter Voltage Calibration (Long) (Upstream)	N/A	N/A	Pass	
18	Apply Stress Voltage Param (long) (Downstream)	N/A	N/A	Pass	
19	Stress Jitter Voltage Test (Long) (Downstream)	N/A	N/A	Fail	SJLF_1
20	Stress Jitter Voltage Test (Long) (Downstream)	N/A	N/A	Fail	SJLF_2
21	Stress Jitter Voltage Test (Long) (Downstream)	N/A	N/A	Fail	SJLF_3
22	Stress Jitter Voltage Test (Long) (Upstream)	N/A	N/A	Fail	SJLF_1
23	Stress Jitter Voltage Test (Long) (Upstream)	N/A	N/A	Fail	SJLF_2
24	Stress Jitter Voltage Margin Test (Long) (Downstream)	N/A	N/A	Fail	SJLF_1
25	Stress Jitter Voltage Margin Test (Long) (Downstream)	N/A	N/A	Fail	SJLF_2

FIGURE 41. SUMMARY TABLE

6.3 Calibration Data Results

If Plot Calibration Data checkbox is checked, then the plots are shown in this part of the report.

3. Launch Amplitude Calibration

Pass/Fail Stats	:	Pass
Cal Parameter	:	LaunchVoltage
Target	:	800mV
Test completed time	:	19 6□ 2019 15:09:53 □□

PCIEBaseGeneratorLaunchVoltageCal Plot

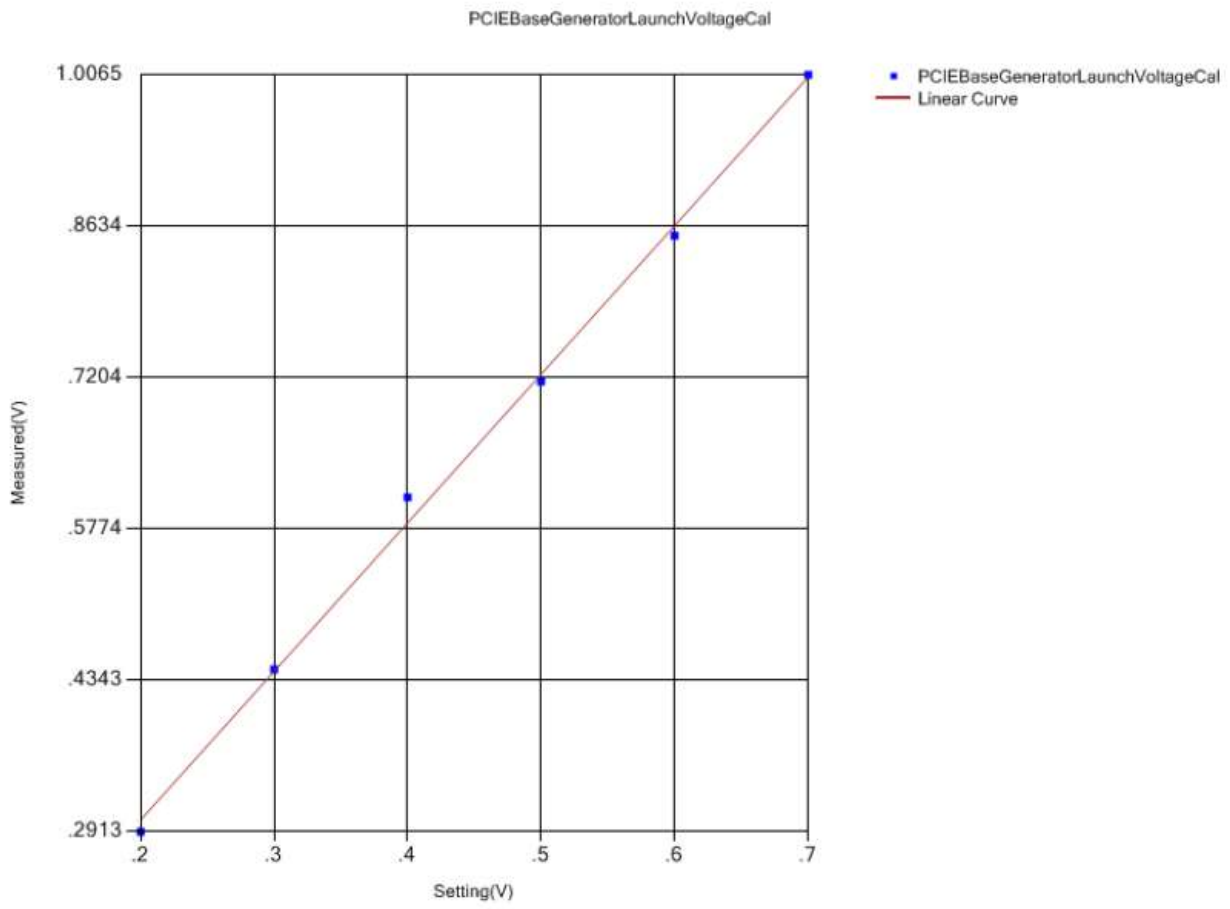

FIGURE 42. CALIBRATION RESULTS EXAMPLE

6.4 Compliance Test Results

22. Stress Jitter Voltage Test (Long) (Upstream) [SJLF_1]

Pass/Fail Stats	:	Fail
Test Frequency	:	30 KHz
ISI Generator	:	PCIE ISI Board
Preshoot (dB)	:	0 (0.26)
DeEmphasis (dB)	:	-6 (-6.74)
RJ (ps RMS)	:	0.5 (0.188)
SJ (ps)	:	31.25 (1)
Amplitude (mV)	:	740 (510)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	13.46(21.17)
CM Freq (MHz)	:	120.0
CMSI (mV)	:	150 (170.390)
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	4.44E-16 (0)
Max Error Allowed	:	0
Error Counts	:	234
Test completed time	:	10 7□ 2019 7:57:20 □□

FIGURE 43. COMPLIANCE TEST RESULTS EXAMPLE

6.5 Margin Test Results

24. Stress Jitter Voltage Margin Test (Long) (Downstream) [SJLF_1]		
Pass/Fail Stats	:	Fail
Preshoot (dB)	:	0 (0.26)
DeEmphasis (dB)	:	-6 (-6.74)
RJ (ps RMS)	:	1 (0.54)
Amplitude (mV)	:	800 (550)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	5 (7.69)
CM Freq (MHz)	:	120.0
CMSI (mV)	:	150 (170.724)
ISI Generator	:	PCIE ISI Board
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	4.440E-16 (0)
Sj Specs	:	31.25 ps
Max Error Allowed	:	0
Last Passing Sj	:	31.2500 ps
Test completed time	:	10 7□ 2019 8:53:15 □□

FIGURE 44. MARGIN TEST RESULTS EXAMPLE

7 Saving and Loading Test Sessions

The GRL-PCIE5-BASE-RXA software enables calibration and test results to be created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test Session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To save a session, with all of the parameter information, the test results, and any waveforms, select the "Options" drop-down menu, then the "Save Session" option.
- To load a session back into the software, including the saved parameter settings, select the "Options" drop-down menu, then the "Load Session" option.
- To create a New session and return the application back to a default configuration, select the "Options" drop-down menu, then the "New Session" option.

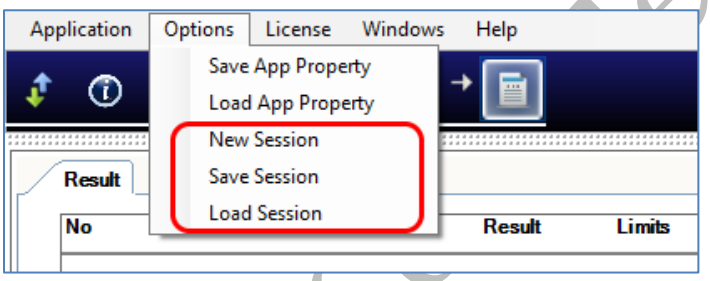

FIGURE 45. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

8 Appendix A: Method of Implementation (MOI) Using Automation

This section provides sample methodology to automate PCIe Gen 5 Base Rx calibration using GRL-PCIE5-BASE-RXA software at 32 GT/s. This procedure will ensure Receiver Impairment adjustments on the MP1900A BERT are accurate before running DUT compliance tests.

8.1 Perform Calibration at TP1

8.1.1 Pre-shoot Calibration

The **Caltable** method is used to calibrate pre-shoot:

1. Set 800mV (p-p) amplitude on BERT.
2. Set 0dB for De-emphasis on BERT.
3. Measure:

   1dB at BERT, then measure Pre-shoot, record
   2dB at BERT, measure again, record
   3dB at BERT, measure again, record
   .....
   5dB at BERT, measure again, record.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured Pre-shoot at 1dB Min and Max 4dB.

8.1.2 De-emphasis Calibration

The Caltable method is used to calibrate De-emphasis:

1. Set 800mV (p-p) amplitude on BERT.
2. Set 0dB for Pre-shoot on BERT.
3. Measure:

   -8dB at BERT, then measure De-emphasis, record
   -7dB at BERT, measure again
   -6dB at BERT, measure again
   .....
   0dB.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured De-emphasis at -1dB Min and Max -6dB.

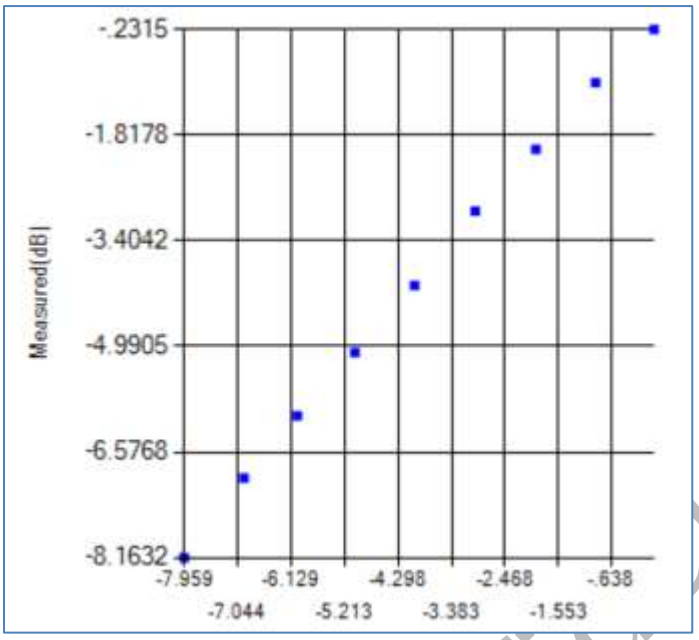

FIGURE 46. DE-EMPHASIS CALIBRATION CALTABLE GRAPH

8.1.3 Launch Amplitude Calibration

The Caltable method is used to calibrate Launch Amplitude:

1. Initialize BERT.
2. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
3. Set 300mV Amplitude at BERT, then measure the amplitude in scope, record it.
4. Increase 100mV on each iteration, measure the amplitude in scope, until measured amplitude meets or exceeds 1200mV.
5. Plot a Caltable graph.
6. Passing criteria is to obtain MEAN value of Launch Amplitude measurement at 720-800mV.

8.1.4 RJ Calibration

The Caltable method is used to calibrate RJ:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set Initial RJ value to 0.04UI(p-p) on BERT.
7. Measure RJ (in ps (RMS)) from scope using EZJIT, record the measured value.
8. Increase 0.1UI (p-p) on each iteration, measure RJ from scope, until measured RJ meets or exceeds 1.0ps (RMS).
9. Plot a Caltable graph.
10. Passing criteria is to obtain measured RJ at 1.0 ps (RMS).

8.1.5 SJ Calibration

The Caltable method is used to calibrate SJ:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set the SJ Frequency of the first Permutation (33KHz, 1MHz, 10MHz, 100MHz).
7. Set 0 (%UI (p-p)) as base value in SJ, measure SJ (in ps (p-p)) from scope using EJZIT, record.
8. Increase 0.1UI (p-p) on each iteration for SJ Frequency 1MHz, 10MHz, 100MHz; Increase 0.2UI (p-p) on each iteration for SJ Frequency 33KHz.
9. Measure SJ from scope until measured SJ meets or exceeds 62.5ps for 33KHz SJ Frequency or 20.0ps for SJ Frequency 1MHz, 10MHz, 100MHz.
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 6ps (p-p) and Max 62.5ps (p-p) for 33KHz, 20.0ps (p-p) for 1MHz, 10MHz, 100MHz.
12. Proceed to next permutation.

8.1.6 SJ Tone Calibration

The Caltable method is used to calibrate SJ Tone:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set SJ2 Frequency (210MHz).
7. Set 0 (%UI (p-p)) as base value in SJ2, measure SJ (in ps (p-p)) from scope using EJZIT, record.
8. Increase 0.1UI (p-p) on each iteration.
9. Measure SJ from scope until measured SJ meets or exceeds 10ps (p-p).
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 5ps (p-p) and Max 10ps (p-p).

8.2 Perform Calibration at TP2

Calibration at TP2 can be performed for Downstream (for Host) or Upstream (for Device).

8.2.1 ISI Calibration (CEM Connector Channel + Replica Channel) *[Applicable only if CTS version '1.0' is being used as the measurement reference method AND supported ISI Generator of either PCIe ISI Board or Artek is used.]*

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set Clk/256 Pattern on BERT.
6. Start with PCIe CEM Variable ISI board Lane 3.
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (start from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain .log file and .csv file from Seasim.
13. Record insertion loss at 16GHz in dB from .csv file. Check against upper and lower specification limits.
14. If insertion loss at 16GHz is above 34-37dB, decrease Lane number and repeat steps 7 to 13.
15. If insertion loss at 16GHz is below 37dB, increase Lane number and repeat steps 7 to 13.
16. Insertion loss (IL) profile curve will be generated to determine Lane number that corresponds to 34dB, 35dB, and 37dB losses for use in next step of calibration.

8.2.2 Common Mode (CM) Sinusoidal Interference Calibration

The Caltable method is used to calibrate CM-SI:

1. Insert ISI trace at 36dB loss from previous calibration step.
2. Initialize BERT.
3. Set 0mV (p-p) amplitude.
4. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
5. Set All Stress to 0mV.
6. Set Frequency on BERT for Common Mode to 120MHz.
7. Set Output on BERT for Common Mode to 20mV, turn On Output.
8. Turn Off Output on BERT for Differential Mode.
9. Initialize scope.
10. Set up Func1 on scope to (Chan1 + Chan3)/2.
11. Measure Vp-p on Func1.
12. Record measured Phase.
13. Set 800mV (p-p) amplitude (based on calibrated value).
14. Set All Zero Pattern on BERT.
15. Set ISI % value based on above calibrated data.
16. Set BERT (Common Mode) to Sine Wave.

17. Measure Amplitude (in mV) from scope, record.
18. Increase 0.174dBm/20mV on each iteration, measure Amplitude from scope until measured value meets or exceeds 150mV.
19. Plot a Caltable graph.
20. Passing criteria is to obtain measured CM-SI at Min 100mV and Max 150mV.

8.2.3 Differential Mode (DM) Sinusoidal Interference Calibration

This calibration is to ensure that the waveform achieves the calibrated eye height.

The Caltable method is used to calibrate DM-SI:

1. Insert ISI trace at 36dB loss from calibration step of Section 8.2.1.
2. Initialize BERT.
3. Set 0mV (p-p) amplitude.
4. Set BERT to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
5. Set All Stress to 0mV.
6. Set Frequency on BERT for Differential Mode to 2.1GHz.
7. Set Output on BERT for Differential Mode to 10mV, turn On Output.
8. Turn Off Output on BERT for Common Mode.
9. Initialize scope.
10. Set up Func1 on scope to (Chan1 – Chan3).
11. Measure Vp-p on Func1.
12. Measure Amplitude (in mV) from scope, record.
13. Increase 0.174dBm/10mV on each iteration, measure Amplitude from scope until measured value meets or exceeds 30mV.
14. Plot a Caltable graph.
15. Passing criteria is to obtain measured DM-SI at Min 10mV and Max 40mV.

8.2.4 Stress Jitter Voltage Eye Calibration

This calibration is to ensure that the waveform achieves the calibrated eye width and eye height.

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set All Stress to 0mV.
4. Set Clk/256 Pattern on BERT.
5. Start with ISI traces of 37dB.
6. Trigger waveform on scope to display waveform.
7. Embed waveform with reference package s4p.
8. Save waveform to .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 5). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for Eye Opening calculation, starting with 0mV DM-SI.
11. Run Seasim with config file and step response.
12. Obtain .log file from Seasim.

13. Read eye height (EH) and eye width (EW).
14. Record EH vs. DM, and EW vs. DM for 800mV.
15. Increase DM-SI (in Seasim config) to 15mV, run Seasim again, obtain EH and EW.
16. Once EH and EW at 5, 15mV are obtained, plot Caltable graph and adjust DM setting needed to achieve 0.3UI and 15mV EH and EW.
17. If adjusted DM setting is out of range, increase/decrease SJ by 0.02UI. Repeat method to obtain EH and EW by adjusting DM.
18. If EH and EW do not fall within 0.3UI and 15mV after SJ variation, reduce ISI by 1dB up to 34dB and repeat steps 15 to 17.
19. If EH and EW still do not fall within specifications, return to starting ISI trace of 37dB while adjusting Amplitude and reducing ISI if necessary.
20. Repeat until EW and EW fall within specifications.
21. Record measured Amplitude, SJ, and DM.

9 Appendix B: Artek CLE Model Series Installation

9.1 ISI Generator Driver Installation

If using a Artek CLE Model unit for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the Artek unit to the PC being used as the controller using a USB 2.0 cable.
2. Turn on the front panel power switch on the Artek unit.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for Artek has been installed, you will see a 'bang' in the Device Manager.

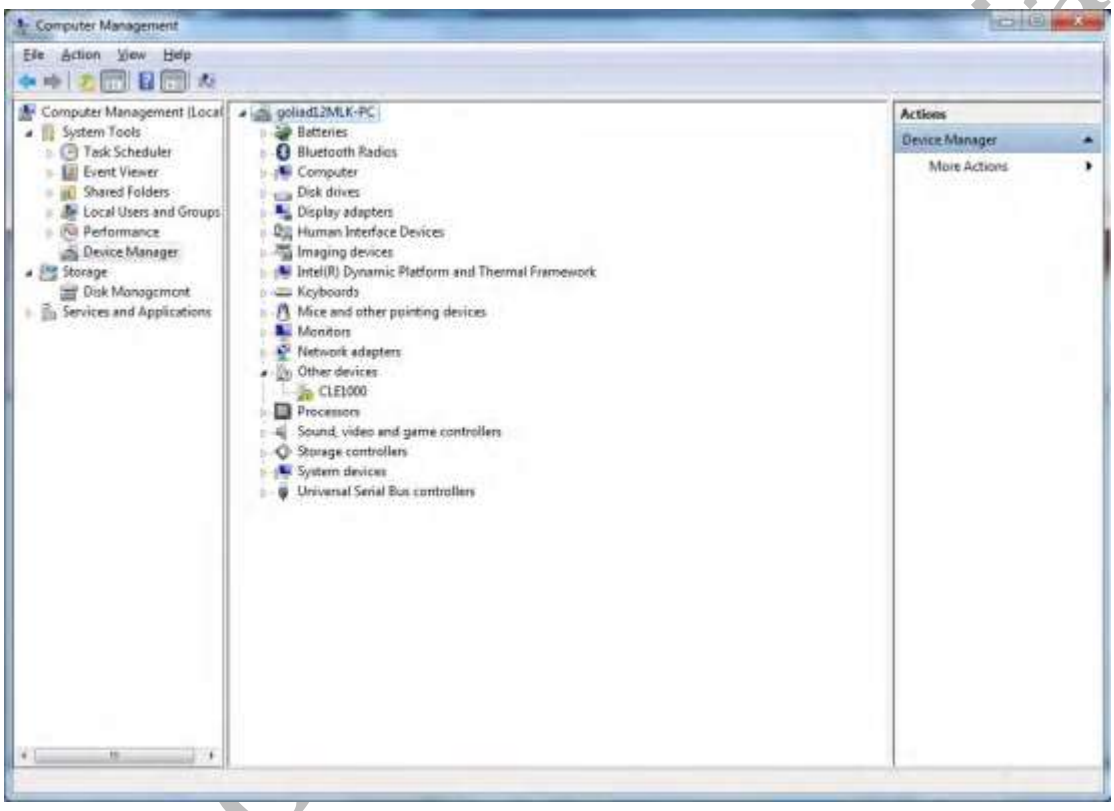

FIGURE 47. DEVICE MANAGER WINDOW

4. To install the Artek driver, go to http://www.aceunitech.com/support.html and download the Control Software package for the Artek CLE Series.
5. Unpack the CLE Series Software .zip file.
6. Install the CLE Series Driver:
   a) In Device Manager, right-click on **CLExxxx > Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 48.
   c) Browse to the root directory of the unzipped CLE Series Software folder.
   d) Click **Next**. You will be asked to confirm your request to install a driver. See Figure 49.
   e) Click **Install**. The driver software will complete the installation.
7. Once installation has completed, the Device Manager should look like Figure 50.

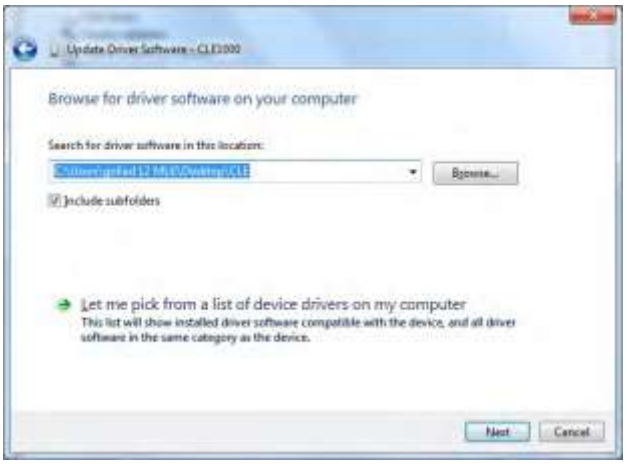

FIGURE 48. UPDATE DRIVER WINDOW

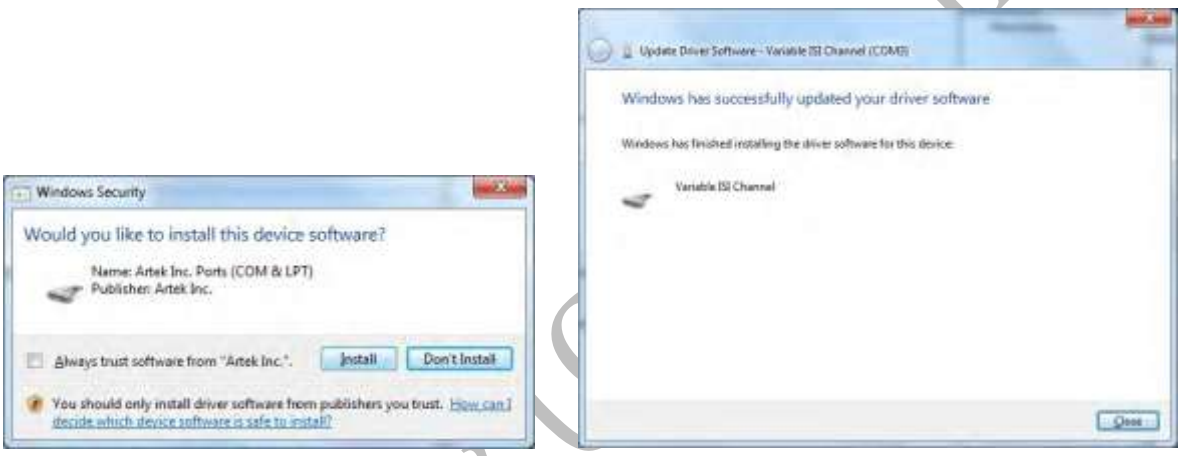

FIGURE 49. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

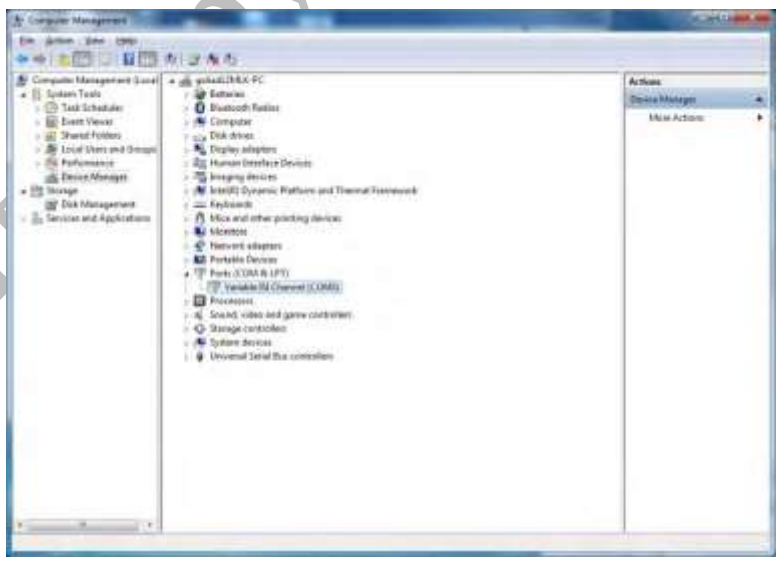

FIGURE 50. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE Series software driver is now installed and the Artek unit can now be selected for use remotely using the GRL software.

9.2 CLE Series GUI Installation

It may also be useful to install the CLE Series GUI, so that the ISI channel can also be controlled manually from the PC. To install the software, do the following:

1. In the CLE Series Software folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you do not want to have manual control.

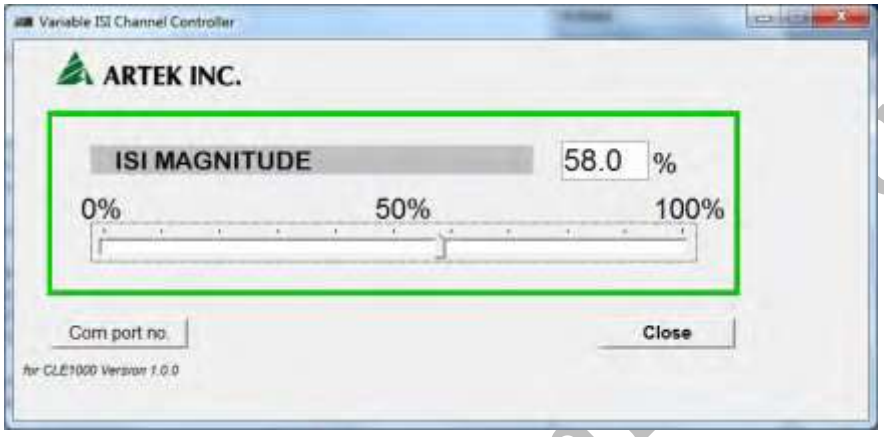

FIGURE 51. CLE SERIES GUI

10 Appendix C: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

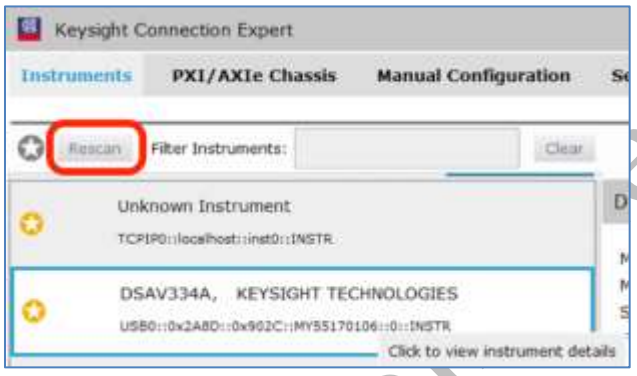

FIGURE 52. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

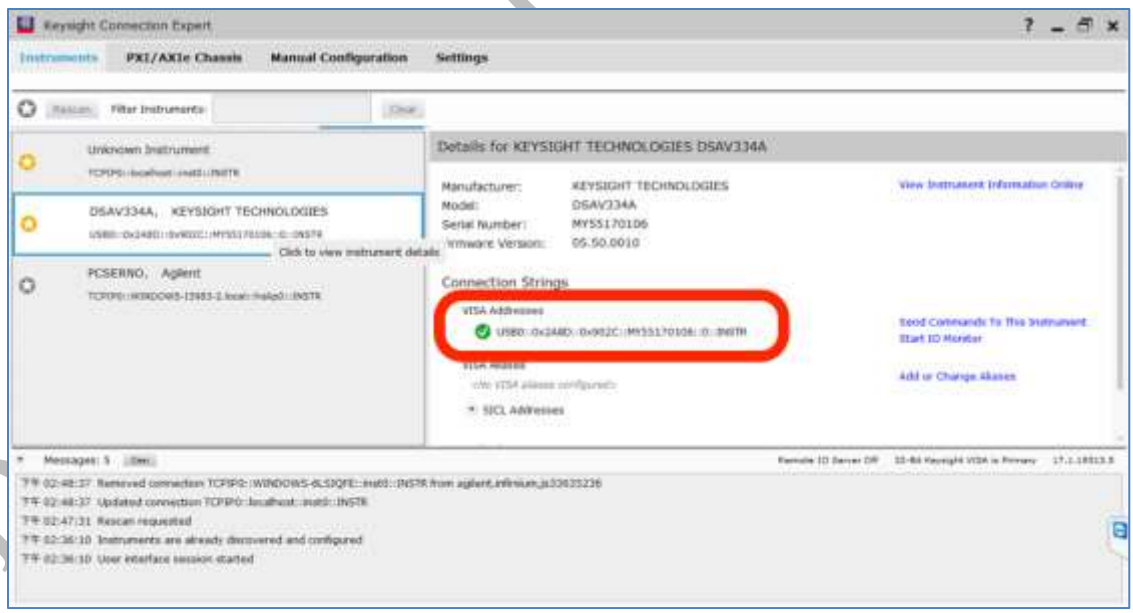

FIGURE 53. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe 5.0 Base Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

11 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

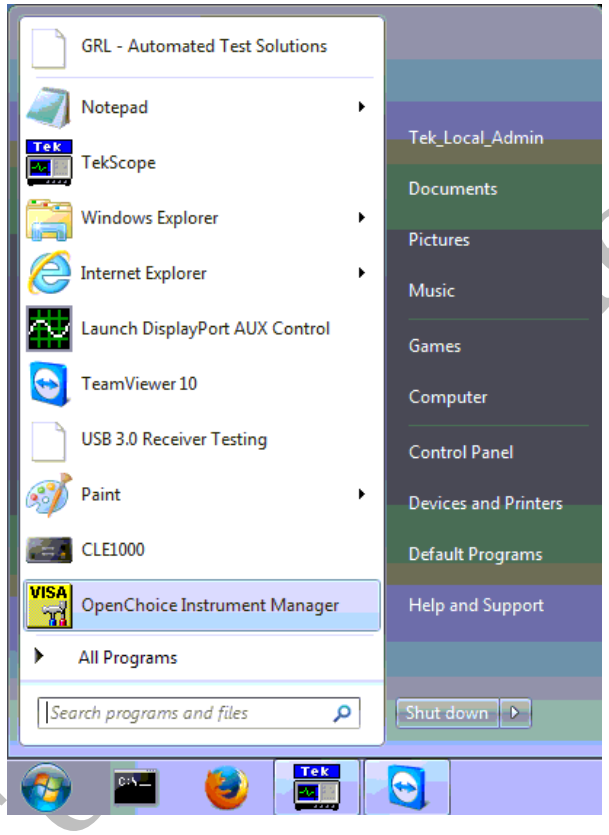

FIGURE 54. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

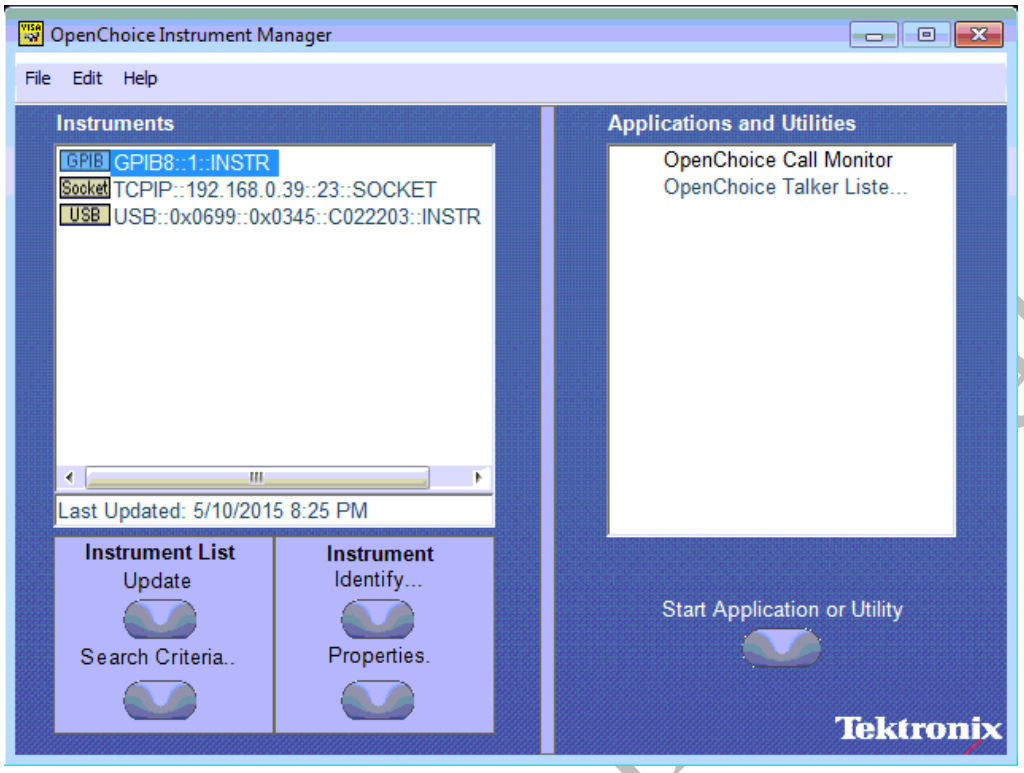

FIGURE 55. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe 5.0 Base Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe 5.0 Base Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

END_OF_DOCUMENT