Granite River Labs

GRL-PCIE4-CEM-RXA PCI Express Card Electromechanical (CEM) 4.0 (16 GT/s & 8 GT/s) Receiver Compliance Test Automation Solution User Guide and MOI

Using GRL-PCIE4-CEM-RXA Automation Test Software, Anritsu MP1900A BERT, and High Performance Oscilloscope

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1 Introduction

This user manual provides information using the GRL-PCIE4-CEM-RXA test automation solution to set up and test an electrical receiver (Rx) device to meet PCI Express Card Electromechanical (CEM) 4.0 compliance (for 16 GT/s and 8 GT/s) as per PCI Express (PCI-SIG) Standards.

The main body of this documentation first describes how to configure the GRL-PCIE4-CEM-RXA test software to calibrate the stressed eye at the receiver of the device under test (DUT) in the PCIe Gen 4.0 or Gen 3.0 system. This includes calibration to be performed at both the physical Test Point 1 (TP1) and the Long Channel at TP2. The GRL software will automate calibration without channel effect at TP1 before measuring the eye opening due to trace length. It also enables running the SigTest post processing analysis application to ensure signal quality compliance.

After completing calibration, the GRL-PCIE4-CEM-RXA software will automate compliance testing for the receiver using Bit Error Ratio (BER) as a metric. The receiver path is tested with worst case eye to ensure a BER of less than 1E-12 can be achieved. The software also provides an optional SJ margin search test for the DUT.

The GRL-PCIE4-CEM-RXA software performs test automation according to PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes and Anritsu BERT using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's). The GRL software is run from the computer or oscilloscope to provide automation control to test the DUT for PCIe Gen 3 & 4 CEM Rx electrical compliance (including PCIe U.2 & M.2 calibration/testing for 8 GT/s). When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

Note: For manual test methodology, refer to Appendix of this documentation or PCI-SIG for approved Method of Implementation (MOI's) as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS AND ACCESSORIES

System & Accessory	Qty.	Description/Key Spec Requirement
High Performance Real-time Oscilloscope[a]	1	≥ 25 GHz bandwidth[b]
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer[c] • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator, or MU196020A 64.2G bit/s or 64.2G baud PAM4 Pulse Pattern Generator[d] • MU195040A 21G/32G bit/s SI Error Detector • MU195050A Noise Generator
PCI-SIG Compliance Base Board (CBB) or PCI-SIG Compliance Load Board (CLB)	1	For add-in cards For host system boards
[Optional for PCIe Gen 3 CEM (8 GT/s):] PCI-SIG U.2 (SFF-8639) or M.2 Key-M Compliance Base Board (CBB) or PCI-SIG U.2 (SFF-8639) or M.2 (Socket-3) Compliance Load Board (CLB)	1	For PCIe Gen 3 add-in cards For PCIe Gen 3 host system boards
ISI Source Generator	1	Compliant Variable ISI channel
Power Divider	2	Anritsu K240C 2-Way Resistive Power Divider, for connecting scope to CLB Tx lanes to perform link equalization tests
Terminator	2	Anritsu J1632A Coaxial Terminator, for termination of the unused MU195020A/MU196020A Aux Out connector and the CLB during link equalization testing
Power Supply	1	ATX Power Supply, for DUT power

System & Accessory	Qty.	Description/Key Spec Requirement
V(m) – K(f) Adapter	*2*	*34VKF50A Coaxial Adapter, only required if using a PAM4 Pulse Pattern Generator*
Computer (laptop or desktop)	1	Windows 7+ OS (For automation control)

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

[c] MU181000B Option 02 is required for testing the System Board DUT.

[d] The GRL-PCIE4-CEM-RXA software supports PAM4 PPG in NRZ mode.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable[a]	Qty.
1-meter SMA coaxial cables	6 pairs
SMA-to-SMP adapters (included with CLB/CBB test fixture kits)	2 pairs
1-ft SMP-to-SMP cables (included with CLB/CBB test fixture kits)	2 pairs
Phase-matched K-K coaxial cables	1 pair
SMA-to-SMA cables	4
BNC cables	2
J1627A GND connection cable	1
LAN cable	1

[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
GRL-PCIE4-CEM-RXA[a]	Granite River Labs PCI Express Card Electromechanical 4.0 (16 GT/s & 8 GT/s) Automated Receiver Calibration and Compliance Test Solution – www.graniteriverlabs.com/download-center

Software	Description/Source
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-PCIE4-CEM-RXA software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
MX183000A	Anritsu High-Speed Serial Data Test Software – For loopback BER testing of the PCIe Gen ¾ CEM DUT receiver. This software is located in the MP1900A BERT.
SigTest Application	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html

[a] *PCIe3-CEM and PCIe4-CEM will need to be installed to test at both 16 GT/s and 8 GT/s data rates. If the GRL-PCIE4-RXA test solution is purchased, the user will need to install the GRL-PCIE4-BASE-RXA and GRL-PCIE4-CEM-RXA solutions included in the package to perform testing for PCIe4-BASE and PCIe4-CEM at 16 GT/s and 8 GT/s.*

3 PCIe Gen 3 & 4 CEM Rx CTS Calibration and Testing

The following table summarizes the differences in calibration and DUT compliance testing configuration between PCIe Gen 3 (8.0 GT/s) and Gen 4 (16.0 GT/s) CEM Rx systems based on the latest Compliance Test Specifications (CTS) requirements.

(Note: The latest CTS being used here is referring to the 'PCI Express Architecture PHY Test Specification Rev 4.0, Nov 8, 2018' version. The calibration and test methodology will be different between PCIe Gen 3 and Gen 4; please refer to the CTS for detailed requirements.)

TABLE 4. PCIE GEN ¾ CTS REQUIREMENTS – CALIBRATION AND TESTING DIFFERENCES

CEM CTS Configuration	PCIe Gen 3 (8.0 GT/s)	PCIe Gen 4 (16 GT/s)
RJ Source Setting	~1.5 ps RMS *(RJ is applied over the frequency range defined in the PCI Express 3.0 Base Specification section 4.3.4.4.1)*	~1.0 ps RMS *(RJ is applied over the frequency range defined in the PCI Express 4.0 Base Specification section 8.3.6)*
Pre-waveform Acquisition and SigTest Analysis	• 1.6 million UI's (1.6 x 10^6 x 125.0ps = 200.0µs) • Use the Gen 3 Rx calibration template *(See Note [1] below)*	• 2.0 million UI's (2.0 x 10^6 x 62.5ps = 125.0µs) • Use the Gen 4 RJ calibration (PCIE_4_0_RX_CAL \ PCIE_4_16GB_CEM_Rj_Sj_CAL.dat) template
RJ Cal Limits	1.5 +.2/-0 ps RMS	1.0 +.1/-0 ps RMS
100 MHz SJ Setting	0.1 UI (12.5 ps)	0.1 UI (6.25 ps) • SJ magnitude = 0.0 ps • 2.1 GHz DM Amplitude = 0.0 mV
SJ Cal Limits	12.5 +1/-0 ps	6.25 +0.5/-0 ps
CLB/CBB revision	3.0	4.0
Measured Tx Equalization	P7	P5, P6
(P0 to P9 must be measured for both the System Board and Add-in Card Rx Link Equalization Test @ 16 GT/s.)		
Measured Preshoot	3.5 +/- .2 dB	For P5: 1.9 +/- .1 dB For P6: 2.5 +/- .1 dB
Measured De-emphasis	6.0 +/- .2 dB	0.0 +/- .1 dB

CEM CTS Configuration	PCIe Gen 3 (8.0 GT/s)	PCIe Gen 4 (16 GT/s)
Measured DM Amplitude	Average peak to peak amplitude over 1.6 million UI's of data ($1.6 \times 10^6 \times 125.0$ ps = 200.0 µs). Adjust to 14-16 mV range.	RMS amplitude over 2.0 million UI's of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs). Adjust to 14 +0/-2 mV diff-amp range.
Measured CM Amplitude	—	RMS amplitude over 2.0 million UI's of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs). Adjust to 150 +0/-2 mV diff-amp range. *Note: CM amplitude should be turned off when calibrating for stressed eye, but turned on when testing for Rx link equalization.*
Final Waveform Acquisition	1.6 million UI's	2.0 million UI's (for P5 and P6)
Final SigTest Analysis *(See Note [2] below)*	Rx CTLE setting fixed to 7 with the template for Gen 3 Rx calibration template *(See Note [1] below)* including embedding the remaining portion of the channel	Use Rx calibration template files (PCIe_4_16G_Rx_CAL_CTLE_8p5dB.dat to PCIe_4_16G_Rx_CAL_CTLE_10p5dB.dat). The CTLE range of 8.5 db to 10.5 dB in 0.25 dB step sizes is run for every P5 and P6 waveform.
Measured Eye Height	46 mV +0/-5 mV	15 mV +1.5/-1.5 mV
Measured Eye Width	41.25 +0/-2 ps	18.75 +0.5/-0.5 ps, with: • SJ: 5 to 10 pspp at TP1 • DM-I: 10 to 25 mVpp at TP2 Differential Voltage Swing: 720 to 800 mVpp at TP1
Eye Height/Eye Width Adjustment	RJ and DM-I	SJ, DM-I, Amplitude, and ISI
Scope Bandwidth	> 13 GHz (8 GHz for only DM-I)	≥ 25 GHz max (with min 80 GS/s sample rate)
Insertion Loss	Fixed ISI Channel (max 22 dB at 4 GHz) *(See Note [3] below)*	Variable ISI Channel including reference package (27, 28, and 30 dB at 8 GHz) Add-in-Card reference package loss: 3 dB System reference package loss: 5 dB

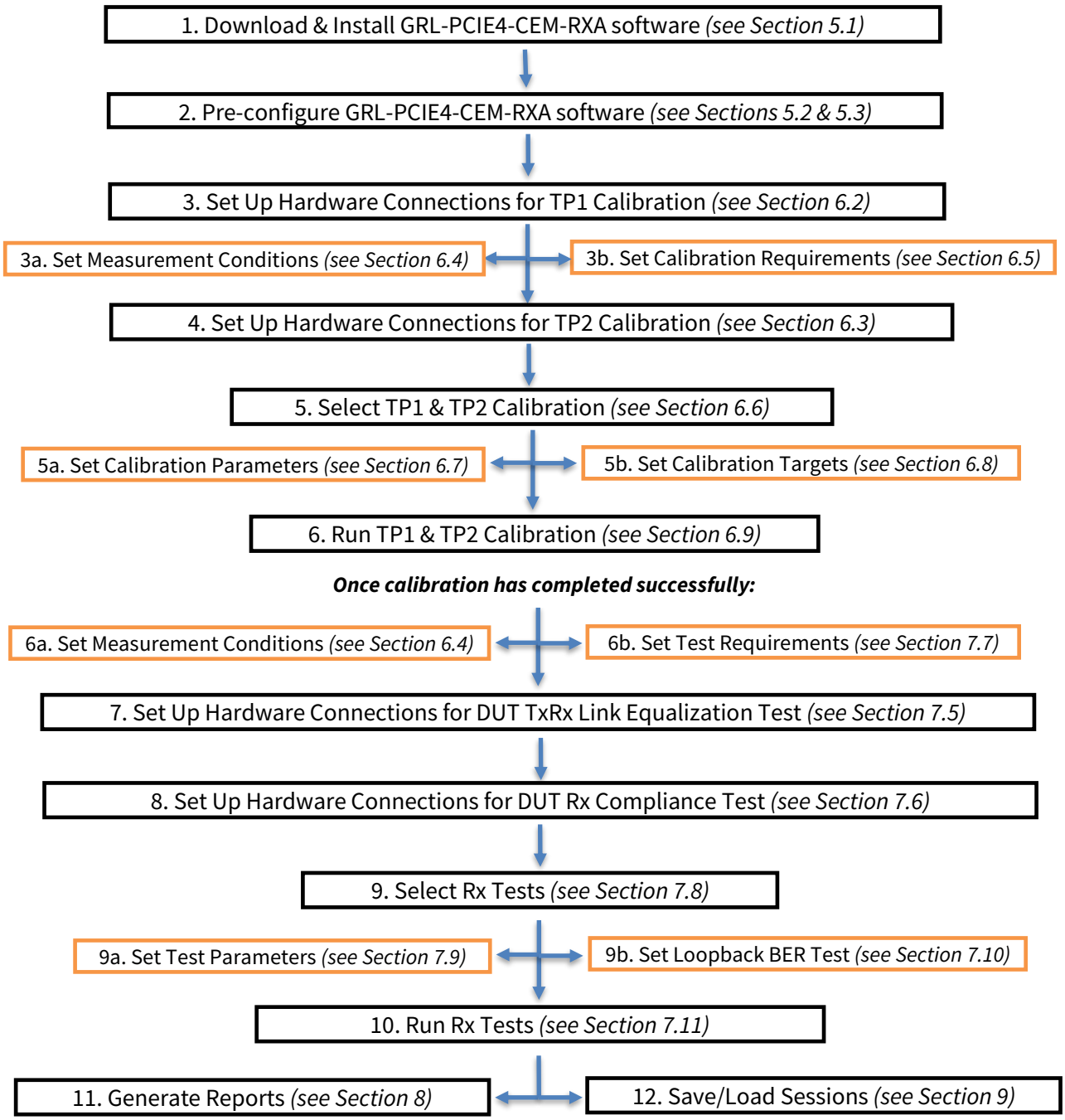
Note [1]: For PCIe Gen 3 U.2 and M.2 CEM calibration, refer to Section 6.3.2, 6.3.3, 6.3.5 and 6.3.6 for the SigTest templates to be used.

Note [2]: If a Clock Recovery error occurs while running SigTest, it could be due to no signal or bad signal integrity. The user is advised to check the setup connection and ensure the correct signal is present on the oscilloscope.

Note [3]: PCIe Gen 3 M.2 CEM system board calibration uses 3.5 dB ISI, while PCIe Gen 3 M.2 CEM add-in card calibration uses 13 dB ISI.

4 GRL-PCIE4-CEM-RXA Automation Software Process Flow

This section summarizes the flow of installation, calibration and compliance testing procedure using the GRL-PCIE4-CEM-RXA automation software.



5 Setting Up GRL-PCIE4-CEM-RXA Software

This section provides the procedures to start up and pre-configure the GRL-PCIE4-CEM-RXA automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the GRL software, follow the procedures in the following sections.

5.1 Download GRL-PCIE4-CEM-RXA Software

Download and install the GRL software as follows:

1. If the GRL software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where GRL-PCIE4-CEM-RXA is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIECEMGen4_AN_PatternFilesInstallationxxxxxxxxxSetup.exe** – Run this on the Anritsu MP1900A BERT Signal Quality Analyzer to install the pattern setup files.
   - **PCIECEMGen4_AN_RxTestApplicationxxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the application.
   - **PCIECEMGen4_AN_RxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

5.2 Launch and Set Up Software

1. Once the software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

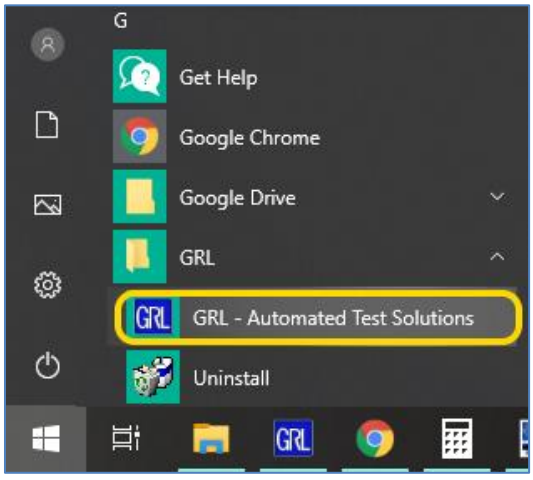


FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

2. From the Application→Rx Test Solution drop-down menu, select 'Anritsu PCIe CEM 4.0 Rx Test' to start the PCIe CEM 4.0 Rx Test Application. If the selection is grayed out, it means that your license has expired.

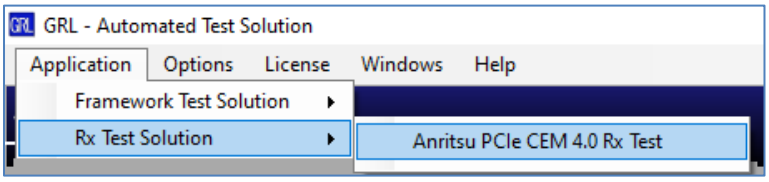


FIGURE 2. START PCIE CEM 4.0 RX TEST APPLICATION

3. To enable license, go to License→License Details.

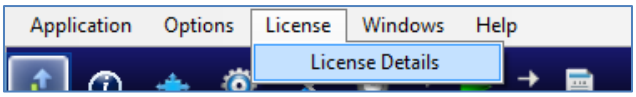


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

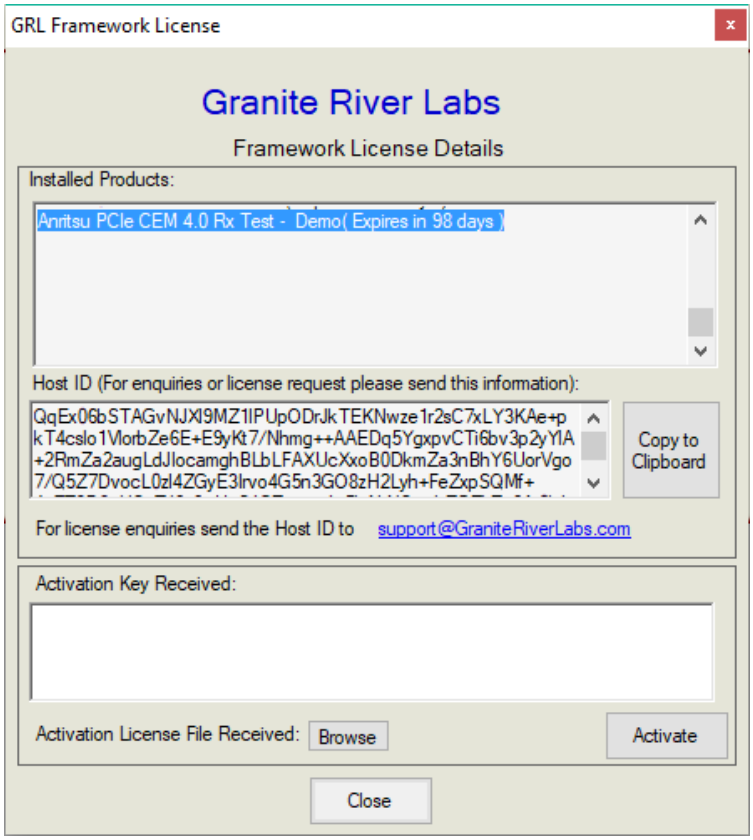


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select “Activate”.
- If you do not have an Activation Key, select “Close” to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

4. Select the Equipment Setup icon  on the PCIe CEM 4.0 Rx Test Application menu.
5. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC. The BERT and MX183000A software can be connected using connection string formats similar to the following examples:
   - BERT: “TCPIP0::192.168.0.14::5001::SOCKET” or “192.168.0.14:5001”
   - MX183000A: “TCPIP0::192.168.0.14::5000::SOCKET” or “192.168.0.14:5000”

   Note the IP addresses listed above are only examples and should be changed according to the actual network connection being used.
6. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.
7. On the Equipment Setup page of the GRL PCIe CEM 4.0 Rx Test Application, type in the address of each connected instrument into the ‘Address’ field.

   *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”.)*

   If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

   *(Note: If the GRL software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as “TCPIP0::192.168.0.4::5025::SOCKET”.)*
8. Then select the “lightning” button () for each connected instrument.

   The “lightning” button should turn green () once the software has successfully established connection with each instrument.

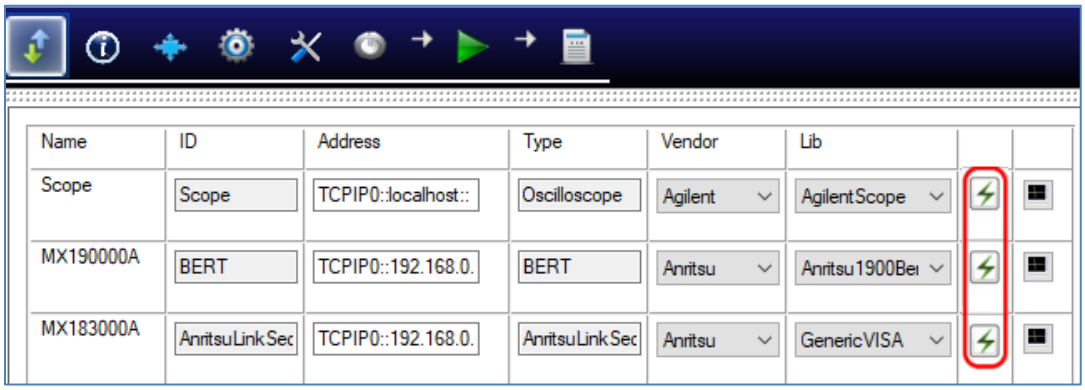


FIGURE 5. CONNECT INSTRUMENTS WITH GRL SOFTWARE

Note: Additional information for connecting supported vendor oscilloscopes (Keysight and Tektronix) to the PC is provided in the Appendix of this document.

5.3 Pre-Configure Software Before Calibration/Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced measurement setup.

5.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

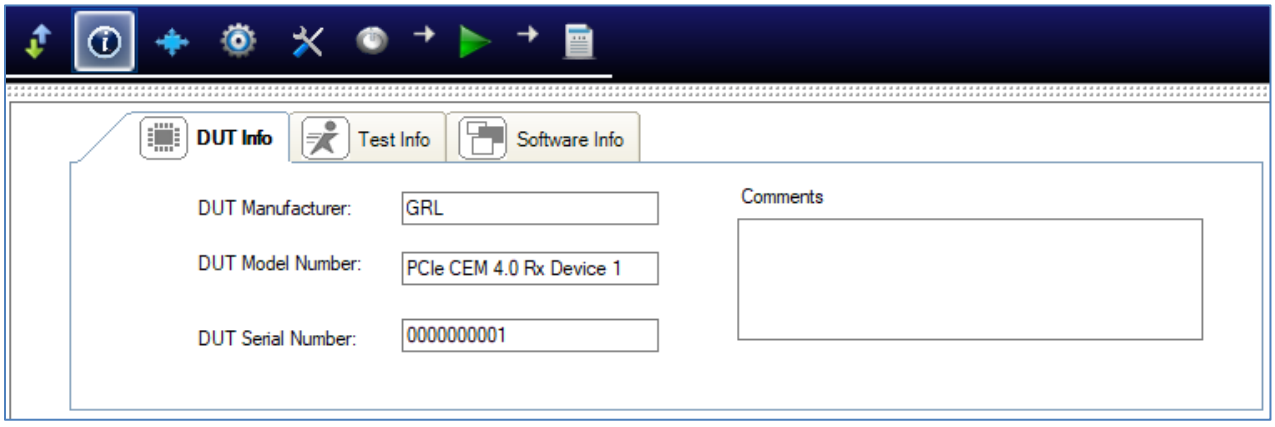


FIGURE 6. SESSION INFO PAGE

6 Calibrating Using GRL-PCIE4-CEM-RXA Software

The GRL-PCIE4-CEM-RXA test solution supports automated Rx calibration using the SigTest signal quality and stress tolerance analysis application for PCIe Gen 3 and Gen 4 system boards and add-in cards. To perform calibration, the GRL-PCIE4-CEM-RXA software is run from the PC or oscilloscope to enable automation control for each step of calibration and signal quality test sequence.

Calibration for the PCIe CEM 4.0 electrical specification will basically be performed at two physical test points: TP1 and TP2 (for the Long Channel). Test Point 1 (TP1) is a physical test point for calibration without the effect of a channel. For PCIe Gen 4 system, an adjustable CEM connector will be used along with the calibration channel for testing the receiver. This will need to adjust the eye amplitude to specification values when measuring eye height/eye width. TP2 is a physical test point that will affect the eye opening due to trace length.

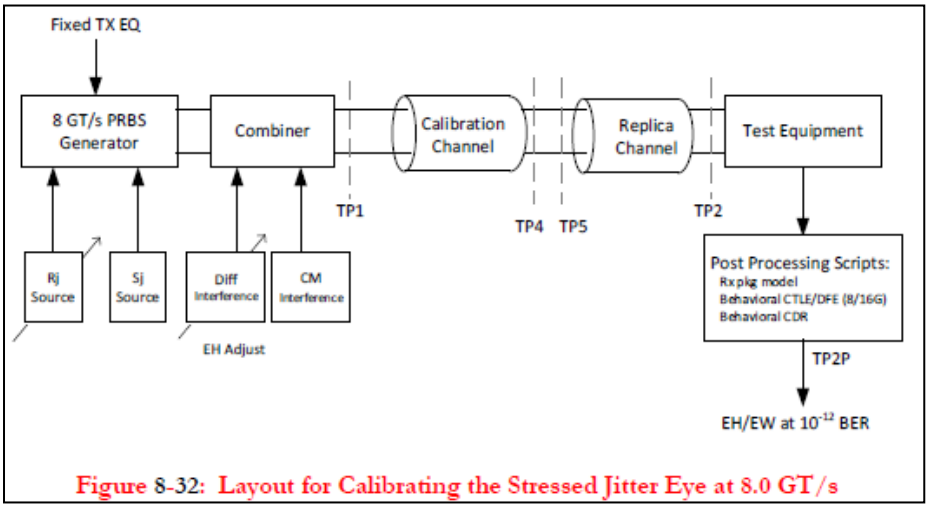


FIGURE 7. CTS RX CALIBRATION DIAGRAM FOR PCIE GEN 3

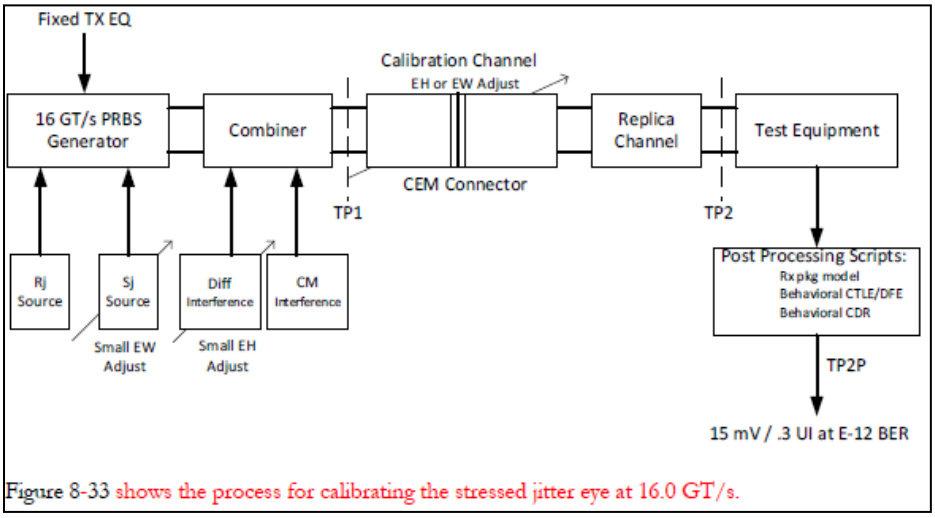


FIGURE 8. CTS RX CALIBRATION DIAGRAM FOR PCIE GEN 4

For the Long Channel TP2 calibration, a PCI-SIG compliance load board (CLB) test fixture will be used for the host system board or a PCI-SIG compliance base board (CBB) test fixture for the add-in card. The board will be connected between the BERT noise generator output and the oscilloscope which will validate the test pattern of the signal and measure for stress tolerance to final stressed eye compliance. When calibration is completed, the GRL software will generate a test report detailing all results obtained from the calibration.

6.1 Connection Setup for MP1900A BERT Generator Set

Figure 9 shows the connection setup between each module of the Anritsu MP1900A BERT Generator Set. *Note that the cable models used in this setup are examples and can be replaced with their equivalent.*

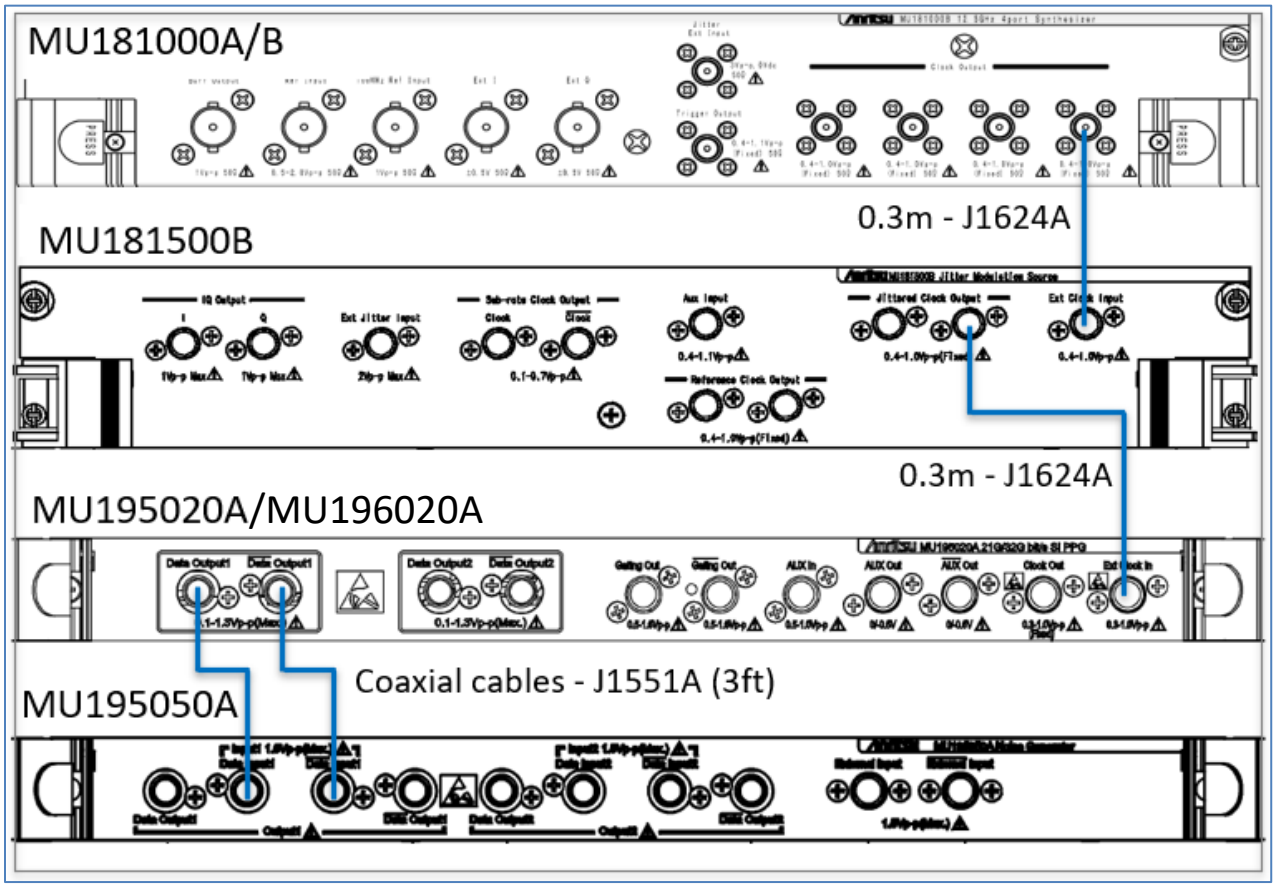


FIGURE 9. CONNECTION SETUP FOR MP1900A BERT GENERATOR SET MODULES

Connection Steps:

1. Using the J1624A SMA-SMA (0.3m) cable, connect the Clock Output of the MU181000A/B Synthesizer to the Ext Clock Input of the MU181500B Jitter Modulator.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU195020A/MU196020A Pulse Pattern Generator.

3. Using the J1551A coaxial cables (3ft), connect the MU195020A/MU196020A Data Outputs to the MU195050A Data Inputs.

6.2 Set Up Automated Rx Calibration for TP1

Once pre-configuration has been completed from previous section, continue with the following calibration setup at TP1 (output of the BERT generator) using a GRL automation control enabled oscilloscope and Anritsu MP1900A BERT.

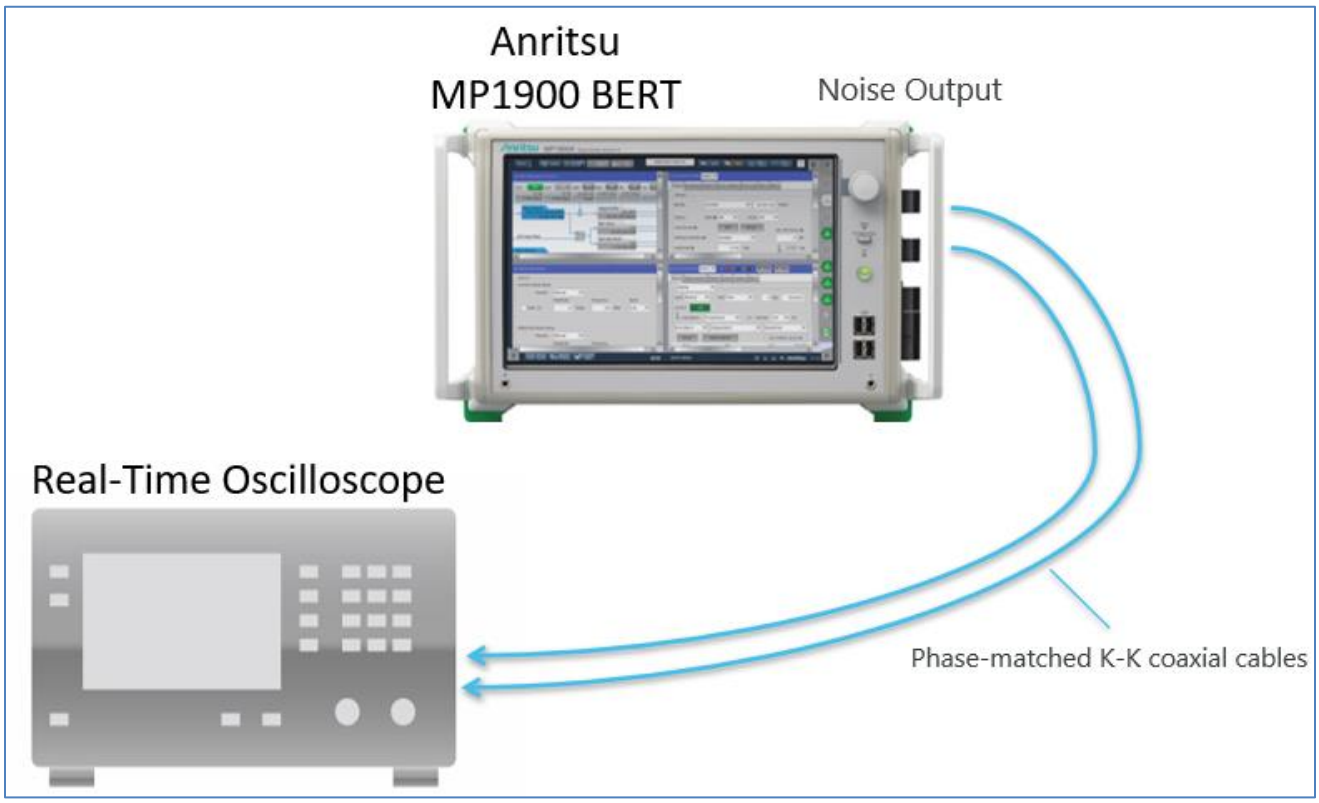


FIGURE 10. RECOMMENDED SETUP FOR TP1 RX CALIBRATION

Connection Steps:

1. Set up the MP1900A BERT connections as described in Section 6.1.
2. Connect the MU195050A noise outputs to the relevant oscilloscope channels using phase-matched K-K coaxial cables.

6.3 Set Up Automated Rx Calibration for TP2

The next step is to calibrate the TP1-TP2 Channel (output of the Long Channel) with the following calibration setups using a GRL automation control enabled oscilloscope, Anritsu MP1900A BERT, and PCIe Gen 4 System Board or Add-In Card test fixtures. These calibration setups should also comply with insertion loss limits of 27 to 30 dB.

6.3.1 Connect Equipment for System Board Calibration

The following calibration setup uses a PCI-SIG compliance load board (CLB) test fixture as the PCIe Gen 4 System Board.

Note: Make sure the CLB is turned ON when connected for all calibrations.

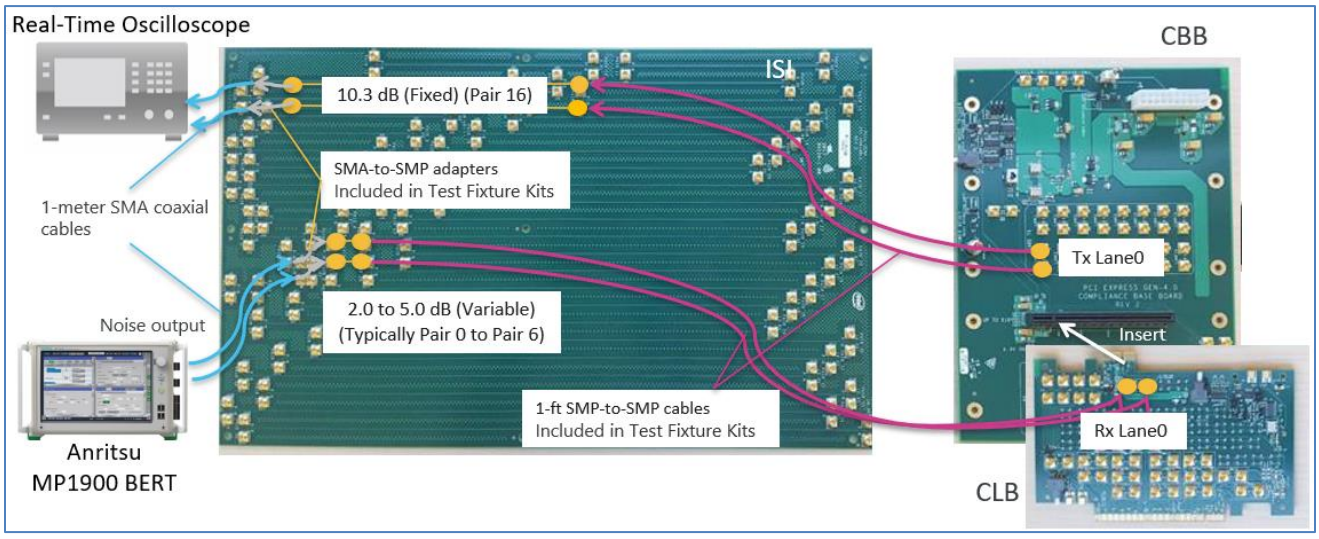


FIGURE 11. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 4 SYSTEM BOARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to 2.0-5.0 dB Variable ISI.
4. Using 1-ft SMP-to-SMP cables, connect both the 2.0-5.0 dB Variable ISI and the CLB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*
5. Insert the CLB into the designated slot on the CBB.
6. Connect the CBB Tx Lane using 1-ft SMP-to-SMP cables to the 10.3 dB Fixed ISI.
7. Connect the 10.3 dB Fixed ISI through the SMA-to-SMP adapters using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: A total loss of 27-30 dB is expected (see Section 6.7.1) from the above setup consisting of:

- *Total 22-25 dB physical loss or Nominal 23 dB physical loss (excluding oscilloscope)*
- *5 dB package loss (post processing via oscilloscope)*

6.3.2 Connect Equipment for PCIE Gen 3 CEM U.2 System Board Calibration (8 GT/s)

The following calibration setup uses a PCIe U.2 (SFF-8639) compliance load board (CLB) test fixture as the PCIe Gen 3 System Board.

Note: Make sure the CLB is turned ON when connected for all calibrations.

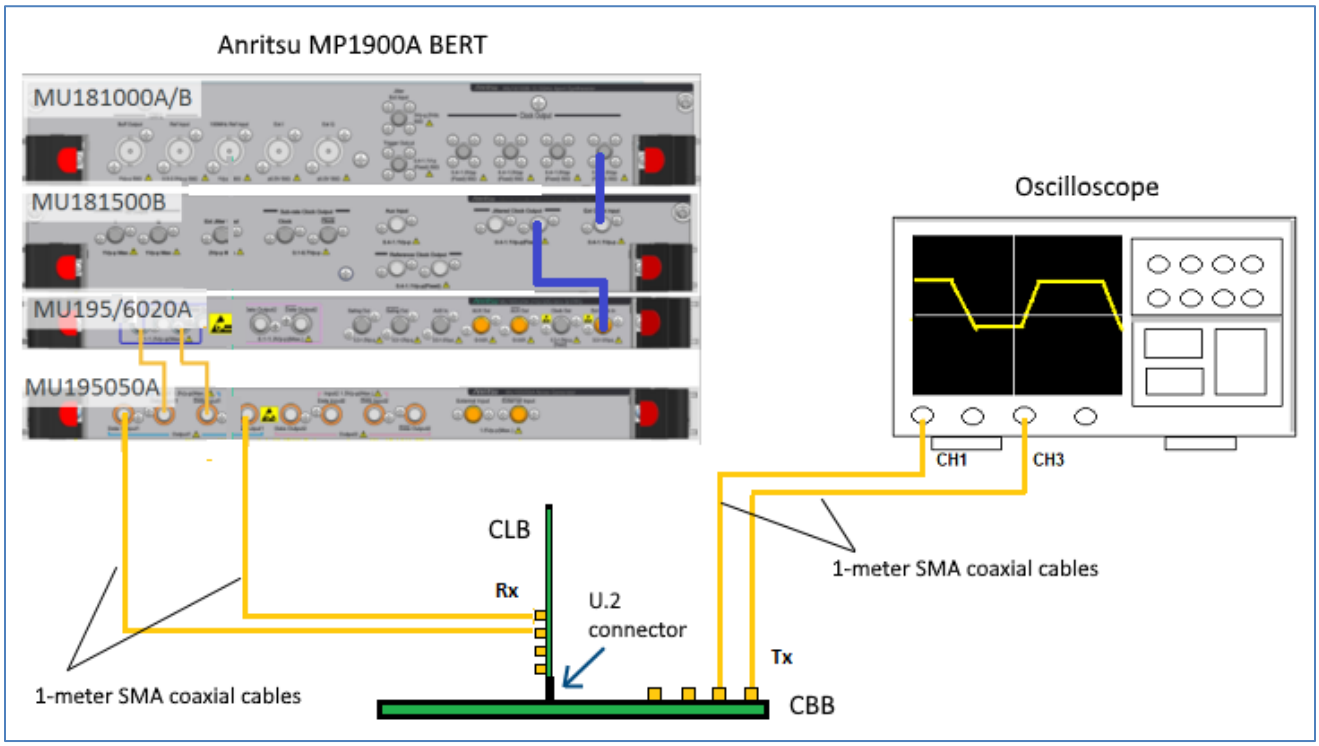


FIGURE 12. RECOMMENDED SETUP FOR U.2 TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 3 SYSTEM BOARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to the U.2 CLB Rx Lane.
3. Insert the U.2 CLB into the U.2 connector slot on the U.2 CBB.
4. Connect the U.2 CBB Tx Lane using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: The PCIE Gen 3 CEM U.2 system board calibration uses the same procedure as the PCIe Gen 3 CEM system board calibration, except for the following change in SigTest templates when performing SigTest signal quality test analysis:

- *For Amplitude, Preset, SJ and RJ calibration: Use the "**U.2_8GB_Rx_Sj_CAL**" SigTest template file.*
- *For DM & CM Amplitude and Eye Height/Eye Width calibration: Use the "**U.2_8GB_Device_Rx_CAL**" SigTest template file.*

6.3.3 Connect Equipment for PCIE Gen 3 CEM M.2 System Board Calibration (8 GT/s)

The following calibration setup uses a PCIe M.2 compliance load board (CLB) test fixture as the PCIe Gen 3 System Board.

Note: Make sure the CLB is turned ON when connected for all calibrations.

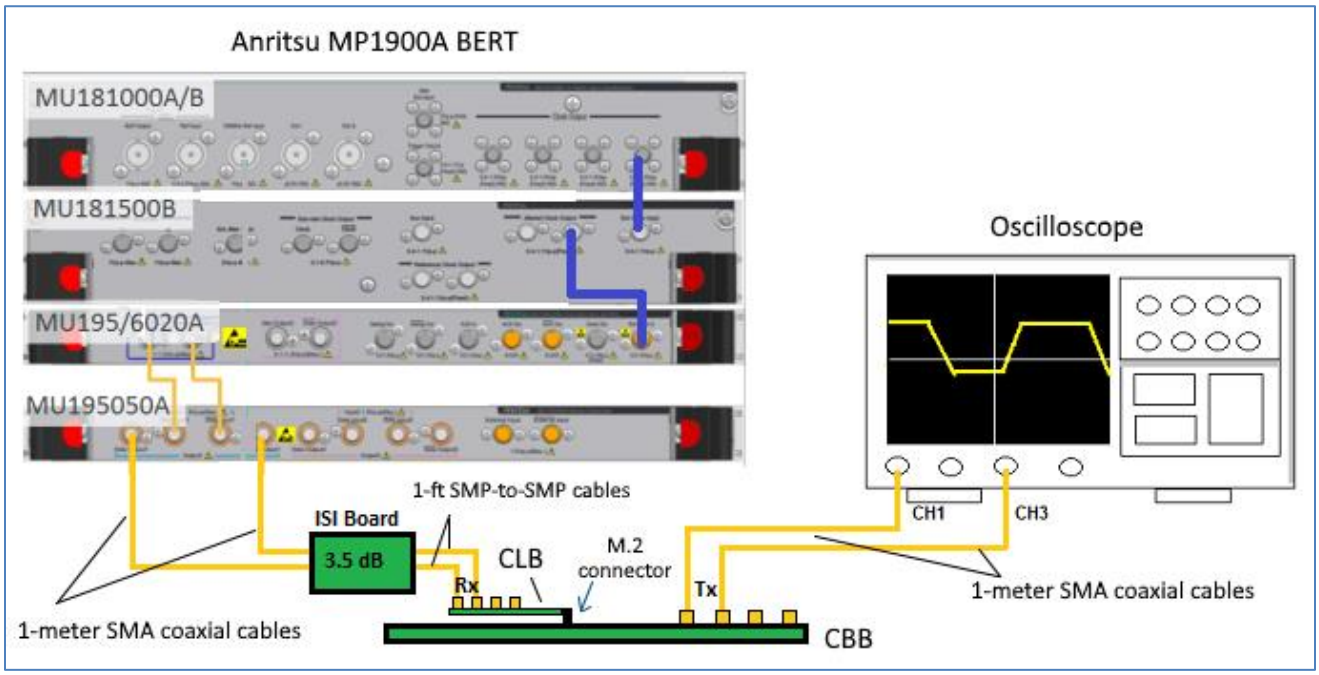


FIGURE 13. RECOMMENDED SETUP FOR M.2 TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 3 SYSTEM BOARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to 3.5 dB ISI.
4. Using 1-ft SMP-to-SMP cables, connect both the 3.5 dB ISI and the M.2 CLB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*
5. Insert the M.2 CLB into the M.2 connector slot on the M.2 CBB.
6. Connect the M.2 CBB Tx Lane using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: The PCIE Gen 3 CEM M.2 system board calibration uses the same procedure as the PCIe Gen 3 CEM system board calibration, except for the following change in SigTest templates when performing SigTest signal quality test analysis:

- *For Amplitude, Preset, SJ and RJ calibration: Use the "**M_2_8Gb_Rx_Sj_CAL**" SigTest template file.*

- *For DM & CM Amplitude and Eye Height/Eye Width calibration: Use the "**M_2_8Gb_Rx_SYS_CAL**" SigTest template file.*

6.3.4 Connect Equipment for Add-In Card Calibration

The following calibration setup uses a PCI-SIG compliance base board (CBB) test fixture as the PCIe Gen 4 Add-In Card.

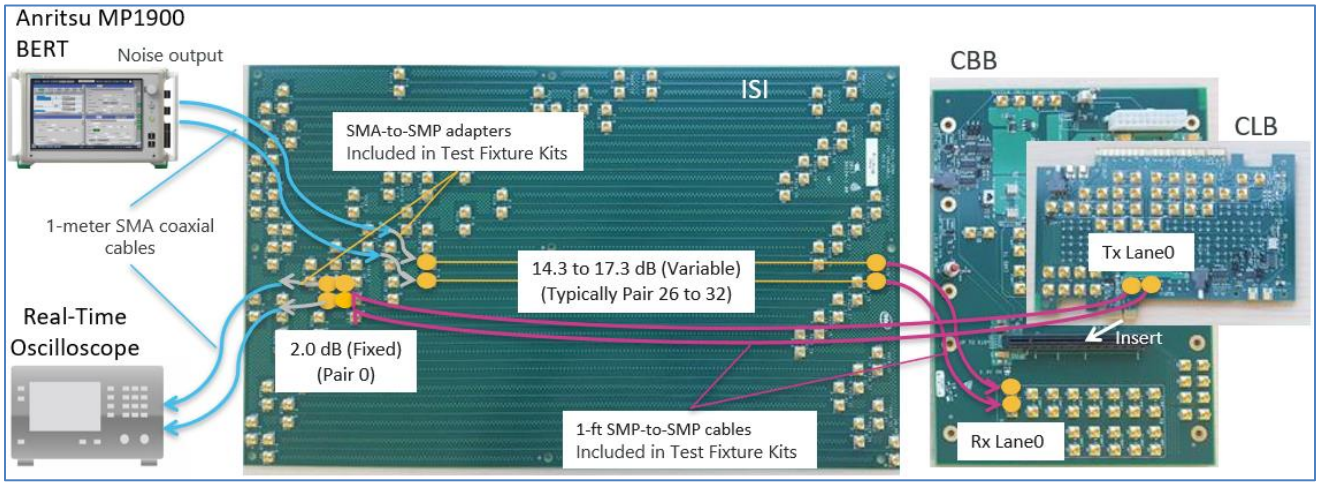


FIGURE 14. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 4 ADD-IN CARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to 14.3-17.3 dB Variable ISI.
4. Using 1-ft SMP-to-SMP cables, connect both the 14.3-17.3 dB Variable ISI and the CBB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*
5. Insert the CLB into the designated slot on the CBB.
6. Connect the CLB Tx Lane using 1-ft SMP-to-SMP cables to the 2.0 dB Fixed ISI.
7. Connect the 2.0 dB Fixed ISI through the SMA-to-SMP adapters using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: A total loss of 27-30 dB is expected (see Section 6.7.1) from the above setup consisting of:

- *Total 24-27 dB physical loss or Nominal 25 dB physical loss (excluding oscilloscope)*
- *3 dB package loss (post processing via oscilloscope)*

6.3.5 Connect Equipment for PCIE Gen 3 CEM U.2 Add-In Card Calibration (8 GT/s)

The following calibration setup uses a PCIe U.2 (SFF-8639) compliance base board (CBB) test fixture as the PCIe Gen 3 Add-In Card.

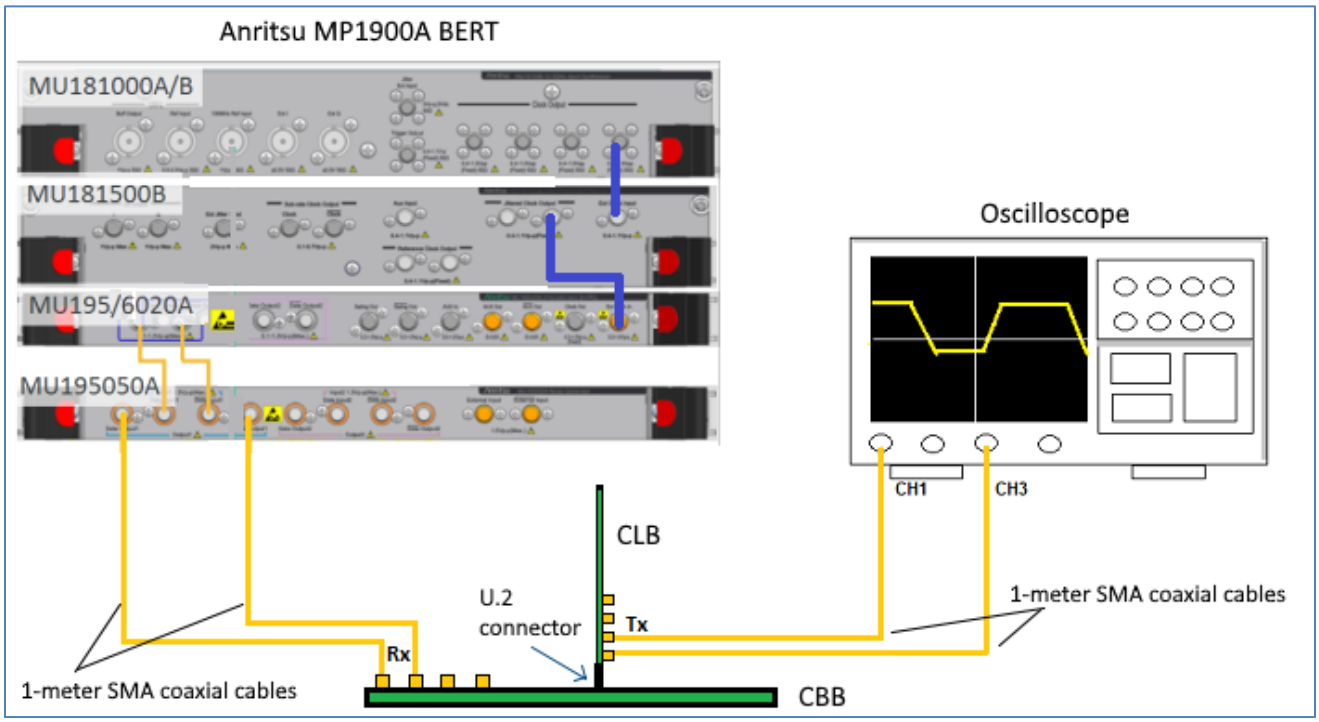


FIGURE 15. RECOMMENDED SETUP FOR U.2 TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 3 ADD-IN CARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to the U.2 CBB Rx Lane.
3. Insert the U.2 CLB into the U.2 connector slot on the U.2 CBB.
4. Connect the U.2 CLB Tx Lane using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: The PCIE Gen 3 CEM U.2 add-in card calibration uses the same procedure as the PCIe Gen 3 CEM add-in card calibration, except for the following change in SigTest templates when performing SigTest signal quality test analysis:

- *For Amplitude, Preset, SJ and RJ calibration: Use the "**U.2_8GB_Rx_Sj_CAL**" SigTest template file.*
- *For DM & CM Amplitude and Eye Height/Eye Width calibration: Use the "**U.2_8GB_Host_Rx_CAL**" SigTest template file.*

6.3.6 Connect Equipment for PCIE Gen 3 CEM M.2 Add-In Card Calibration (8 GT/s)

The following calibration setup uses a PCIe M.2 compliance base board (CBB) test fixture as the PCIe Gen 3 Add-In Card.

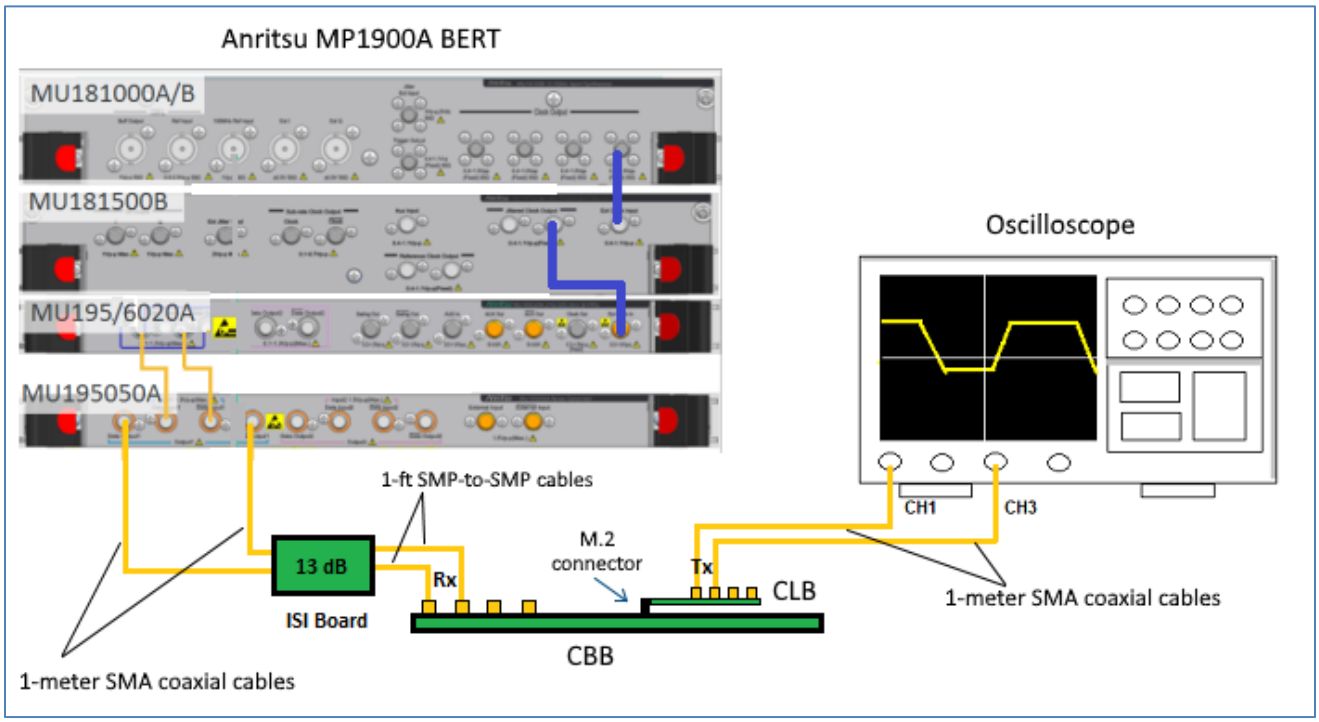


FIGURE 16. RECOMMENDED SETUP FOR M.2 TP2 LONG CHANNEL RX CALIBRATION (PCIE GEN 3 ADD-IN CARD)

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A noise outputs from the oscilloscope channels.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to 13 dB ISI.
4. Using 1-ft SMP-to-SMP cables, connect both the 13 dB ISI and the M.2 CBB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*
5. Insert the M.2 CLB into the M.2 connector slot on the M.2 CBB.
6. Connect the M.2 CLB Tx Lane using 1-meter SMA coaxial cables to the oscilloscope channels.

Note: The PCIE Gen 3 CEM M.2 add-in card calibration uses the same procedure as the PCIe Gen 3 CEM add-in card calibration, except for the following change in SigTest templates when performing SigTest signal quality test analysis:

- *For Amplitude, Preset, SJ and RJ calibration: Use the "**M_2_8Gb_Rx_Sj_CAL**" SigTest template file.*
- *For DM & CM Amplitude and Eye Height/Eye Width calibration: Use the "**M_2_8Gb_Rx_CARD_CAL**" SigTest template file.*

6.4 Set Measurement Conditions

Select  from the GRL PCIe CEM 4.0 Rx Test Application menu to access the **Conditions** page to set the conditions for calibration and testing. The GRL software will perform calibration and testing for selected defined SJ frequencies.

Recommended procedure:

- *Step 1*: When calibrating, select all conditions that may be used for testing, and perform the calibration.
- *Step 2*: Once calibration is completed and ready for testing, re-select the necessary test conditions. For example, if required to test for a single SJ frequency, then select only the required SJ frequency for testing.

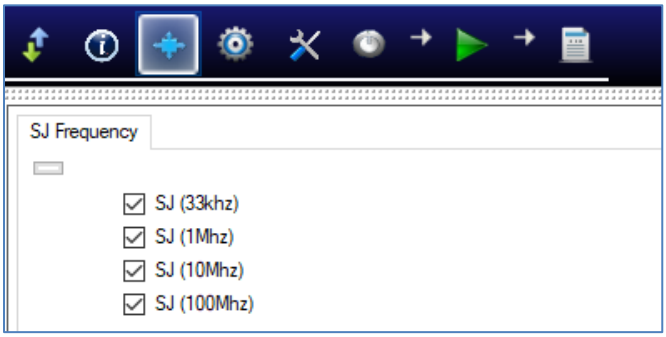


FIGURE 17. SELECT TEST CONDITION

6.5 Set Up Calibration Requirements

After setting up the physical equipment, select  from the GRL PCIe CEM 4.0 Rx Test Application menu to access the Setup Configuration page.

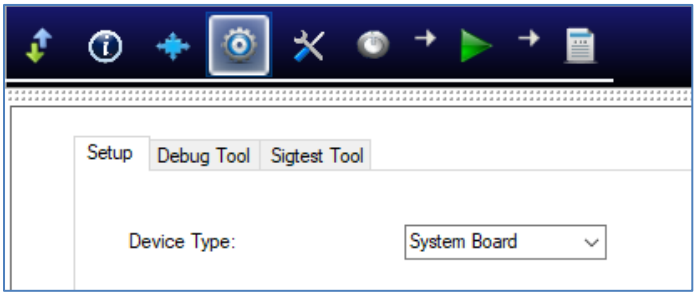


FIGURE 18. SET UP CALIBRATION REQUIREMENTS

6.5.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the calibration device.

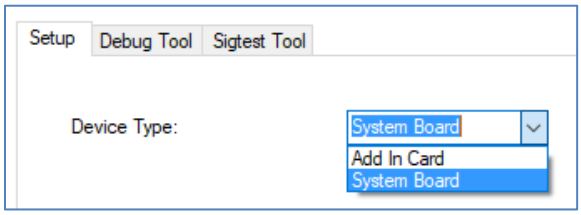


FIGURE 19. SELECT DEVICE FOR CALIBRATION

The GRL PCIe CEM 3.0 Rx Test Application supports the PCIe U.2 (SFF-8639) and M.2 platforms for PCIe Gen 3 (8 GT/s) CEM Rx add-in card and system board calibration and testing.

Select to use a compliant PCIe **U.2** or **M.2** test fixture for the system board or add-in card. Otherwise, select **CEM** if not using the U.2 or M.2 interface.

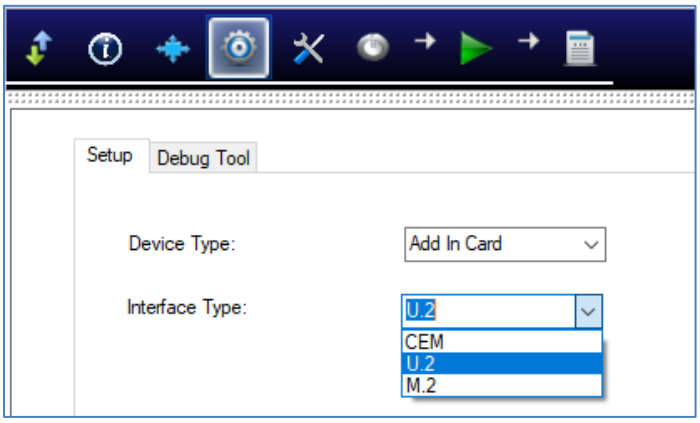


FIGURE 20. SELECT PCIE INTERFACE TYPE FOR CALIBRATION

6.6 Select PCIe CEM 4.0 Rx Calibration

After selecting the device to be calibrated, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 4.0 based receiver calibration to be performed. Select the check box(s) of the desired Rx calibration.

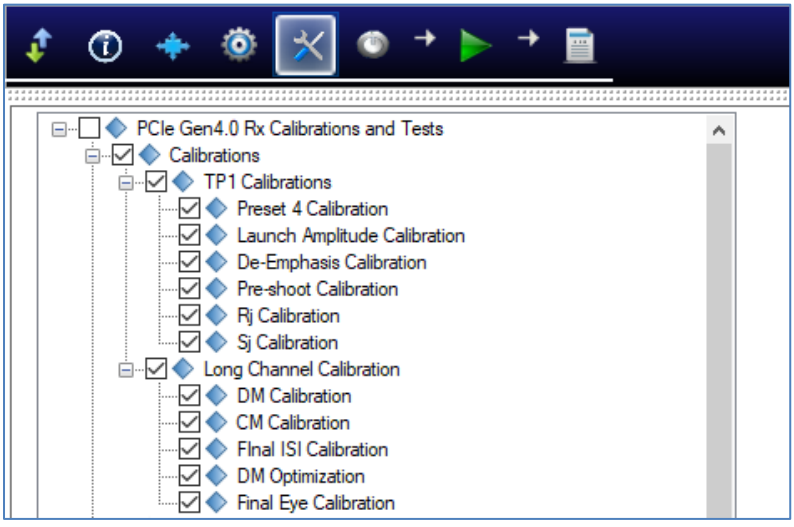


FIGURE 21. SELECT RX CALIBRATION

6.6.1 Select to Perform TP1 Calibration

Under 'TP1 Calibrations', select to calibrate for initial Tx equalization preset, BERT de-emphasis and pre-shoot (which form a linear curve fit), launch amplitude, random jitter (RJ), and sinusoidal jitter (SJ) (for PCIe Gen ¾ frequencies as per PCIe CEM 4.0 Rx specs and forms a linear curve fit for each SJ frequency).

The GRL software will automatically run the selected calibration when initiated.

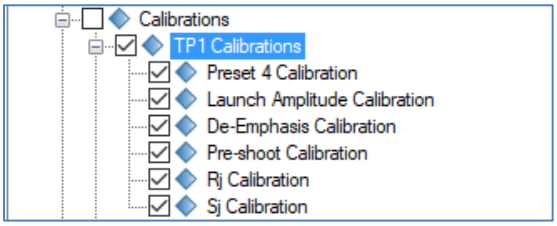


FIGURE 22. SELECT TP1 CALIBRATION

6.6.2 Select to Perform Long Channel TP2 Calibration

Under 'Long Channel Calibration', select to calibrate for differential mode (DM), common mode (CM), final intersymbol interference (ISI), DM optimization, and final eye by default to achieve calibrated eye height and width to produce a final stressed eye diagram. *Note that running DM Optimization will produce results that mention 'Final Eye Reached' in the GRL test report which shows 'True' if the specified final stressed eye is met or 'False' if the final stressed eye does not fall within specifications.*

The GRL software will automatically run the selected calibration when initiated.

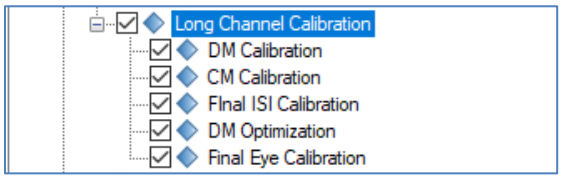


FIGURE 23. SELECT LONG CHANNEL TP2 CALIBRATION

*Note: The **Preset EQ Optimization** calibration option is not enabled by default. To enable this option, set the **Preset Scan On ISI Calibration** field to "False" on the **Configurations** page. See Section 6.7, Configure Calibration Parameters below for more details.*

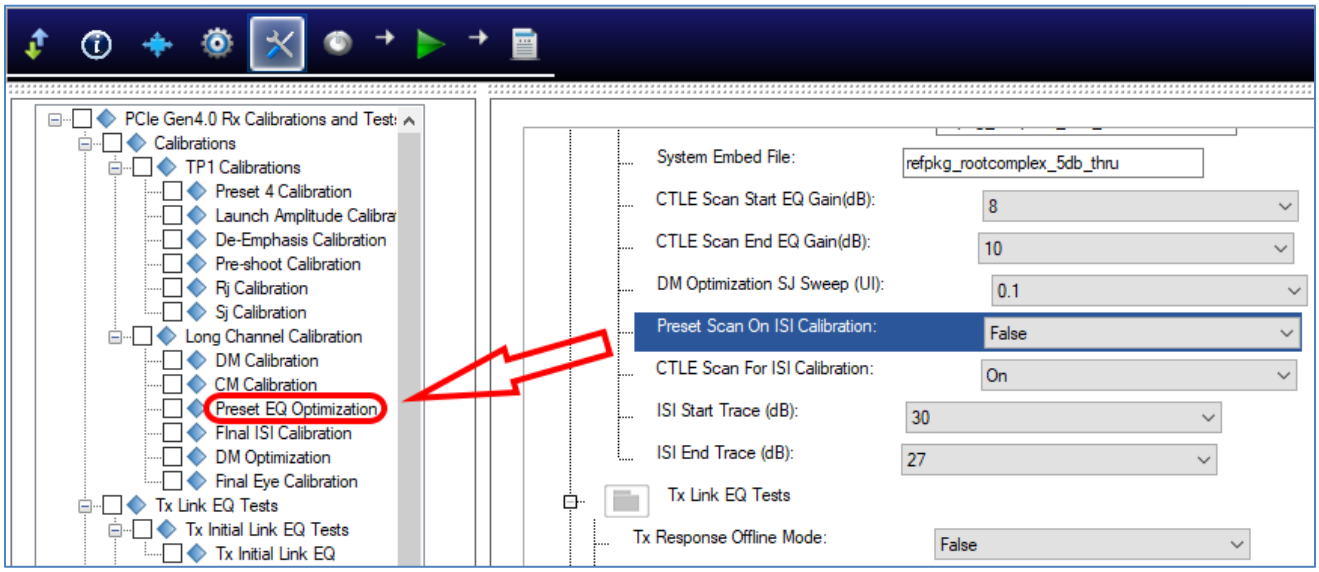


FIGURE 24. ENABLE PRESET EQ OPTIMIZATION CALIBRATION OPTION

6.7 Configure Calibration Parameters

After selecting the desired calibration, select  from the menu to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

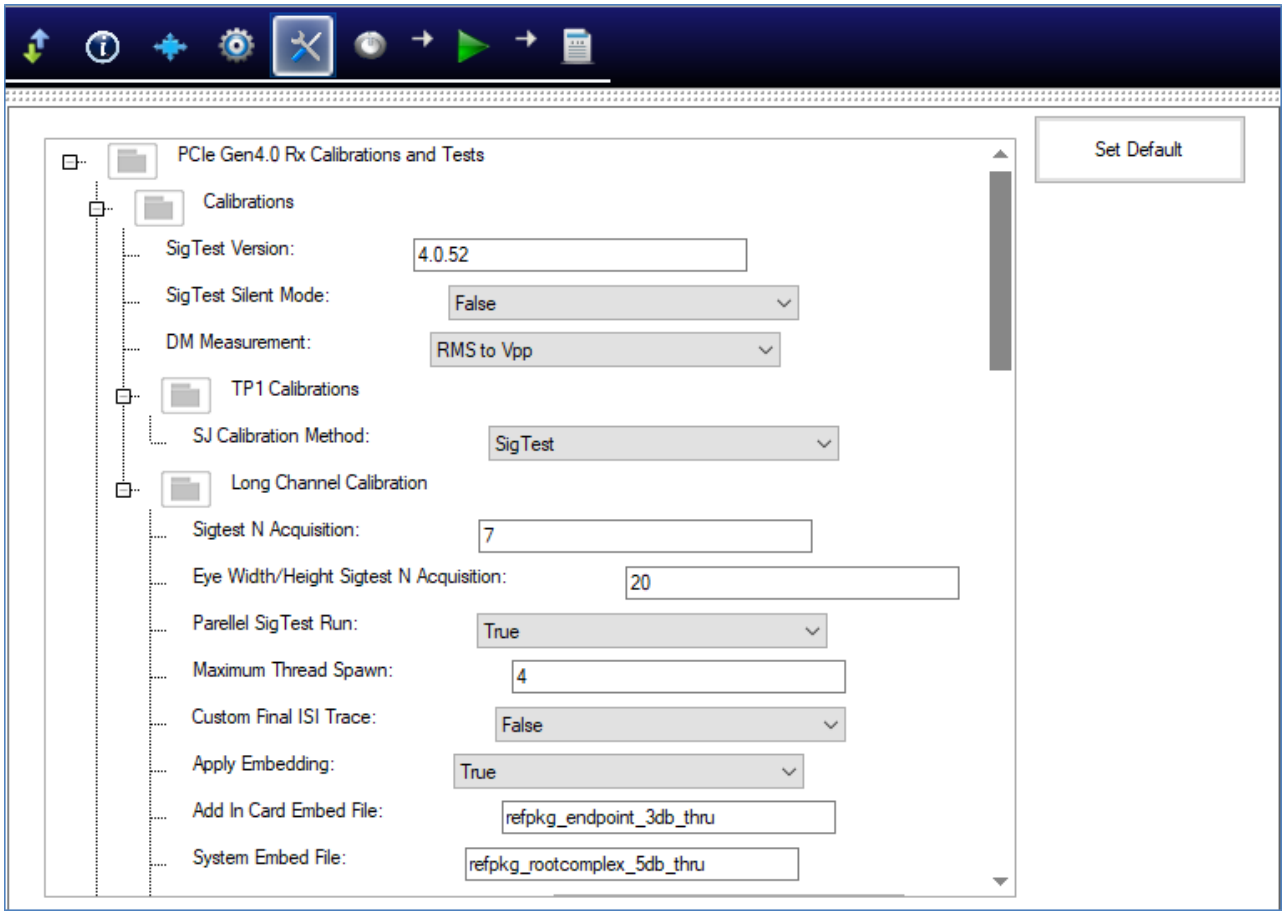


FIGURE 25. CALIBRATION PARAMETERS CONFIGURATION PAGE

TABLE 5. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
SigTest Version	Enter the Version number of the SigTest signal quality test to be run during calibration to ensure waveform compliance. Make sure that the SigTest application is already installed in the test controller system.
SigTest Silent Mode	Select 'True' to enable running the SigTest in silent mode during calibration.
DM Measurement	Select the unit for measuring differential mode (DM).
SJ Calibration Method	Select 'SigTest' to apply the SigTest method for calibration of all SJ frequencies; or Select 'System Defined' to use the Vendor-specific method (Tektronix DPOJET or Keysight EZ-JIT Plus software) for low SJ frequency calibration and the SigTest method for high SJ frequency calibration.
SigTest N Acquisition	Enter the number of measurements to acquire when running SigTest over the Long Channel TP2 calibration.

Eye Width/Height SigTest N Acquisition	Enter the number of measurements to acquire when running SigTest for the Eye calibration.
Parallel SigTest Run	Select 'True' to enable running the SigTest in parallel mode with the Long Channel TP2 calibration.
Maximum Thread Spawn	Set the maximum process threads to generate for checking the Rx device functionality during Long Channel TP2 calibration.
Custom Final ISI Trace	Select 'True' to enable generating custom ISI trace for the final ISI calibration.
Apply Embedding	Select 'True' to embed the add-in card or system board DUT reference package for calibration. *See Section 6.7.2 for more information.*
Add-In Card/System Embed File	Specify the file name for the embedded add-in card or system board DUT reference package. *See Section 6.7.2 for more information.*
CTLE Scan Start & End EQ Gain (dB)	Select the optimized CTLE Equalization Gain setting index to be used based on the CTLE model to measure the Eye area.
DM Optimization SJ Sweep (UI)	Select the SJ scan range to be applied during DM optimization calibration.
Force Use Custom DM	Select 'True' to force custom DM values to be applied during DM optimization calibration.
DM Optimization Array (mV)	If 'Force Use Custom DM' is set to 'True', specify the array of DM values in mV to be applied during DM optimization calibration.
Preset Scan On ISI Calibration	Select 'True' to enable rescan of presets to be performed for each ISI trace that has been changed. Or, select 'False' to enable the 'Preset EQ Optimization' calibration option in the calibration/test list (see Figure 24).
CTLE Scan For ISI Calibration	Select 'On' to enable CTLE optimization scan to be applied during ISI calibration.
ISI Start & End Trace (dB)	Select the optimized ISI trace setting index range for ISI calibration.
DM Optimization Target	Select the Eye Width or Eye Height to prioritize as a target during DM optimization calibration.

6.7.1 Total Channel Loss and Physical Channel Loss

As defined by the PCIE standard requirements, if a waveform post processing tool is used for Rx stressed eye calibration, the tool should comply with the following:

- *The test channel which is the long Rx calibration channel with the Root reference package applied in post-processing should give a total loss of 28.0 dB. This means that the physical channel loss is 23.0 dB or 25.0 dB depending on the DUT setup.*

For example, for the add-in card setup, the total loss of 28.0 dB will consist of a nominal 25 dB physical channel loss and an embedded 3 dB package loss. The nominal 25 dB physical channel

loss excludes the oscilloscope input whereas the 3 dB package loss or embedding loss comes from post processing via the oscilloscope input.

For the system board setup, the total loss of 28.0 dB will consist of a nominal 23 dB physical channel loss and an embedded 5 dB package loss. Similarly, the nominal 23 dB physical channel loss excludes the oscilloscope input whereas the 5 dB package loss or embedding loss comes from post processing via the oscilloscope input.

6.7.2 Apply DUT Reference Package Embedding for Calibration

Note: This section has been referenced from the Anritsu Release Note M3T-1QAMP1900A0406 "Anritsu_GRL_PCIe4CEM_ReleaseNote_E_03.pdf".

To embed the add-in card or system board DUT reference package for calibration, ensure that the oscilloscope being used supports the Embed function. Hence, select **True** for the 'Apply Embedding' parameter on the Configurations page.

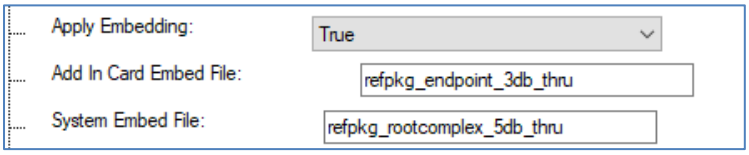


FIGURE 26. SET UP DUT REFERENCE PACKAGE EMBEDDING FOR CALIBRATION

Embedding is applied on the scope as follows:

- 3 dB for the add-in card DUT
- 5 dB for the system board DUT

The DUT reference package embedding files should be named in the 'Add In Card Embed File' or 'System Embed File' parameter respectively. Default embedding files are included with the GRL scope setup files installer (*PCIECEMGen4_AN_RxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe*) and are to be installed on the scope. Make sure that the default embedding files are available if using different embedding files. On the Keysight scope, the embedding files must be present in the "C:\GRL\Agilent\Setup\Anritsu PCIe CEM 4.0 Rx Test\TransferFunction" directory in the TF4 format. On the Tektronix scope, the embedding files must be present in the "C:\TekApplications\DPOJET\Setups\Anritsu PCIe CEM 4.0 Rx Test\Sparam" directory in the FLT format.

The user can disable DUT reference package embedding by selecting **False** for the 'Apply Embedding' parameter on the Configurations page. In this case, the scope will not apply reference package embedding. This is useful if the user chooses to use a replica trace instead of reference package embedding.

The following diagram shows the difference of connection between Embedding and No Embedding Channel Loss during Rx stressed eye calibration for the PCIe Gen 4 Add-In Card:

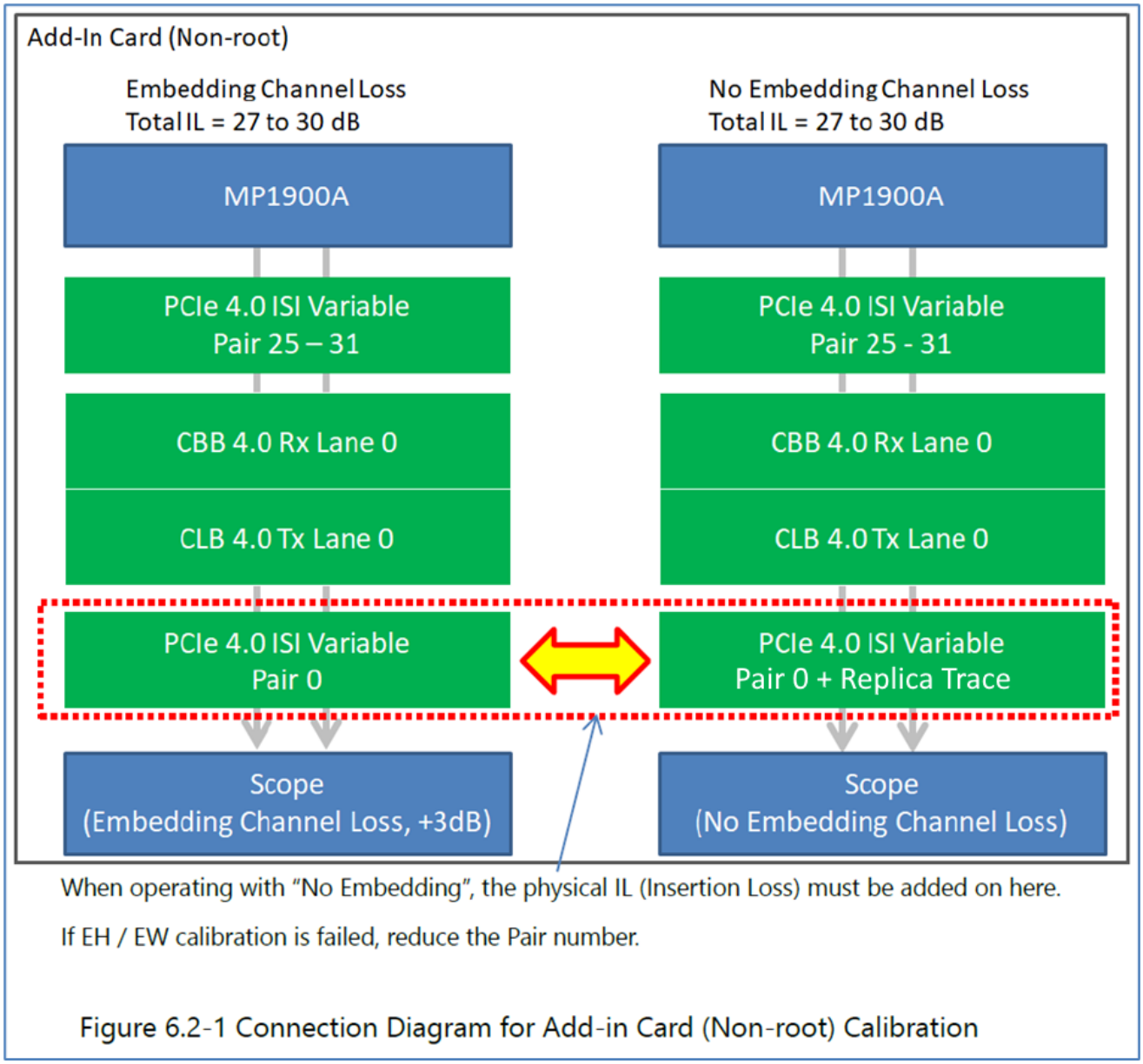


Figure 6.2-1 Connection Diagram for Add-in Card (Non-root) Calibration

The following diagram shows the difference of connection between Embedding and No Embedding Channel Loss during Rx stressed eye calibration for the PCIe Gen 4 System Board:

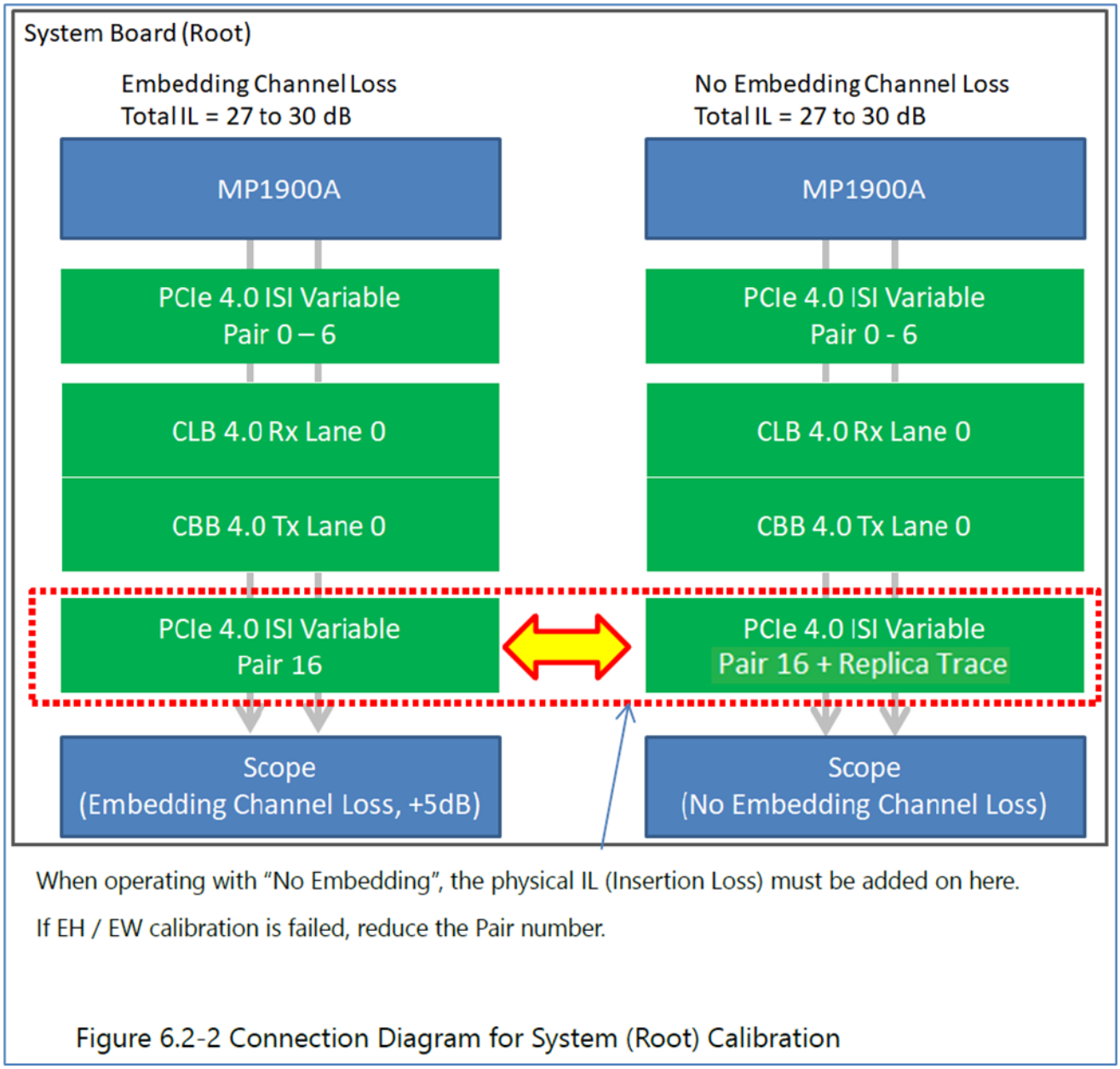


Figure 6.2-2 Connection Diagram for System (Root) Calibration

6.8 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for the RJ, SJ, DM and CM calibration. To do this, select  from the menu to access the Calibration page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the Use Default Value checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

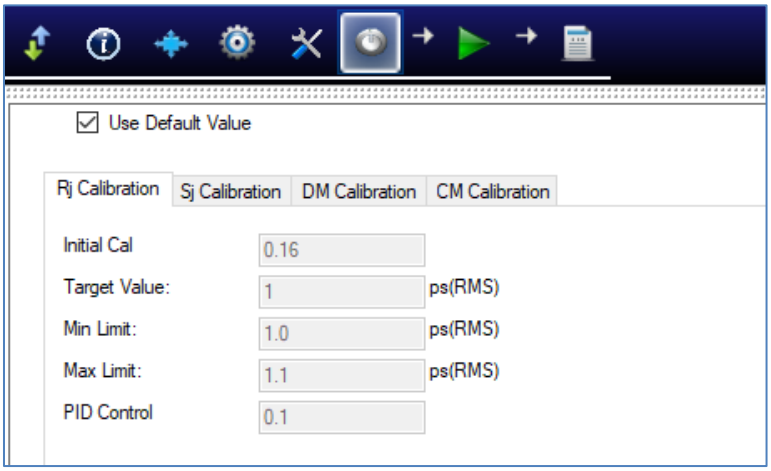


FIGURE 27. CALIBRATION TARGET OVERWRITE PAGE

6.9 Run Automation Calibration

Once calibration have been selected and set up from the previous sections, the calibration are now ready to be run.

Select from the menu to access the Run Tests page. The GRL-PCIE4-CEM-RXA software automatically runs the selected calibration when initiated.

Before running the calibration, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration exist, the software will *skip* those calibration.
- **Replace if Result Exists** – If results from previous calibration exist, the software will *replace* those calibration with new results.

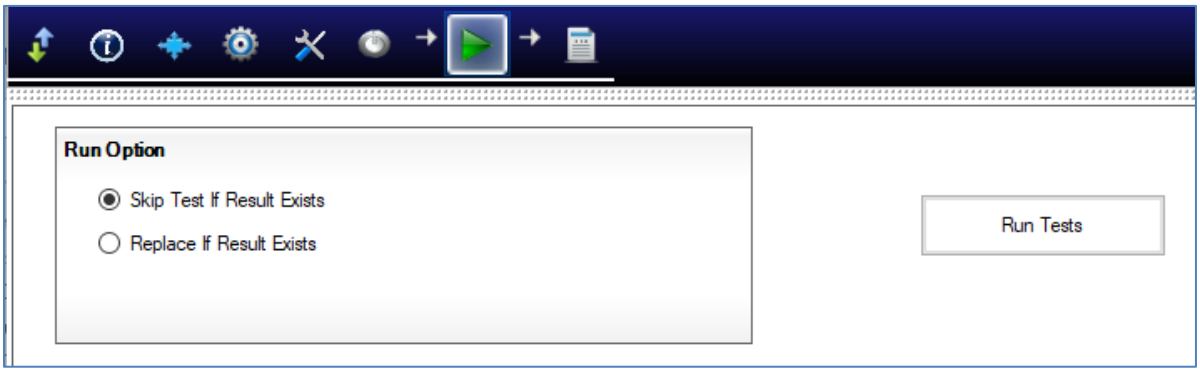


FIGURE 28. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration. The connection diagram for the calibration being run will initially appear to allow the user to make sure that the calibration environment has been properly set up before calibration can proceed.

7 Testing Using GRL-PCIE4-CEM-RXA Software

The GRL-PCIE4-CEM-RXA test solution supports automated Rx compliance testing as well as optional SJ margin search testing for PCIe Gen 3 and 4 system board and add-in card DUT's. Rx compliance testing includes Tx preset test, initial Tx equalization test, Tx link equalization response test, and Rx link equalization test performed at 8.0 GT/s and 16.0 GT/s respectively. The GRL software will initially run through link training with the DUT to prepare it for Loopback mode. Once the DUT is ready for next transition state, the software will start to initiate loopback on the DUT and then measuring the Bit Error Ratio (BER) using the calibration stressed signals. The Rx path is tested with worst case eye to ensure a BER of less than 1E-12 can be achieved.

When testing is completed, the GRL software will generate a test report detailing all results obtained from the test runs.

7.1 Overview of DUT Tx Preset Test

Note: This only applies for the add-in card DUT and is not required for the system board DUT.

The PCIe Gen ¾ add-in card DUT will be tested for Tx preset compliance as defined by the CTS at 8.0 GT/s or 16.0 GT/s. This will first ensure the DUT is able to generate the correct Tx equalization values for each of the total 11 presets before being tested for Tx equalization.

Note: This test requires the DUT to be in the polling.compliance state. No Variable ISI channel will be used in the setup.

7.1.1 Add-In Card Tx Preset Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CBB with no power applied.
- Connect the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board to the Rx lane 0 (SMP connectors J18 and J2) on the CBB riser board.
- Apply 50-ohm terminations on all Tx lanes other than the Tx lane under test.
- Connect the Tx lane under test to the input of the oscilloscope.

Once the CBB is powered on, set the CBB compliance toggle to initially place the DUT in the 8.0 GT/s or 16 GT/s test state and capture the following:

- 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0$ ps = 200.0 µs) for 8.0 GT/s, or
- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs) for 16.0 GT/s.

Save the captured waveform for the initial preset value, using a compliance pattern of 64 ones and 64 zeros. Then, repeat the test for all 11 presets at 8.0 GT/s or 16.0 GT/s respectively.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 8.0 GT/s or 16.0 GT/s respectively.

7.2 Overview of DUT Initial Tx Equalization Test

Note: This only applies for the add-in card DUT and is not required for the system board DUT.

The PCIe Gen ¾ add-in card DUT will be tested for initial Tx equalization as defined by the CTS at 8.0 GT/s or 16.0 GT/s. This will ensure the DUT is able to use the correct Tx equalization preset as required during the initial stage of testing.

7.2.1 Add-In Card Initial Tx Equalization Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB riser board to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Keep additional Tx lanes other than the Tx lane under test unterminated.

Once the CBB is powered on, the DUT should start link training and negotiation to 8.0 GT/s or 16.0 GT/s while requesting P0 as the initial preset for the DUT. *Note that Tx equalization adjustments will not be required in phase 3. Ensure that the Tx equalization preset for the DUT is maintained when changing to 8 GT/s or 16.0 GT/s.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0$ ps = 200.0 µs) for 8.0 GT/s, or
- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs) for 16.0 GT/s.

Save the captured waveform for preset P0. Then, repeat the test with presets from P0 to P9 at 8.0 GT/s or 16.0 GT/s respectively.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 8.0 GT/s or 16.0 GT/s respectively.

7.3 Overview of DUT Tx Link Equalization Response Test

The PCIe Gen ¾ system board or add-in card DUT will be tested for Tx link equalization response as defined by the CTS at 8.0 GT/s or 16.0 GT/s. This will ensure the DUT can accurately respond to commands to adjust the transmitter equalization values during link training for DUT loopback.

7.3.1 System Board Tx Link Equalization Response Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the BERT signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.
- If necessary depending on the DUT, add 50-ohm terminations to additional Tx lanes.

Note the setup will not include any Variable ISI channel.

Once the system board DUT is powered on, it should start link training and negotiation to 8.0 GT/s or 16.0 GT/s. Send a command from the BERT to the DUT to set the Tx equalization to the following:

- preset 4 (both preshoot and de-emphasis to 0.0 dB) for 8.0 GT/s, or
- preset 0 (preshoot to 0.0 dB and de-emphasis to -6.0 dB) for 16.0 GT/s.

Ensure that this Tx equalization transition is able to complete within a 1 microsecond timeframe. Record the cursors reported by the DUT for that preset.

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0$ ps = 200.0 µs) for 8.0 GT/s, or
- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs) for 16.0 GT/s.

Save the captured waveform for preset 4 at 8.0 GT/s or preset 0 at 16.0 GT/s. Then, repeat the test with presets from P0 to P9 at 8.0 GT/s or P1 to P9 at 16.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 8.0 GT/s or 16.0 GT/s respectively.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

7.3.2 Add-In Card Tx Link Equalization Response Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB riser board to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- If necessary depending on the DUT, add 50-ohm terminations to additional Tx lanes.

Note the setup will not include any Variable ISI channel.

Once the CBB is powered on, the DUT should start link training and negotiation to 8.0 GT/s or 16.0 GT/s. *(Note: An initial preset other than the following presets should be used.)* Send a command from the BERT to the DUT to set the Tx equalization to preset 4 (for 8.0 GT/s) or preset 0 (for 16.0 GT/s). *Ensure that this Tx equalization transition is able to complete within a 1 microsecond timeframe. Record the cursors reported by the DUT for that preset.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0$ ps = 200.0 µs) for 8.0 GT/s, or
- 2.0 million unit intervals of data ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs) for 16.0 GT/s.

Save the captured waveform for preset 4 at 8.0 GT/s or preset 0 at 16.0 GT/s. Then, repeat the test with presets from P0 to P9 at 8.0 GT/s or P1 to P9 at 16.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 8.0 GT/s or 16.0 GT/s respectively.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

7.4 Overview of DUT Rx Link Equalization Test

The PCIe Gen ¾ system board or add-in card DUT will be tested for Rx link equalization as defined by the CTS at 8.0 GT/s or 16.0 GT/s. This will ensure the DUT can successfully send commands to adjust the transmitter equalization of its link partner as required.

7.4.1 System Board Rx Link Equalization Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.

- Connect the CLB 100 MHz clock output from the system board DUT to the BERT synthesizer (that has passed PCIe 3.0 or 4.0 base specification PLL compliance or equivalent for the respective data rate).
- If necessary depending on the DUT, add 50-ohm terminations to additional Tx lanes.

Adjust the Tx equalization (EQ) of the BERT error detector to align with the initial Tx EQ preset at 8.0 GT/s or 16.0 GT/s requested by the system board DUT.

Once the system board DUT is powered on, it should start link training and equalization sequence by the BERT error detector at 8.0 GT/s or 16.0 GT/s, which should eventually place the DUT in the loopback state.

The test is considered as successful if detected no more than one error in 10^{12} bits transmitted.

7.4.2 Add-In Card Rx Link Equalization Test at 8.0 GT/s or 16.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 3.0 (for 8.0 GT/s) or 4.0 (for 16.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB riser board to the signal source.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- If necessary depending on the DUT, add 50-ohm terminations to additional Tx lanes.

Set the BERT error detector to initially transmit with preset P7 at 8.0 GT/s or 16.0 GT/s. *(Note for 16.0 GT/s, this is required only if the DUT does not request any preset to be transmitted by the BERT.)*

Once the CBB is powered on, the DUT should start link training and equalization sequence by the BERT error detector at 8.0 GT/s or 16.0 GT/s, which should eventually place the DUT in the loopback state.

The test is considered as successful if detected no more than one error in 10^{12} bits transmitted. For 8.0 GT/s, repeat the test by setting the BERT error detector to initially transmit with preset P8.

7.4.3 Link Training

During link training process, the DUT basically goes through multiple states via the status state machine (SSM) method to enter Loopback mode as shown below.

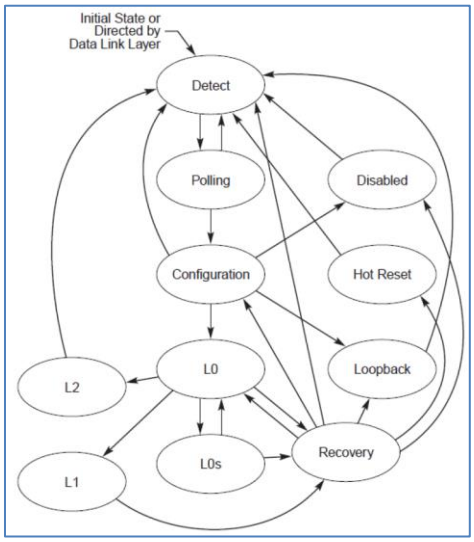


FIGURE 29. MAIN STATE DIAGRAM FOR LINK TRAINING AND STATUS STATE MACHINE (FROM CTS)

Below is a loopback training sequence example from CTS:

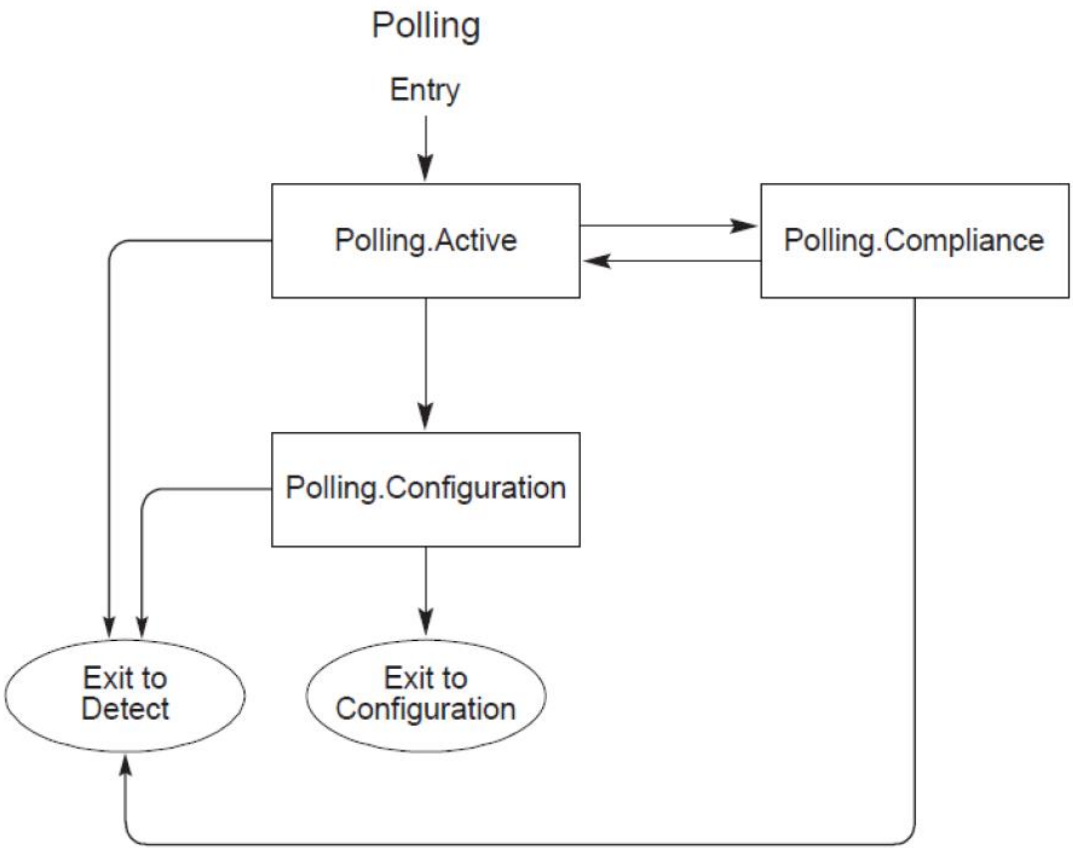


FIGURE 30. POLLING SUBSTATE MACHINE (FROM CTS)

1. Enable the DUT to enter the Polling.Active state by sending TS1 with PAD (K23.7).

2. The DUT will go into the Polling.Configuration state after sending more than 1024 TS1 and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The DUT will next enter the Configuration state after 8 consecutive TS2 with PAD have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Start speed negotiation by sending TS1 at 2.5 GT/s advertising the supported speeds. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
5. The DUT will finally switch to the Loopback mode after having two consecutive TS1 at the requested speed with Loopback bit asserted.

7.5 Set Up Automated DUT Tx Link Equalization Test

Once calibration has been completed from Section 6, continue with the following setup to perform initial Tx link equalization (EQ) tests to prepare the DUT for the final stage of Rx compliance testing. The setup requires the Anritsu MP1900A BERT (including the MU195040A SI Error Detector), PCIe Gen ¾ System Board or Add-In Card DUT, and oscilloscope to be used.

7.5.1 Connect Equipment for System Board Tx Link EQ Testing

The following Tx link EQ test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen ¾ System Board DUT.

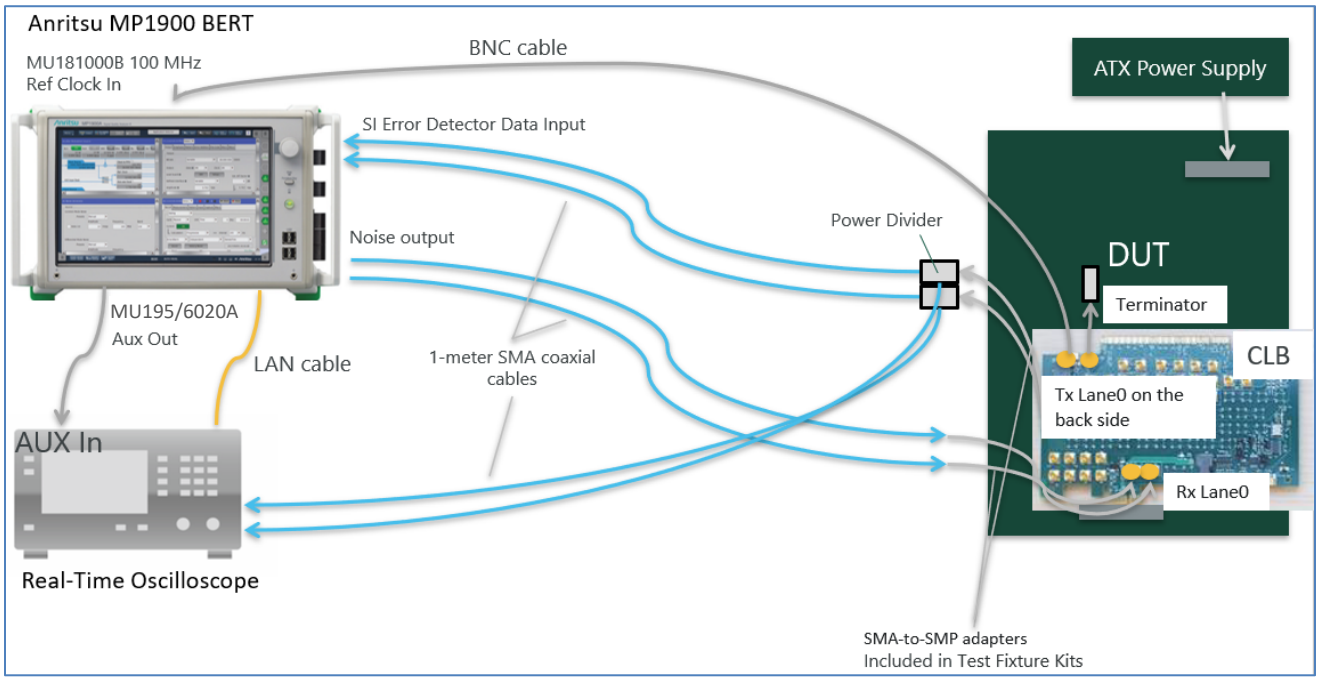


FIGURE 31. RECOMMENDED SETUP FOR DUT TX LINK EQ TESTING (PCIE GEN ¾ SYSTEM BOARD)

1. Connect an ATX power supply to the DUT.

2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to the CLB Rx Lane.
4. Connect the Tx Lane on the back of the CLB to the power divider input ports through another set of SMA-to-SMP adapters.
5. Using a BNC cable, connect a CLB Ref Clock Out connector to the MU181000B 100 MHz Ref Clock In.
6. Terminate the other unused CLB Ref Clock Out connector using the J1632A coaxial terminator.
7. Using 1-meter SMA coaxial cables, connect the power divider outputs to the MU195040A data inputs for loopback error detection.
8. Using 1-meter SMA coaxial cables, connect the oscilloscope channels to the power divider tapped input ports.
9. Using a SMA-to-SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
10. Connect a LAN cable between the MP1900A BERT and the oscilloscope.

7.5.2 Connect Equipment for Add-In Card Tx Link EQ Testing

The following Tx link EQ test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen ¾ Add-In Card DUT.

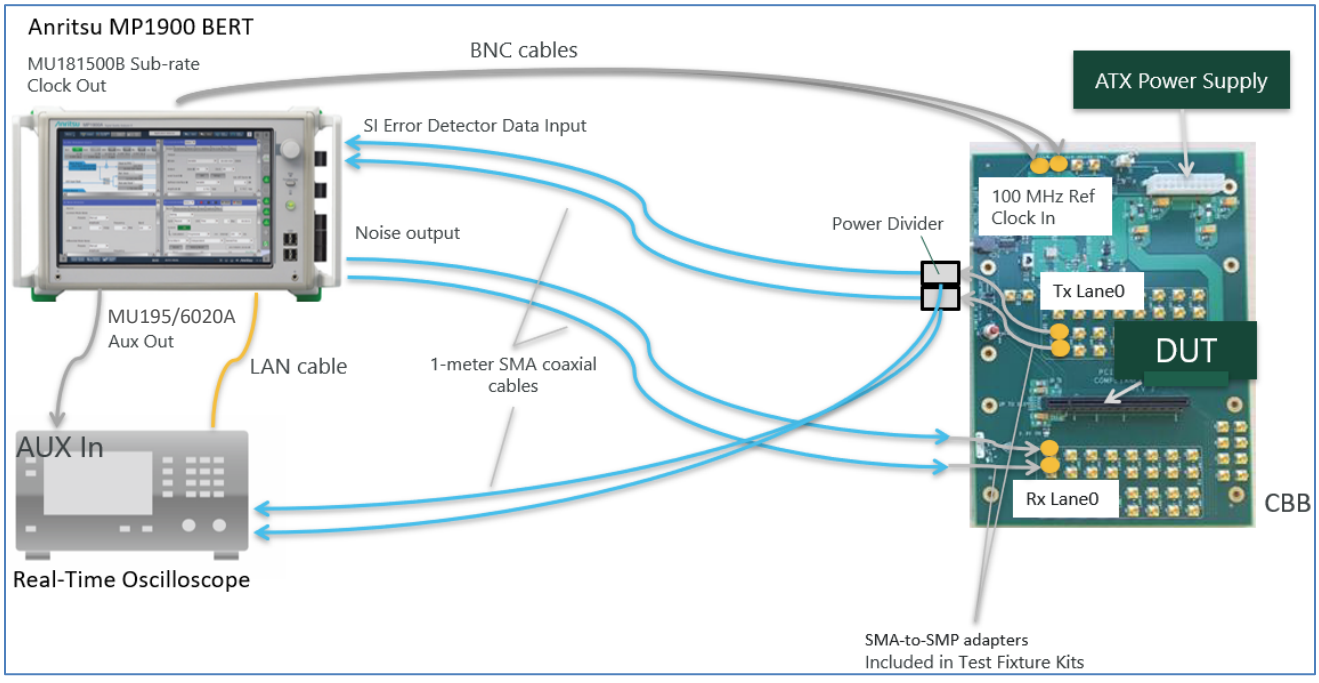


FIGURE 32. RECOMMENDED SETUP FOR DUT TX LINK EQ TESTING (PCIE GEN ¾ ADD-IN CARD)

1. Connect an ATX power supply to the CBB with DUT inserted.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to the CBB Rx Lane.
4. Connect the CBB Tx Lane to the power divider input ports through another set of SMA-to-SMP adapters.
5. Using BNC cables, connect the MU181500B sub-rate clock outputs to the CBB 100 MHz Ref Clock In connectors.
6. Using 1-meter SMA coaxial cables, connect the power divider outputs to the MU195040A data inputs for loopback error detection.
7. Using 1-meter SMA coaxial cables, connect the oscilloscope channels to the power divider tapped input ports.
8. Using a SMA-to-SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
9. Connect a LAN cable between the MP1900A BERT and the oscilloscope.

7.6 Set Up Automated DUT Rx Compliance Test

After Tx link EQ testing has successfully completed from previous section, proceed with testing for DUT Rx compliance (Rx link equalization / jitter tolerance) with the following setup.

7.6.1 Connect Equipment for System Board Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen 4 System Board DUT.

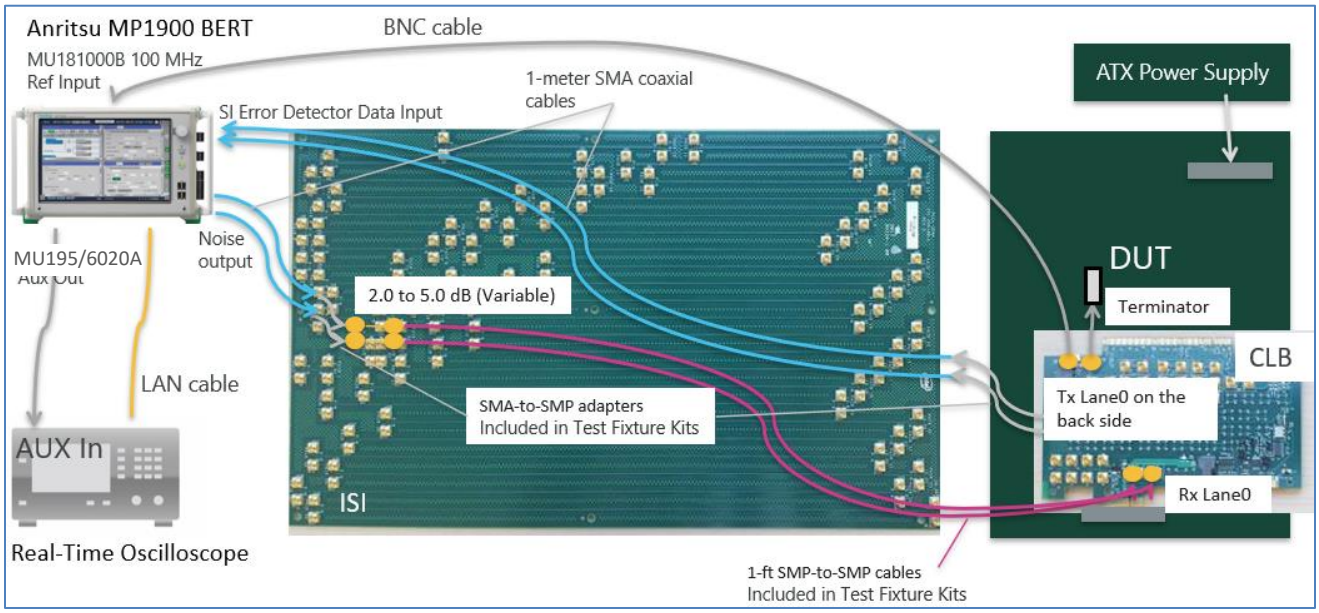


FIGURE 33. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIE GEN 4 SYSTEM BOARD)

1. Using the same setup from the system board Tx link EQ test, remove the power divider and its connection from the oscilloscope.
2. Connect the MU195050A noise outputs to 2.0-5.0 dB Variable ISI through the SMA-to-SMP adapters.
3. Using 1-ft SMP-to-SMP cables, connect the 2.0-5.0 dB Variable ISI with the CLB Rx Lane.
4. Connect the Tx Lane on the back of the CLB directly to the MU195040A data inputs for loopback error detection.

7.6.2 Connect Equipment for PCIE Gen 3 CEM M.2 (8 GT/s) System Board Rx Compliance Testing

The following Rx compliance test setup uses a PCIe M.2 compliance load board (CLB) test fixture for the PCIe Gen 3 System Board DUT.

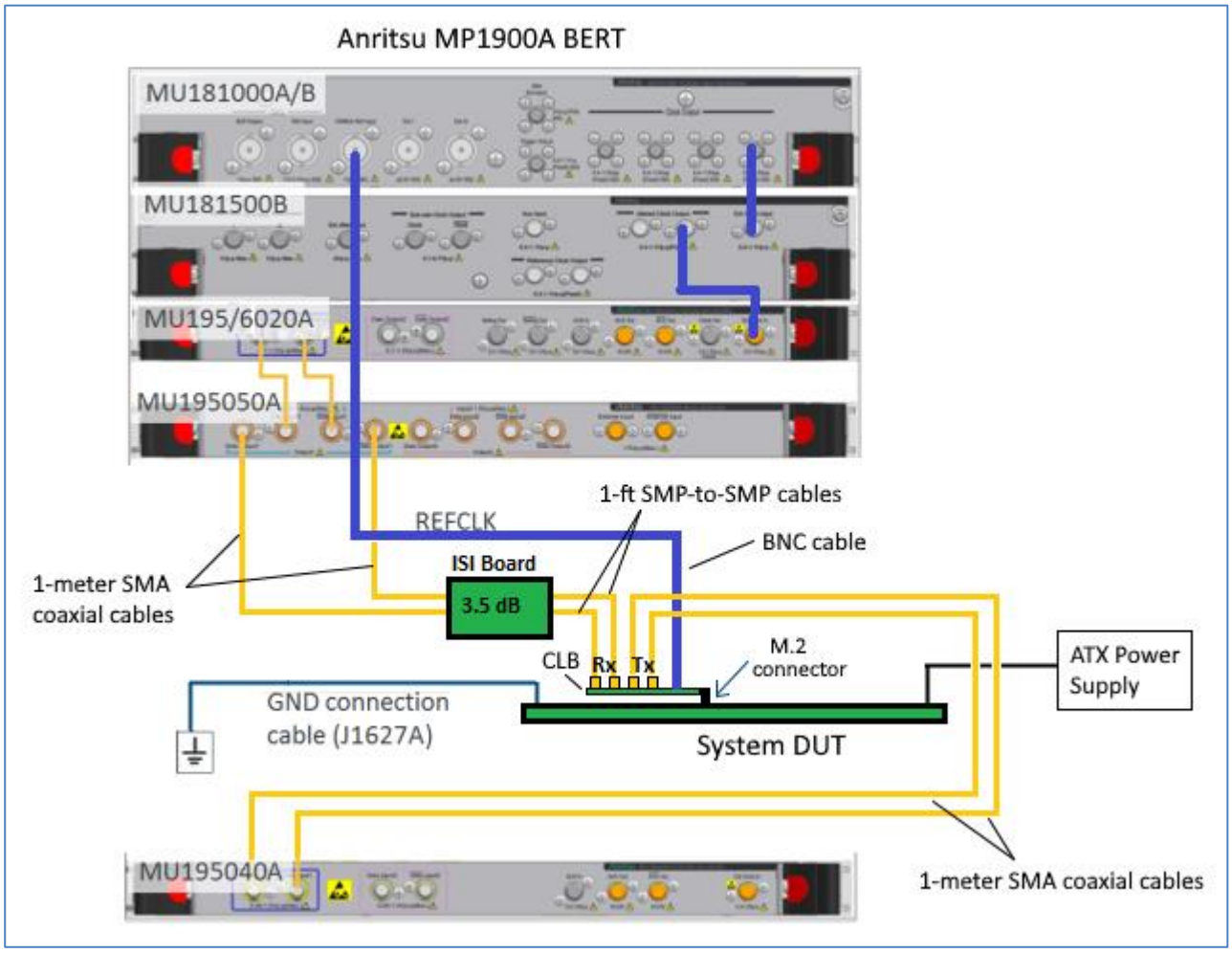


FIGURE 34. RECOMMENDED SETUP FOR DUT M.2 RX COMPLIANCE TESTING (PCIE GEN 3 SYSTEM BOARD)

1. Connect an ATX power supply to the DUT.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to 3.5 dB ISI through SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Using 1-ft SMP-to-SMP cables, connect the 3.5 dB ISI to the M.2 CLB Rx Lane.
4. Connect the Tx Lane of the M.2 CLB to the MU195040A data inputs for loopback error detection using 1-meter SMA coaxial cables.
5. Insert the M.2 CLB into the M.2 connector slot on the M.2 test fixture of the DUT.
6. Using a BNC cable, connect a M.2 CLB Ref Clock Out connector to the MU181000B 100 MHz Ref Clock In.
7. Using the J1627A GND connection cable, connect the M.2 CLB to ground.

7.6.3 Connect Equipment for Add-In Card Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen 4 Add-In Card DUT.

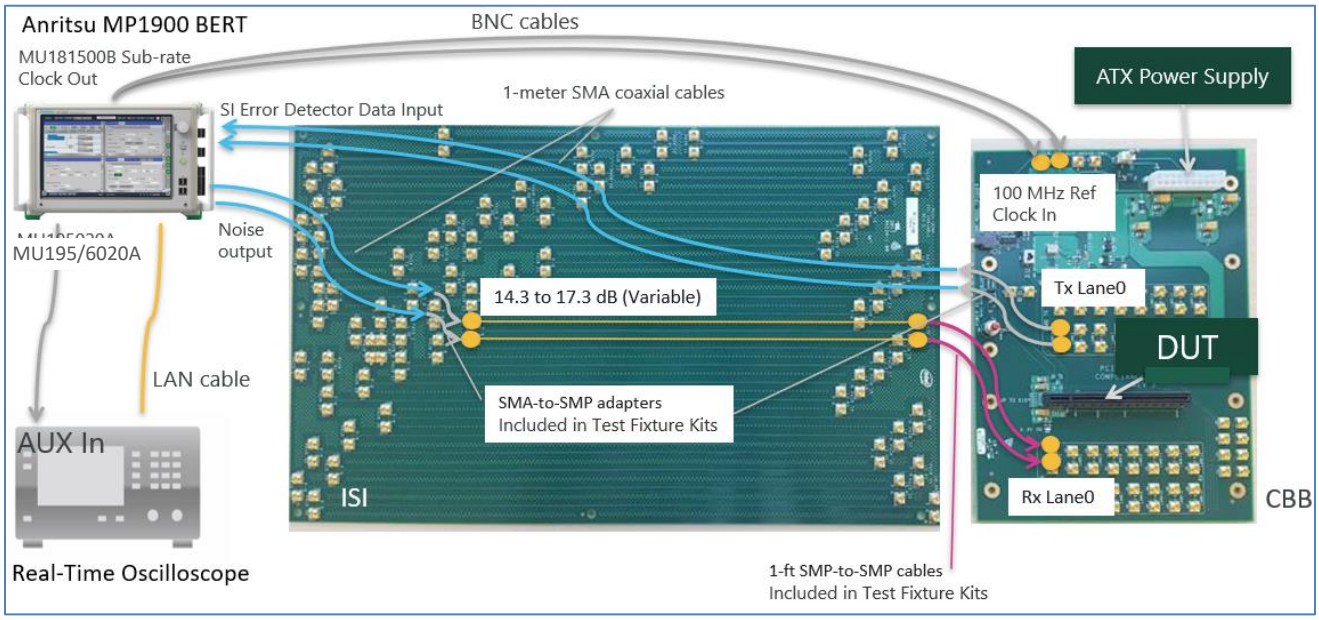


FIGURE 35. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIE GEN 4 ADD-IN CARD)

1. Using the same setup from the add-in card Tx link EQ test, remove the power divider and its connection from the oscilloscope.
2. Connect the MU195050A noise outputs to 14.3-17.3 dB Variable ISI through the SMA-to-SMP adapters.
3. Using 1-ft SMP-to-SMP cables, connect the 14.3-17.3 dB Variable ISI with the CBB Rx Lane.
4. Connect the CBB Tx Lane directly to the MU195040A data inputs for loopback error detection.

7.6.4 Connect Equipment for PCIE Gen 3 CEM M.2 (8 GT/s) Add-In Card Rx Compliance Testing

The following Rx compliance test setup uses a PCIe M.2 compliance base board (CBB) test fixture for the PCIe Gen 3 Add-In Card DUT.

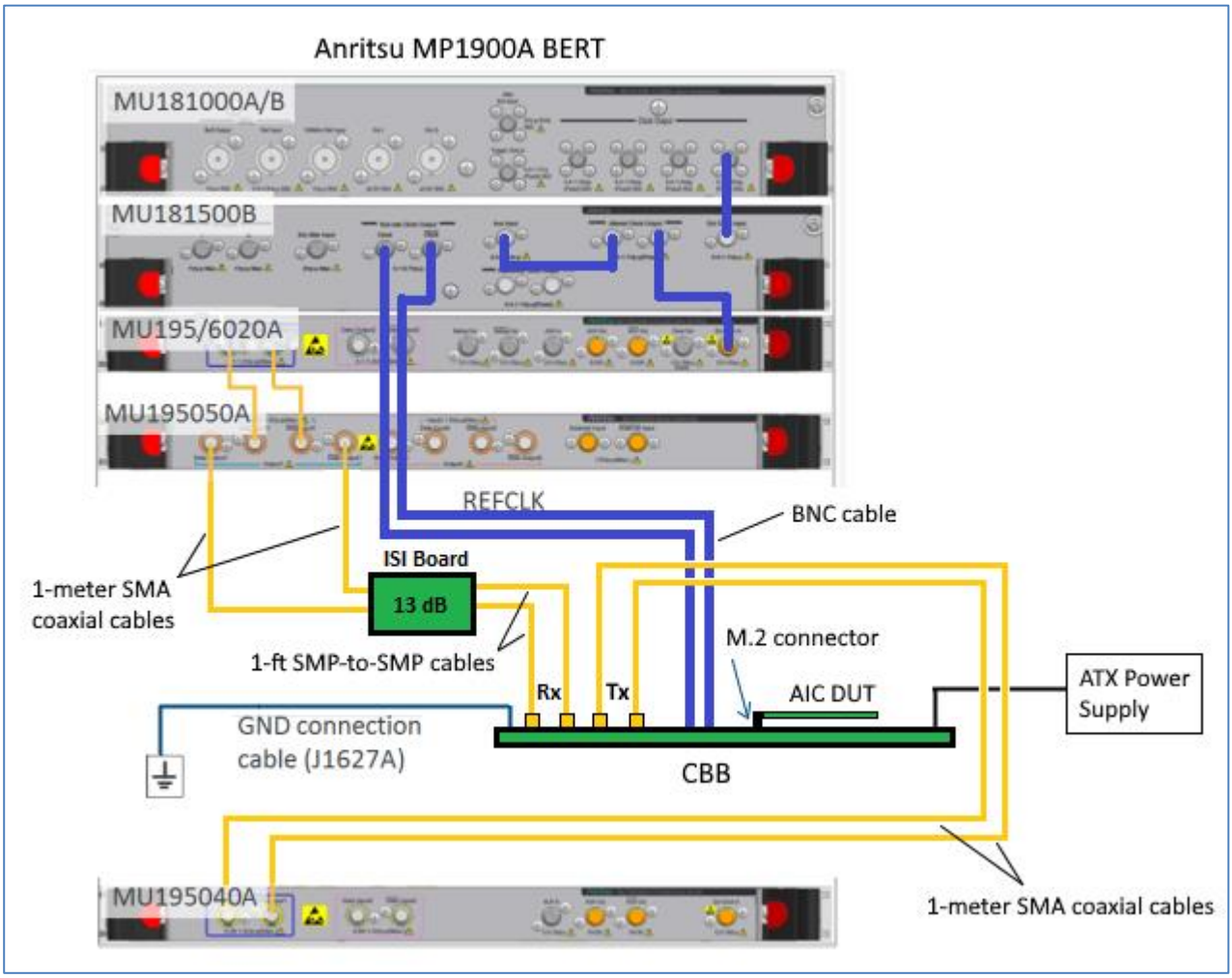


FIGURE 36. RECOMMENDED SETUP FOR DUT M.2 RX COMPLIANCE TESTING (PCIE GEN 3 ADD-IN CARD)

1. On the MU181500B, connect the jittered clock output to the Aux input using a SMA-SMA short cable.
2. Connect an ATX power supply to the M.2 CBB with DUT inserted into the M.2 connector slot.
3. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to 13 dB ISI through SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
4. Using 1-ft SMP-to-SMP cables, connect the 13 dB ISI to the M.2 CBB Rx Lane.
5. Connect the Tx Lane of the M.2 CBB to the MU195040A data inputs for loopback error detection using 1-meter SMA coaxial cables.
6. Using BNC cables, connect the MU181500B sub-rate clock outputs to the M.2 CBB 100 MHz Ref Clock In connectors.
7. Using the J1627A GND connection cable, connect the M.2 CBB to ground.

7.7 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL PCIe CEM 4.0 Rx Test Application menu to access the Setup Configuration page.

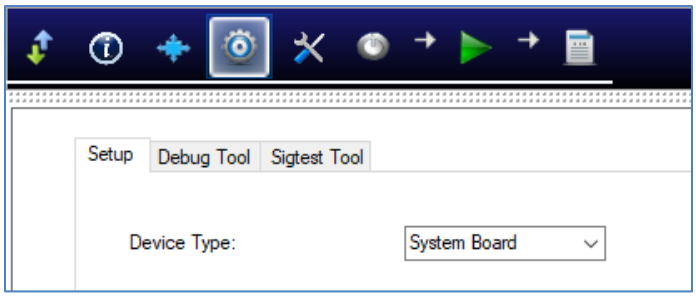


FIGURE 37. SET UP TEST REQUIREMENTS

7.7.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the DUT.

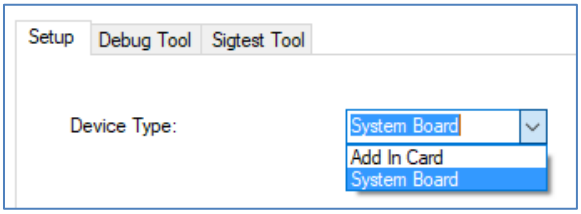


FIGURE 38. SELECT DUT TYPE

7.8 Select PCIe CEM 4.0 Rx Tests

After selecting the DUT type, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 4.0 Rx tests to be run. Select the check box(s) for the required Rx tests.

Note: When running tests for the first time or changing anything in the setup, it is suggested to perform calibration first. If calibration is not completed, attempting to run the Rx tests will throw errors.

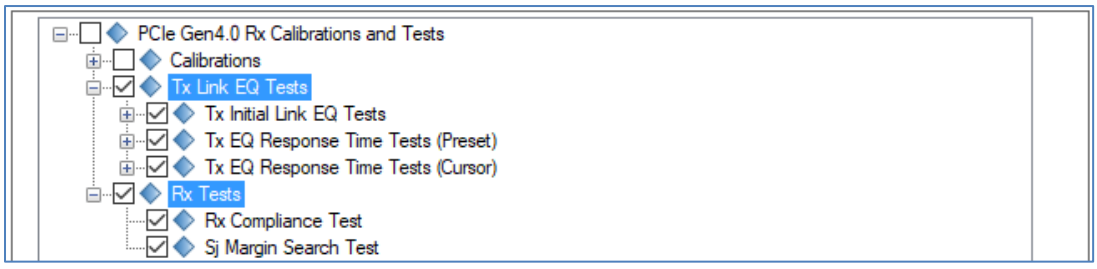


FIGURE 39. SELECT RX TESTS

7.8.1 Select to Run DUT Link Training and Rx Compliance Test

Select the 'Tx Link EQ Tests' group and 'Rx Compliance Test' to prepare and test the DUT for compliance with the PCIe CEM 4.0 Rx specifications. The GRL software will automatically run the link equalization test sequence when initiated. *Note the 'Tx Initial Link EQ' test is only available when Add-in Card is selected as the DUT in the Setup Configuration page (see Figure 38).*

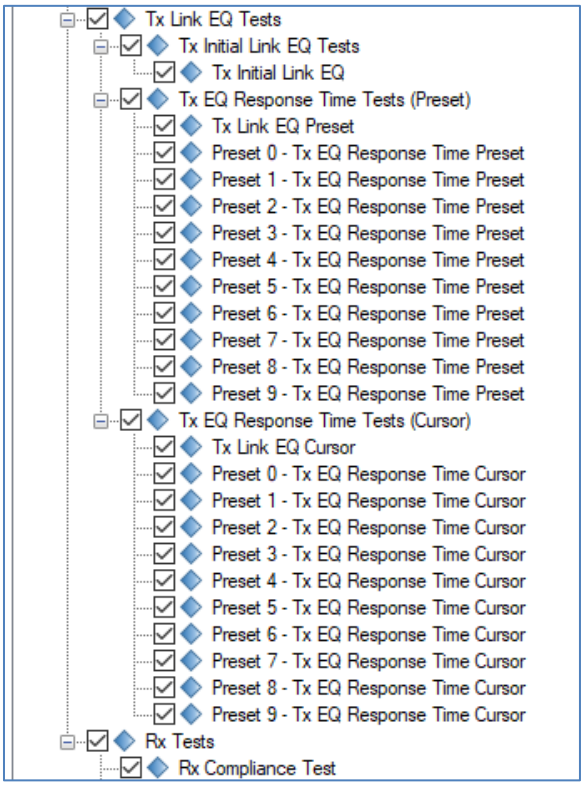


FIGURE 40. SELECT DUT TX LINK EQ AND RX COMPLIANCE TESTS

7.8.2 Select to Run SJ Margin Search Test

Select 'Sj Margin Search Test' to perform an optional test to conduct a SJ margin search for jitter tolerance. The GRL software will automatically run the selected test when initiated.

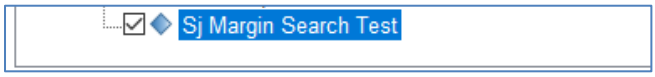


FIGURE 41. SELECT SJ MARGIN SEARCH TEST

7.9 Configure Test Parameters

After selecting the desired tests, select from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.

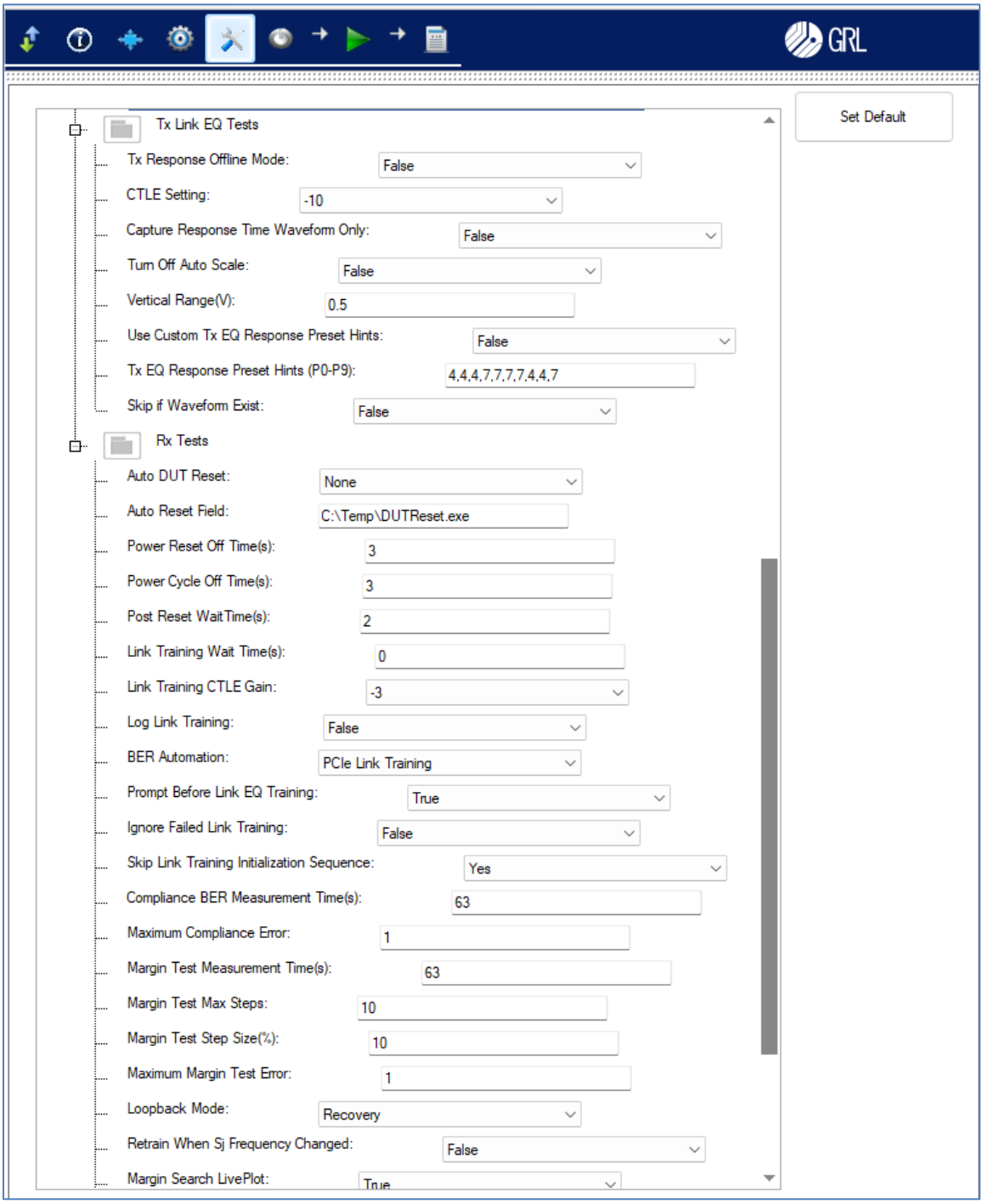


FIGURE 42. TEST PARAMETERS CONFIGURATION PAGE

TABLE 6. TEST PARAMETERS DESCRIPTION

Parameter	Description
Tx Response Offline Mode	Select 'True' to enable running Tx link equalization response tests in offline mode using appropriate offline PCIe compliant waveforms.
CTLE Setting	Select the CTLE method or gain setting index to be used when decoding PCIe compliant waveforms to verify Tx equalization change during link equalization response tests.
Capture Response Time Waveform Only	Select 'True' to enable capturing waveform data for time response verification only when running Tx link equalization response tests.
Turn Off Auto Scale	Select 'True' to disable auto scaling during Tx link equalization response tests.
Vertical Range	Set the vertical range of the Scope to easily detect a change to the voltage level when running Tx link equalization response tests.
Use Custom Tx EQ Response Preset Hints	Select 'True' to enable custom preset hints to be used when running Tx link equalization response tests.
Tx EQ Response Preset Hints (P0-P9)	If 'True' is selected from the '**Use Custom Tx EQ Response Preset Hints**' field, specify the custom preset hints for Preset 0 to Preset 9.
Skip If Waveform Exist	Select 'True' to skip the Tx link equalization response tests if there are existing waveforms.
Auto DUT Reset	Select which controller device connected with the GRL software to be used to perform auto reset for the DUT as required during test runs.
Auto Reset Field	If auto DUT reset is enabled, specify the directory of the auto DUT reset file to be used.
Power Reset Off Time	Set the duration in seconds to reset the power for the system under test when internal power reset mechanism is used.
Power Cycle Off Time	Set the duration in seconds to cycle the power for the system under test when internal power cycle mechanism is used.
Post Reset Wait Time	Set the delay/buffer in seconds after power is reset for the system under test.
Link Training Wait Time	Set the delay/buffer in seconds before initiation of each link training step.
Link Training CTLE Gain	Select the CTLE gain for the BERT error detector.
Log Link Training	Select 'True' to enable logging for the link training steps.
BER Automation	Select 'PCIe Link Training' to run BER automation tests using Anritsu PCIe Link Sequencer software loopback method, or select 'Manual' to run BER automation tests manually.

Prompt Before Link EQ Training	Select 'True' to enable a prompt to come up prior to start running Rx link equalization tests.
Ignore Failed Link Training	Select 'True' to ignore tests that have failed when running the PCIe loopback link training sequence.
Skip Link Training Initialization Sequence	Select 'Yes' to skip the initial loopback link training sequence.
Compliance BER Measurement Time	Set the duration in seconds to complete the Rx compliance testing to measure Bit Error Ratio (BER).
Maximum Compliance Error	Set the maximum error count for error checking during Rx compliance test runs.
Margin Test Measurement Time	Set the duration in seconds to complete the Rx SJ margin search testing.
Margin Test Max Steps	Set the maximum number of steps for stepping through margins during the SJ margin search test.
Margin Test Step Size	Set the step size in percentage for stepping through margins during the SJ margin search test.
Maximum Margin Test Error	Set the maximum error count for error checking during the SJ margin search test.
Loopback Mode	Select 'Recovery' (recommended) or 'Configuration' to be used as the link training method for placing the DUT in the loopback state.
Retrain When SJ Frequency Changed	Select 'True' to re-send link training sequence when there is a change in the SJ frequency.
Margin Search Live Plot	Select 'True' to enable a graphical margin plot that updates as the margin test is performed to indicate progress of the test results.
Apply CM	Select 'Yes' to integrate the common mode component in a specific test.
PPG Start Preset	Select the preset co-efficient to be used at the start of link training.
DUT Initial Preset	Select the initial preset co-efficient for the DUT to be applied during Rx compliance test runs.
PPG Final Preset	Select the preset co-efficient to be used after link training is successful for the final BER test. If 'Auto' is selected, a negotiated preset will be applied during the final BER test.
DUT Final Preset	Select the preset co-efficient for the DUT to be applied during the final BER test.

7.10 Enable Loopback BER Test

To set up the GRL software to automate loopback testing for error detection, go to the Equipment Setup page and type in the VISA address that connects to the Anritsu MX183000A High-Speed Serial Data Test Software.

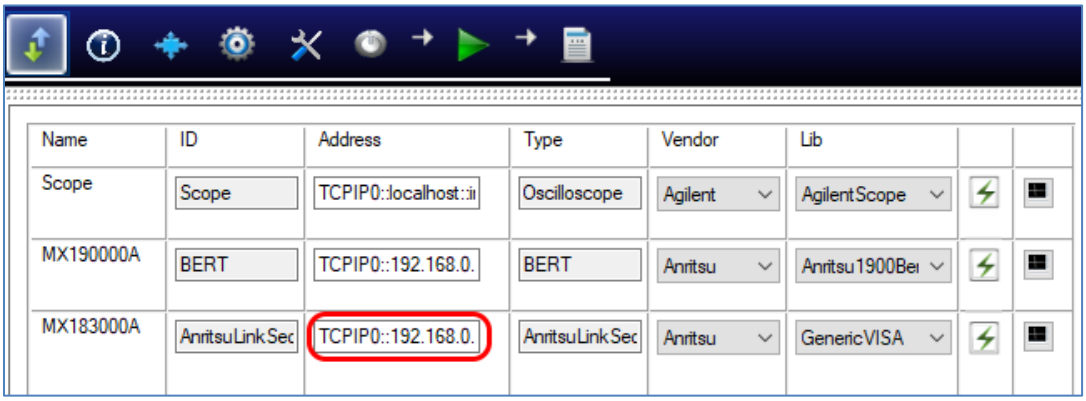


FIGURE 43. CONNECT EQUIPMENT FOR LOOPBACK BER TEST

On the Configurations page, select the BER Automation test method as 'PCIe Link Training' to enable the Anritsu PCIe Link Sequencer software loopback mode. Additional configurations can also be made through this page.

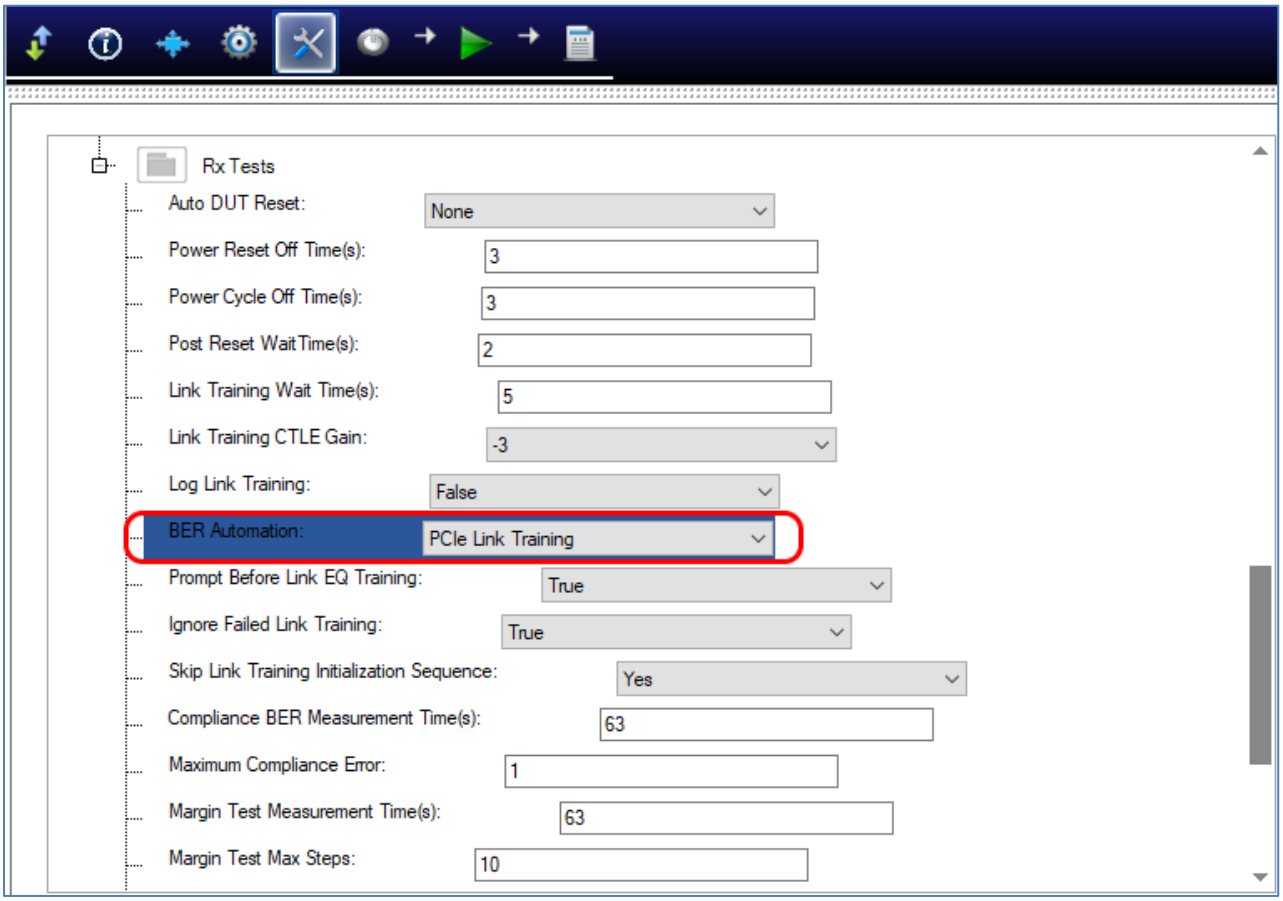


FIGURE 44. SELECT BER LOOPBACK TEST METHOD

7.11 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE4-CEM-RXA software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

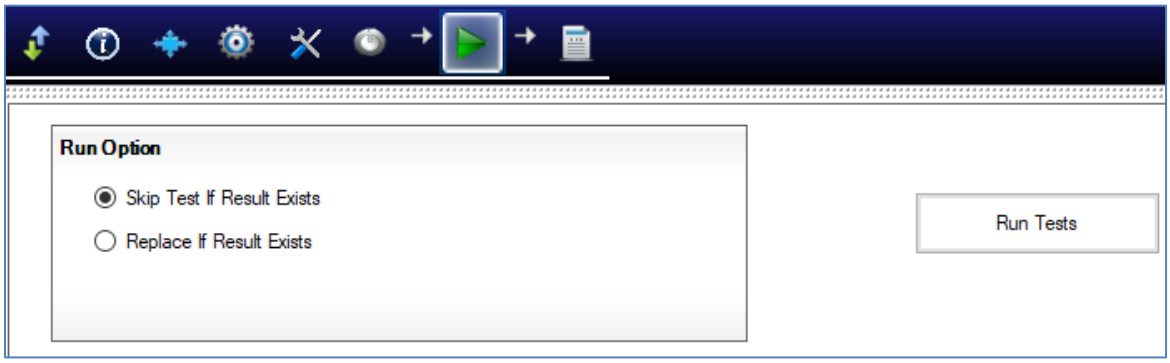


FIGURE 45. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed.

8 Interpreting GRL-PCIE4-CEM-RXA Test Report

When all calibration and test runs have completed from the previous section, the GRL-PCIE4-CEM-RXA software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

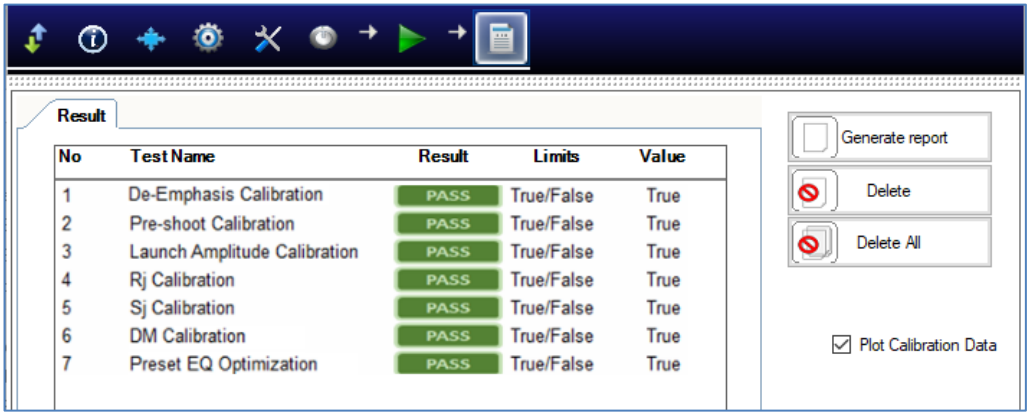


FIGURE 46. TEST REPORT PAGE

8.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

8.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.

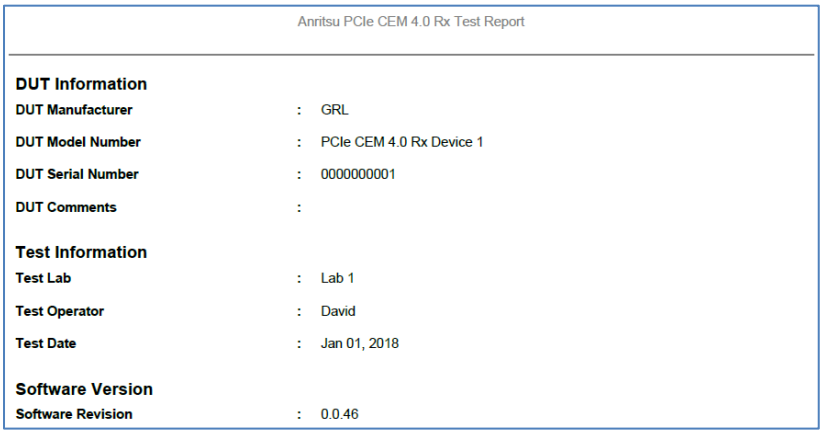


FIGURE 47. TEST SESSION INFORMATION EXAMPLE

8.1.2 Test Summary Table

This table provides an overall view of all the calibration and tests performed along with their conditions and results.

Anritsu PCIe CEM 4.0 Rx Test Report

No	TestName	Limits	Value	Results
1	De-Emphasis Calibration	True/False	True	Pass
2	Pre-shoot Calibration	True/False	True	Pass
3	Launch Amplitude Calibration	True/False	True	Pass
4	Rj Calibration	True/False	True	Pass
5	Sj Calibration	True/False	True	Pass
6	DM Calibration	True/False	True	Pass
7	Preset EQ Optimization	True/False	True	Pass
8	FInal ISI Calibration	True/False	True	Pass
9	DM Optimization	True/False	True	Pass
10	Final Eye Calibration	True/False	True	Pass
11	Rx Compliance Test	True/False	True	Pass
12	Sj Margin Search Test	True/False	True	Pass

FIGURE 48. TEST SUMMARY TABLE EXAMPLE

8.1.3 Test Results

This portion displays the results in detail along with supporting data points and screenshots for each calibration/test run.

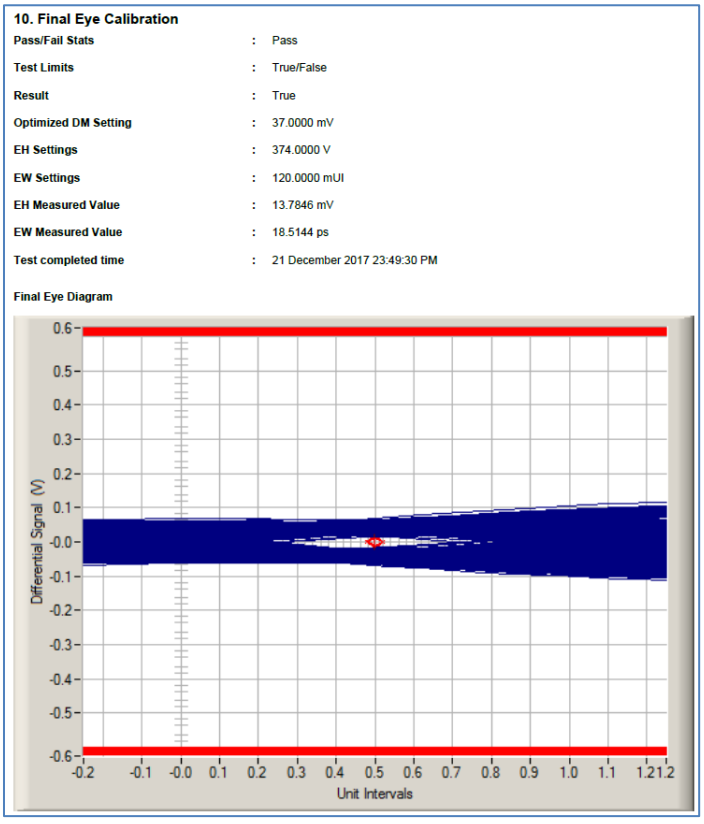


FIGURE 49. TEST RESULTS EXAMPLE

8.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

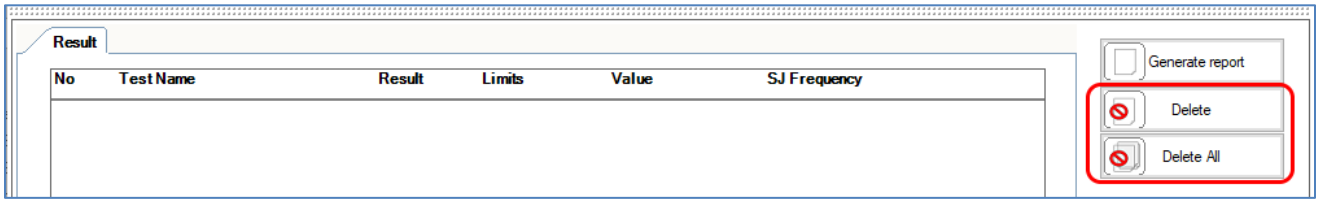


FIGURE 50. DELETE TEST RESULTS

9 Saving and Loading GRL-PCIE4-CEM-RXA Test Sessions

The usage model for the GRL-PCIE4-CEM-RXA software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To ***create a new test session*** and return the application back to the default configuration, select Options → 'New Session'.

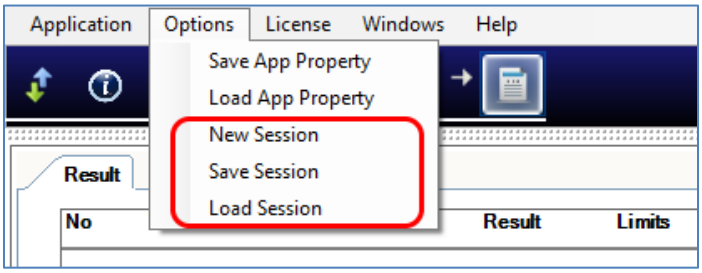


FIGURE 51. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

10 Appendix A: Method of Implementation (MOI) for Manual PCIe CEM 4.0 Receiver Measurements

This section describes how to manually perform PCIe CEM 4.0 Rx calibration and DUT compliance testing based on Anritsu's recommended test procedure using the MP1900A BERT.

The following steps give a general overview for testing the PCIe CEM 4.0 receiver.

i) Calibrate for the following components:
   - Channel Loss measurement with a vector network analyzer (VNA)
   - Eye Amplitude, Preset, SJ and RJ measurements with MP1900A BERT and high-performance real-time oscilloscope
   - DM Amplitude and Eye Height/Eye Width measurements with MP1900A BERT and high-performance real-time oscilloscope

ii) Perform link training sequence for BER loopback testing:
   - Enable DUT loopback mode for error detection with MP1900A BERT
   - Troubleshoot in the case of link training failure

iii) Test for DUT Rx compliance to target specifications:
   - BER compliance checking for <1E-12 with stressed eye
   - SJ marginal testing (optional)

Note: Existing PCI-SIG Compliance Load Boards (CLB's) and Compliance Base Boards (CBB's) will be used as test fixtures for system host and device DUT's respectively.

10.1 Perform Calibration

This section describes how to calibrate for the stressed test signal before testing the receiver for compliance.

Calibration is initially performed for Channel Loss, followed by Eye Amplitude and Presets, RJ and SJ, and DM-SI. The final step is to determine the Eye Width (EW) and Eye Height (EH).

The main equipment required for calibration consists of the MP1900A BERT, high performance real-time oscilloscope, and vector network analyzer. The SigTest application will also be used to ensure signal quality compliance.

10.1.1 Calibration Settings

Configure the following settings to be applied for PCIe Gen 3 and Gen 4 based Rx calibration.

Note: In addition to these settings, you will need to load a pre-defined preset file for the MP1900A Pulse Pattern Generator. Please refer to Anritsu for this preset file.

TABLE 7. CALIBRATION SETTINGS

Component	Setting	PCIe Gen 3	PCIe Gen 4
Variable ISI Board	Insertion Loss (dB)	28	30*
	CBB Pair No.	–	No. 31*
	CLB Pair No.	–	No. 0*
SigTest	CTLE Gain (dB)	–	8.5 to 10.5
MP1900A BERT	Tx Emphasis Preset	P7	P5, P6
	Amplitude (mV)	550 *(800 mVpp-diff at output of Noise Module)*	550 *(800 mVpp-diff at output of Noise Module)*
	RJ (mUIpp)	240	224
	SJ @100 MHz (Uipp)	0.1	0.1
	DM-I (mV)	59	27
	CM-I (mVpp)	–	190.0
	BUJ (pspp)	10.0	–

** Using the Serial 10 add-in card full channel configuration for 30dB channel. Note the insertion loss measures in between 27, 28, and 30 dB for all configurations using different variable ISI pairs that provide the correct amount of insertion loss being measured.*

The following results have been obtained from calibration using the above configuration setup and measured with the oscilloscope and SigTest application.

TABLE 8. CALIBRATION RESULTS

Setting	PCIe Gen 3	PCIe Gen 4
Amplitude (mV)	792.3790	780.8660
RJ (psrms)	3.25	1.0321
SJ @100 MHz (mUIpp)	83.6735	88.8416
DM-I (mVpp)	40	13.9740
CM-I (mVpp)	–	150.2
EH (mV)	44.9907 *(Target range: 41 to 46 mV)*	15.7582 *(Target range: 13.5 to 16.5 mV)*

Setting	PCIe Gen 3	PCIe Gen 4
EW (ps)	40.3372 *(Target range: 39.25 to 41.25 ps)*	18.6501 *(Target range: 18.25 to 19.25 ps)*

10.1.2 Calibration Process

Calibration for the PCIe CEM 4.0 electrical specification will basically be performed at two physical test points: TP1 and TP2 (for the Long Channel). Test Point 1 (TP1) is a physical test point for calibration without the effect of a channel. For PCIe Gen 4, an adjustable CEM connector will be used along with the calibration channel for testing the receiver. This will need to adjust the eye amplitude to specification values when measuring eye height/eye width. TP2 is a physical test point that will affect the eye opening due to trace length.

For the Long Channel TP2 calibration, an existing PCI-SIG CLB test fixture will be used as the host system board or PCI-SIG CBB test fixture for the add-in card device. The board will be connected between the BERT noise generator output and the oscilloscope which will validate the test pattern of the signal and measure for stress tolerance to final stressed eye compliance.

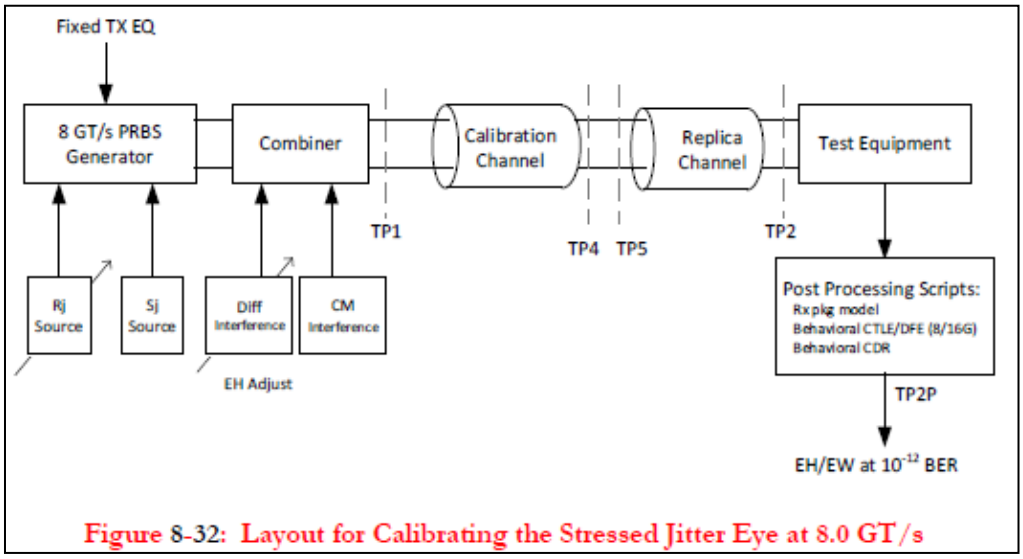


FIGURE 52. CTS RX CALIBRATION DIAGRAM FOR PCIE GEN 3

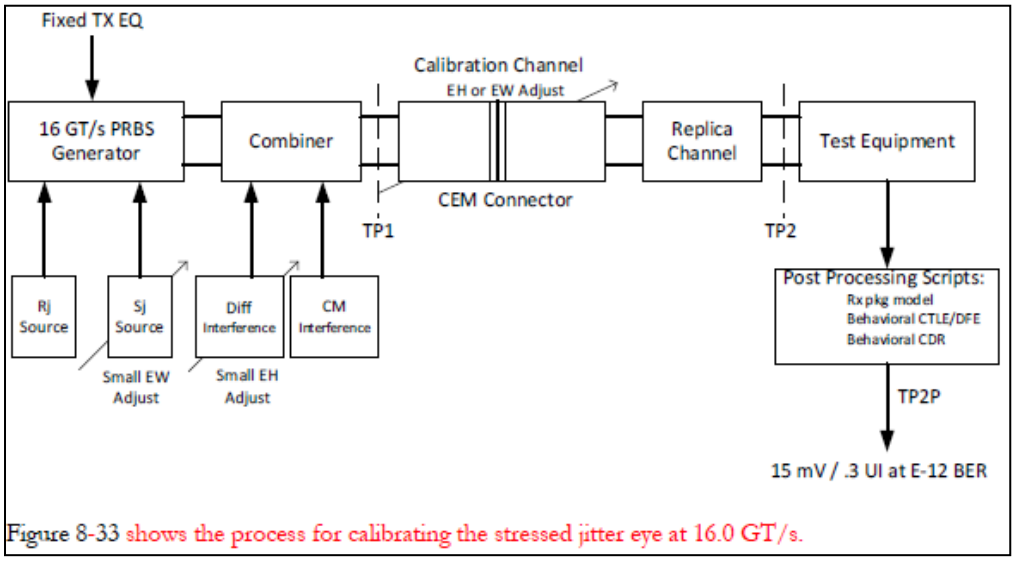


FIGURE 53. CTS RX CALIBRATION DIAGRAM FOR PCIE GEN 4

10.1.3 Channel Loss Calibration (for PCIe Gen 4)

The following connection diagram shows the channel loss calibration setup for PCIe Gen 4 using a 4-port (differential) vector network analyzer (VNA) and a compliant CLB/CBB test fixture. *Note this setup refers to the parameters given in Section 10.1.1, Calibration Settings.*

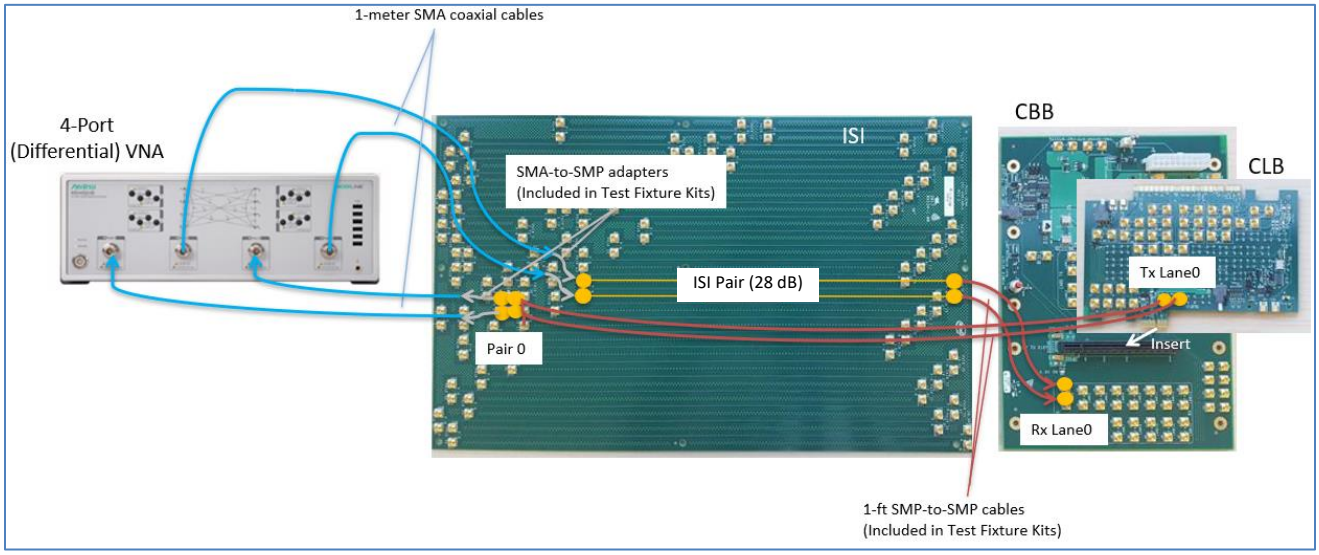
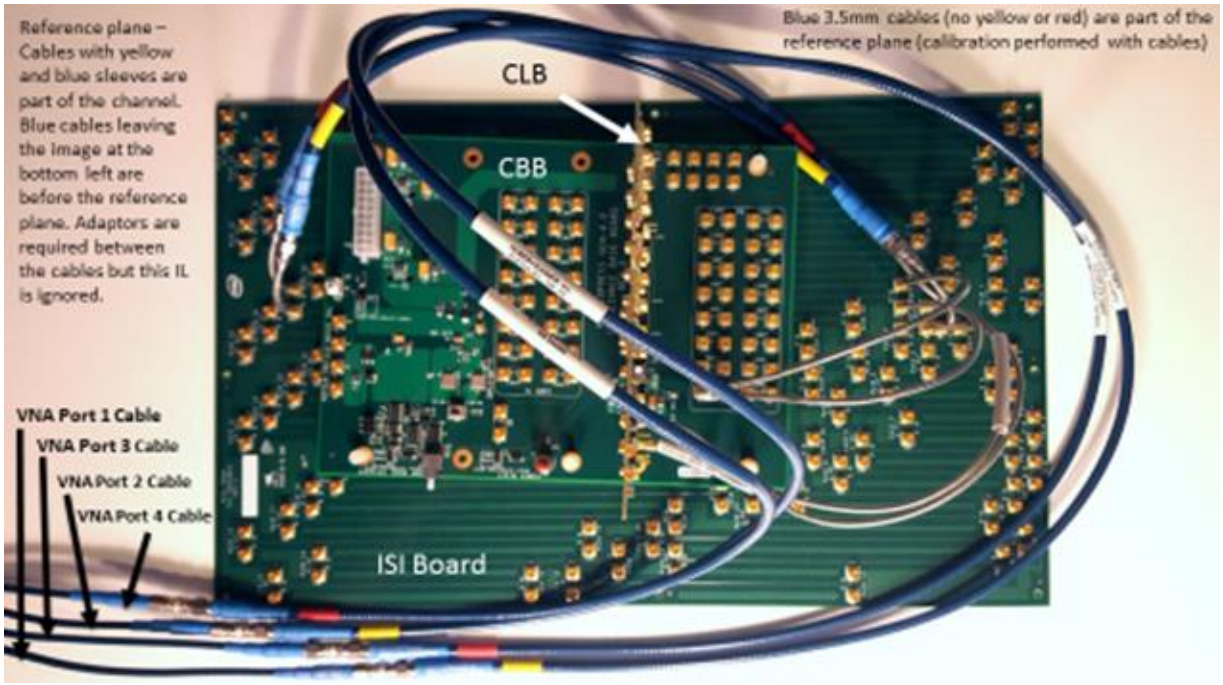


FIGURE 54. CONNECTION DIAGRAM FOR CHANNEL LOSS CALIBRATION

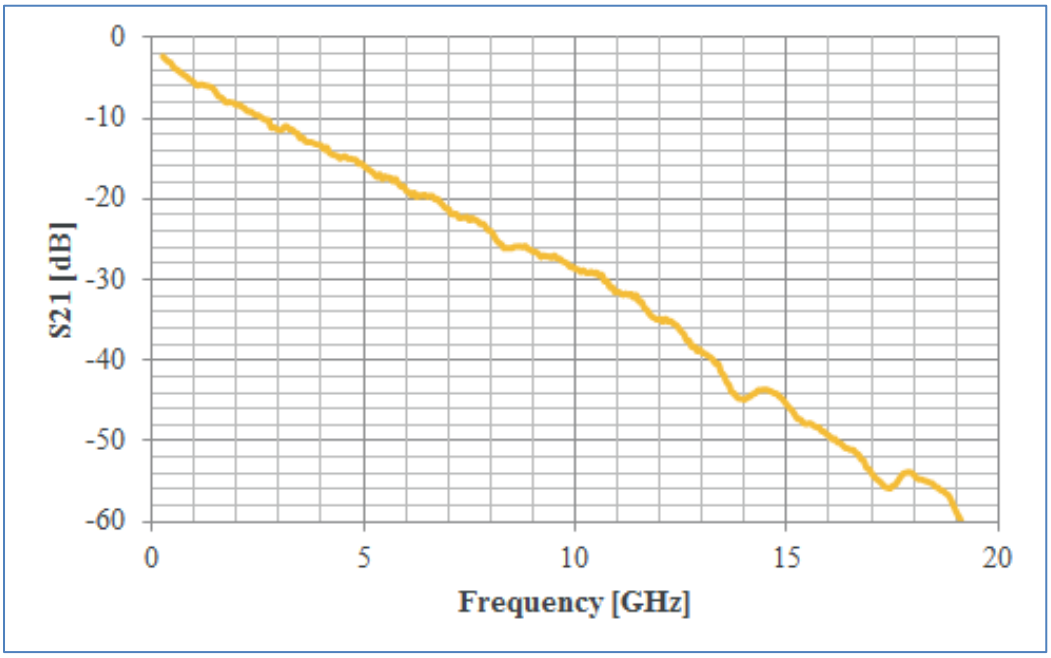
1. Using 1-meter SMA coaxial cables, connect the VNA outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
2. Connect the SMA-to-SMP adapters to ISI Pair (28 dB) *[physical ISI loss of 23 dB for the system board or 25 dB for the add-in card]*.

3. Using 1-ft SMP-to-SMP cables, connect the ISI Pair (28 dB) with the CBB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*
4. Insert the CLB into the designated slot on the CBB.
5. Connect the CLB Tx Lane using 1-ft SMP-to-SMP cables to ISI Pair 0.
6. Connect the ISI Pair 0 through the SMA-to-SMP adapters using 1-meter SMA coaxial cables to the oscilloscope channels.

An example of PCIe Gen 4 CLB/CBB test fixture connections for device Rx channel loss calibration is as shown below *(extracted from the PCI Express Architecture PHY Test Specification Revision 4.0)*.



Calibrate the Insertion Loss to within the limits of 27 to ~30 dB as shown in the following graph example.



10.1.4 Amplitude, Preset, SJ and RJ Calibration Setup

The following connection diagram shows the calibration setup for amplitude, preset, SJ, and RJ at TP1 without any channel effect. The MP1900A BERT is directly connected to a digital oscilloscope supporting >25 GHz bandwidth and >80 GS/s sampling rate.

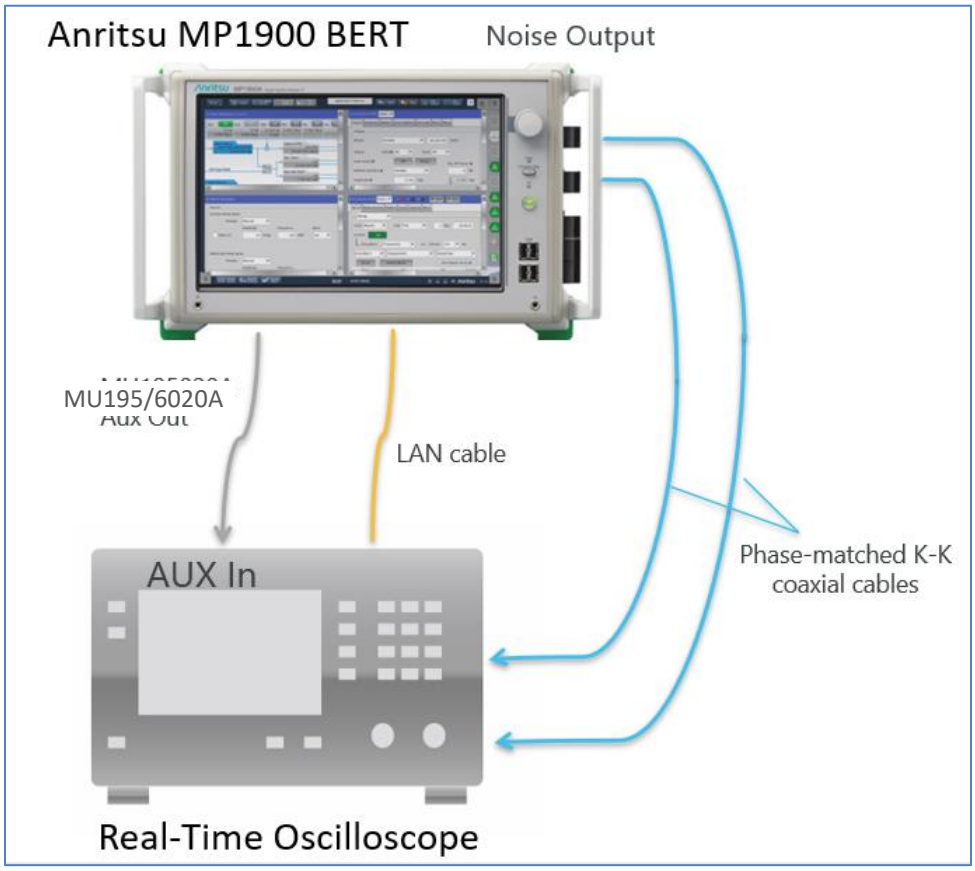


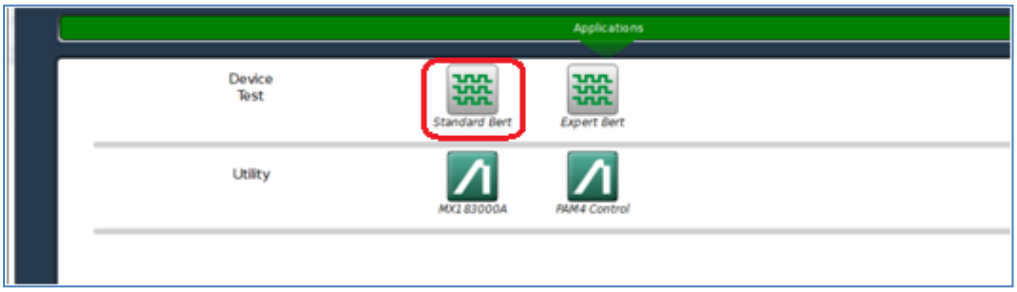
FIGURE 55. CONNECTION DIAGRAM FOR AMPLITUDE, PRESET, SJ AND RJ CALIBRATION

1. Set up the MP1900A BERT connections as described in Section 6.1.
2. Connect the MU195050A noise outputs to the relevant oscilloscope channels using phase-matched K-K coaxial cables.
3. Using a SMA-to-SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope for pattern sync triggering. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
4. Connect a LAN cable between the MP1900A BERT and the oscilloscope.

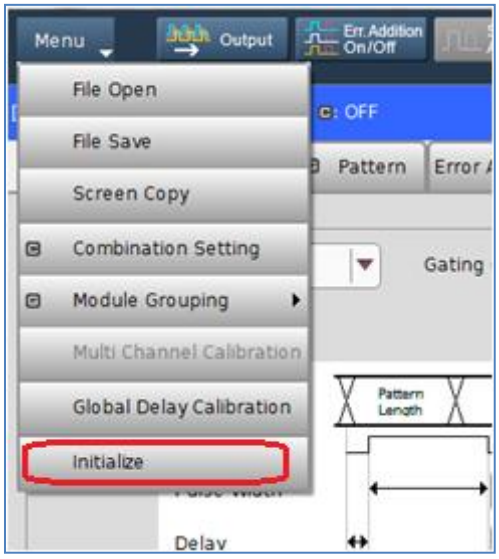
10.1.5 Anritsu Standard BERT Device Test Application (MX190000A) Startup

To adjust the calibration parameters when measuring on the Scope, use the MX190000A Standard test application on the MP1900A BERT.

1. On the BERT's Applications screen, select the MX190000A Standard Bert application.



2. In the drop-down Menu, select 'Initialize' to start using the application.

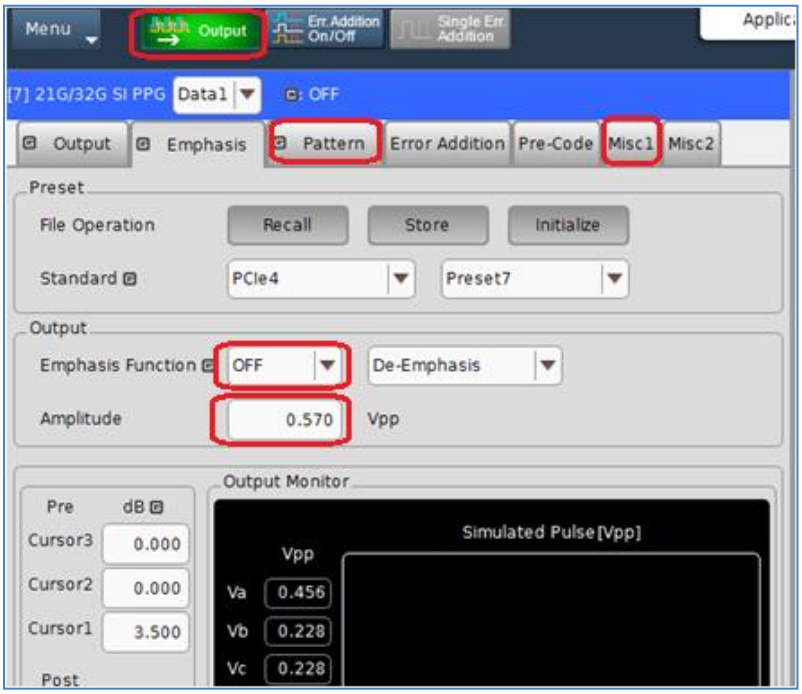


10.1.6 Amplitude Calibration Adjustment

Adjust the Amplitude with Scope markers to 800 mVpp(diff) using the following configuration.

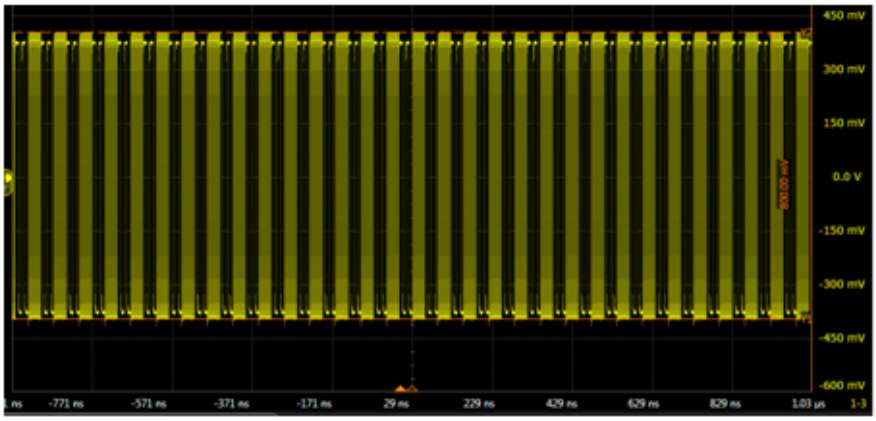
a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: 64zeros_64ones_128bit10
- Select the Misc1 tab- Aux Output: Pattern Sync



b) Scope Settings:

- Averaging: 16 points
- Horizontal Scale: 100 ns/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s



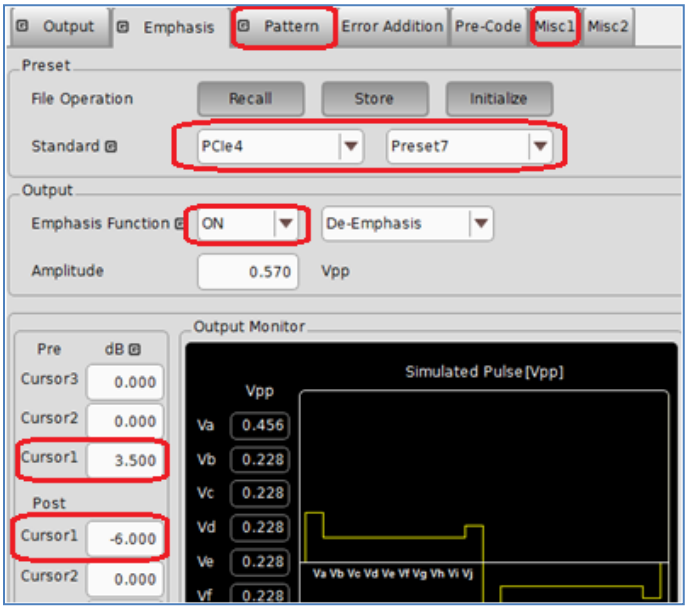
Peak amplitude measurement on Scope

10.1.7 Preset Calibration Adjustment

Adjust the Pre and Post Cursor1 of Presets 0 to 9 with Scope markers using the following configuration.

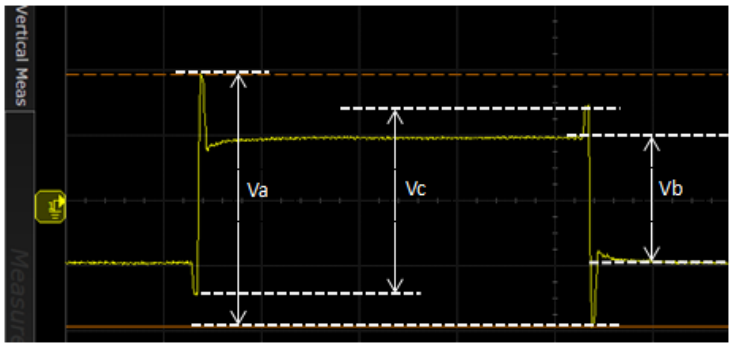
a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: ON
- Select the Pattern tab- Test Pattern: 64zeros_64ones_128bit10
- Select the Misc1 tab- Aux Output: Pattern Sync



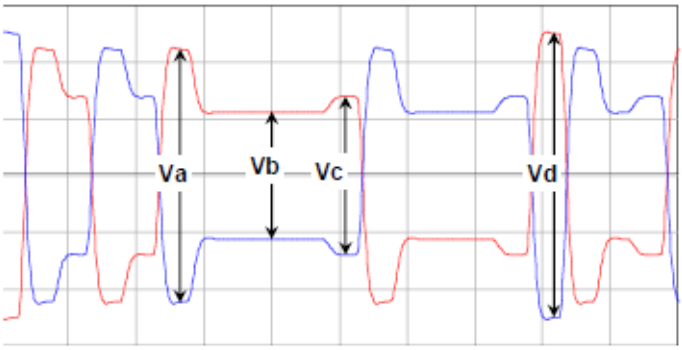
b) Scope Settings:

- Averaging: 16 points
- Horizontal Scale: 1 ns/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s



De-emphasis = 20log10(Vb/Va)

Preshoot = 20log10(Vc/Vb)



De-emphasis = 20 $\log_{10}$Vb/Va
Preshoot = 20$\log_{10}$Vc/Vb
Boost = 20$\log_{10}$ Vd/Vb

Figure 8-5: Definition of Tx Voltage Levels and Equalization Ratios

Table 8-1. Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c-1	c+1	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Notes:

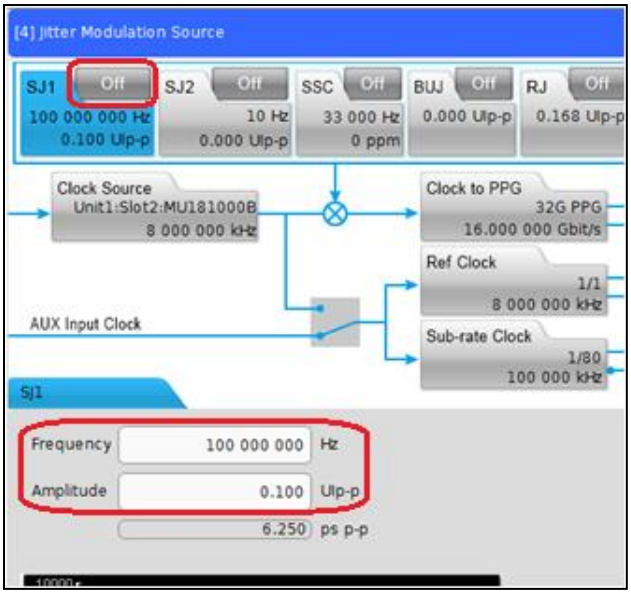
1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises

10.1.8 SJ Calibration

Capture five waveforms for each condition on the Scope and analyze SJ using SigTest. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen4_P0
- Select Jitter Modulation Source- SJ1: ON
- SJ1 Frequency and Amplitude: 100 MHz, 0.000 Uipp (as reference)
- SJ1 Frequency and Amplitude: 100 MHz, 0.100 Uipp



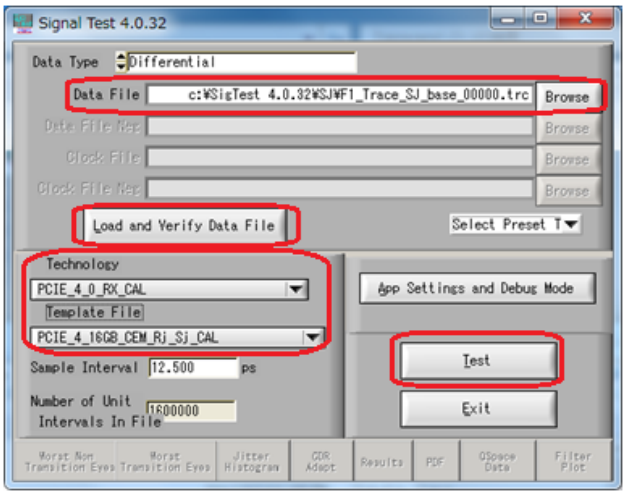
b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 10 µs/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s

c) SigTest Settings:

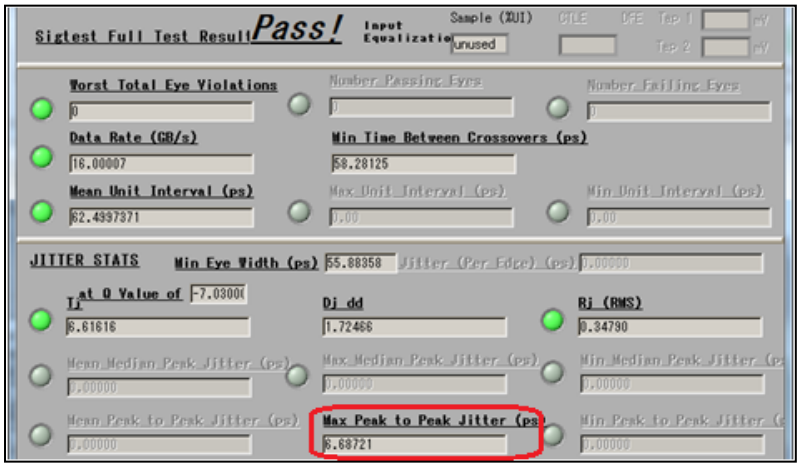
- Select a Data File
- Select 'Load and Verify Data File'
- Select Technology as 'PCIE_4_0_RX_CAL'

- Select Template File as 'PCIE_4_16GB_CEM_Rj_Sj_CAL'
- Select 'Test'

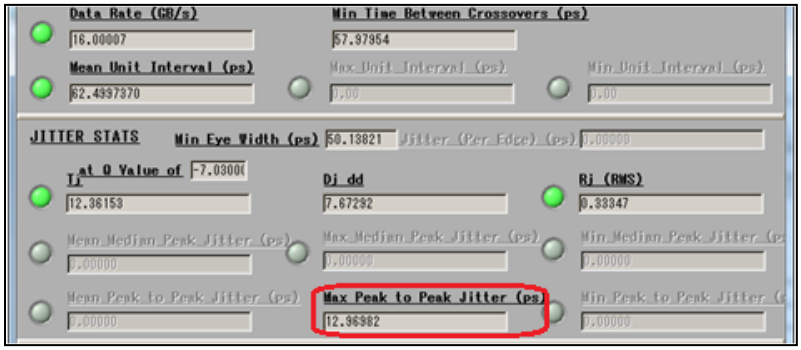


d) SigTest Results:

- Read 'Max Peak to Peak Jitter (ps)' value



Base value: 6.69 pspp



Jittered value: 12.97 pspp (at 0.110 Uipp)

- Calculate SJ by subtracting the Jittered and Base values- *12.97 – 6.69 = 6.28 pspp*

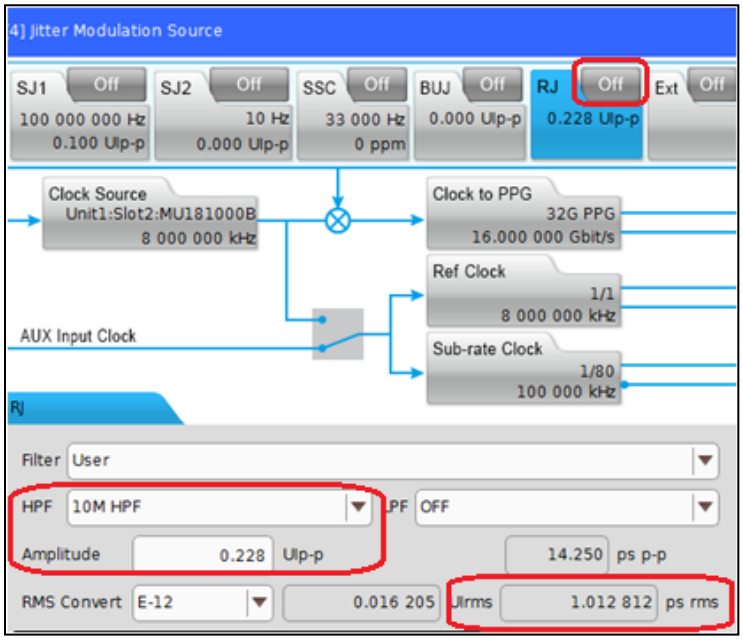
(Note: Use the average value for 5 times.)

10.1.9 RJ Calibration

Capture five waveforms for each condition on the Scope and analyze RJ using SigTest. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: Toggle_1bit
- Select Jitter Modulation Source- RJ: ON
- RJ HPF and Amplitude: 10 MHz, 0.228 Uipp



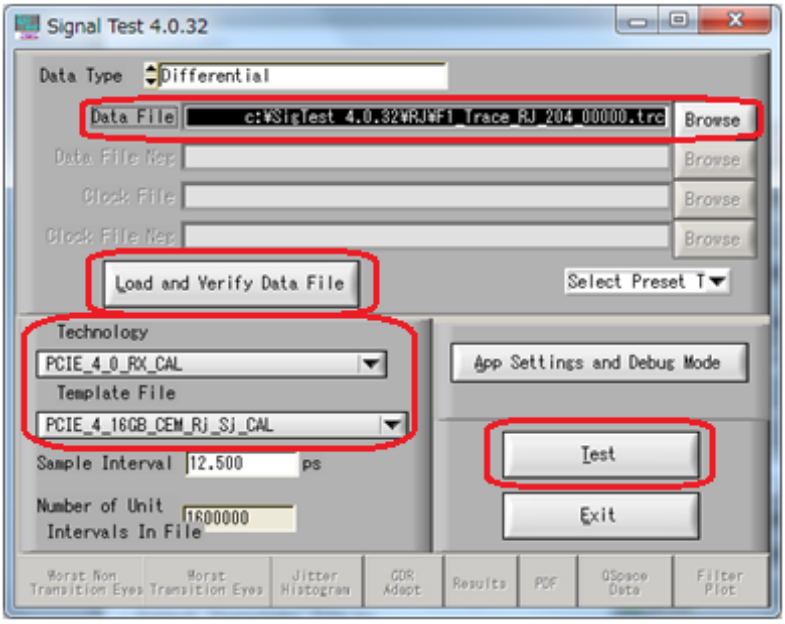
b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 10 µs/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s

c) SigTest Settings:

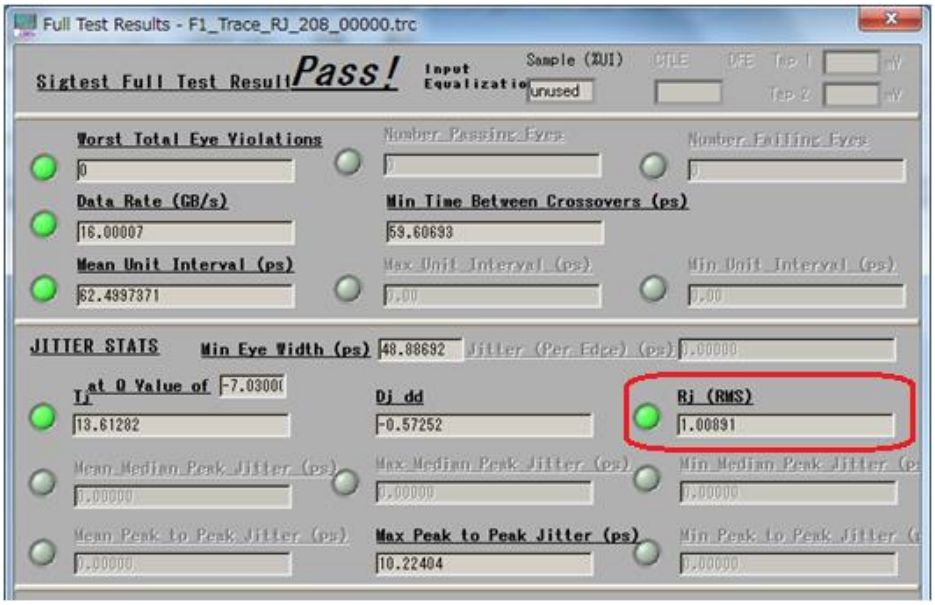
- Select a Data File

- Select ‘Load and Verify Data File’
- Select Technology as ‘PCIE_4_0_RX_CAL’
- Select Template File as ‘PCIE_4_16GB_CEM_Rj_Sj_CAL’
- Select ‘Test’



d) SigTest Results:

- Read ‘Rj (RMS)’ value



RJ value: 1.00 ps rms (at 0.208 Uipp)

(Note: Use the average value for 5 times.)

10.1.10 DM & CM Amplitude and Eye Height/Eye Width Calibration Setup

The following connection diagram shows the calibration setup at TP2 for DM amplitude (DM-I), CM amplitude (CM-I) and Eye Height (EH)/Eye Width (EW) for PCIe Gen 4. The CLB/CBB test fixture is connected in between the MP1900A BERT and a digital oscilloscope supporting >25 GHz bandwidth and >80 GS/s sampling rate.

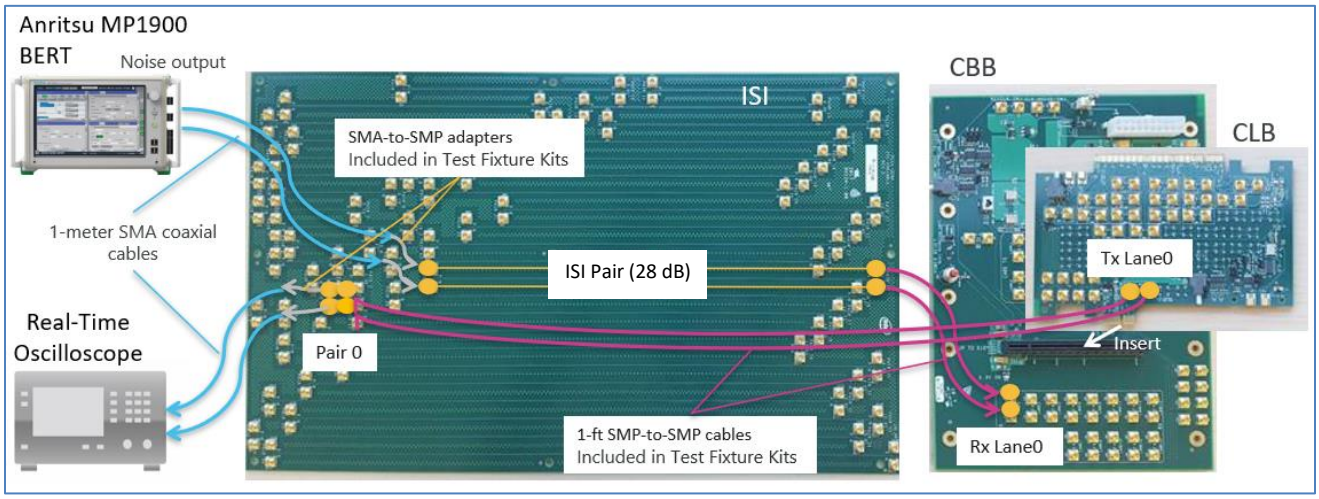


FIGURE 56. CONNECTION DIAGRAM FOR PCIE GEN 4 DM-I, CM-I AND EH/EW TP2 CALIBRATION

1. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
2. Connect the SMA-to-SMP adapters to ISI Pair (28 dB) *[physical ISI loss of 23 dB for the system board or 25 dB for the add-in card]*.
3. Using 1-ft SMP-to-SMP cables, connect the ISI Pair (28 dB) with the CBB Rx Lane. *(Note: The SMP-to-SMP cables should be included along with the test fixture kits.)*

   [Note: DM-I and CM-I should be calibrated with no reference package embedding applied.]
4. Insert the CLB into the designated slot on the CBB.
5. Connect the CLB Tx Lane using 1-ft SMP-to-SMP cables to ISI Pair 0.
6. Connect the ISI Pair 0 through the SMA-to-SMP adapters using 1-meter SMA coaxial cables to the oscilloscope channels.

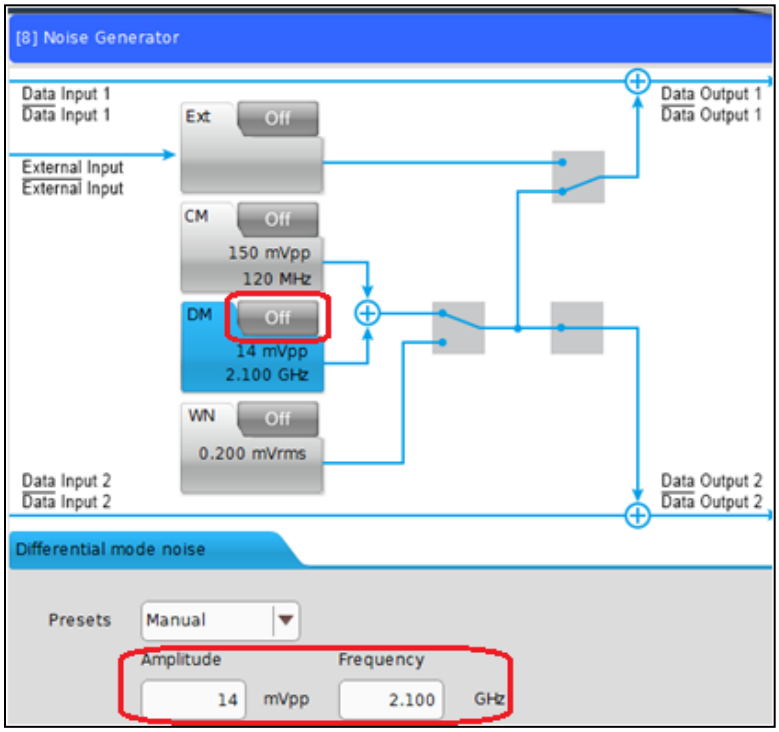
10.1.11 DM-I Calibration Adjustment

Adjust the DM Amplitude using the Scope RMS function with the following configuration. Compute V_{Diff} = (RMS * 2)/0.707.

a) BERT Settings:

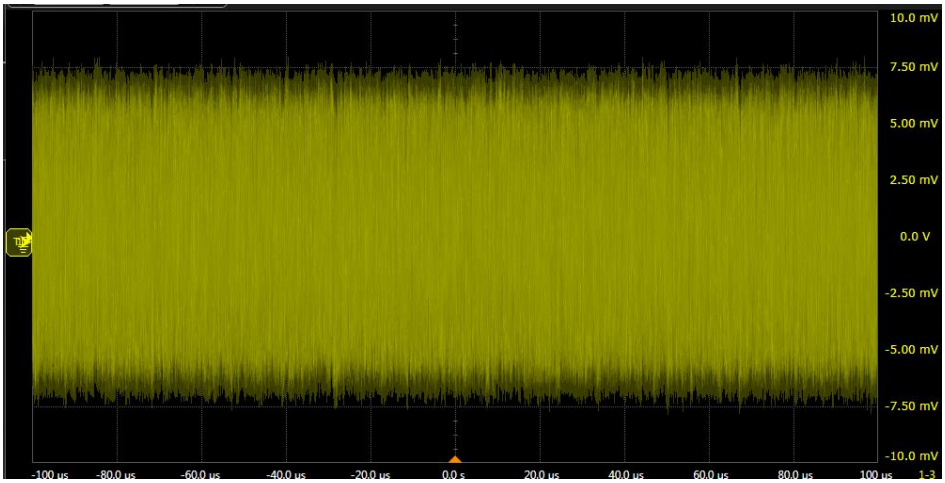
- Loss Channel
- General Output: ON

- Select SI-PPG and Emphasis tab
- PPG Data Output: OFF
- Select Noise Generator- DM: ON
- Differential mode noise Amplitude and Frequency: 14 mVpp and 2.1 GHz



b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 5 ns/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s

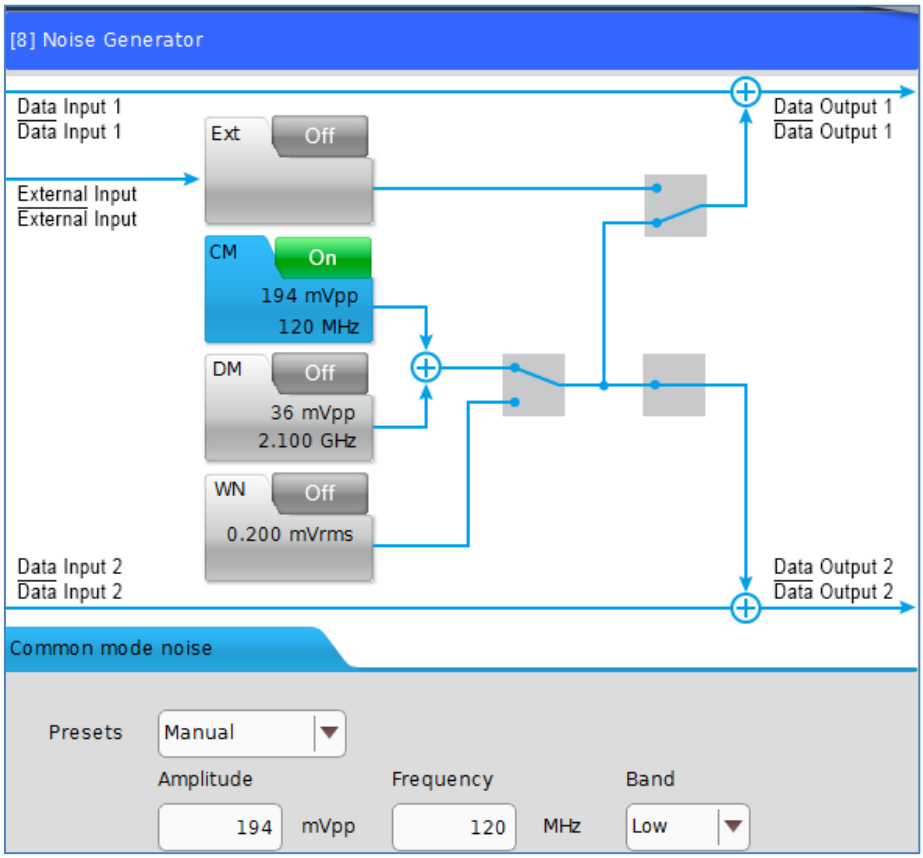


10.1.12 CM-I Calibration Adjustment

Adjust the CM Amplitude using the Scope RMS function with the following configuration. Compute V_{Diff} = RMS/0.707.

a) BERT Settings:

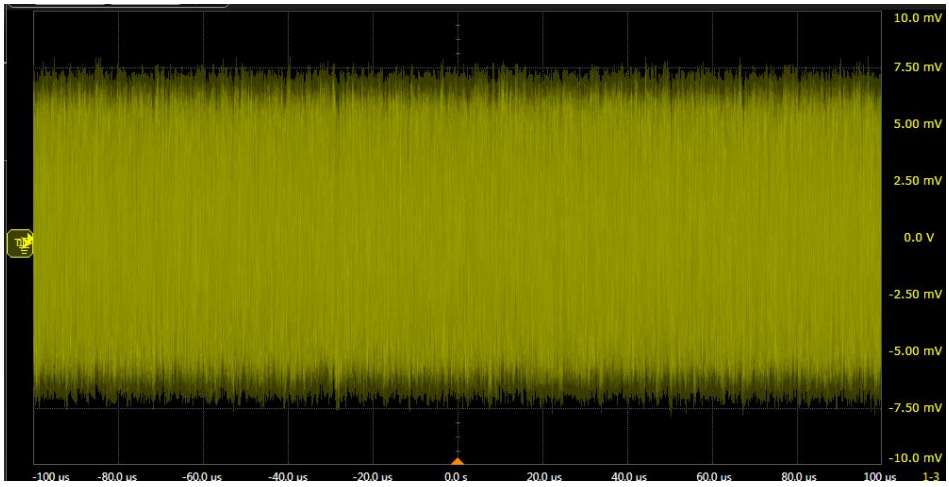
- Loss Channel
- General Output: ON
- Select SI-PPG and Emphasis tab
- PPG Data Output: OFF
- Select Noise Generator- CM: ON
- Common mode noise Amplitude and Frequency: 150 mVpp and 120 MHz



b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 12.5 µs/div
- Bandwidth: 25 GHz
- Sampling Rate: 80 GS/s

Measure RMS on (CH1+CH3)/2 and calculate Vpp = RMS/0.707.



10.1.13 EH/EW Calibration Adjustment

10.1.13.1 PCIe Gen 3 Calibration

The following Eye Height/Eye Width calibration procedure applies for PCIe Gen 3:

Capture seven waveforms for each condition on the Scope and analyze Eye Height/Eye Width using SigTest. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: ON
- Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen3_P0
- Set all Jitter, Noise, and Amplitude values.
- Set BUJ values as follows:
  - BUJ: 0.080 UI (10.0 pspp)
  - 2.0 Gbit/s
  - PRBS31
  - 200 MHz LPF

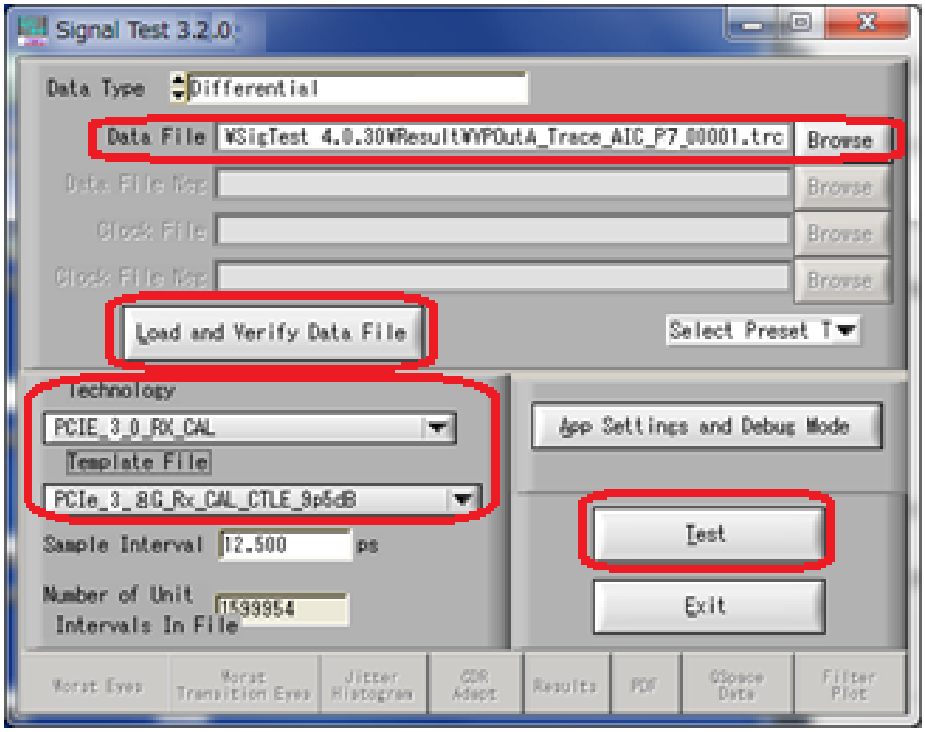
  Note: Since the PPG has very small intrinsic Jitter, some BUJ must be added for PCIe 3.0 testing. The BUJ does not require separate calibration, as its effect is incorporated during final eye calibration.
- Save seven waveforms and read in SigTest.
- Adjust the Eye Height/Eye Width to target specification values using *RJ* and *DM-I*:
  - RJ: 1.5 +.2/-0 ps RMS
  - DM: 14 to 16 mV at TP2

b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 12.5 µs/div (2M UI)
- Bandwidth: 25 GHz

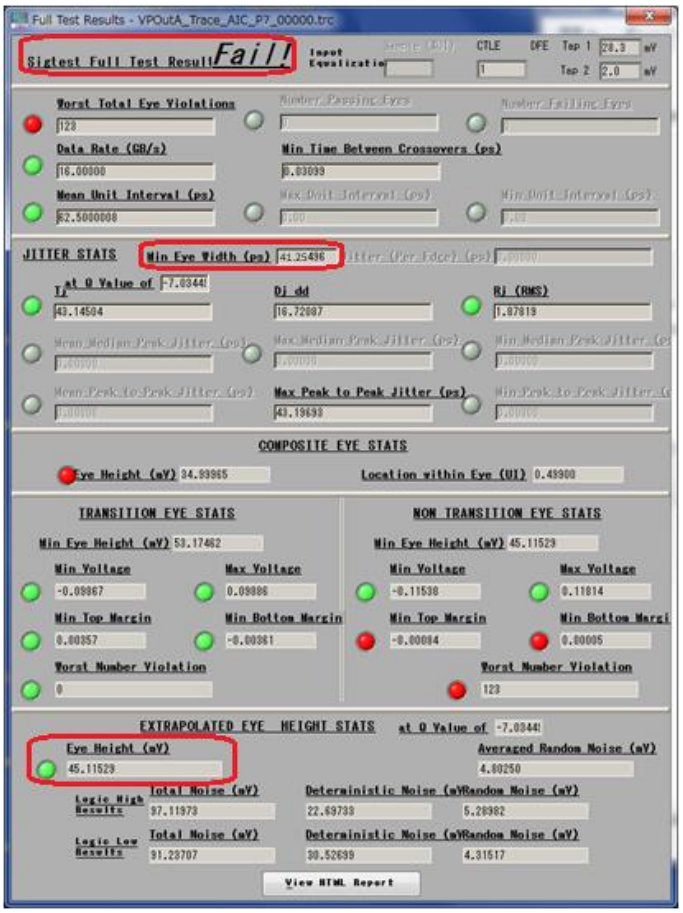
c) SigTest Settings:

- Select a Data File
- Select 'Load and Verify Data File'
- Select Technology as 'PCIE_3_0_RX_CAL'
- Select Template File as 'PCIe_3_8G_Rx_CAL_CTLE_x.xdB'
- Select 'Test'



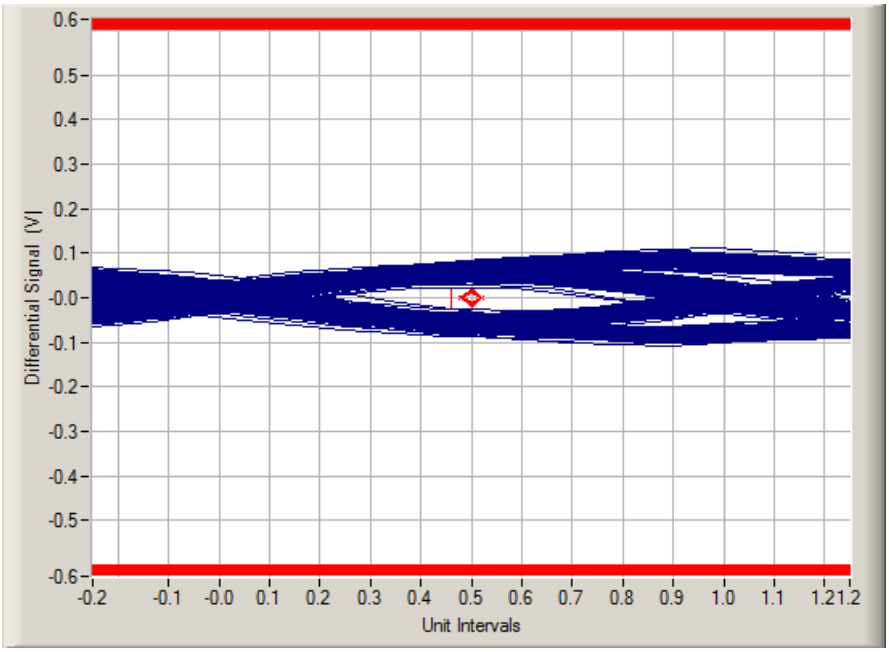
d) SigTest Results:

Note that the SigTest Full Test Result always shows 'Fail!' which can be ignored.



Target Eye Width: 41.25 +0/-2 ps

Target Eye Height: 46 mV +0/-5 mV



10.1.13.2 PCIe Gen 4 Calibration

The following Eye Height/Eye Width calibration procedure applies for PCIe Gen 4:

Set the ISI Trace to 30 dB ISI Trace (physical loss of 25 dB for the system board and 27 dB for the add-in card).

Capture seven waveforms for each condition on the Scope and analyze Eye Height/Eye Width using SigTest. Set up the following parameters.

a) BERT Settings:

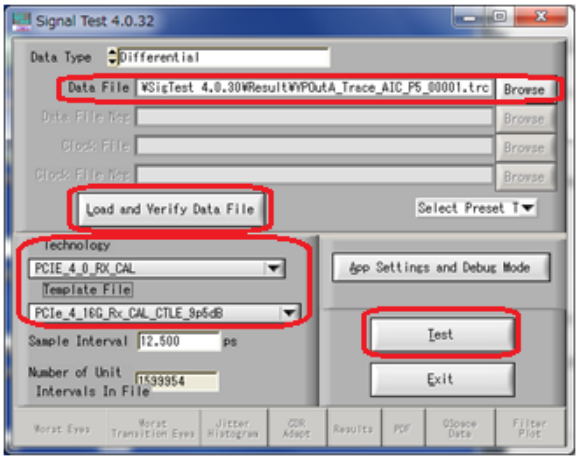
- General Output: ON
- Select SI-PPG and Emphasis tab- Emphasis Function: ON
- Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen4_P0
- Set all Jitter, Noise, and Amplitude values.
- Save seven waveforms and read in SigTest.
- Determine the Optimized ISI Trace, Preset and CTLE as follows:
  - Set Preset 5 on BERT and capture seven waveforms.
  - Measure all the seven waveforms for all CTLE's ranging from 8.5 db to 10.5 dB in 0.25 dB steps using SigTest. For each CTLE and Preset combination, calculate EW/EH through averaging after filtering the outliers (see below):
    - The waveform is considered an outlier if the Eye Width is < 1.0 ps or deviates from the median by 5.0 ps.
    - The waveform is considered an outlier if the Eye Height is < 1.0 mV or deviates from the median by 8.0 mV.
  - Repeat above steps using Preset 6. Determine which CTLE and Preset combination provides the largest Eye Area (Eye Width * Eye Height) and record these values.
- If the Eye Width/Eye Height is below the calibration target value, reduce the ISI trace by 0.5 dB and repeat the Preset and CTLE optimization steps until the Eye Width/Eye Height is above the calibration target value.
  - *Save more than seven waveforms and obtain the average value.*
- Adjust the Eye Height/Eye Width to target specification values using *SJ, DM-I,* and *Eye Amplitude*:
  - SJ: 5 to 10 pspp
  - DM: 10 to 25 mV at TP2
  - Differential Voltage Swing: 720 to 800 mVpp at TP1
  - Apply 20 EH/EW averaging

b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 12.5 µs/div (2M UI)
- Bandwidth: 25 GHz

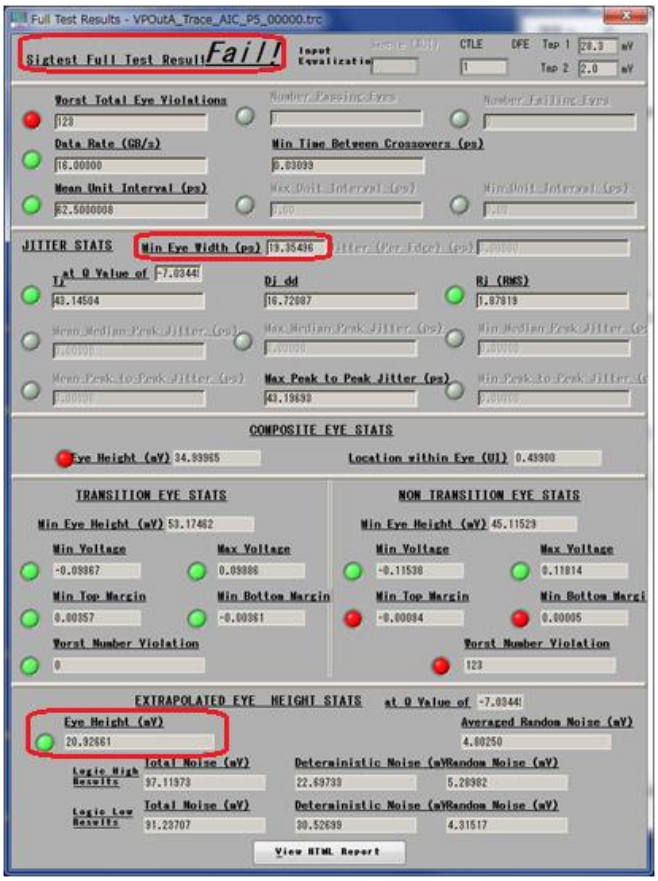
c) SigTest Settings:

- Select a Data File
- Select 'Load and Verify Data File'
- Select Technology as 'PCIE_4_0_RX_CAL'
- Select Template File as 'PCIe_4_16G_Rx_CAL_CTLE_x.xdB'
- Select 'Test'



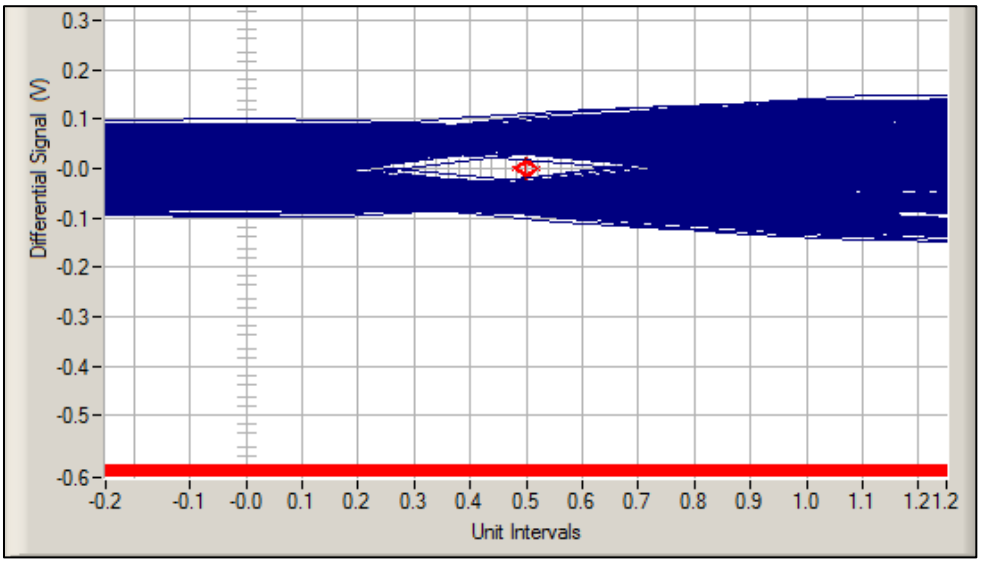
d) SigTest Results:

Note that the SigTest Full Test Result always shows 'Fail!' which can be ignored.



Target Minimum Eye Width: 18.75 +0.5/-0.5 ps

Target Extrapolated Eye Height: 15 +1.5/-1.5 mV



For final eye calibration, adjust Voltage Swing, SJ, and DM Amplitude until the target Eye Width and Eye Height are achieved and then save 20 waveforms.

10.2 Perform Initial Tx Equalization & Tx Link Equalization Response Tests

This section describes how to set up the DUT to perform initial Tx equalization (EQ) and Tx link EQ response testing (for both the system board and add-in card). This is to ensure that the DUT will be able to apply the correct Tx EQ preset as required along the test.

To perform the initial Tx EQ & Tx link EQ response tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to reference clock with the DUT fixture. After data is processed, the signals will be separated to flow through two different directions- one part of the signal will be sent back through the test fixture to the stress signal generator for error detection while the other part will be sent to the oscilloscope for waveforms to be captured and analyzed for target EQ values.

Note: Refer to Sections 7.2 and 7.3 for more details on test setup requirements for the DUT.

10.2.1 Equipment Setup for Add-in Card DUT Initial Tx EQ / Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform initial Tx EQ / Tx link EQ response test for the PCIe Gen ¾ add-in card DUT. The setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CBB test fixture for the DUT.

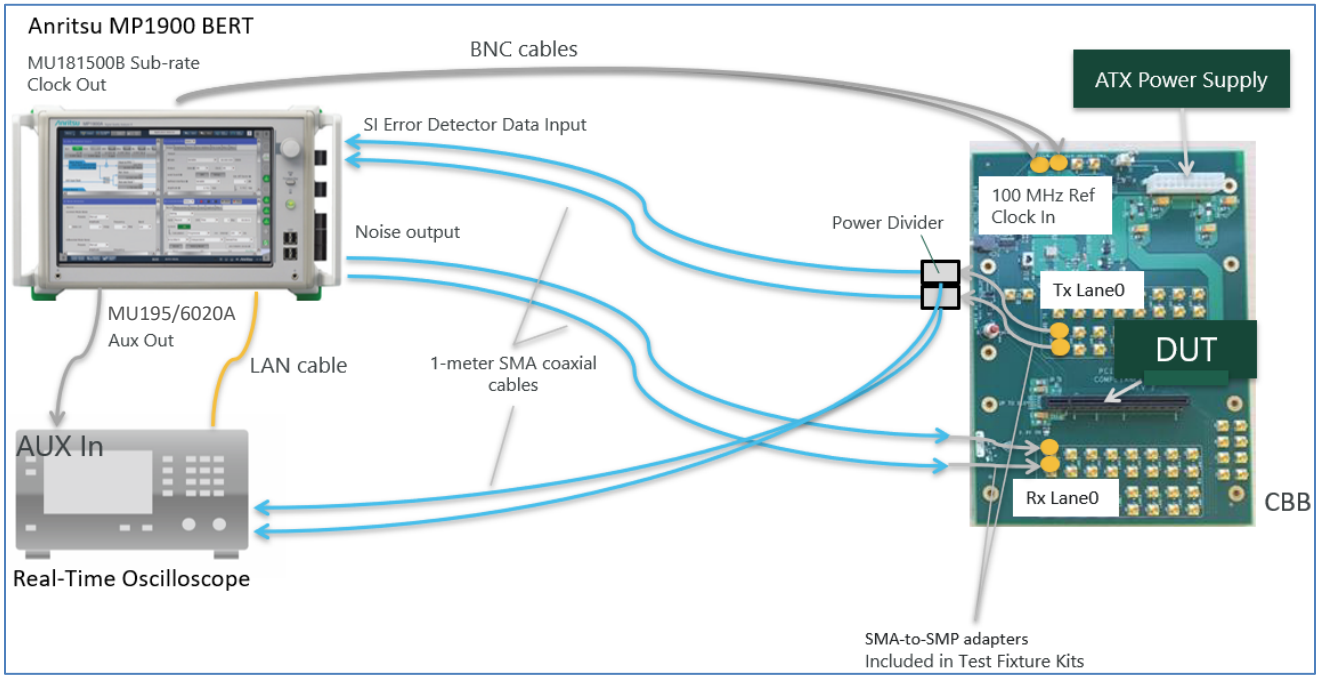


FIGURE 57. CONNECTION DIAGRAM FOR PCIE GEN ¾ ADD-IN CARD DUT INITIAL TX EQ / TX LINK EQ RESPONSE TEST

1. Connect an ATX power supply to the CBB with DUT inserted.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to the CBB Rx Lane.

4. Connect the CBB Tx Lane to the power divider input ports through another set of SMA-to-SMP adapters.
5. Using BNC cables, connect the MU181500B sub-rate clock outputs to the CBB 100 MHz Ref Clock In connectors.
6. Using 1-meter SMA coaxial cables, connect the power divider outputs to the MU195040A data inputs for loopback error detection.
7. Using 1-meter SMA coaxial cables, connect the oscilloscope channels to the power divider tapped input ports.
8. Using a SMA-to-SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
9. Connect a LAN cable between the MP1900A BERT and the oscilloscope.

10.2.2 Equipment Setup for System Board DUT Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform Tx link EQ response test for the PCIe Gen ¾ system board DUT. The setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CLB test fixture for the DUT.

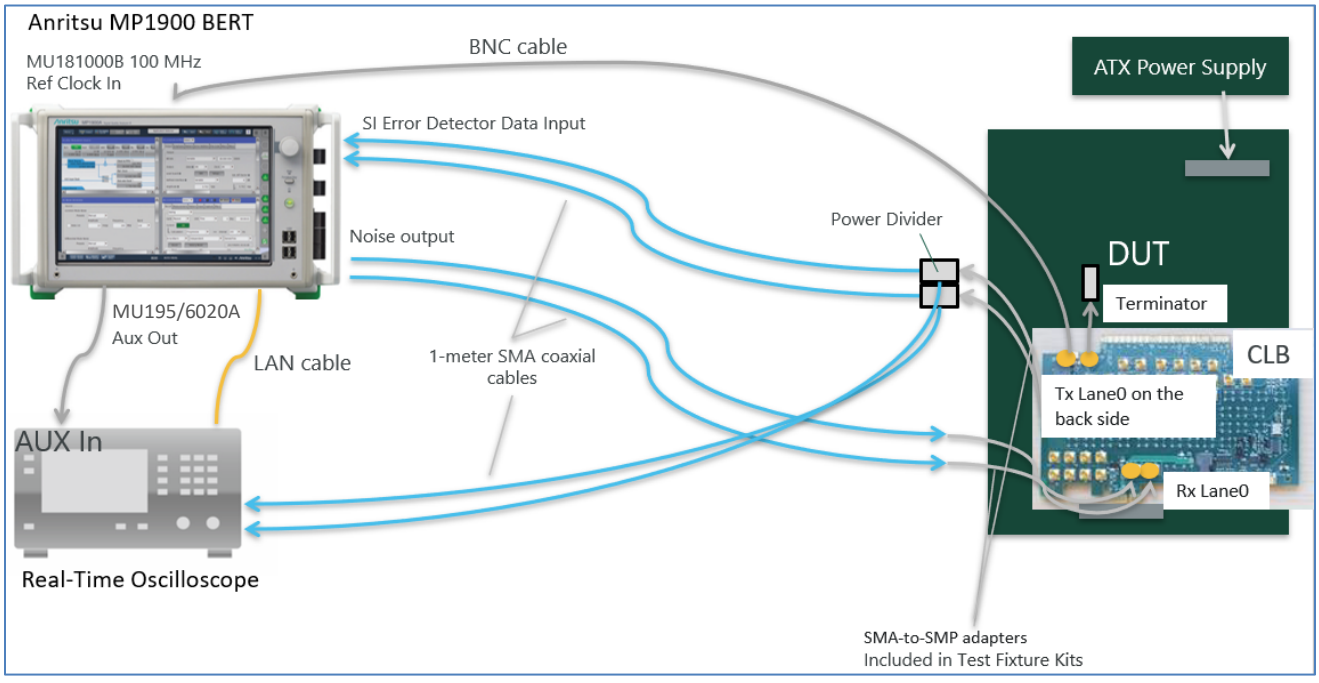


FIGURE 58. CONNECTION DIAGRAM FOR PCIE GEN ¾ SYSTEM BOARD DUT TX LINK EQ RESPONSE TEST

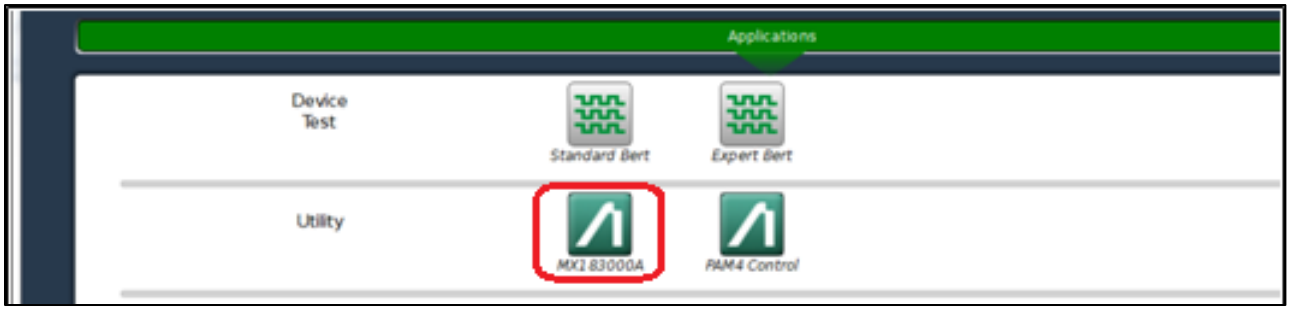
1. Connect an ATX power supply to the DUT.
2. Using 1-meter SMA coaxial cables, connect the MU195050A noise outputs to SMA-to-SMP adapters. *(Note: The SMA-to-SMP adapters should be included along with the test fixture kits.)*
3. Connect the SMA-to-SMP adapters to the CLB Rx Lane.

4. Connect the Tx Lane on the back of the CLB to the power divider input ports through another set of SMA-to-SMP adapters.
5. Using a BNC cable, connect a CLB Ref Clock Out connector to the MU181000B 100 MHz Ref Clock In.
6. Terminate the other unused CLB Ref Clock Out connector using the J1632A coaxial terminator.
7. Using 1-meter SMA coaxial cables, connect the power divider outputs to the MU195040A data inputs for loopback error detection.
8. Using 1-meter SMA coaxial cables, connect the oscilloscope channels to the power divider tapped input ports.
9. Using a SMA-to-SMA cable, connect a MU195020A/MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU195020A/MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
10. Connect a LAN cable between the MP1900A BERT and the oscilloscope.

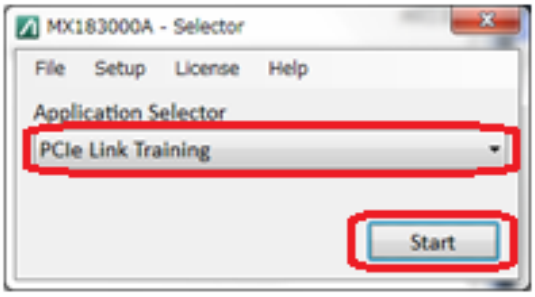
10.2.3 Initial Tx EQ Startup and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the initial Tx EQ test. The oscilloscope will also be used to capture waveforms for post processing analysis.

1. Configure the oscilloscope as follows:
   - Averaging: OFF
   - Horizontal Scale: 12.5 µs/div (2M UI)
   - Bandwidth: 25 GHz
   - Trigger: 0 V, Channel 1
2. Set Preset 0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.

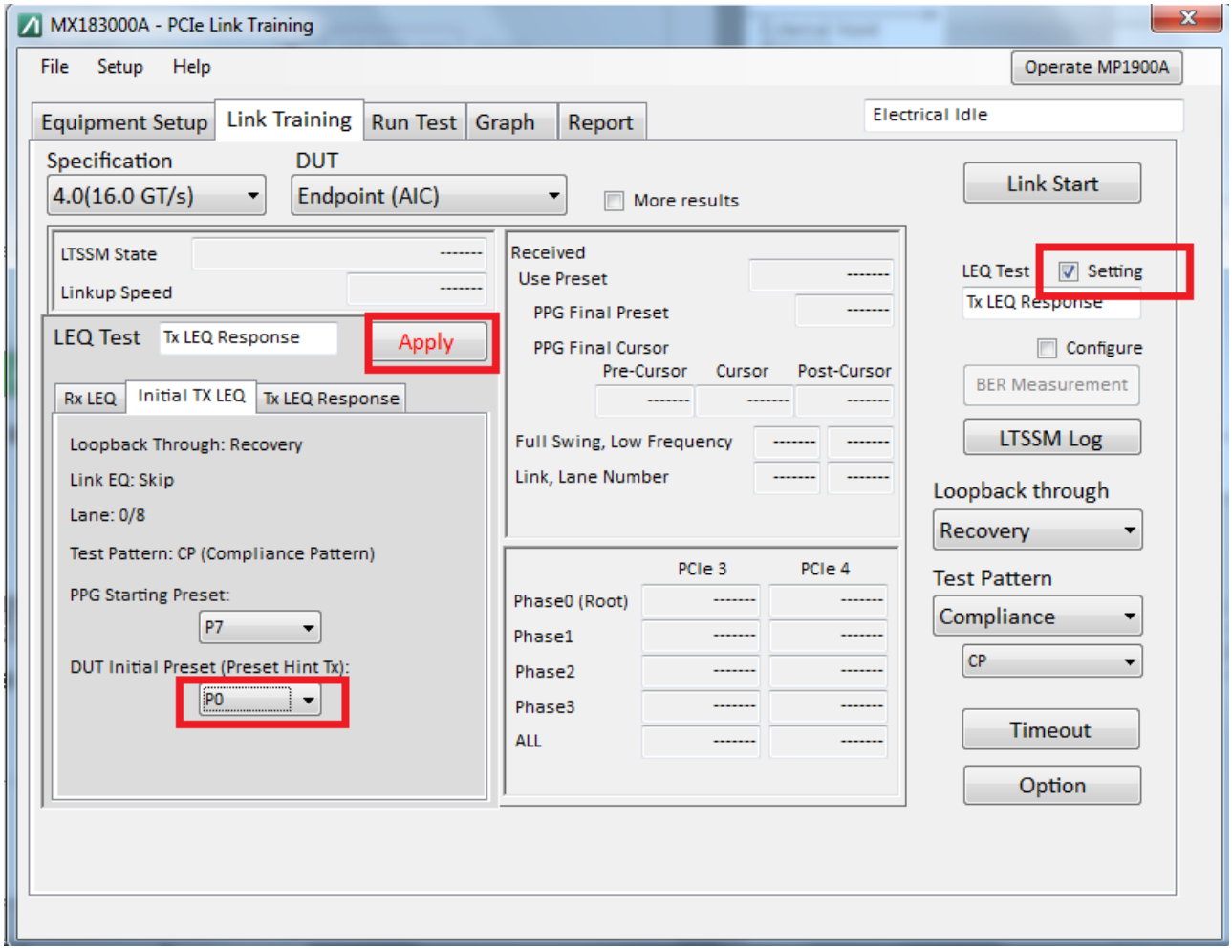


4. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



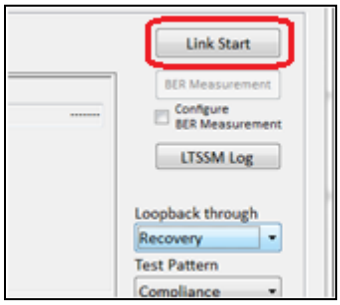
5. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.

6. In the MX183000A – PCIe Link Training window, select the Link Training tab. Select the "Setting" check box on the right of the screen.
7. When the LEQ Test pane appears, select the Initial Tx LEQ tab. Set the "DUT Initial Preset (Preset Hint Tx)" to Preset 0 (P0). Then select "Apply" at the top right of the LEQ Test pane.

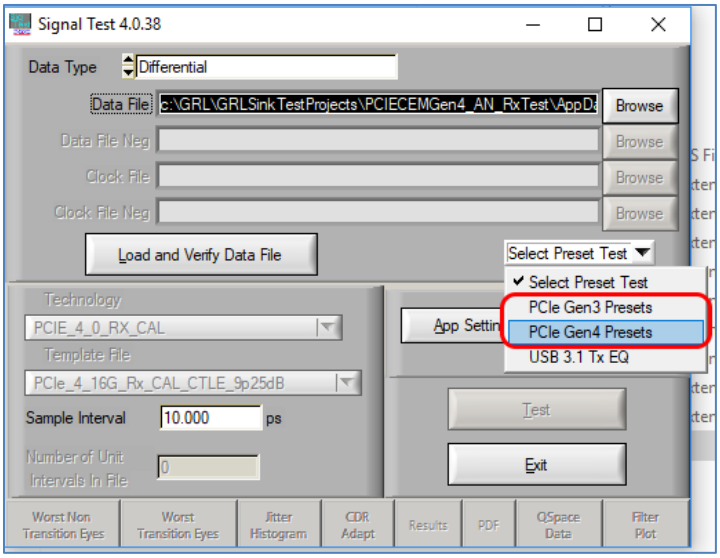


8. Press the Power Reset button on the CBB test fixture to reset the DUT.

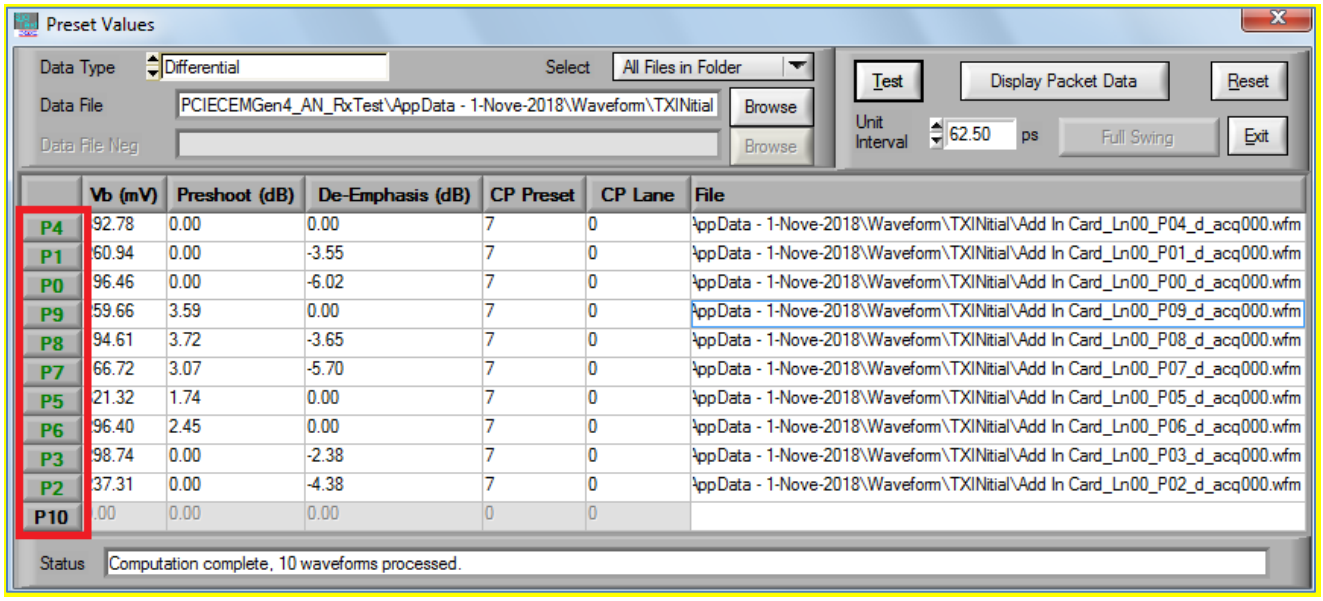
9. In the MX183000A – PCIe Link Training window, select ‘Link Start’ in the Link Training tab.



10. On the Scope, capture the Preset 0 waveforms and save to a file labeled as either *"Add In Card_Ln00_TXResponse_P0X_d_acq000"* (for the add-in card where P0X represents the Preset Number) or *"System Board_TXResponse_P0_d_acq000"* (for the system board). For example if using a add-in card DUT, the Preset 0 waveform should be saved as *"Add In Card_Ln00_TXResponse_P00_d_acq000"*. If using a system board DUT, the Preset 0 waveform should be saved as *"System Board_TXResponse_P0_d_acq000"*.
11. Repeat steps 1 to 9 to capture all waveforms for all Presets (up to Preset 9). All waveforms must be saved to same file directory.
12. Launch SigTest and select "PCIe Gen3 Presets" or "PCIe Gen4 Presets" under the Select Preset Test drop down.



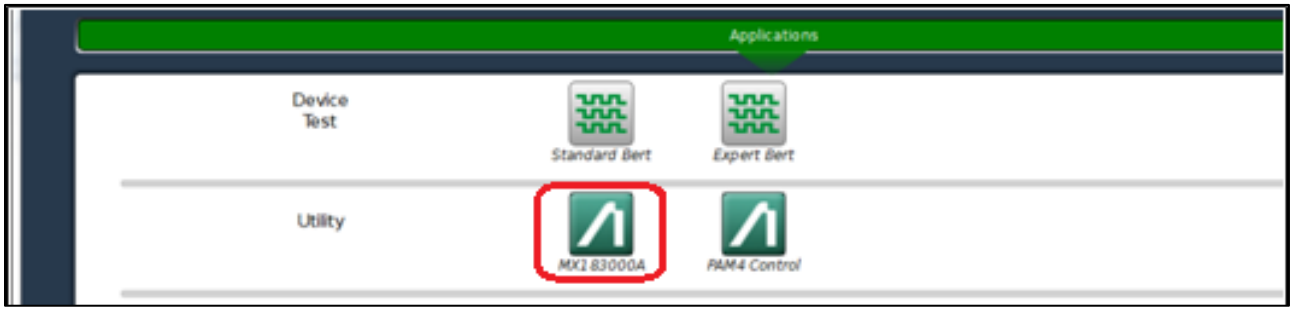
13. Browse to select the directory of the saved waveform file to be tested and then select the "Test" button on the top right to start the test run. All preset numbers must turn green once the test completes to indicate a Pass as shown below.



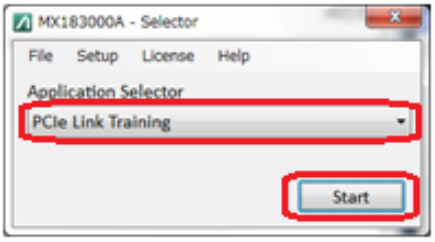
10.2.4 Tx Link EQ Time Response (with Presets/Cursors) Startup and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the Tx link EQ time response test with presets or cursors. The oscilloscope will also be used to capture waveforms for post processing analysis.

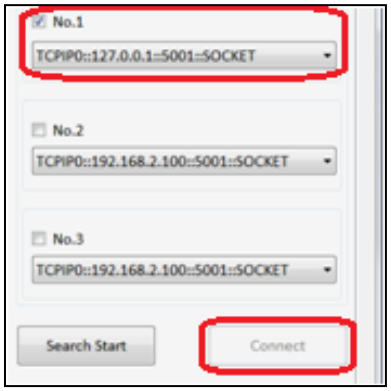
1. Configure the oscilloscope as follows:
   - Averaging: OFF
   - Horizontal Scale: 12.5 µs/div (2M UI)
   - Bandwidth: 25 GHz
   - Trigger: -350 mV, AUX channel
2. Set Preset 0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.



4. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



4. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.

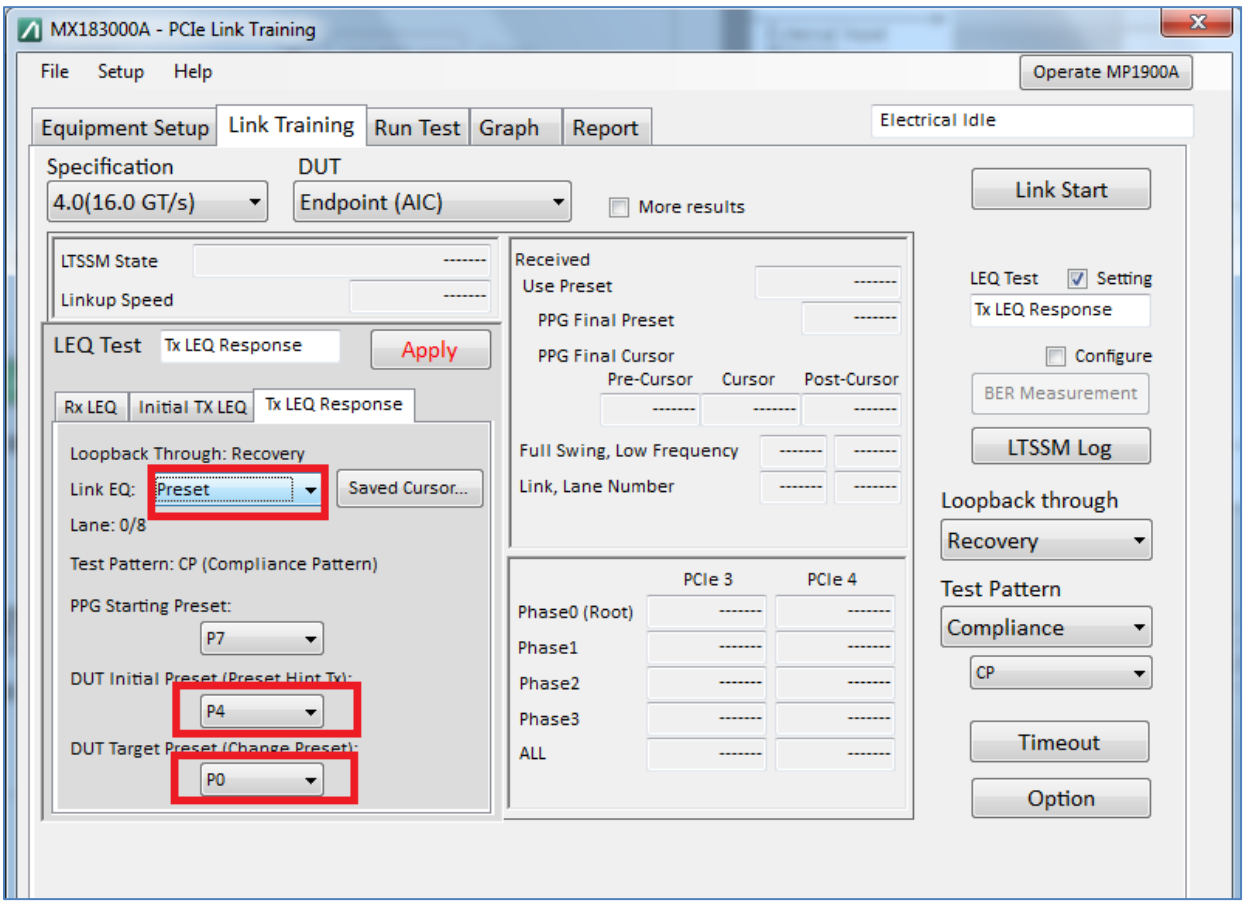


5. In the MX183000A – PCIe Link Training window, select the Link Training tab. Select the "Setting" check box on the right of the screen.
6. When the LEQ Test pane appears, select the Tx LEQ Response tab. Set the "DUT Initial Preset (Preset Hint Tx)" to Preset 4 (P4) and the "DUT Target Preset (Change Preset)" to P0.

   Note: Use the following "DUT Initial Preset (Preset Hint Tx)" and "DUT Target Preset (Change Preset)" combinations for this step:

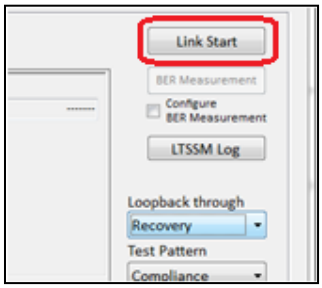
Preset # to be Tested	DUT Initial Preset (Preset Hint Tx)	DUT Target Preset (Change Preset)
P0	P4	P0
P1	P4	P1
P2	P4	P2
P3	P7	P3
P4	P7	P4
P5	P7	P5
P6	P7	P6
P7	P4	P7
P8	P4	P8
P9	P7	P9

Set Link EQ to “Preset” if testing for Tx Response Preset or “Cursor” if testing for Tx Response Cursor.

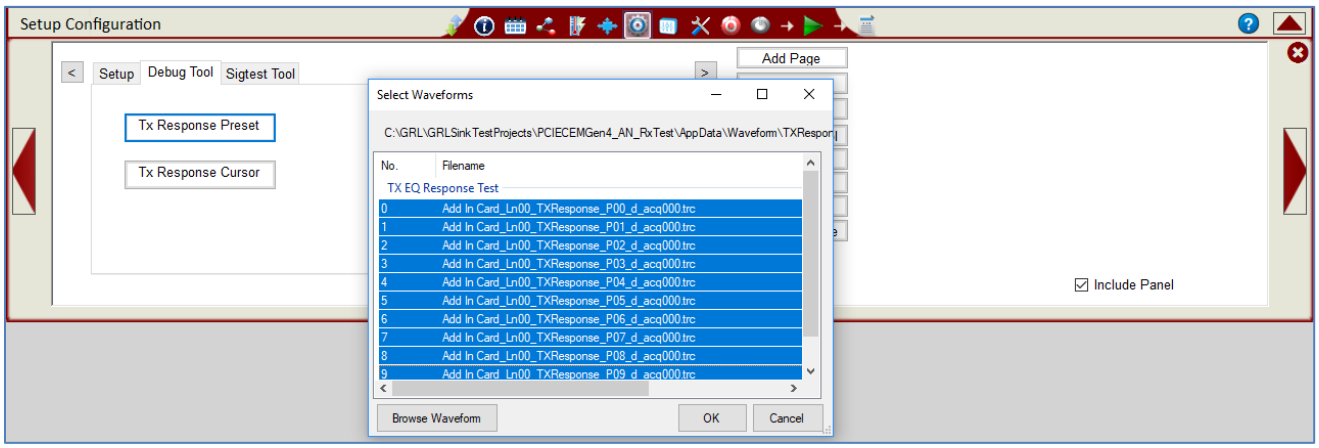


7. Press the Power Reset button on the CBB test fixture to reset the DUT.

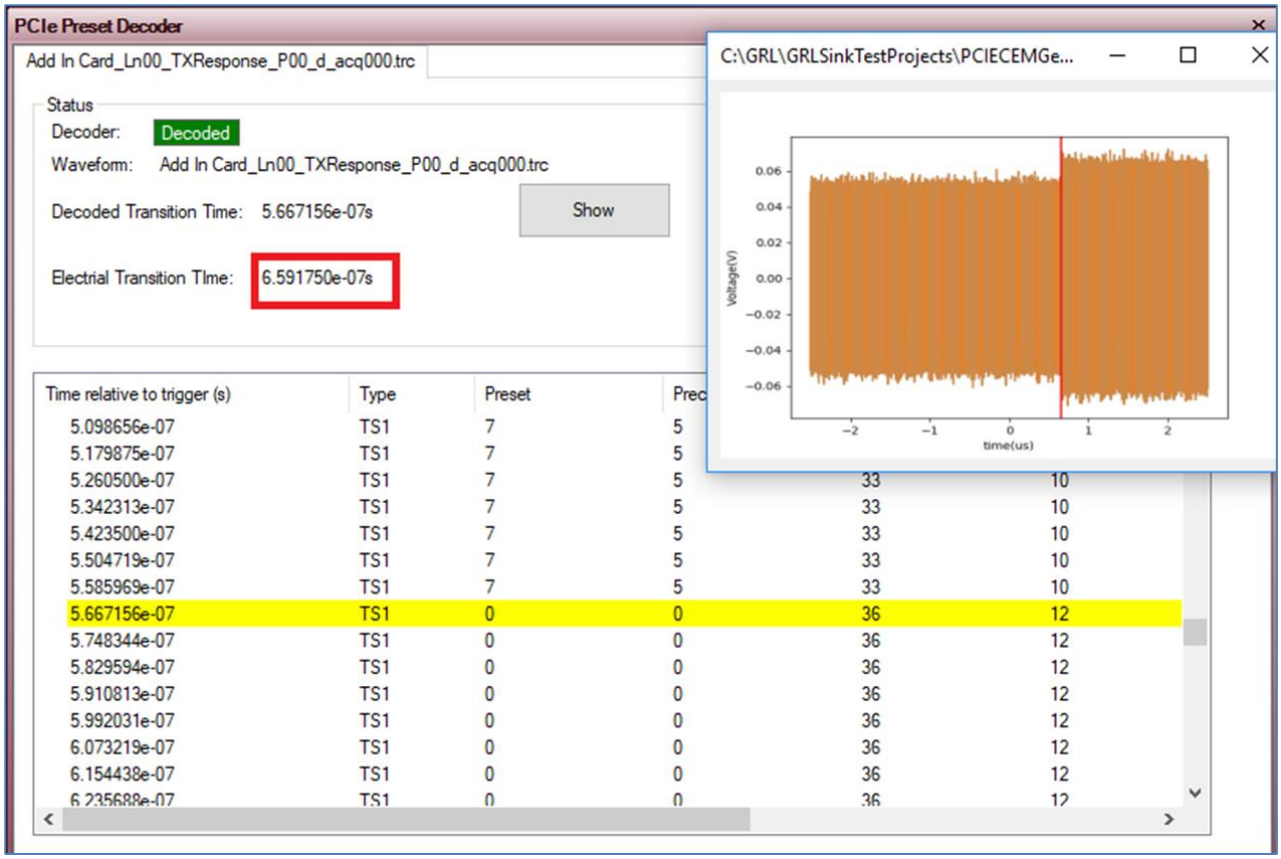
8. In the MX183000A – PCIe Link Training window, select ‘Link Start’ in the Link Training tab.



9. On the Scope, capture the Preset 0 waveforms and save to a file labeled as either *"Add In Card_Ln00_TXResponse_P0X_d_acq000"* (for the add-in card where P0X represents the Preset Number) or *"System Board_TXResponse_P0_d_acq000"* (for the system board). For example if using a add-in card DUT, the Preset 0 waveform should be saved as *"Add In Card_Ln00_TXResponse_P00_d_acq000"*. If using a system board DUT, the Preset 0 waveform should be saved as *"System Board_TXResponse_P0_d_acq000"*.
10. Repeat steps 1 to 8 for each Preset change.
11. Repeat steps 1 to 9 for each Cursor change.
12. Perform post processing analysis for each waveform to locate the transition time between the preset/cursor change.
13. On the GRL software, go to the Setup Configuration page and select the Debug Tool tab. Select either the "Tx Response Preset" or "Tx Response Cursor" button depending on which is being tested. In the Select Waveforms pop-up window, select all the waveforms that were previously captured and click "OK".



14. In the PCIe Preset Decoder screen, verify that the Electrical transition time is showing < 1 µs to pass the test. *Note: The Decoded transition time serves as an informative value only and is not required for compliance.*



10.3 Perform Rx Link EQ Test

This section describes how to set up the DUT for loopback testing to measure the Bit Error Rate (BER) using the link equalization test method.

To perform link training loopback tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to reference clock with the DUT fixture. After data is processed, the signals will be sent back through the test fixture to the stress signal generator for error detection. To enable this loopback mode, the error detector on the stress signal generator will run link training procedure on the DUT. When the DUT enters loopback state, the error detector will proceed to measure BER of the loopback signals.

Note: Refer to Section 7.5 to set up the DUT for link equalization testing to verify initially that the DUT is ready for link training and loopback.

10.3.1 Equipment Setup for Add-in Card DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 4 add-in card DUT. The setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CBB test fixture for the DUT.

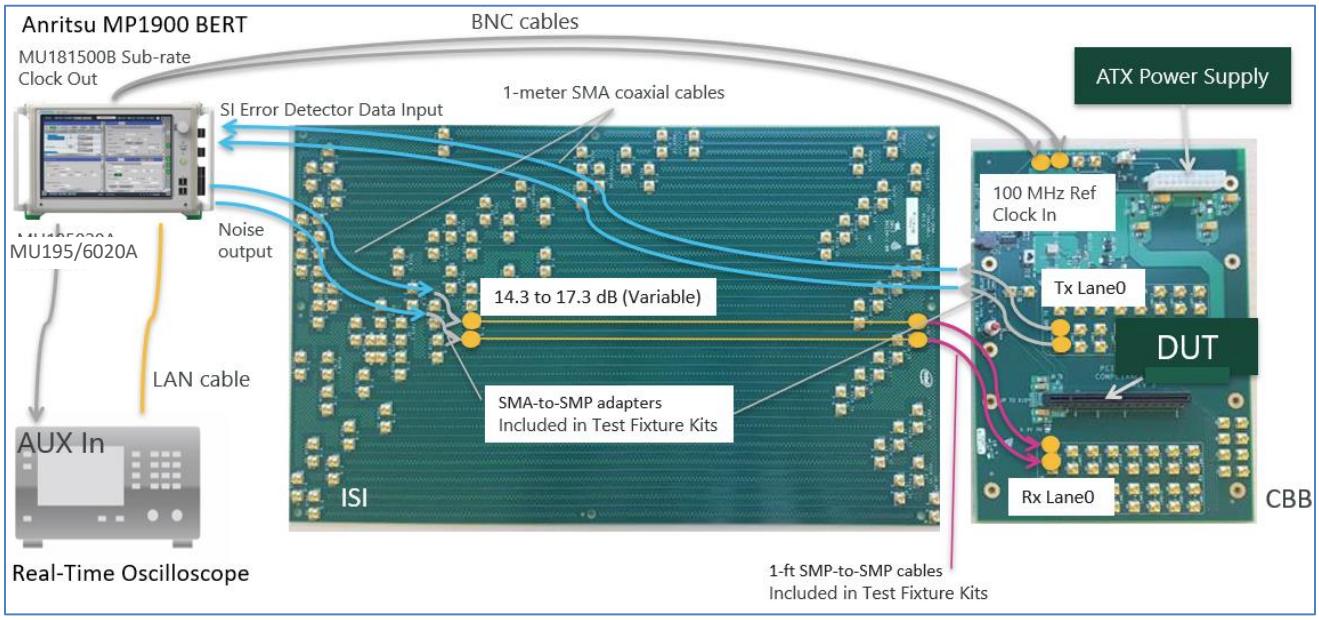


FIGURE 59. CONNECTION DIAGRAM FOR PCIE GEN 4 ADD-IN CARD DUT LOOPBACK TEST

1. Using the same setup from the add-in card Tx link EQ test (Section 10.2.1), remove the power divider and its connection from the oscilloscope.
2. Connect the MU195050A noise outputs to 14.3-17.3 dB Variable ISI through the SMA-to-SMP adapters.
3. Using 1-ft SMP-to-SMP cables, connect the 14.3-17.3 dB Variable ISI with the CBB Rx Lane.
4. Connect the CBB Tx Lane directly to the MU195040A data inputs for loopback error detection.

10.3.2 Equipment Setup for System Board DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 4 system board DUT. The setup is using the MP1900A BERT that includes the MU195040A SI Error Detector module and a compliant CLB test fixture for the DUT.

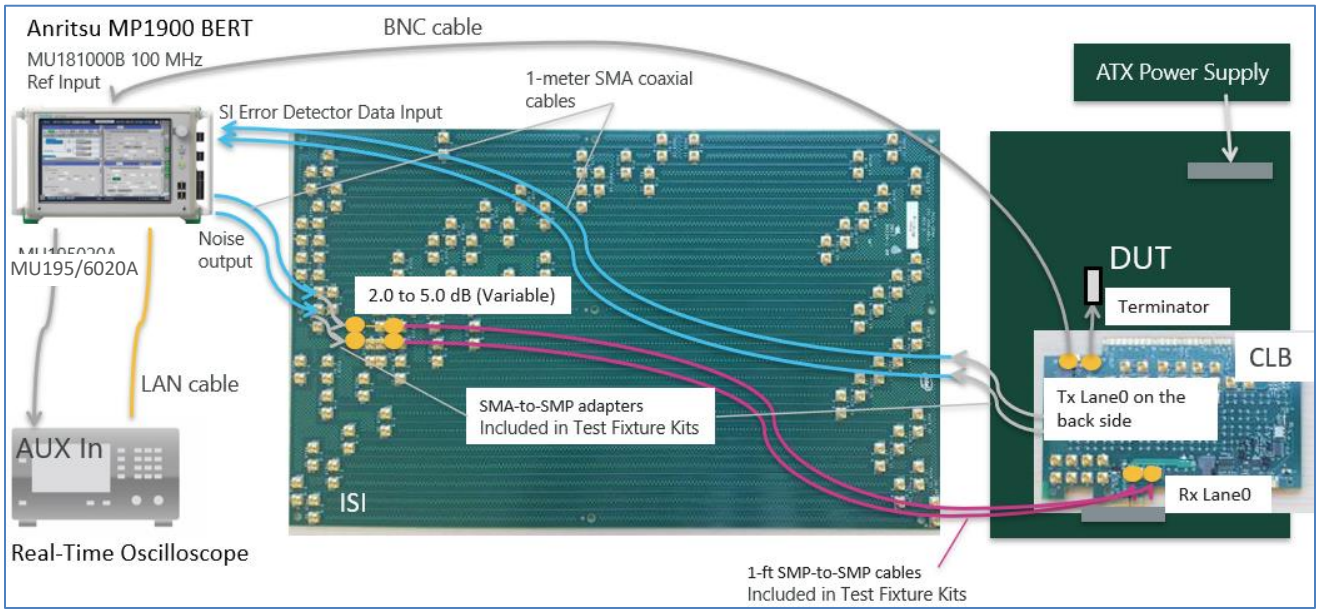


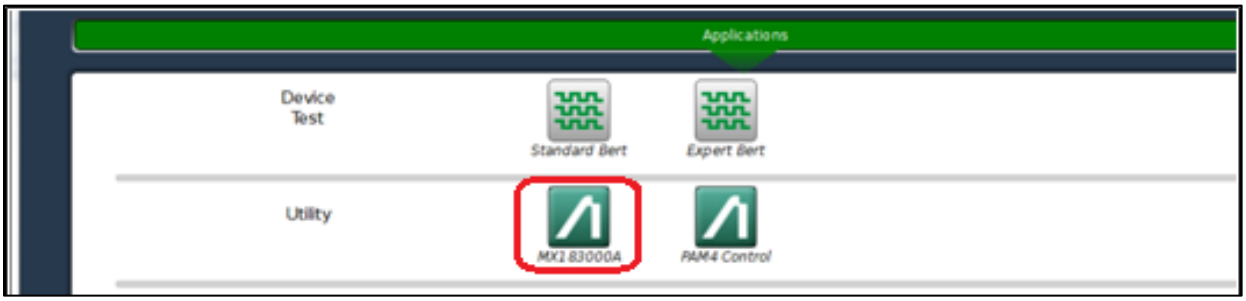
FIGURE 60. CONNECTION DIAGRAM FOR PCIE GEN 4 SYSTEM BOARD DUT LOOPBACK TEST

1. Using the same setup from the system board Tx link EQ test (Section 10.3.2), remove the power divider and its connection from the oscilloscope.
2. Connect the MU195050A noise outputs to 2.0-5.0 dB Variable ISI through the SMA-to-SMP adapters.
3. Using 1-ft SMP-to-SMP cables, connect the 2.0-5.0 dB Variable ISI with the CLB Rx Lane.
4. Connect the Tx Lane on the back of the CLB directly to the MU195040A data inputs for loopback error detection.

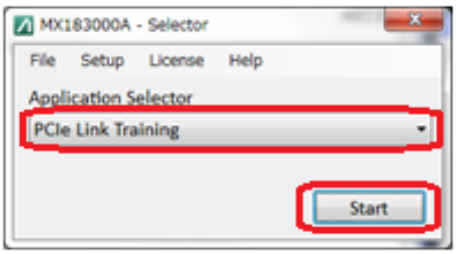
10.3.3 Link Training Initialization and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform link training.

1. Enable all calibrated stresses on the BERT.
2. On the BERT's Applications screen, select the MX183000A Utility application.

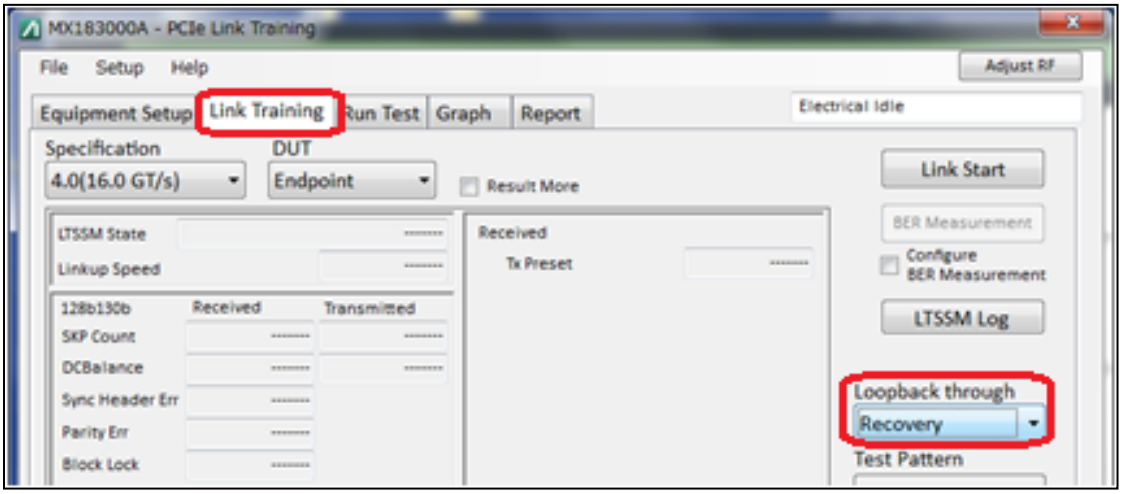


3. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.

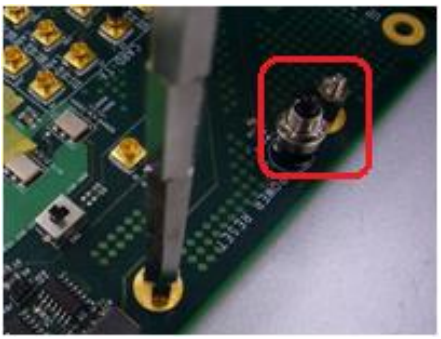


4. In the next window, select the network address of the MX190000A BERT application followed by ‘Connect’ to link up with the MX190000A.

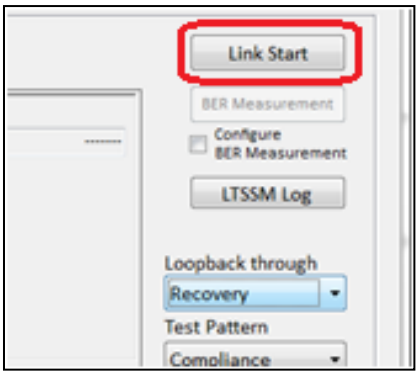
5. In the MX183000A - PCIe Link Training window, select the Link Training tab. Select ‘Recovery’ under the Loopback through field. The Recovery mode is a recommended setting for the DUT loopback state.



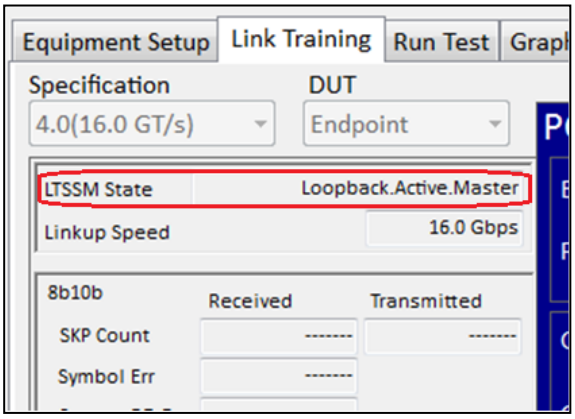
6. Press the Power Reset button on the CBB test fixture to reset the DUT.



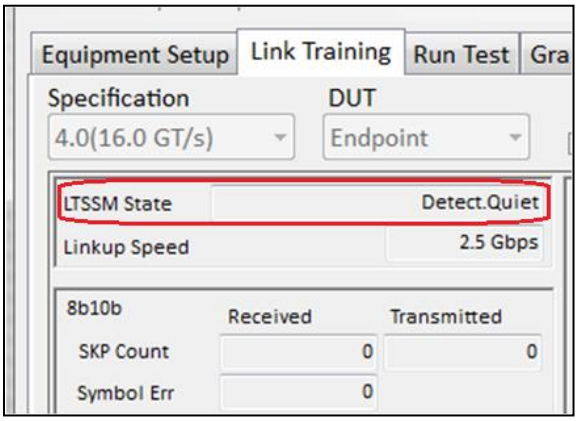
7. In the MX183000A - PCIe Link Training window, select ‘Link Start’ in the Link Training tab.



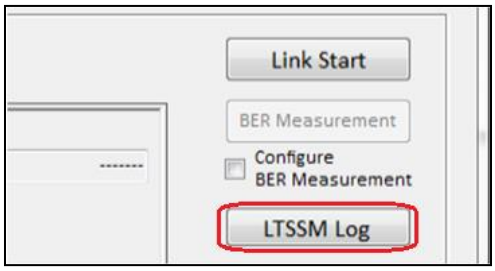
8. If the LTSSM (Link Training and Status State Machine) State shows ‘Loopback.Active.Master’, it means link training is successful.



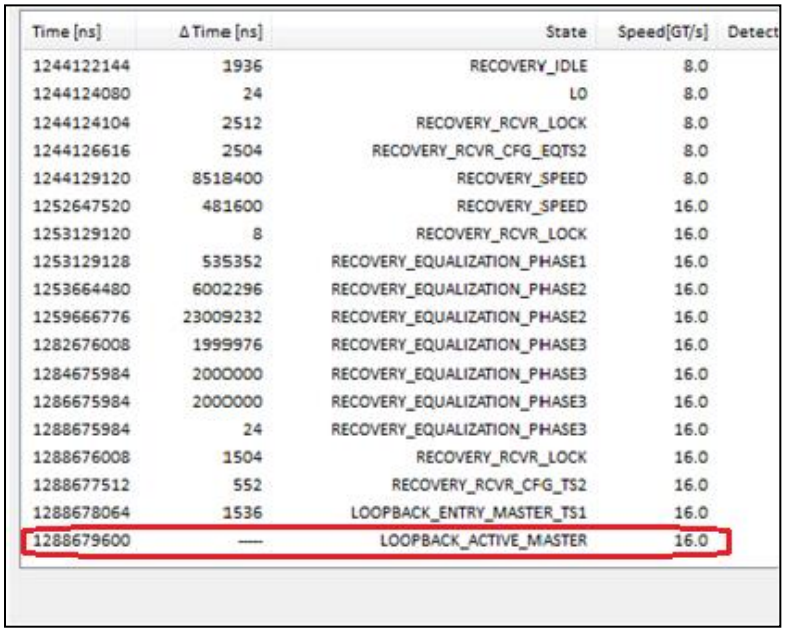
If ‘Detect.Quiet’ is shown instead, it means that link training has failed.



9. Select 'LTSSM Log' to generate a log of the link training results.

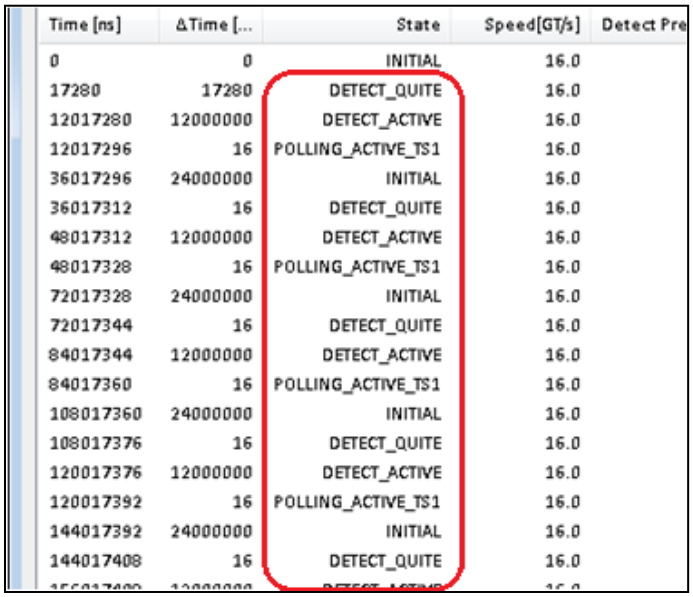


If the link training is successful, the log will show the DUT enter a Loopback Active state in the following example:



Time [ns]	Δ Time [ns]	State	Speed[GT/s]	Detect
1244122144	1936	RECOVERY_IDLE	8.0	
1244124080	24	L0	8.0	
1244124104	2512	RECOVERY_RCVR_LOCK	8.0	
1244126616	2504	RECOVERY_RCVR_CFG_EQTS2	8.0	
1244129120	8518400	RECOVERY_SPEED	8.0	
1252647520	481600	RECOVERY_SPEED	16.0	
1253129120	8	RECOVERY_RCVR_LOCK	16.0	
1253129128	535352	RECOVERY_EQUALIZATION_PHASE1	16.0	
1253664480	6002296	RECOVERY_EQUALIZATION_PHASE2	16.0	
1259666776	23009232	RECOVERY_EQUALIZATION_PHASE2	16.0	
1282676008	1999976	RECOVERY_EQUALIZATION_PHASE3	16.0	
1284675984	2000000	RECOVERY_EQUALIZATION_PHASE3	16.0	
1286675984	2000000	RECOVERY_EQUALIZATION_PHASE3	16.0	
1288675984	24	RECOVERY_EQUALIZATION_PHASE3	16.0	
1288676008	1504	RECOVERY_RCVR_LOCK	16.0	
1288677512	552	RECOVERY_RCVR_CFG_TS2	16.0	
1288678064	1536	LOOPBACK_ENTRY_MASTER_TS1	16.0	
1288679600	----	LOOPBACK_ACTIVE_MASTER	16.0	

If the link training has failed, the log will show Detect and Polling states in the following example:



Time [ns]	ΔTime [...	State	Speed[GT/s]	Detect Pre
0	0	INITIAL	16.0	
17280	17280	DETECT_QUITE	16.0	
12017280	12000000	DETECT_ACTIVE	16.0	
12017296	16	POLLING_ACTIVE_TS1	16.0	
36017296	24000000	INITIAL	16.0	
36017312	16	DETECT_QUITE	16.0	
48017312	12000000	DETECT_ACTIVE	16.0	
48017328	16	POLLING_ACTIVE_TS1	16.0	
72017328	24000000	INITIAL	16.0	
72017344	16	DETECT_QUITE	16.0	
84017344	12000000	DETECT_ACTIVE	16.0	
84017360	16	POLLING_ACTIVE_TS1	16.0	
108017360	24000000	INITIAL	16.0	
108017376	16	DETECT_QUITE	16.0	
120017376	12000000	DETECT_ACTIVE	16.0	
120017392	16	POLLING_ACTIVE_TS1	16.0	
144017392	24000000	INITIAL	16.0	
144017408	16	DETECT_QUITE	16.0	

10.3.4 Link Training Failure Troubleshooting

If the link training has been unsuccessful, perform troubleshooting for any of the following cases that may have been encountered during testing.

a) The LTSSM state for link training is repeated at 2.5 GT/s:
- Check that the instruments and fixtures have been properly connected.
- Ensure sufficient power supply to the DUT.
- Press the Power Reset button on the CBB or reboot the DUT.
- Connect the MU195050A noise generator data outputs directly to the MU195040A SI error detector data inputs, and try to run link training by selecting 'Configuration' under the Loopback through field in the Link Training tab.

b) The DUT enters the 8 or 16 GT/s LTSSM state, but the Loopback Active state is not shown.

- Set all Jitter and Noise to OFF on the BERT.
- Remove the ISI channel and connect data signals to the DUT directly.
- Press the Power Reset button on the CBB or reboot the DUT.
- Ensure the PPG Output setting is ON.
- Change to other Preset values, for example:
  - P7 is recommended to be used for PCIe Gen 3.
  - P5, P6, P8 and P9 are recommended for PCIe Gen 4.
- Ensure the correct EIEOS pattern revision of the DUT is being used.

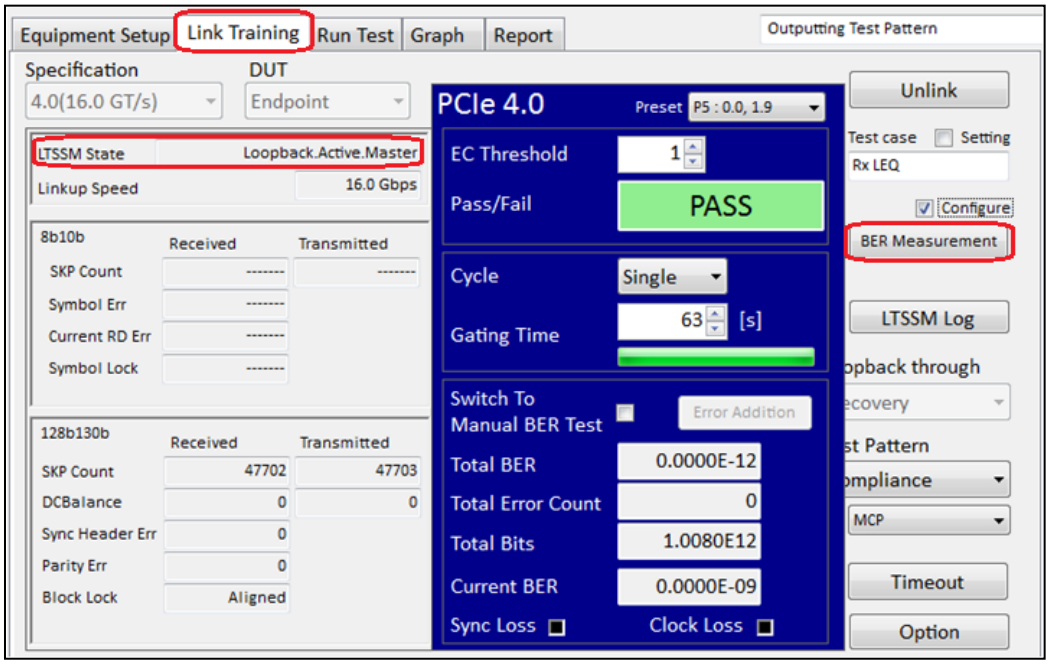
If link training still fails, restart both the MX190000A and MX183000A applications.

10.4 Perform DUT Rx Compliance Testing

This section describes how to test the DUT to meet PCIe CEM 4.0 Rx electrical compliance specs. The Rx path is tested with worst case stressed eye to ensure a BER of less than 1E-12 can be achieved. An optional jitter tolerance test is also described here.

The Rx compliance test can be performed once the DUT has passed the link training loopback tests (as described in the previous section).

1. Enable all calibrated stresses on the BERT.
2. In the same link training window from the previous test, the LTSSM State will show 'Loopback.Active.Master' to indicate link training has been successful. From there, select 'BER Measurement' to start the error detection process for the DUT.

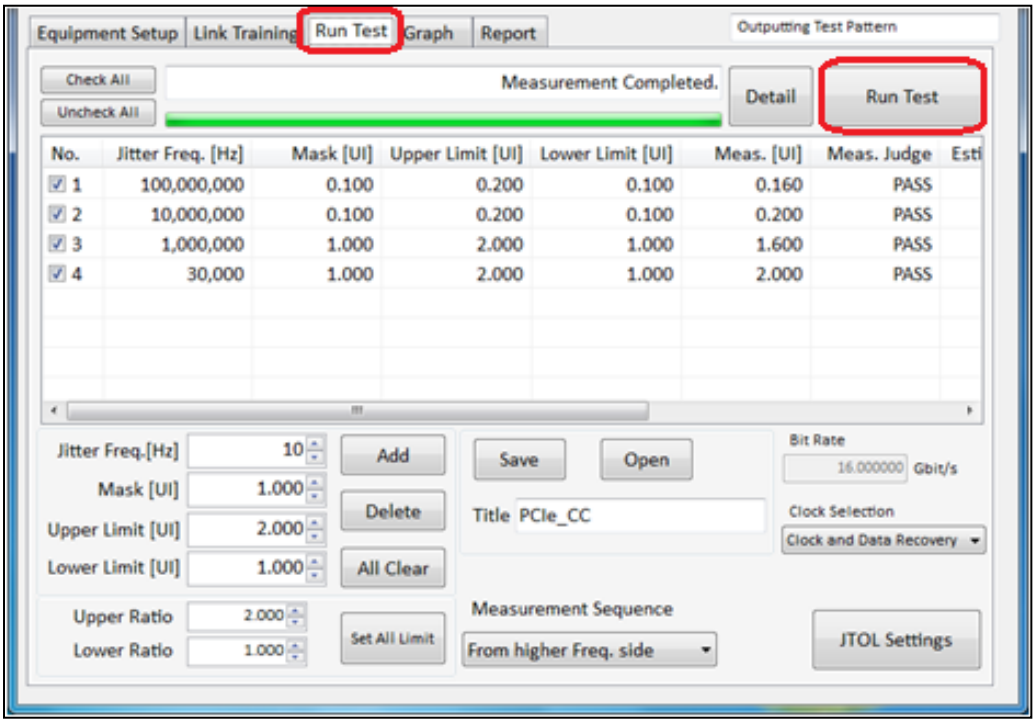


3. Run the test for 63 seconds (for the PCIe Gen 4 DUT) or 125 seconds (for the PCIe Gen 3 DUT) with maximum of one error at a single preset.

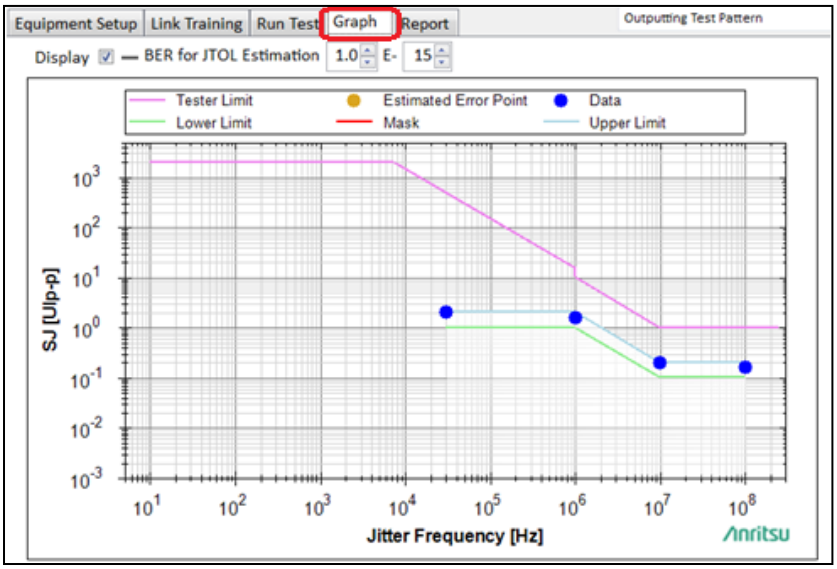
10.4.1 Jitter Tolerance Testing (Optional)

The DUT can be additionally tested for jitter tolerance after it has passed Rx compliance testing. The optional jitter tolerance test is basically carried out to search for SJ margins and measure the BER.

1. Continuing from the same Rx compliance test window, select the Run Test tab. Select 'Run Test' to start running measurements for jitter tolerance.



2. When completed, select the Graph tab to view a data plot from the measurement results.



11 Appendix B: SigTest Tool Tab

The SigTest Tool allows the user to manually perform SigTest verification tests for the DUT using appropriate offline PCIe compliant SigTest template and waveform files. This function is used for debugging purposes.

1. Select  from the GRL PCIe CEM 4.0 Rx Test Application menu to access the Setup Configuration page.

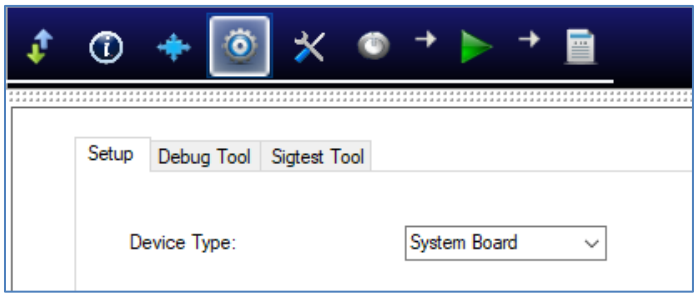


FIGURE 61. SETUP CONFIGURATION PAGE

2. Select the **SigTest Tool** tab.

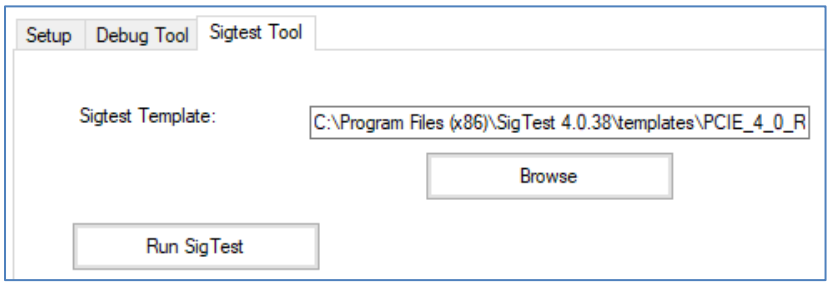


FIGURE 62. PERFORM SIGTEST DEBUGGING

3. Select the 'Browse' button to go to the specific SigTest template file directory and select the template file to be used. Then select the 'Run SigTest' button to perform SigTest using a selected saved offline waveform file. When selected, the GRL software will automatically run the SigTest for the waveform as shown in below example.

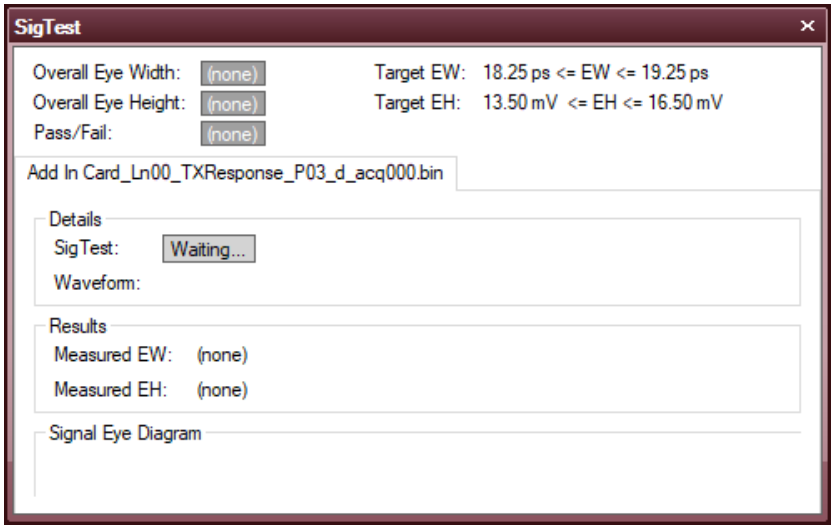


FIGURE 63. RUNNING OFFLINE SIGTEST VERIFICATION

4. Once test is completed, the results will be displayed like in the following example.

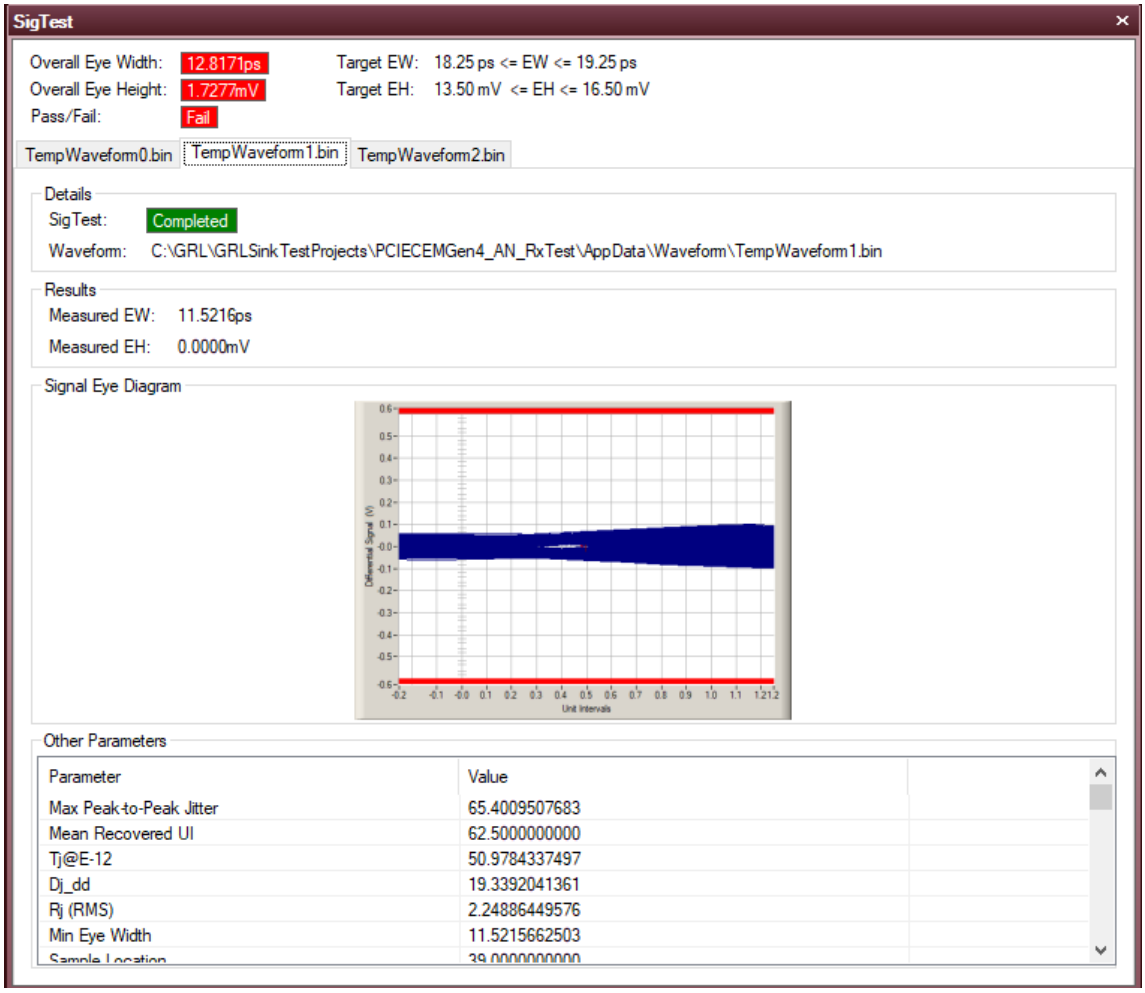


FIGURE 64. VIEWING SIGTEST ANALYSIS RESULTS

12 Appendix C: Debug Tool Tab

The Debug Tool allows the user to manually perform Tx link equalization time response tests with presets and cursors for the DUT using appropriate offline PCIe compliant waveforms. This function is used for debugging purposes.

1. Select  from the GRL PCIe CEM 4.0 Rx Test Application menu to access the Setup Configuration page.

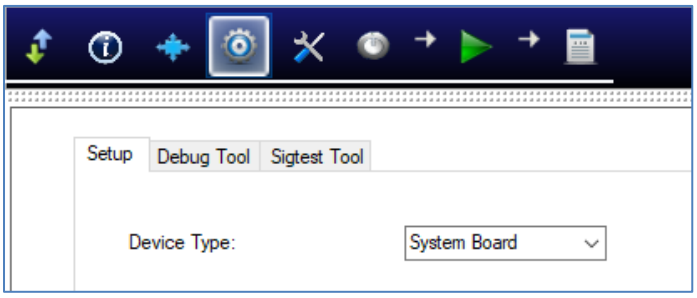


FIGURE 65. SETUP CONFIGURATION PAGE

2. Select the **Debug Tool** tab.

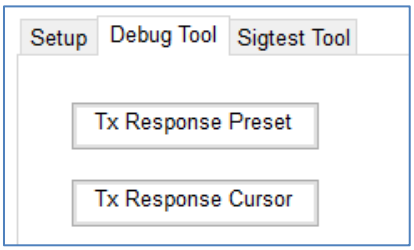


FIGURE 66. PERFORM TX LINK EQ TIME RESPONSE OFFLINE TESTS DEBUGGING

3. Select the 'Tx Response Preset' or 'Tx Response Cursor' button to initiate the respective Tx link EQ time response test. The Select Waveforms pop-up will appear as below.

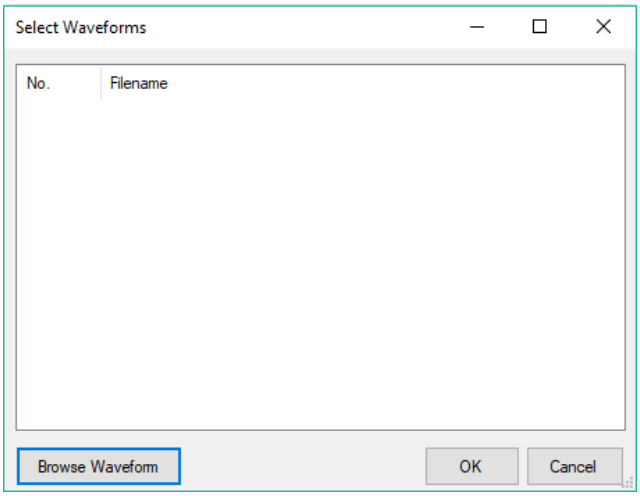


FIGURE 67. INITIATE TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST

4. Select the 'Browse Waveform' button to go to the specific offline waveform file directory and select the waveform file to be used. When selected, the GRL software will automatically run the Tx link EQ time response preset/cursor test for the waveform as shown in below example.

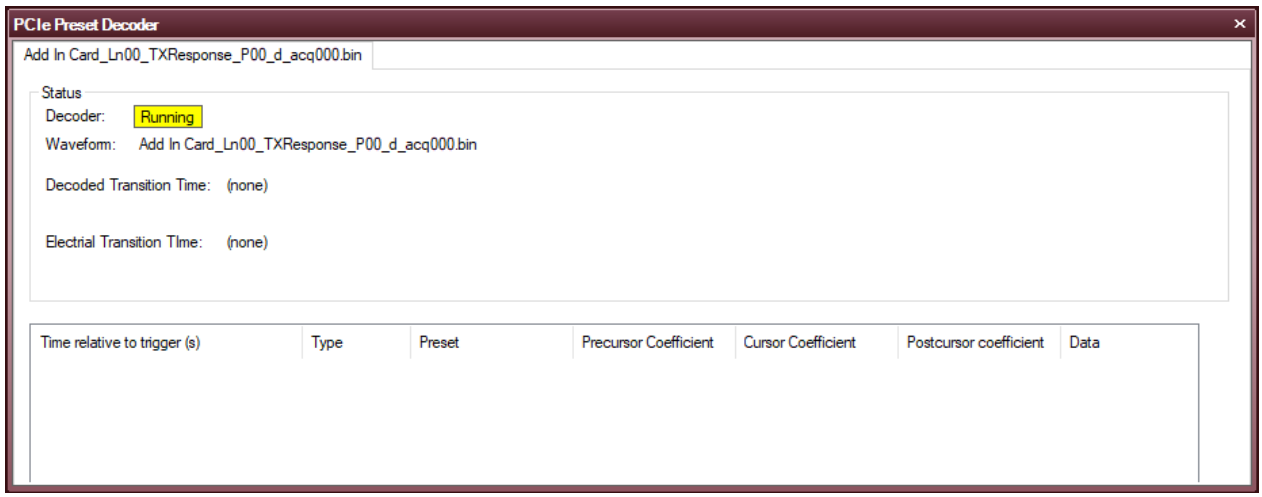


FIGURE 68. RUNNING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST

5. Once test is completed, the results will be displayed like in the following example. A detailed list of the entire requested equalization change can be viewed at the bottom of the window. To quickly determine at which point the Tx equalization change starts to happen in the DUT, select the 'Show' button which will display the row highlighted in yellow.

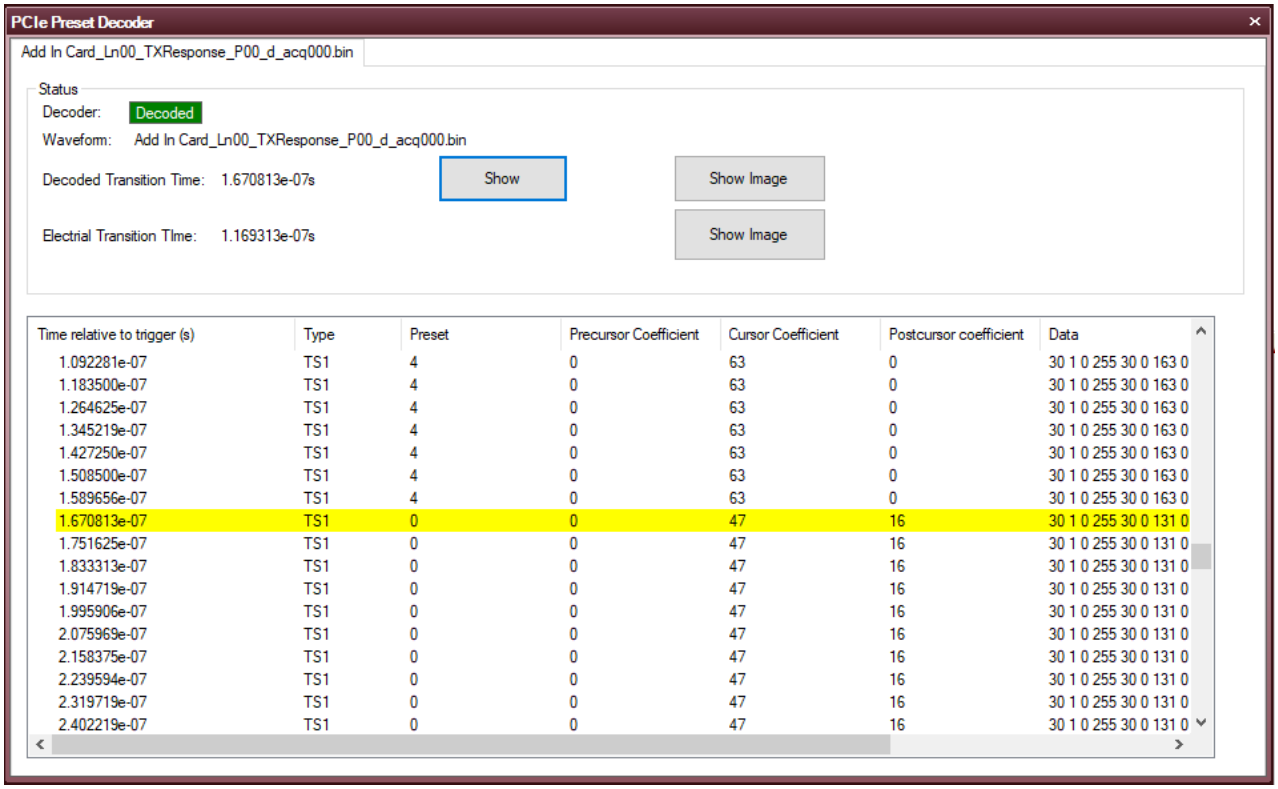


FIGURE 69. VIEWING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST RESULTS

6. For further analysis of the test results, respective traces for the decoded and electrical transition times can be viewed by selecting the 'Show Image' button for each category. An example is shown below.

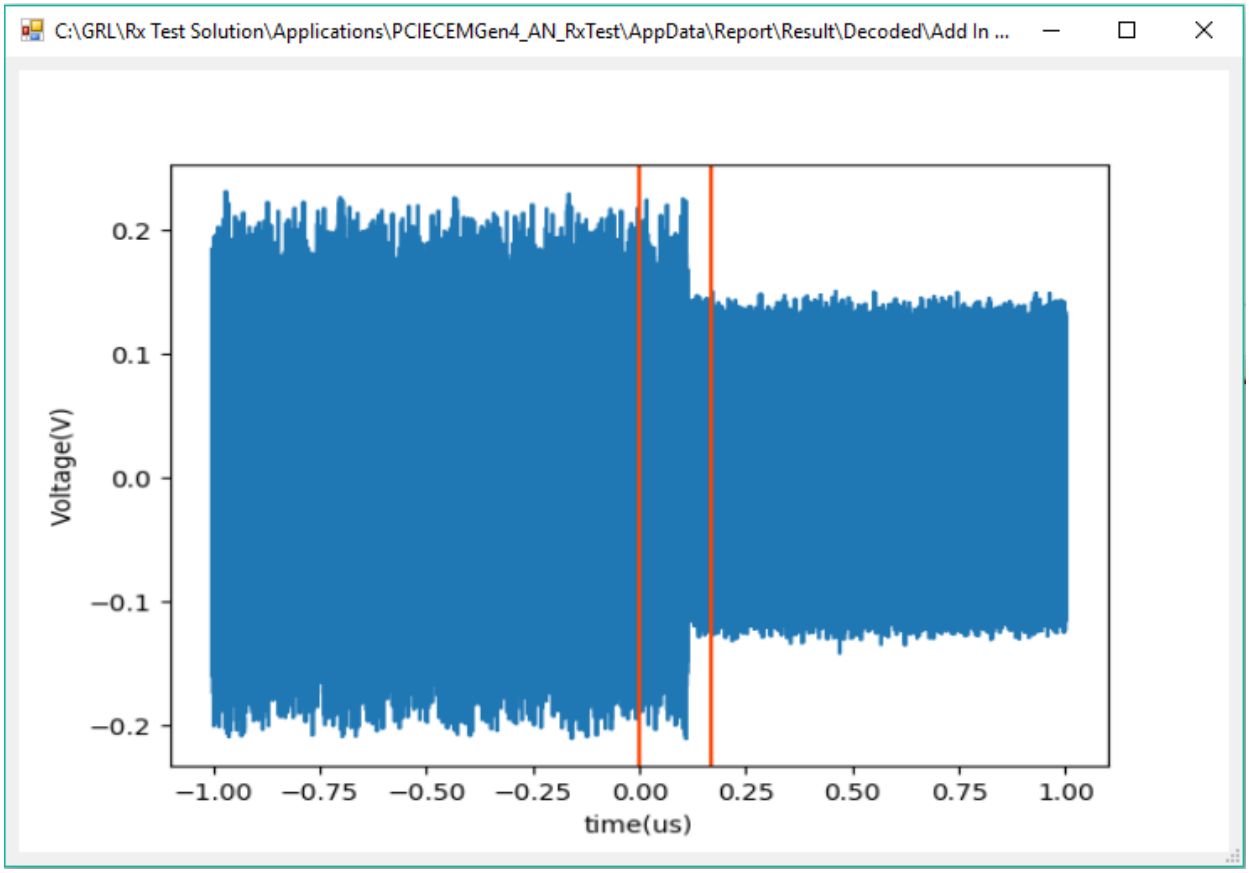


FIGURE 70. VIEWING TX LINK EQ TIME RESPONSE PRESET/CURSOR TEST TRACE FOR TRANSITION TIME

Note: The Decoded transition time serves as an informative value only and not required for compliance.

13 Appendix D: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

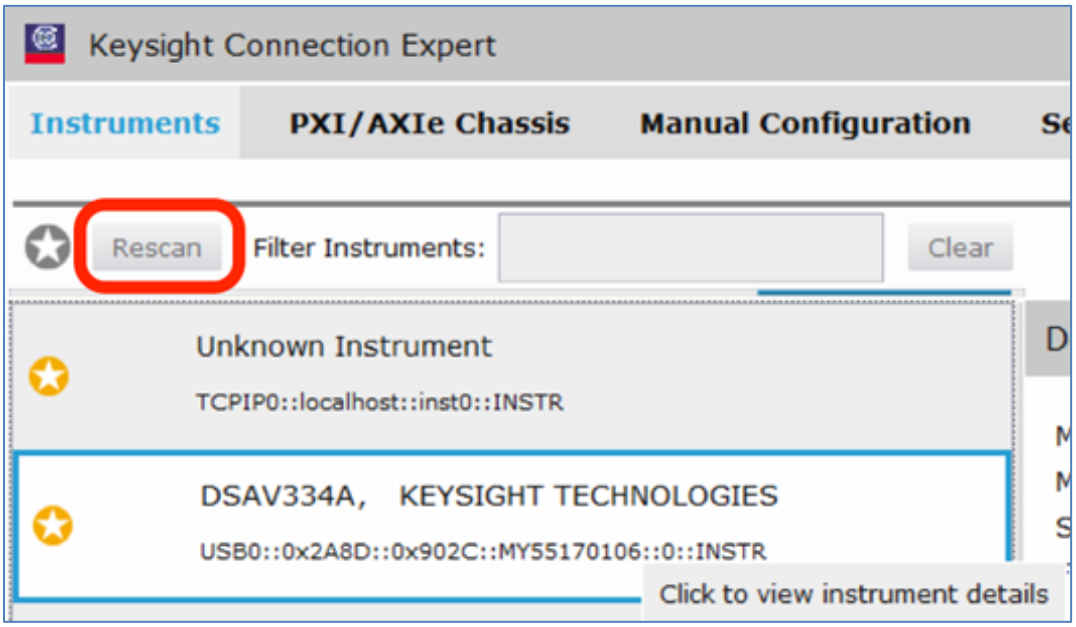


FIGURE 71. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

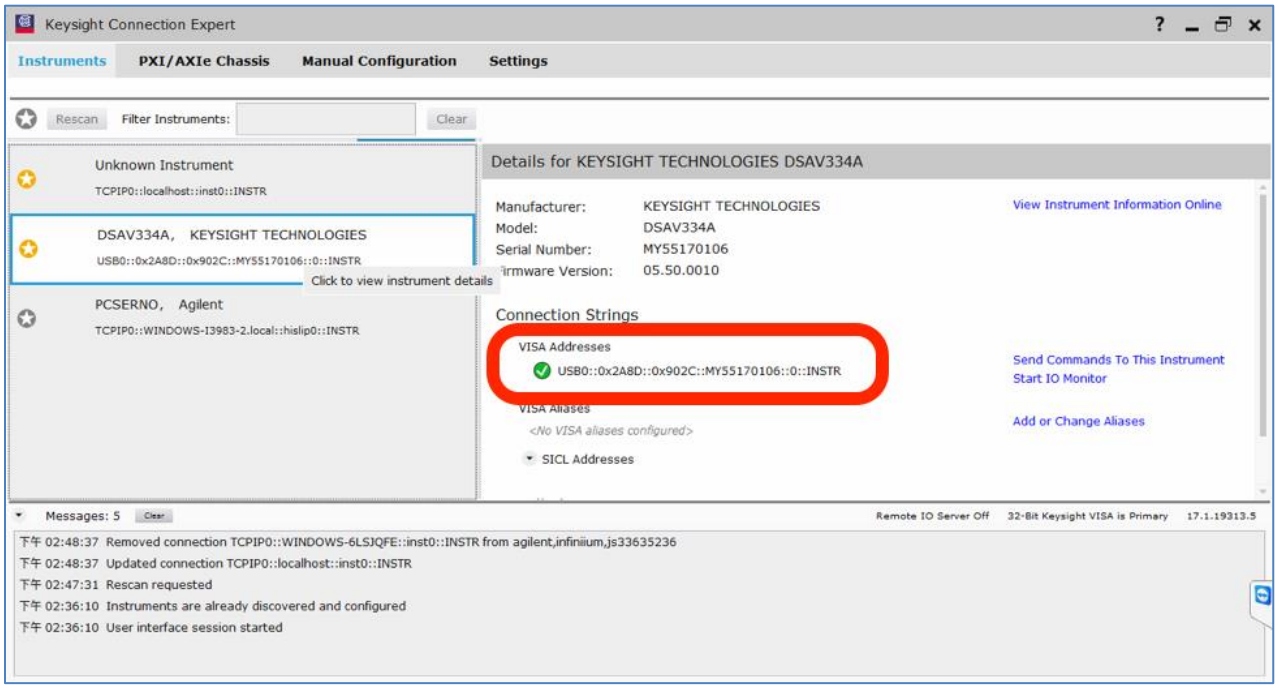


FIGURE 72. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe CEM 4.0 Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

   If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".

14 Appendix E: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

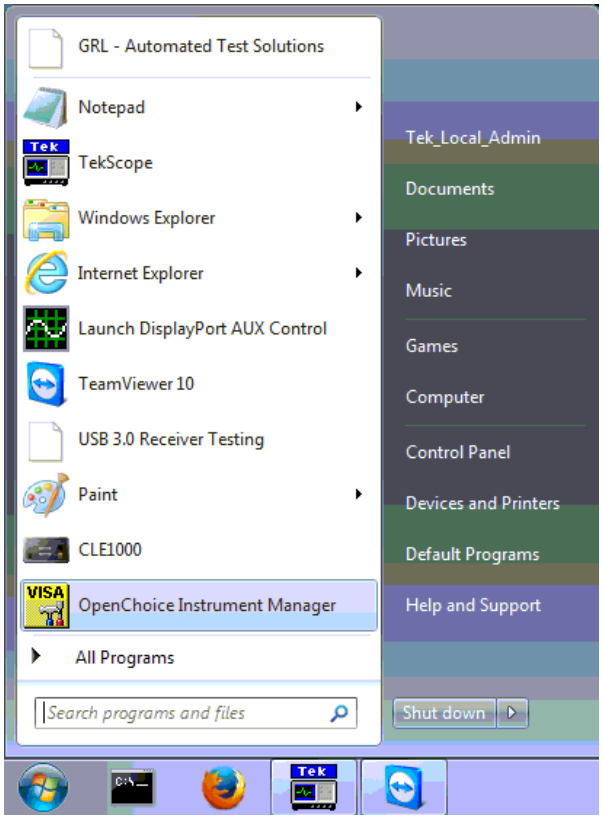


FIGURE 73. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
   a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
   b) “Search Criteria”: Select to configure the instrument search function.
   c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
   d) “Properties”: Select to display and view the selected instrument properties.

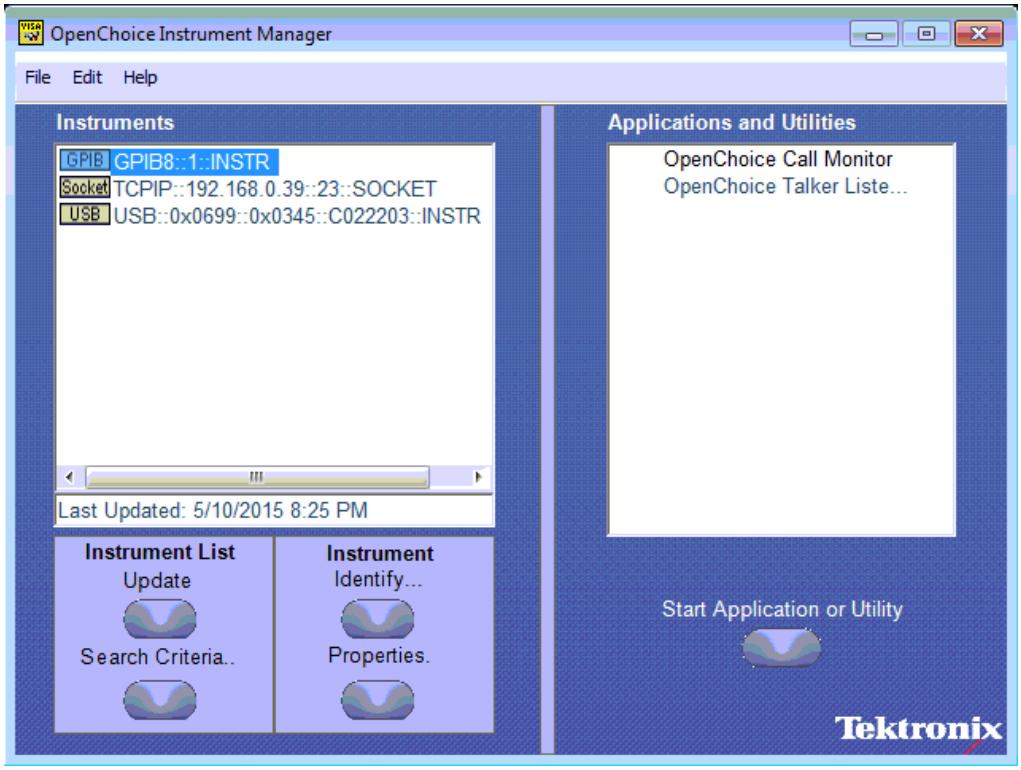


FIGURE 74. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe CEM 4.0 Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe CEM 4.0 Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

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