Granite River Labs
PCI Express® 4.0 Base Specification (Version 1.0)
Receiver Test Method of Implementation (MOI)
for Anritsu 16Gbps Physical Layer Test Suite
Using Anritsu MP1800A/MP1900A BERT,
High Performance Real-time Oscilloscope,
and GRL-PCIE4-BASE-RXA Calibration and Test Software

Contact the GRL office to obtain the latest revision of this document

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TABLE OF CONTENTS

List of Figures

Revision Record

Revision	Date	Description of Changes	Author(s)
0.5	6/2016	GRL-PCIE4-RXA MOI Add Software Guide. Add Advanced Features.	Bill Altmann (GRL)
0.7	8/2016	PCIe4 Rev 0.7 updates.	Bill Altmann (GRL)
0.71	8/2016	Add Scope Deskew Method	Bill Altmann (GRL)
0.72	1/2017	Update Scope Deskew Method Add Artek CLE1000-A2 Installation	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
0.73	2/2017	Update Content Flow	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
0.74	5/2017	Update Select Tests Info	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
0.8	12/2017	Update Equipment and related content	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.0	2/2018	Update per V1.0 specs	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.03	6/2018	Update per latest SW version and feedback	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.04	7/2018	Update per latest SW version	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.05	8/2018	Update equipment connection	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.06, 1.07	10/2018	Update setup configuration and test selection list. Update Appendix E.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.08	11/2019	Update UI screenshot images.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.09	05/2020	Update Calibration Parameters per latest SW version.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.1	10/2020	Added V-K adapter (for PAM4 PPG) to Equipment Requirements	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com

1 Introduction

This User Guide & MOI describes the procedures for receiver (Rx) calibration and jitter tolerance testing based on the PCIe Base 4.0 (ASIC) Specification (for 16 GT/s), using the GRL-PCIE4-BASE-RXA PCIe 4.0 Base Specification Receiver Calibration and Test Software to automate the Anritsu BERT Model (MP1800A/MP1900A) and a high performance real-time oscilloscope to calibrate the stressed eye opening and test receiver conformance and jitter tolerance. The GRL-PCIE4-BASE-RXA software uses Seasim statistical data eye simulator to establish the calibrated test channel DDJ. The final calibrated eye diagram uses both Seasim and SigTest software to achieve the final stressed eye calibration.

The BERT and appropriate accessories provide the necessary test patterns with jitter, ISI, and crosstalk. Additionally, the BERT is used to add the required transmitter (Tx) equalization. The receiver jitter tolerance test includes various Differential Mode Sinusoidal Interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver eye opening has been calibrated, the receiver jitter tolerance and margin testing can then be performed on the device under test (DUT). The BERT is used to transmit a modified compliance pattern to the receiver DUT and monitors that the loopback pattern conforms to a Bit Error Ratio (BER) that is less than 10^{-12} with a confidence level of 95%.

In summary, this User Guide & MOI basically describes using the GRL-PCIE4-BASE-RXA software to:

1. Calibrate the stressed eye at the receiver of the DUT.
    - This includes calibrating Voltage Swing, Random Jitter (RJ), Sinusoidal Jitter (SJ), Differential Noise, Common Mode Noise, Tx Equalization and Eye Height & Width.
2. Test the receiver using Bit Error Ratio (BER) as a metric. The receiver path is tested with worst case eye to ensure a BER of less than 10^{-12} can be achieved.

Note: Important information detailing method of implementation using automation, oscilloscope and cable calibration, as well as other setup information are included in Appendixes of this document. It is highly recommended to thoroughly review these information prior to performing any testing or data collection.

The GRL-PCIE4-BASE-RXA software is designed to work with the Anritsu BERT as a signal source and error detector for automation of the PCIe Gen 4.0 Base Receiver calibration and testing. Details on how to set up and configure the GRL software are provided in this document.

1.1 Glossary

SJ	Sinusoidal Jitter
ISI	Inter Symbol Interference
RJ	Random Jitter
CTLE	Continuous Time Linear Equalization
DFE	Decision Feedback Equalization
CDR	Clock / Data Recovery
BER	Bit Error Rate
BERT	Bit Error Rate Tester
EH	Eye Height
EW	Eye Width
DPP	Digital Pre-emphasis Processor
Upstream	Reference to Host Test Setup (Calibrated with Device Channel)
Downstream	Reference to Device Test Setup (Calibrated with Host Channel)
DUT	Device Under Test

1.2 Reference Documents

[1] PCI Express® Base Specification Rev. 4.0; Version 0.7; March, 2016
[2] PCI Express® Base Specification Rev. 4.0; Version 1.0; September 27, 2017
[3] PCI Express Card Electromechanical Specification, Revision 4.0
[4] PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
[5] PCI Express Mini Card Electromechanical Specification, Revision 2.1
[6] PCI Express OCuLink Specification, Revision 1.0
[7] PCI Express M.2 Specification, Revision 1.1
[8] PCI Express External Cabling Specification, Revision 2.0
[9] PCI Express ExpressModule Electromechanical Specification, Revision 1.0
[10] PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0
[11] PCI Hot-Plug Specification, Revision 1.1
[12] PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0
[13] PCI Code and ID Assignment Specification, Revision 1.9 (or later)
[14] PCI Firmware Specification, Revision 3.2
[15] Advanced Configuration and Power Interface Specification, Revision 6.2
[16] Unified Extensible Firmware Interface (UEFI) Specification Version 2.7 Errata A
[17] Guidelines for 64-bit Global Identifier (EUI-64) Registration Authority
[18] Multi-Root I/O Virtualization and Sharing Specification, Revision 1.0

The most current versions of above documents and ECNs are available to PCI-SIG Working Group members at: http://www.pcisig.com/specifications/pciexpress/

1.3 Acknowledgements

The following individuals and their companies have contributed to the creation and maintenance of this document:

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1.4 Feedback

Please send feedback on this document to info@graniteriverlabs.com.

2 Resource Requirements

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS AND ACCESSORIES

Equipment	Qty.	Description	Key Specification Requirement
Keysight/Tektronix Oscilloscope	1	High Performance Real-time Oscilloscope [a]	≥ 32 GHz bandwidth with Windows 7+ OS [b]
Anritsu MP1800A/ MP1900A BERT	1	MP1800A Signal Quality Analyzer (Option: 002, 007, 014, 032), with following modules: • MU181000A/B 12.5GHz Synthesizer (Option 001) • MU181500B Jitter Modulation Source • MU183020A 28G/32Gbit/s SI Pulse Pattern Generator (Option 012 or 022 [1-channel or 2-channel], 030 or 031) • MU183040B 28G/32Gbit/s SI High Sensitivity Error Detector (Option 010 or 020 [1-channel or 2-channel], 022)	
	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator • MU195040A 21G/32G bit/s SI Error Detector • MU195050A Noise Generator	
Anritsu MP1825B	1	De-Emphasis Signal Converter	Option: 002 Applies for MP1800A BERT only
Anritsu MG3710A	2	Vector Signal Generator	Option: 002, 029, 036, 041, 066, 071 Applies for MP1800A BERT only
ISI Generator	1	PCIe-4 Base Spec compliant Fixed or Variable ISI Channel [c]	
Anritsu K241C	2	Power Splitter	Applies for MP1800A BERT only
Anritsu 41KC-3	2	Attenuator	Applies for MP1800A BERT only
Anritsu 41KC-6	2	Attenuator	Applies for MP1800A BERT only
Anritsu 41KC-20	2	Attenuator	Applies for MP1800A BERT only
Anritsu J1510A	2	Pick-off Tees	Applies for MP1800A BERT only
Anritsu 34VKF50A	*2*	*V(m) - K(f) Coaxial Adapter*	**Only required if using a PAM4 Pulse Pattern Generator*
Computer	1	Laptop or desktop (Windows 7+ OS) for automation control	

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

[c] The Artek CLE Model Series is supported for variable ISI generation. Refer to Appendix of this document for the Artek CLE Series driver installation procedure.

Note: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table below is a recommended list. Please also refer to the respective manufacturer for detailed cabling recommendations related to PCI Express.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable	Qty.	Key Specification Requirement
Anritsu J1508A BNC to SMA cable pair	1 pair	For MU181000A/B to MU181500B
Anritsu J1349A SMA-SMA cable	2	30cm
Anritsu J1343A SMA-SMA cable	4	100cm
Anritsu J1551A or Huber Suhner 0130-314-00 SMA-SMA phase matched cable pair	2 pairs	3ft
Anritsu J1615A K-K cable set	1	For MU183020A PPG clock (130cm) / data (80cm) to connect to MP1825B de-emphasis box *(if using MP1800A BERT)* Or For MU195050A output connections *(if using MP1900A BERT)*
Rosenberger L71-456-102 or Rosenberger RNA 0111 603841, phase matched SMA-SMP adapters	2 pairs	

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Source
GRL-PCIE4-BASE-RXA[a]	Granite River Labs PCIe® 4.0 (16 GT/s and 8 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com Included with Node Locked License to single oscilloscope or PC OS
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-PCIE4-CEM-RXA software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
Seasim	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software at TP2P) – www.pcisig.com Used for Channel (DDJ) calibration
SigTest	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html SigTest used with Seasim for final eye calibration
MX183000A	Anritsu High-Speed Serial Data Test Software – For loopback BER testing of the PCIe Gen 4 Base Rx DUT. This software is located on the BERT.

[a] PCIe3-BASE and PCIe4-BASE will need to be installed to test at both 16 GT/s and 8 GT/s data rates. If the GRL-PCIE4-RXA test solution is purchased, the user will need to install the GRL-PCIE4-BASE-RXA and GRL-PCIE4-CEM-RXA solutions included in the package to perform testing for PCIe4-BASE and PCIe4-CEM at 16 GT/s and 8 GT/s.

3 Setting Up GRL-PCIE4-BASE-RXA Software

3.1 Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL-PCIE4-BASE-RXA PCIe 4.0 Base Receiver Test software at 16 GT/s. It also helps you familiarize yourself with the basic operation of the application.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

3.1.1 Download Software

Install, launch and set up the GRL-PCIE4-BASE-RXA software:

1. If the GRL-PCIE4-BASE-RXA software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The zip file contains:
   a) **PCIe4_0_BaseANPatternFilesInstallation001xxxxxxxSetup.exe** – Run this on the Anritsu Signal Quality Analyzer to install the test pattern setup files.
   b) **PCIEGen4ANBaseSpecTestApplication001xxxxxxxSetup.exe** – Run this on the controller PC or oscilloscope to install the GRL-PCIE4-BASE-RXA application.
   c) **PCIe4_0_BaseANRxTestScopeSetupFilesInstallation001xxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.
4. Launch and set up the software as follows:
   a) Open the GRL Folder under the Windows Start Menu. Click on GRL Framework within the GRL Folder. The GRL Framework will launch.

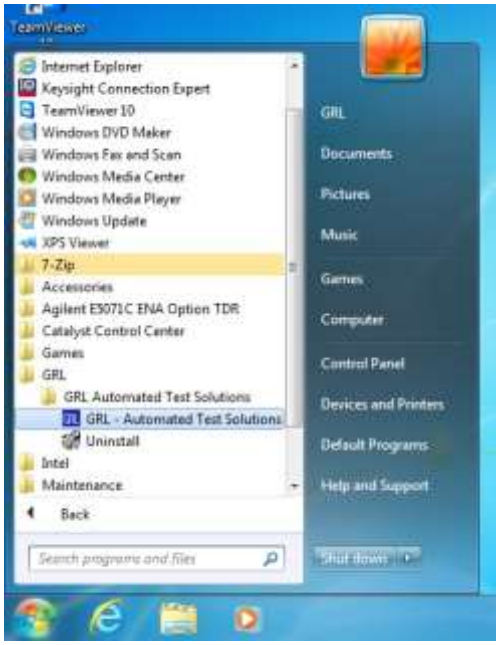


FIGURE 1. LAUNCHING GRL FRAMEWORK

b) From Application→Rx Test Solution drop-down menu, select "Anritsu PCIe 4.0 Base Rx Test". If the selection is grayed out, it means that your license has expired.

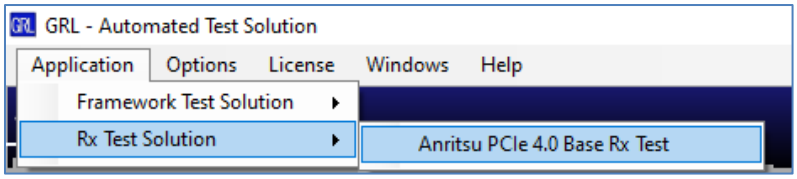


FIGURE 2. LAUNCHING PCIE 4.0 BASE RX TEST APPLICATION

i) To enable license, go to License→License Details.

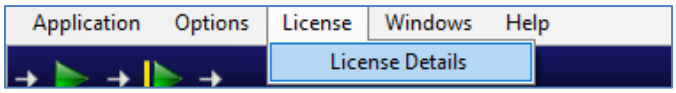


FIGURE 3. LICENSE DETAILS

ii) Review the installed applications.

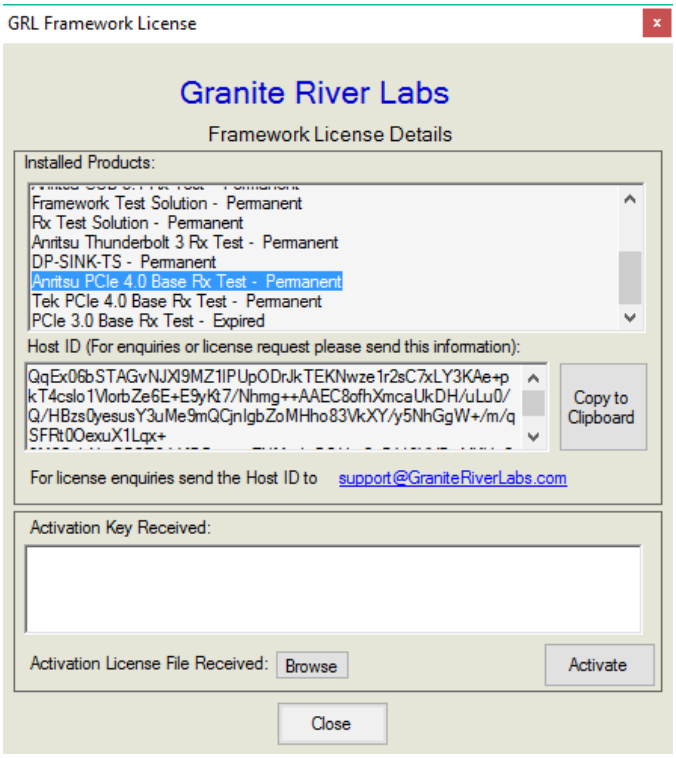


FIGURE 4. INSTALLED APPLICATIONS

iii) Activate a License:

[1] If you have an Activation Key, enter it in the box provided, and select Activate.
[2] If you do not have an Activation Key, select Close to use the software for 10 days free of charge.

Note: Once the 10-day trial times out, you will need to request an Activation Key for future usage on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device.

For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.

3.1.2 Connection Configuration on the Scope's OS

3.1.2.1 Connecting Anritsu Signal Quality Analyzer with PC

Connect the Anritsu Signal Quality Analyzer with the PC through LAN.

3.1.2.2 Connecting Anritsu MG3710A with PC

Connect the Anritsu Vector Signal Generator with the PC through LAN.

3.1.2.3 Connecting Artek CLE Series with PC

Connect the Artek ISI Generator with the PC through USB. (*Note: The USB driver software for the ISI Generator must be installed on the PC. The driver is available from the ISI Generator manufacturer. Refer to Appendix of this MOI for driver installation information.)*

3.1.2.4 Connecting Oscilloscope with PC

Connect the oscilloscope with the PC through either GPIB, USB or LAN. *(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the PC is provided in the Appendix of this MOI.)*

3.1.3 Launch and Set Up Software

3.1.3.1 On the Scope or PC

1. Launch GRL Host Application from Start Menu -> GRL -> GRL – Automated Test Solutions.
2. Select Application -> Rx Test Solution -> Anritsu PCIe 4.0 Base Rx Test Application.
3. On the Scope or PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.
4. If instruments are connected using LAN, type in the IP Address of each instrument into "Address" field, or if using USB, type in the COM address, and click the "lightning" button ().

   The "lightning" button should turn green () once the software has successfully established connection with each instrument.

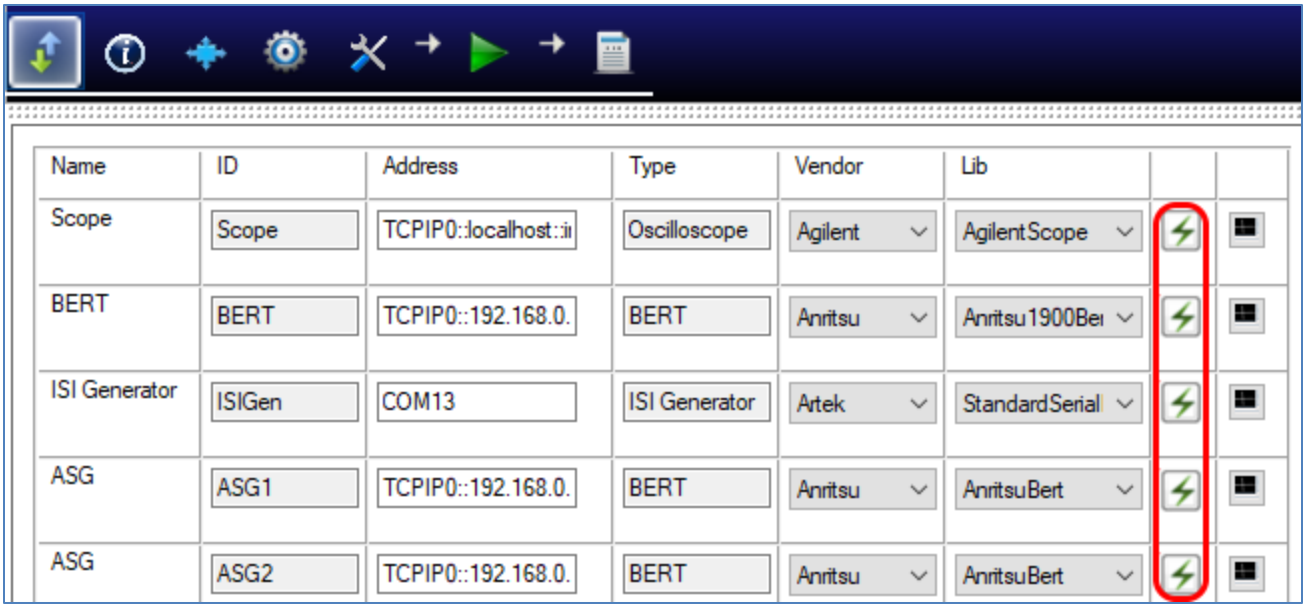


FIGURE 5. GRL RX TEST SOFTWARE INSTRUMENT ADDRESSING

5. *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR.)* If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address. The "lightning" button should turn green if successfully connected to the instrument.

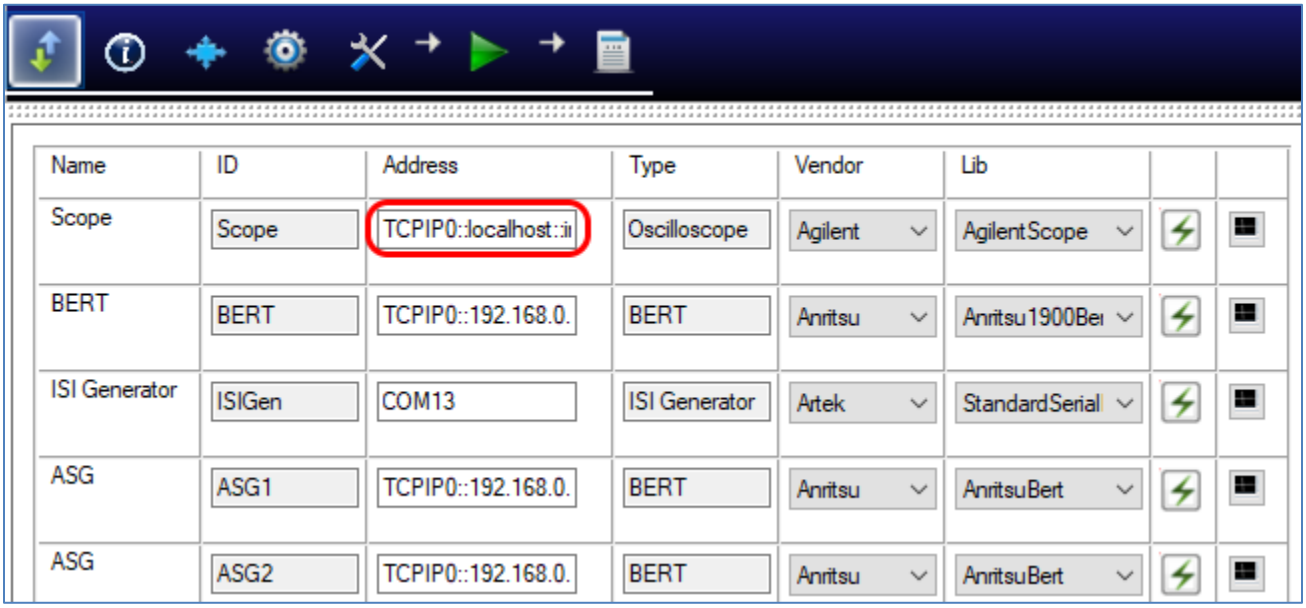


FIGURE 6. GRL RX TEST SOFTWARE IP ADDRESSING ON SCOPE

3.2 Configuring the Software Before Calibration

3.2.1 Session Info

Select  to enter the information for the current calibration/test session which will also be included in the results report.

- The **DUT Info** and **Test Info** are input by the user.
- The **Software Info** is automatically populated.

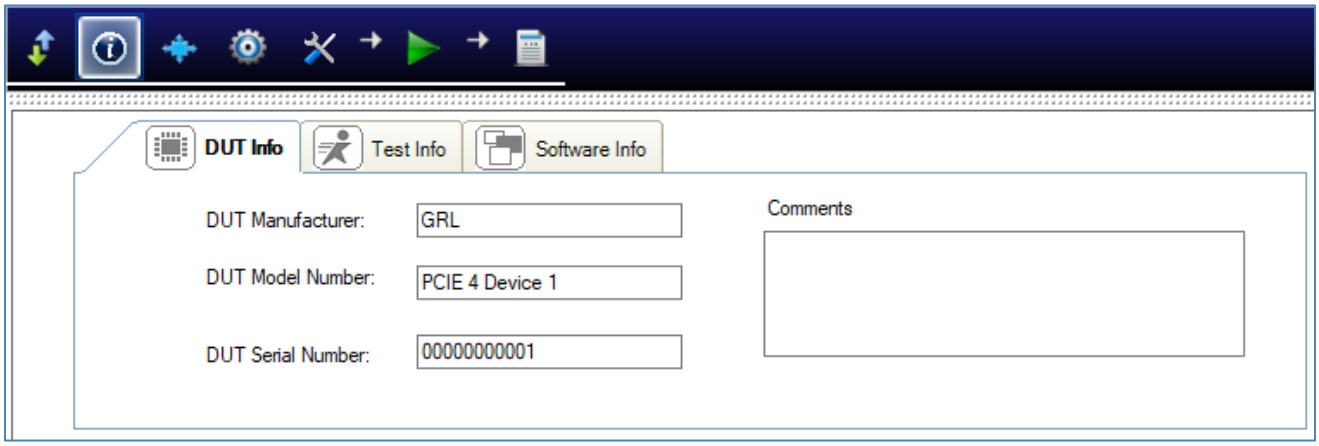


FIGURE 7. SESSION INFO

3.2.2 Conditions for Testing and Calibration

Select  to access the Conditions page to set the conditions for calibration and testing.

When calibrating, the software will calibrate for the selected range, SJ frequency, common mode voltage and differential voltage that the user chooses.

Recommended procedure:

1. When calibrating: select conditions for calibration and perform desired calibration.
2. When testing: re-select desired conditions for testing. For example, it may be only necessary to test range A at SJ frequency. The user would select the appropriate conditions for testing.

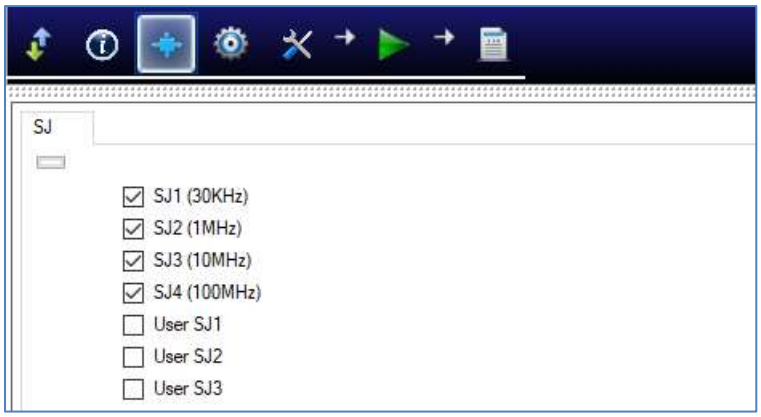


FIGURE 8. CONDITIONS FOR TESTING AND CALIBRATION

3.2.3 Setup Configuration

Select  to access the Setup Configuration page to configure the calibration/test parameters.

3.2.3.1 ISI Generator Setup

Select the type of supported ISI generators to be used:

- "None": This is the recommended method which is used to provide 22 to 27 dB physical channel Insertion Loss for calibration and testing. A PCIe 4.0 CEM Fixture can be used in the setup for this method.
- "Artek": This is provided as an Option. The Artek CLE1000-S2 ISI channel and an additional ISI board can be used in the setup for ISI automation. *(Also see Appendix for more information on installing the Artek CLE Series.)*
- "PCIe ISI Board": This is provided as an Option which can be used to measure Insertion Loss when a Vector Network Analyzer is not available.

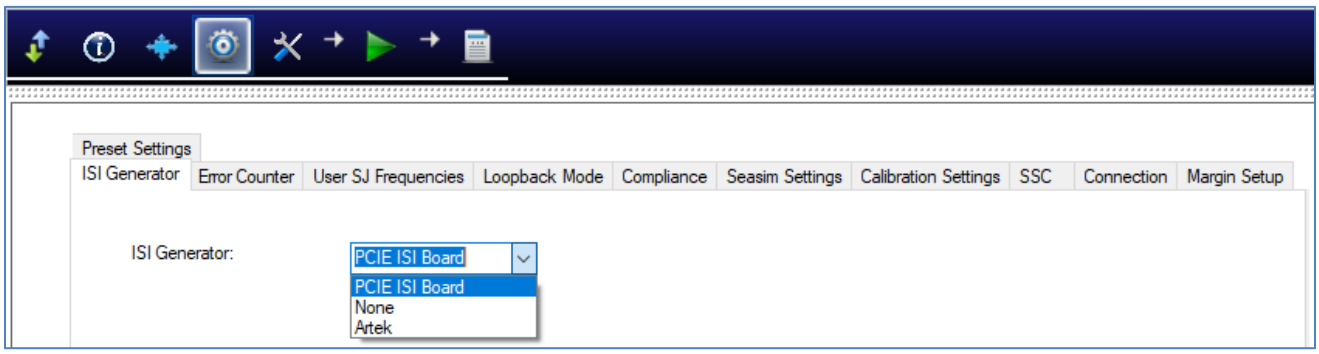


FIGURE 9. ISI GENERATOR SETUP

3.2.3.2 Error Counter Setup

Enable loopback test mode for the Rx base DUT for error detection. If the DUT can be configured to loopback mode, select 'LoopBack', if not select 'Manual'.

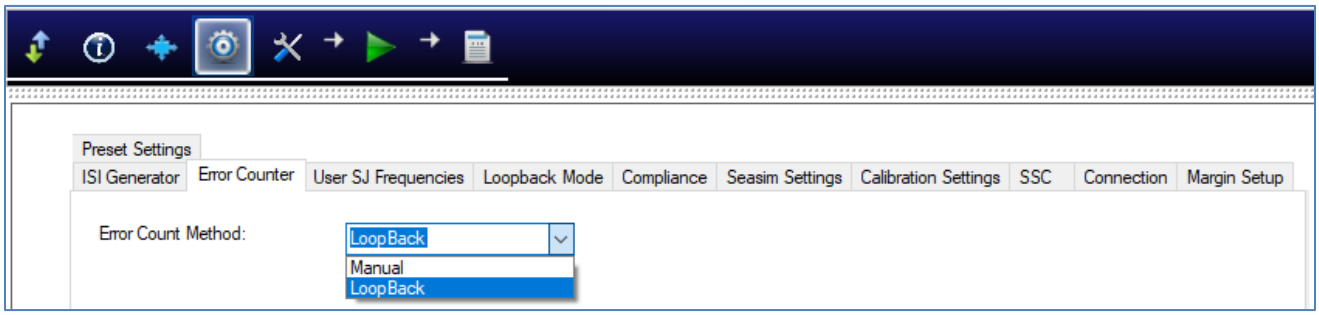


FIGURE 10. BER LOOPBACK TEST METHOD

3.2.3.3 User SJ Frequencies Setting

Set custom SJ frequencies to test for condition setup on the Conditions page.

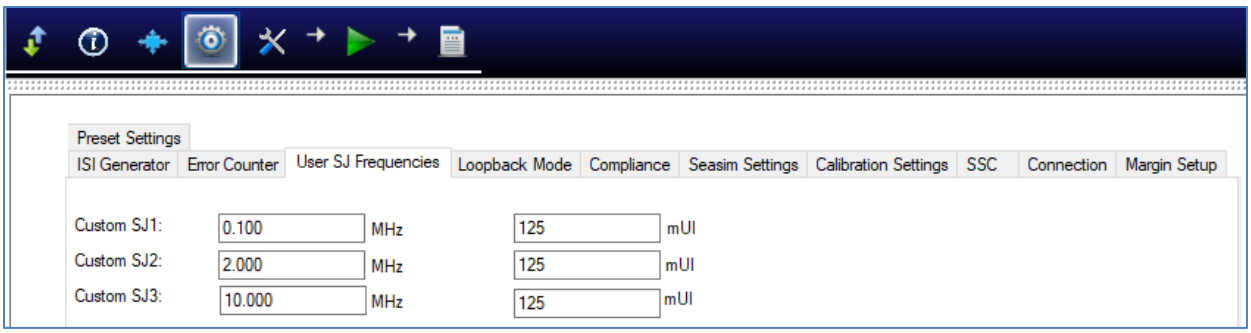


FIGURE 11. USER SJ FREQUENCIES SETTING

3.2.3.4 Loopback Mode Setup

If "LoopBack" has been selected from the Error Counter tab, then select "Clock Recovery" in the Clock Recovery Method drop-down on the Loopback Mode tab. *Other options on the Clock Recovery Method drop-down are not yet supported.*

If a Custom Pattern is to be used for error detection analysis, select the checkbox and then select the test pattern type. If the checkbox is not selected, a default test pattern will be used.

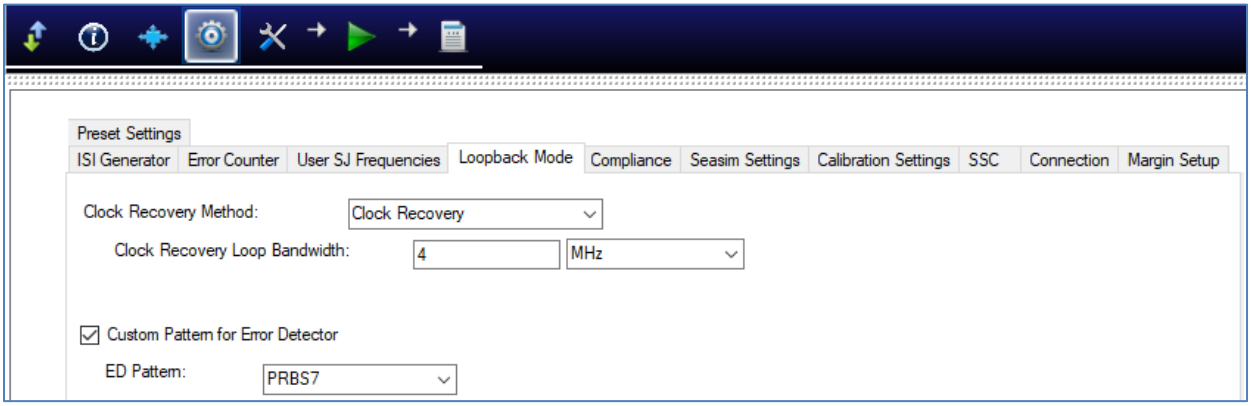


FIGURE 12. LOOPBACK MODE SETUP

3.2.3.5 Compliance BER Setup

Set the allowable BER and Maximum Error limits to be tested for compliance. By default, these limits are set to Specification, but can be defined by the user. The syntax '1e-12' indicates $1x10^{-12}$, and is the only syntax supported in this field. In normal circumstances, any error count above one constitutes a fail.

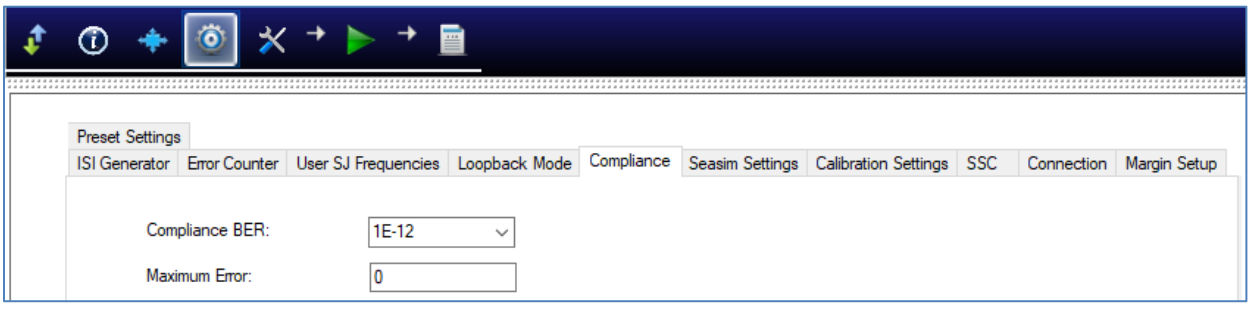


FIGURE 13. COMPLIANCE BER AND MAXIMUM ERRORS SETUP

3.2.3.6 Seasim Settings

Set up user-defined Rx Behavioral package to be applied during post processing analysis for the Eye Height and Eye Width Calibration. Also set the intrinsic jitter (if required) to be used in the Seasim calculation.

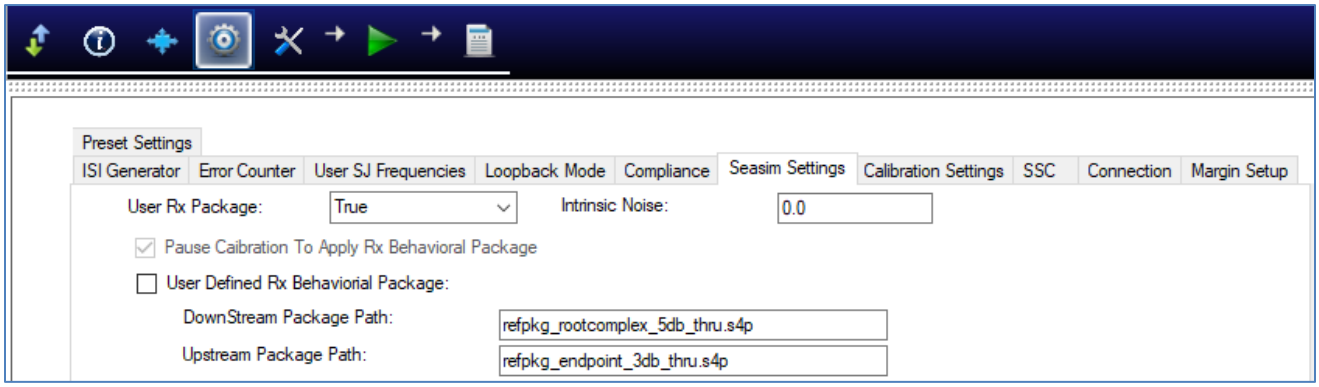


FIGURE 14. SEASIM SETTINGS

3.2.3.7 DM and CM Calibration Settings

Specify or use the default frequency values for Differential Mode (DM) and Common Mode (CM) calibration.

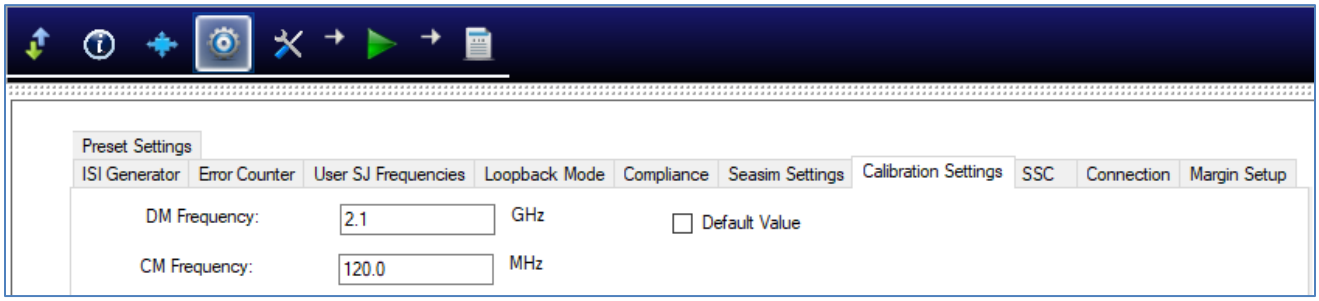


FIGURE 15. DM AND CM CALIBRATION SETTINGS

3.2.3.8 Spread Spectrum Clock (SSC) Setup

Select the checkbox to enable SSC capabilities for calibration and receiver testing (if supported by the DUT) for informative purpose. Set the Frequency and Deviation values for SSC.

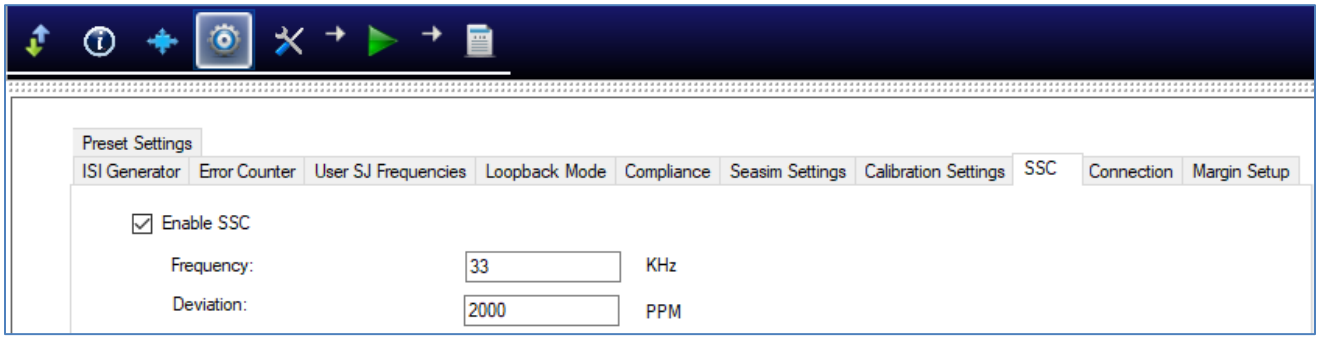


FIGURE 16. SSC SETUP

3.2.3.9 Connection Setup

Set to use Real Edge connection for test setup on the Oscilloscope. *Note: This setting is only applicable for the Keysight Scope and will be disabled when the Tektronix Scope is used.*

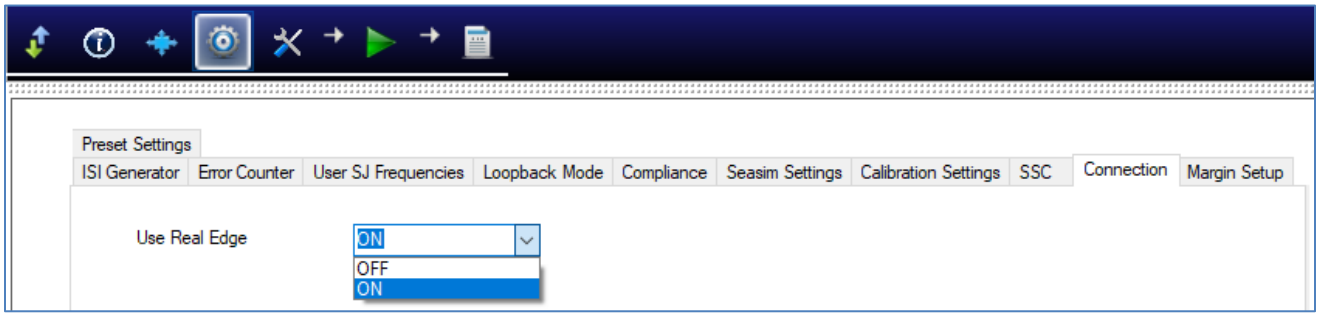


FIGURE 17. CONNECTION SETUP

3.2.3.10 Margin Setup

Select the target BER, step size, and limits to be applied during marginal testing.

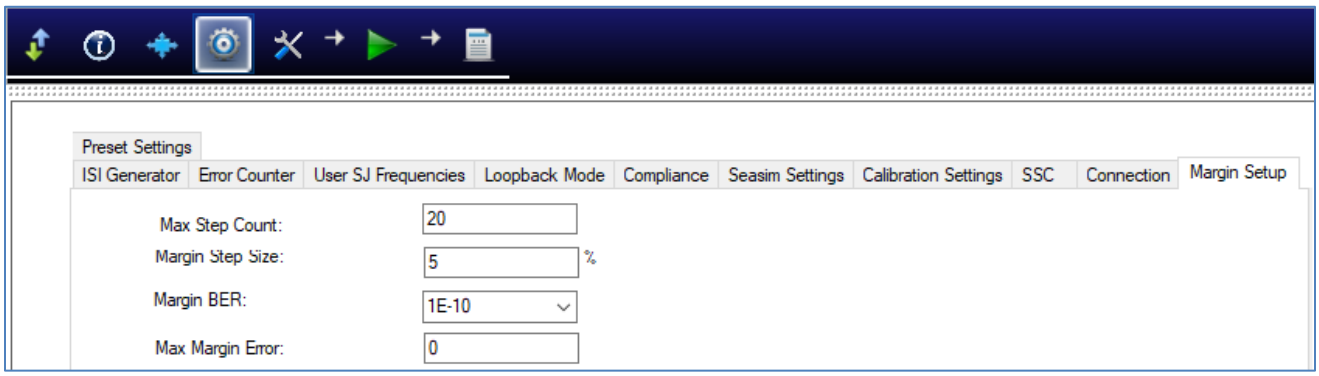


FIGURE 18. MARGIN SEARCH PARAMETERS SETUP

3.2.3.11 Preset Settings

Select the preset to use, and optionally custom Pre-shoot and De-emphasis settings.

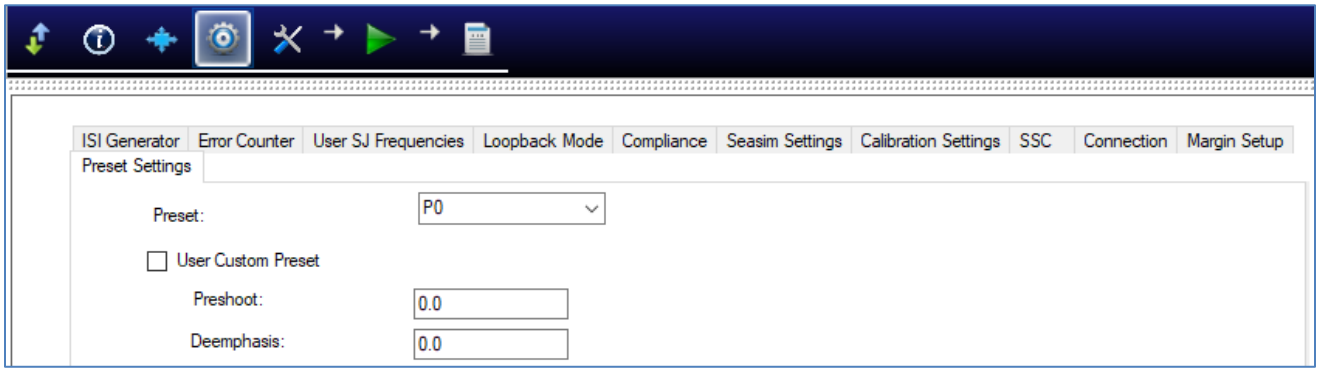


FIGURE 19. PRESET SETTINGS

4 Calibrating Using GRL-PCIE4-BASE-RXA Software

Calibration for PCI Express 4.0 Base Specification are performed at two physical test points – TP1 and TP2. TP1 is a physical test point for calibration without the effect of a channel. An adjustable Calibrated CEM connector is defined that is to be used along with the Replica Channel for the DUT for testing. TP2 is a physical test point that will affect the eye opening due to trace length. Post processing analysis of the signal is performed at the TP2P test point using the Seasim or SigTest application to simulate the stressed eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

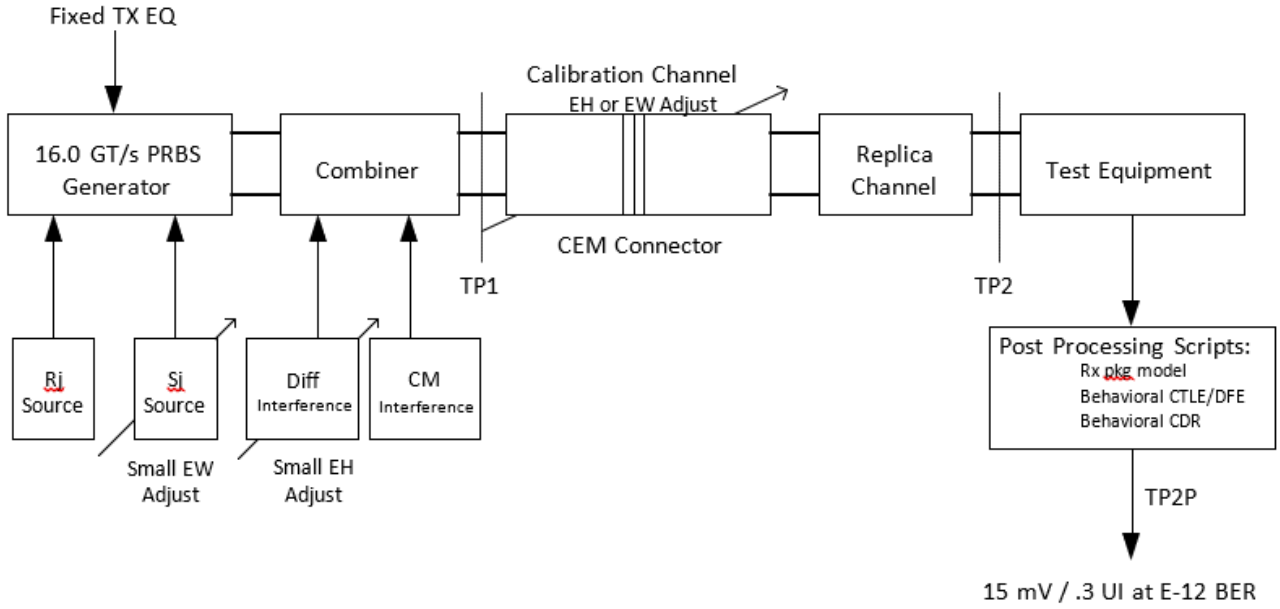


FIGURE 20. RX CALIBRATION BLOCK DIAGRAM FROM THE PCIE 4.0 BASE SPECIFICATION

To calibrate the stressed eye at TP2, the calibration channel shall receive signals with appropriate test patterns generated by the signal source. After calibration, the signal source shall be used for testing Rx DUT compliance.

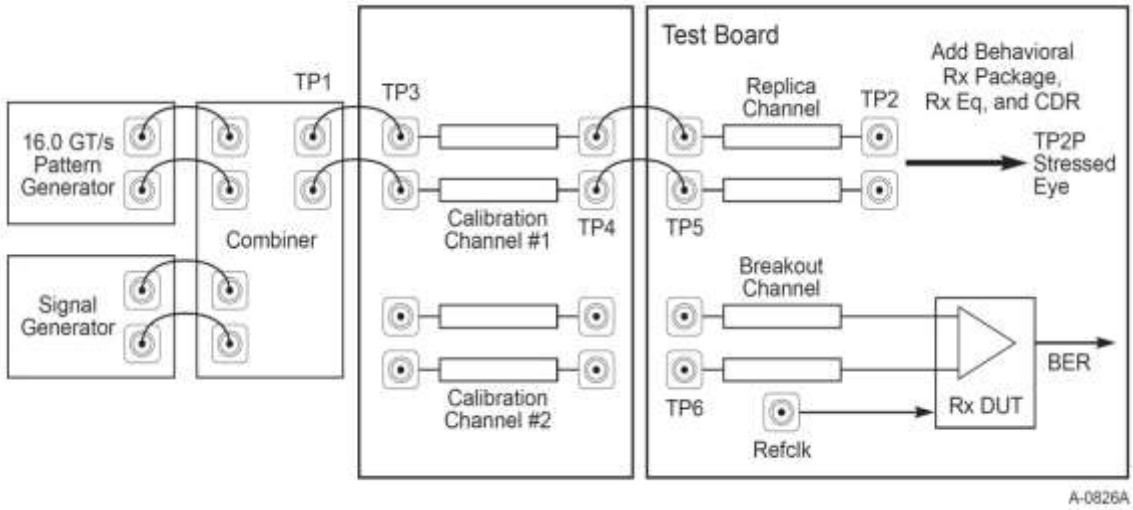


FIGURE 21. RX CALIBRATION/TEST SCHEMATIC OVERVIEW FROM THE PCIE 4.0 BASE SPECIFICATION

4.1 Stressed Jitter Eye Parameters

The following table is an excerpt of the PCIe 4.0 Base Specs showing the target measurement values for each calibration parameter.

TABLE 4. STRESSED JITTER EYE PARAMETERS FROM THE PCIE 4.0 BASE SPECIFICATION

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to1200	800-to 1200	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	ps	
T_{RX-ST}	Eye width	≤0.4	≤0.32	≤0.30	≤0.30	UI	Note 3, 4, 8,10
V_{RX-ST}	Eye height	≤175	≤100	≤25	≤15	mV PP	Note 2,4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	3.0 (max)	1.0	ps RMS	Note 6,7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	mV PP	Note 8
$V_{SSC-RES}$	SSC Residual	N/A	75	N/A	500	ps	Note 11, 13

Notes:

1. $V_{RX-LAUNCH}$ may be adjusted to meet V_{RX-ST} as long as the outside eye voltage at TP2 does not exceed 1300 mV PP for calibration at 2.5, 5.0 and 8.0 GT/s. $V_{RX-LAUNCH}$ is adjusted from 720 to 800 mV for 16 GT/s calibration.
2. Voltages shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
3. Eye widths shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
4. V_{RX-ST} and T_{RX-ST} are referenced to TP2P for 8.0 GT/s and 16.0 GT/s and TP2 for 2.5 GT/s and 5.0 GT/s. For 8.0 GT/s and 16.0 GT/s behavioral equalization are applied to the data at TP2.
5. $T_{RX-ST-SJ}$ may be measured at either TP1 or TP2. Only 8.0 GT/s and 16.0 GT/s Receivers are tested with Sj mask.
6. $T_{RX-ST-RJ}$ may be adjusted to meet the target value for T_{RX-ST} at 8.0 GT/s. Rj is measured at TP1 to prevent data-channel interaction from adversely affecting the accuracy of the Rj calibration. Rj is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
7. Both $T_{RX-ST-RJ}$ and $V_{RX-DIFF-INT}$ are limited to prevent the stressed eye from containing excessive amounts of jitter or noise distortion that are unrepresentative of a real channel. Too many of these distortion components produces a signal that cannot be equalized by an actual Receiver.
8. Defined as a single tone at 120 MHz. Measurement made at TP2 without post-processing. Common mode is turned off during T_{RX-ST} and V_{RX-ST} calibration and then turned on for the stressed eye jitter test.
9. For 2.5 GT/s and 5.0 GT/s Rx calibration variable channel loss is used to achieve the target eye height.
10. For 2.5 GT/s Rx calibration 100 MHz Sj is used to achieve the target eye width.
11. For 33 kHz SSC residual for common clock architecture testing only when testing at 5 GT/s.
12. Frequency for $V_{RX-DIFF-INT}$ is chosen to be slightly above the first pole of the reference CTLE.
13. Applied for CC testing only as a triangular phase modulation with a frequency between 30 kHz to 33 kHz when testing at 16 GT/s.

4.2 Common Receiver Parameters

The following table is an excerpt of the PCIe 4.0 Base Specs showing the target values for the common base Rx parameters. *Note: These parameters are not directly linked to the stressed eye measurement.*

TABLE 5. COMMON RECEIVER PARAMETERS

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	**124.9625 (min) 125.0375 (max)**	62.48125 (min) 62.51875 (max)	ps	UI is tolerance is equivalent to ±300 ppm and does not include SSC effects
$BW_{RX-PKG-PLL1}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL1}$	22 (max), 1.5 (min)	16 (max), 8 (min)	**4.0 (max), 2.0 (min)**	4.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$BW_{RX-PKG-PLL2}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL2}$	Not Specified	16 (max), 5.0 (min)	**5.0 (max), 2.0 (min)**	5.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$PKG_{RX-PLL1}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL1}$	3.0 (max)	3.0	**2.0**	2.0	dB	Second order PLL transfer bounding function
$PKG_{RX-PLL2}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL2}$	Not specified	1.0	**1.0**	1.0	dB	Second order PLL transfer bounding function
$RL_{RX-DIFF}$	Differential receiver return loss	See Figure 8-19	See Figure 8-19	See Figure 8-19	See Figure 8-19	dB	
RL_{RX-CM}	Common mode receiver return loss	See Figure 8-20	See Figure 8-20	See Figure 8-20	See Figure 8-20	dB	
$RX_{GND-FLOAT}$	Rx termination float time	500 (max)	500 (max)	500 **(max)**	500 (max)	ns	Limits added for 2.5 GT/s and 5.0 GT/s that match those for 8.0 GT/s
$V_{RX-CM-AC-P}$	Rx AC common Mode Voltage	150 (max)	150 (max)	**75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP**	75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP	mVP	Measured at Rx pins into a pair of 50Ω terminations to ground

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
Z_{RX-DC}	Receiver DC single ended impedance	40 (min) 60 (max)	40 (min) 60 (max)	Not specified	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. For 8.0 and 16.0 GT/s is bounded by RLRX-CM. See Note 5.
$Z_{RX-HIGH-IMP-DCPOS}$	DC input CM input impedance for V≥0 during Reset or power-down	≥10K (0200 mV) ≥20K (> 200 mV)	≥10K (0-200 mV ≥20K (> 200 mV)	**≥10K (0-200 mV** **≥20K (> 200 mV)**	≥10K **(0-200 mV** **≥20K (> 200 mV)**	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology.
$Z_{RX-HIGH-IMP-DCNEG}$	DC input CM input impedance for V<0 during Reset or power-down	1.0K (min)	1.0K (min)	**1.0K (min)**	1.0K (min)	Ω	Parameters may not scale with process technology.
$V_{RX-IDLE-DET-DIFFPP}$	Electrical Idle Detect threshold	65 (min) 175 (max)	65 (min) 175 (max)	**65 (**min**)** **175 (max)**	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2*|V_{RX-D+} - V_{RXD-}|. Measured at the package pins of the Receiver.
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	10 (max)	10 (max)	**10 (max)**	10 (max)	ms	An unexpected Electrical Idle ($V_{RX-DIFF-PP}$ < $V_{RXIDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Lane to Lane skew	20 (max)	8 (max)	**6 (max)**	5 (max)	ns	Across all Lanes on a Port. $L_{RX-SKEW}$ comprehends Lane-Lane variations due to channel and repeater delay differences.

Notes:

1. Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in.
2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.
4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.
5. The Rx DC single ended impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance is permitted to start immediately and the Rx Common Mode Impedance (constrained by RL_{RX-CM} to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V_{-CMDC}|}.
7. $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.
8. Defines the time for the Receiver's input pads to settle to new common-mode on 2.5/5.0 GT/s transition to 8.0 GT/s.

4.3 Calibration for TP1 (Output of BERT Generator)

4.3.1 Setup for TP1 Calibration (Using MP1800A BERT)

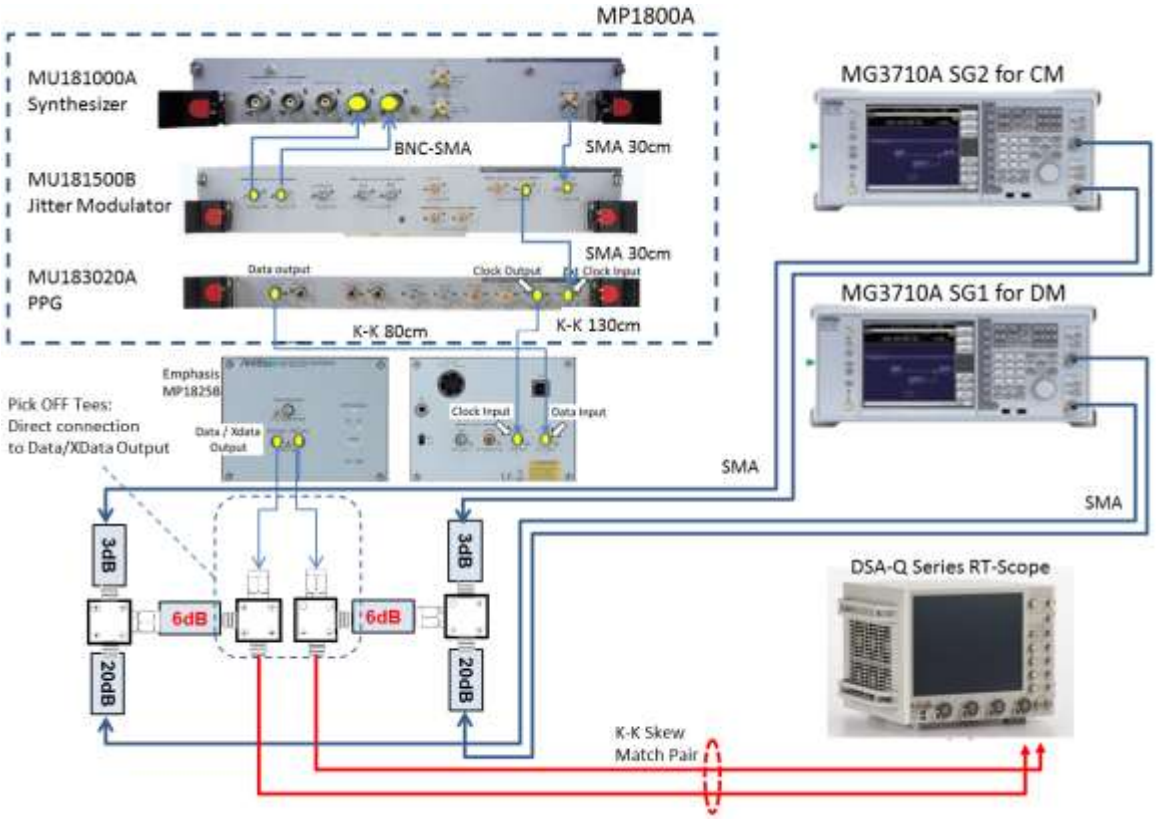


FIGURE 22. TYPICAL SETUP FOR TP1 CALIBRATION (USING MP1800A BERT)

Connection Steps:

1. Using the BNC-SMA Cable Pair (Anritsu J1508A), connect the MU181000A Synthesizer Ext I_Ext Q to the MU181500B Jitter Modulator I_Q output.
2. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181000A Synthesizer clock output to the MU181500B Jitter Modulator Ext clock input.
3. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181500B Jitter Modulator jittered clock output to the MU183020A PPG Ext clock input.
4. Using the 80cm K-K cable (Anritsu J1615A), connect the MU183020A PPG data output to the MP1825B De-emphasis Box data input.
5. Using the 130cm K-K cable (Anritsu J1615A), connect the MU183020A PPG clock output to the MP1825B De-emphasis Box clock input.
6. Assign the MP1825B as a Slot number on the MP1800A GUI.
7. Connect the MP1825B data/Xdata output to the Pick-off Tees (Anritsu J1510A) with two 6dB attenuators (Anritsu 41KC-6).
8. Using a K-K skew matched cable pair, connect the outputs of the Pick-off Tees to the DSA-Q Series RT Scope.
9. Connect both Pick-off Tees to the ends of the 6dB attenuators with a 3dB attenuator (Anritsu 41KC-3) attached on one side and a 20dB (Anritsu 41KC-20) attenuator on another side.

10. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 3dB attenuators to the outputs of the MG3710A SG (for CM).
11. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 20dB attenuators to the outputs of another MG3710A SG (for DM).

4.3.2 Setup for TP1 Calibration (Using MP1900A BERT)

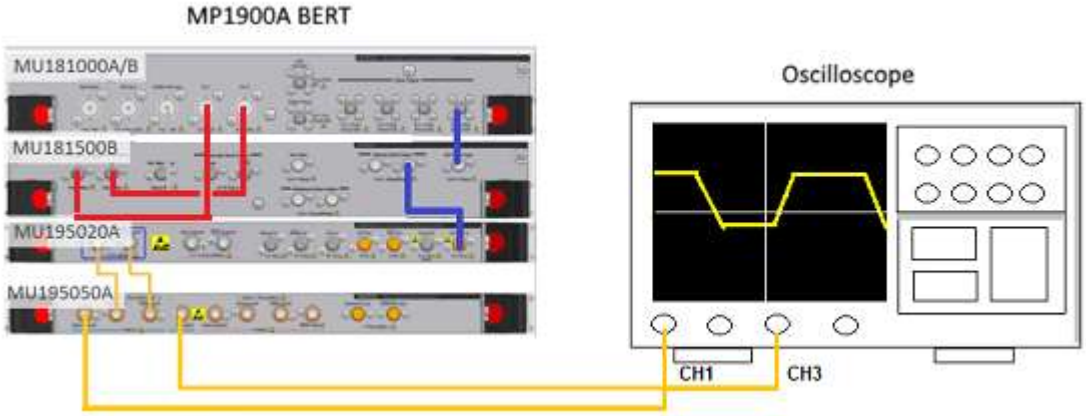


FIGURE 23. TYPICAL SETUP FOR TP1 CALIBRATION (USING MP1900A BERT)

Connection Steps:

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A Ext clock input.
3. Using BNC-SMA cables, connect the MU181000A/B Ext I_Ext Q to the MU181500B I_Q output.
4. Using coaxial cables, connect the MU195020A data outputs to the MU195050A data inputs.
5. Using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 3 on the oscilloscope.

4.3.3 Select Calibration

The following calibration are defined at TP1 and TP2 Test Points.

Calibration at TP1:

1. PG Delay Calibration *(Only applicable if using the MP1800A BERT)*
2. Pre-shoot Calibration
3. De-emphasis Calibration
4. Launch Amplitude Calibration
5. RJ Calibration
6. SJ Calibration
7. SJ Tone Calibration

Calibration at TP2, can be Downstream (for Host) or Upstream (for Device):

8. Downstream or Upstream:
    a. Insertion Loss Calibration *[Only applicable if CTS version '0.7' is selected from the Configurations page menu – see Section 4.3.4]*
    b. ISI Calibration (CEM Connector Channel + Replica Channel) *[Only applicable if CTS version '1.0' is selected from the Configurations page menu – see Section 4.3.4 AND ISI Generator other than "None" is selected from the Setup Configuration menu – see Section 3.2.3.1]*
    c. Common Mode (CM) Sinusoidal Interference Calibration
    d. Differential Mode (DM) Sinusoidal Interference Calibration (Achieves Calibrated Eye Height)
    e. Optimized Preset/Final ISI Calibration
    f. Stressed Jitter Voltage Calibration (Final stressed voltage and jitter eye adjustment to achieve Calibrated Eye Width)
    g. SigTest DM Optimization & Final Eye Calibration (Produces final stressed Eye Diagram if SigTest is used as post processing tool)

    [SigTest Final Eye Calibration is only applicable if CTS version '1.0' is selected from the Configurations page menu – see Section 4.3.4]

GRL-PCIE4-BASE-RXA automatically calibrates these parameters when initiated. See Appendix for an implementation method with automation for the above calibration.

The test selection list allows calibration/tests that need to be performed to be selected. Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Rx Tests will throw an error when initiated.

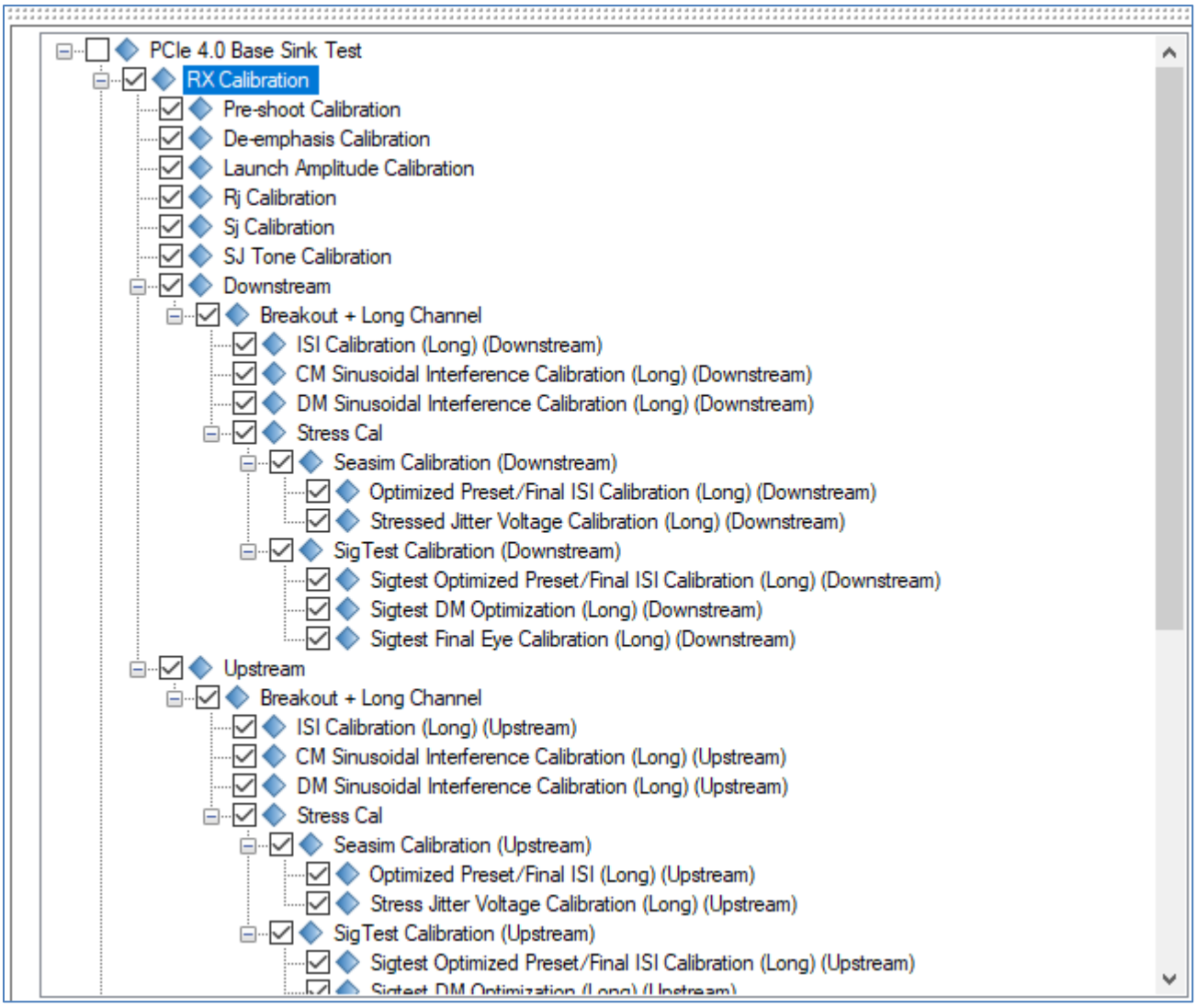


FIGURE 24. CALIBRATION SELECTION

4.3.4 Configure Calibration Parameters

After selecting the desired calibration, select  to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

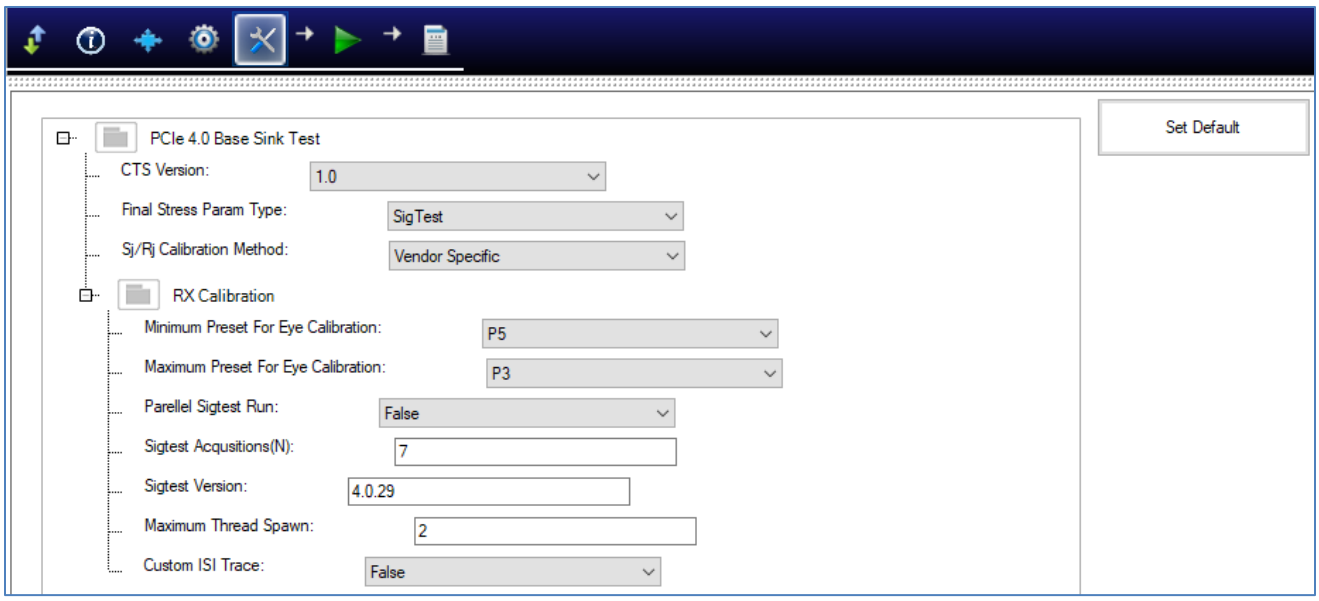


FIGURE 25. CALIBRATION PARAMETERS CONFIGURATION PAGE

TABLE 6. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
CTS Version	Select the Version of the CTS that is used as the reference specs to perform calibration and tests. (*Note: This selection causes the Select Tests page to display different test lists for the specific CTS version.)*
Final Stress Parameter Type	Select either the SigTest or Seasim application to be used for post processing signal quality testing. Make sure that the SigTest or Seasim application is already installed in the test controller system.
SJ/RJ Calibration Method	Select the SigTest, a vendor-specific, or a system-defined based methodology to be applied during calibration of SJ or RJ: • Select the 'SigTest' option to apply the SigTest method for calibration of all SJ/RJ frequencies; or • Select the 'Vendor Specific' option to use the Vendor-specific method (Tektronix DPOJET or Keysight EZ-JIT Plus software) for calibration of all SJ/RJ frequencies; or • Select the 'System Defined' option to use the Vendor-specific method (Tektronix DPOJET or Keysight EZ-JIT Plus software) for low SJ frequency calibration and the SigTest method for high SJ frequency and RJ calibration.
Minimum & Maximum Preset for Eye Calibration	Select the range of presets to be applied for stressed eye calibration.
Parallel SigTest Run	Select 'True' to enable running the SigTest application in parallel mode with the Long Channel TP2 calibration.
SigTest Acquisitions (N)	Enter the number of measurements to acquire when running the SigTest application over the Long Channel TP2 calibration.

SigTest Version	Enter the Version number of the SigTest application if used.
Maximum Thread Spawn	Set the maximum process threads to generate for checking the Rx device functionality during Long Channel TP2 calibration.
Custom ISI Trace	Select 'True' to enable generating custom ISI trace for ISI calibration.

4.3.5 Run Calibration at TP1

Select the Run icon: 

Skip Test if Result Exists. If previous calibration results exist, then the software will *skip* the calibration steps that have existing reports.

Replace if Result Exists. If previous calibration results exist, then the software will *replace* each step in the calibration with new results.

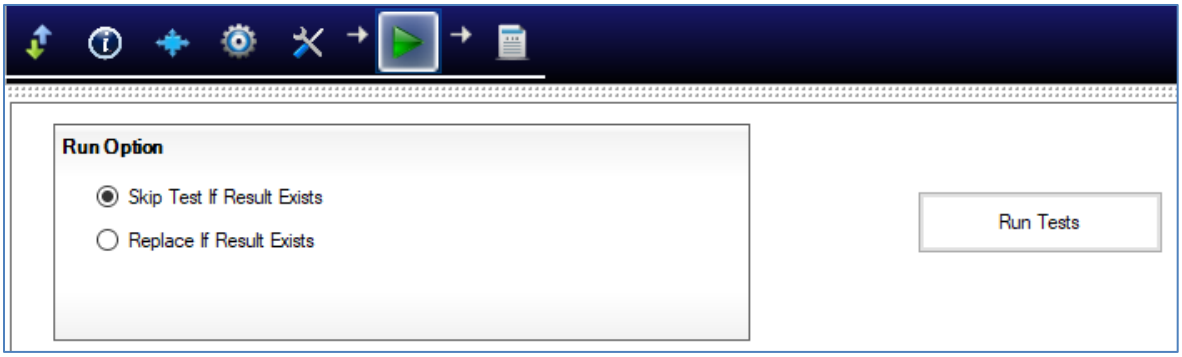


FIGURE 26. RUN TESTS

When running Calibration at TP1, the connection diagram will be shown as a first step to help the user make sure all connections are made before the tests are run. See Figure 27.

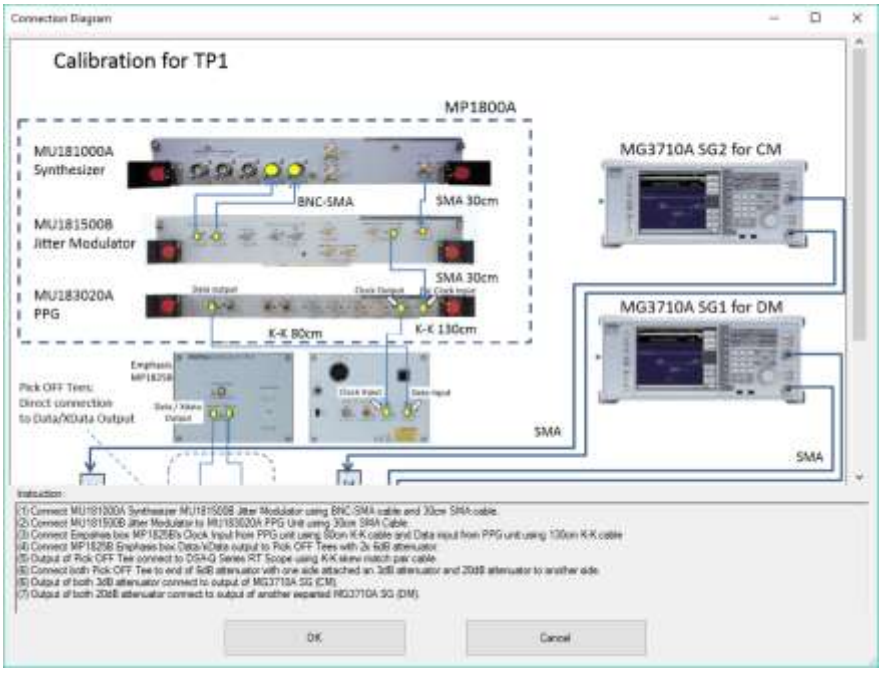


FIGURE 27. TP1 CONNECTION DIAGRAM DIALOG

4.4 Calibration for TP2 (Output of Long Channel)

The next step is to calibrate the TP1-TP2 Channel. As shown in Figure 20, the total TP1-TP2 calibration channel includes an Adjustable Calibration Channel, that requires the Insertion loss to fit within the limits called out in the PCI Express 4.0 Base specification. Figure 28 shows the limits for both Upstream (Host) and Downstream (Device) Channels.

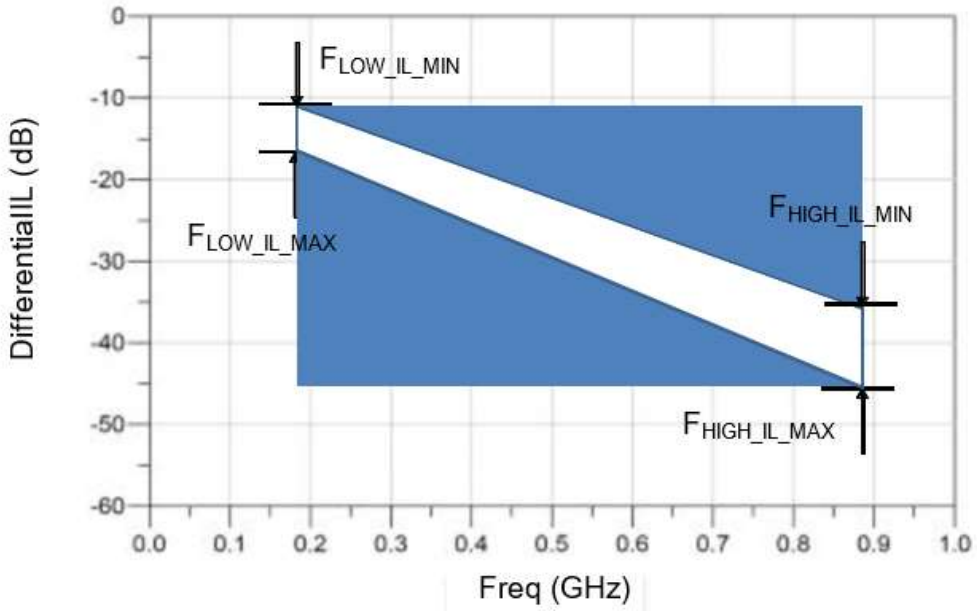


Table 2-1: Calibration Channel IL Limits

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
2.5 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	4.7 dB @ 1.25 GHz	5.2 dB @ 1.25 GHz
5.0 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	10.0 dB @2.5 GHz	11.0 dB @2.5 GHz
8.0 GT/s	5 dB @ 1 GHz	8 dB @ 1 GHz	~20 dB @ 4 GHz	~22 dB @ 4 GHz
16.0 GT/s Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~22.5 dB @ 8 GHz	~23.5 dB @ 8 GHz
16.0 GT/s Non-Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~24.5 dB @ 8 GHz	~25.5 dB @ 8 GHz

Note: Calibration channel plus Rx package is 28 dB nominally (informative) for 16.0 GT/s.

Note: Different reference packages are defined for devices containing Root Ports and all other device types at 16.0 GT/s.

Note: It is recommended that some validation be done with shorter channels at 16.0 GT/s.

FIGURE 28. INSERTION LOSS CALIBRATION LIMITS FROM THE PCIE 4.0 BASE SPECIFICATION

The GRL-PCIE4-BASE-RXA software uses a combination of a variable ISI channel, CEM connector, and replica channel to achieve the target IL profile. After calibrated using the GRL software, the calibrated channel IL should look like the example shown in Figure 30 after being analyzed with a post processing tool.

Note: The PCIe 4.0 Base Specification requires the calibration channel to meet a return loss (RL) mask at -15 dB up to Nyquist. See Appendix for more details on the return loss specs.

4.4.1 Setup for TP2 Calibration (Using MP1800A BERT)

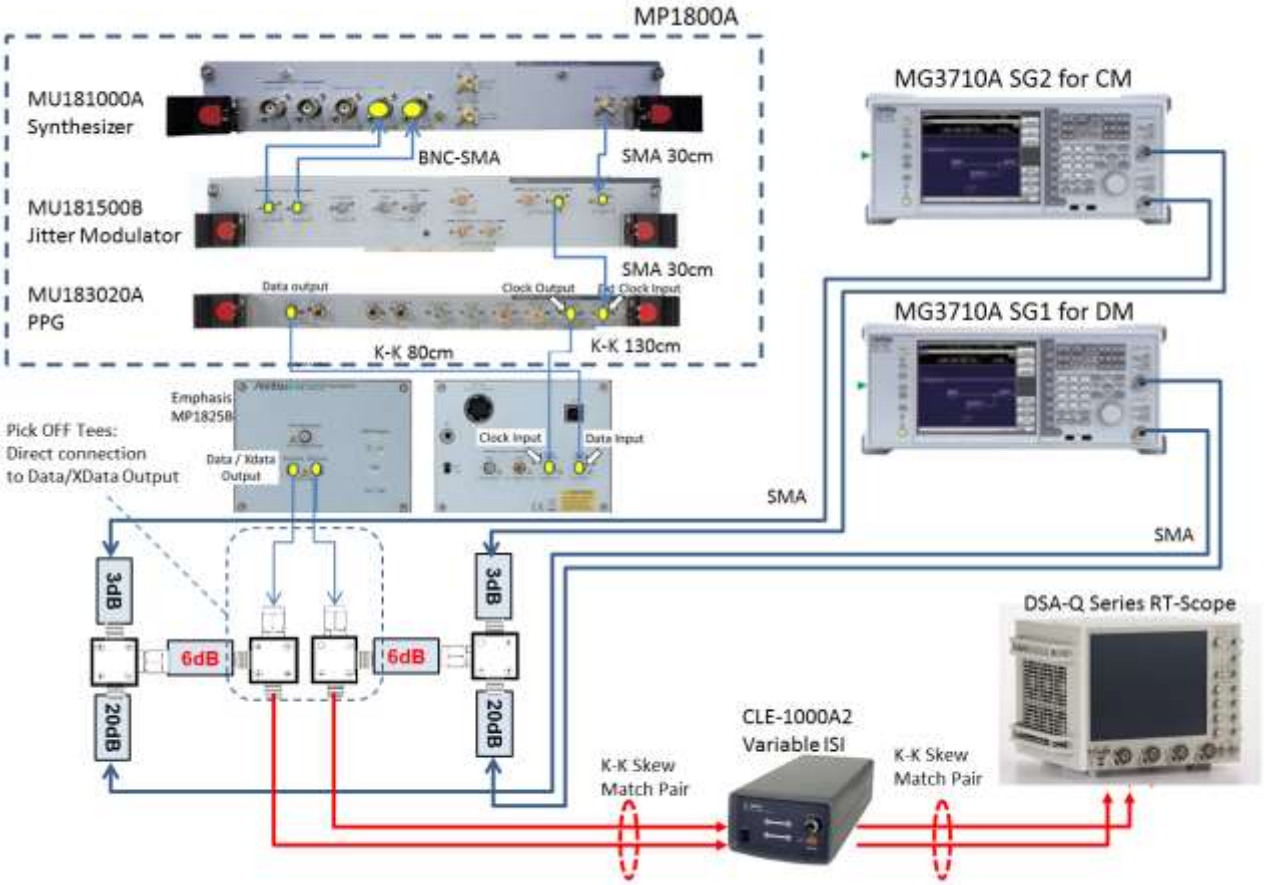


FIGURE 29. TYPICAL SETUP FOR TP2 CALIBRATION (USING MP1800A BERT)

Connection Steps:

1. Using the BNC-SMA Cable Pair (Anritsu J1508A), connect the MU181000A Synthesizer Ext I_Ext Q to the MU181500B Jitter Modulator I_Q output.
2. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181000A Synthesizer clock output to the MU181500B Jitter Modulator Ext clock input.
3. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181500B Jitter Modulator jittered clock output to the MU183020A PPG Ext clock input.
4. Using the 80cm K-K cable (Anritsu J1615A), connect the MU183020A PPG data output to the MP1825B De-emphasis Box data input.
5. Using the 130cm K-K cable (Anritsu J1615A), connect the MU183020A PPG clock output to the MP1825B De-emphasis Box clock input.

6. Assign the MP1825B as a Slot number on the MP1800A GUI.
7. Connect the MP1825B data/Xdata output to the Pick-off Tees (Anritsu J1510A) with two 6dB attenuators (Anritsu 41KC-6).
8. Using a K-K skew matched cable pair, connect the outputs of the Pick-off Tees to the Artek Variable ISI Generator.
9. Using a K-K skew matched cable pair, connect the Artek outputs to the DSA-Q Series RT Scope.
10. Connect both Pick-off Tees to the ends of the 6dB attenuators with a 3dB attenuator (Anritsu 41KC-3) attached on one side and a 20dB (Anritsu 41KC-20) attenuator on another side.
11. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 3dB attenuators to the outputs of the MG3710A SG (for CM).
12. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 20dB attenuators to the outputs of another MG3710A SG (for DM).

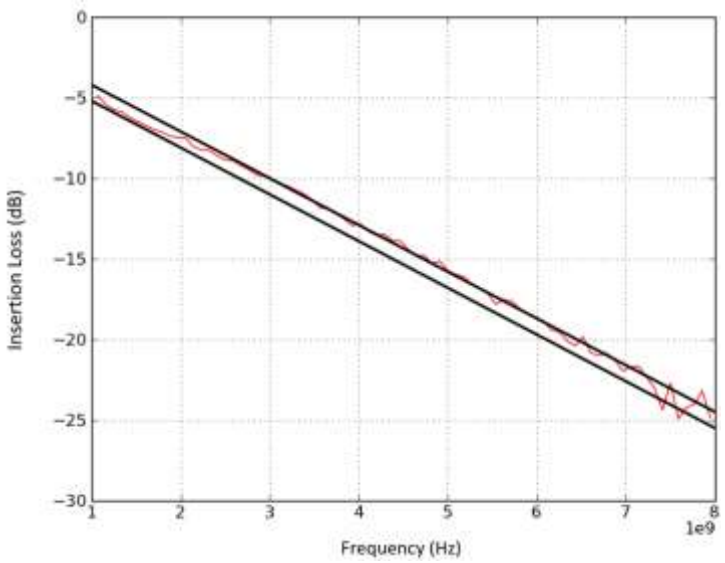


FIGURE 30. CALIBRATED IL EXAMPLE USING GRL-PCIE4-BASE-RXA

4.4.2 Setup for TP2 Calibration (Using MP1900A BERT)

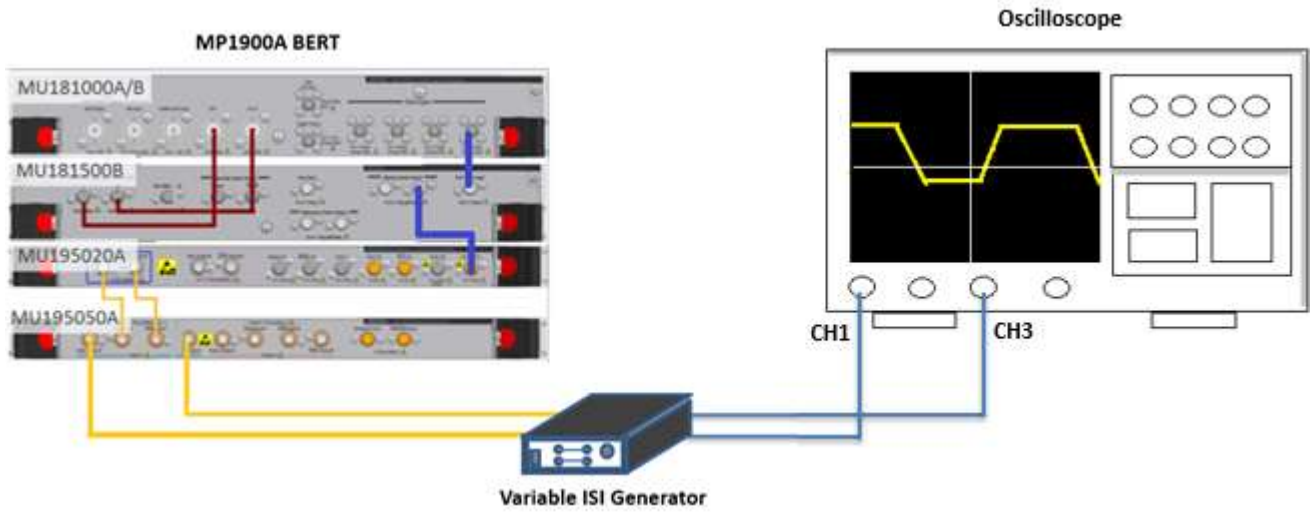


FIGURE 31. TYPICAL SETUP FOR TP2 CALIBRATION (USING MP1900A BERT)

Connection Steps:

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to the inputs of the variable ISI generator.
3. Connect the ISI generator outputs to Channels 1 and 3 on the oscilloscope.

4.4.3 Run Calibration Steps at TP2

Repeat Section 4.3.3 to complete the selected calibration steps at TP2.

After Calibrating the Loss profile to be used by adjustment of De-Emphasis as shown in Figure 28; ISI Measurement, CM Sinusoidal Interference, DM Sinusoidal Interference, Final ISI and SJ adjustments to achieve calibrated eye height and width, the final calibrated stressed Eye diagram is calculated by Seasim and SigTest, and should look similar to the below example.

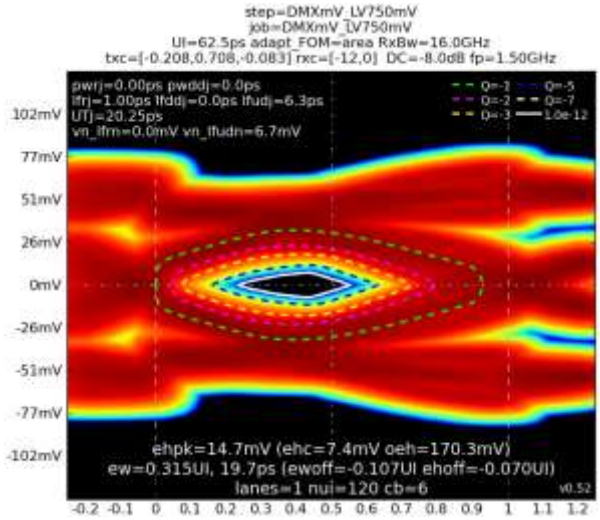


FIGURE 32. FINAL CALIBRATED STRESSED EYE DIAGRAM EXAMPLE

4.4.4 Set Up SigTest for Final Stressed Eye Calibration

The following example describes how to use the SigTest post processing tool to achieve the final calibrated stressed Eye diagram.

Assuming waveforms have been captured on the Scope for each test condition, set up the following parameters to analyze Eye Height/Eye Width using SigTest.

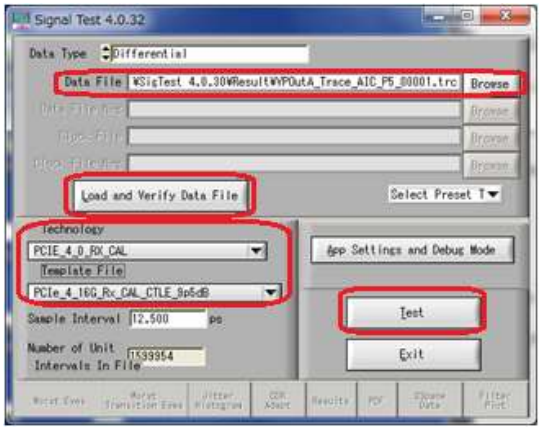
Note below settings are example of a typical setup for final eye calibration.

a) BERT Settings:
   - General Output: ON
   - Select SI-PPG and Emphasis tab- Emphasis Function: ON
   - Select the Pattern tab- Test Pattern: 128b130b_CP_L0_Gen4_P0
   - Set all Jitter, Noise, and Amplitude values.
   - Save five waveforms and read in SigTest.
   - Adjust Eye Height/Eye Width to target specification values using *SJ, DM-I, Eye Amplitude*.

b) Scope Settings:
   - Averaging: OFF
   - Set appropriate Horizontal Scale and Bandwidth

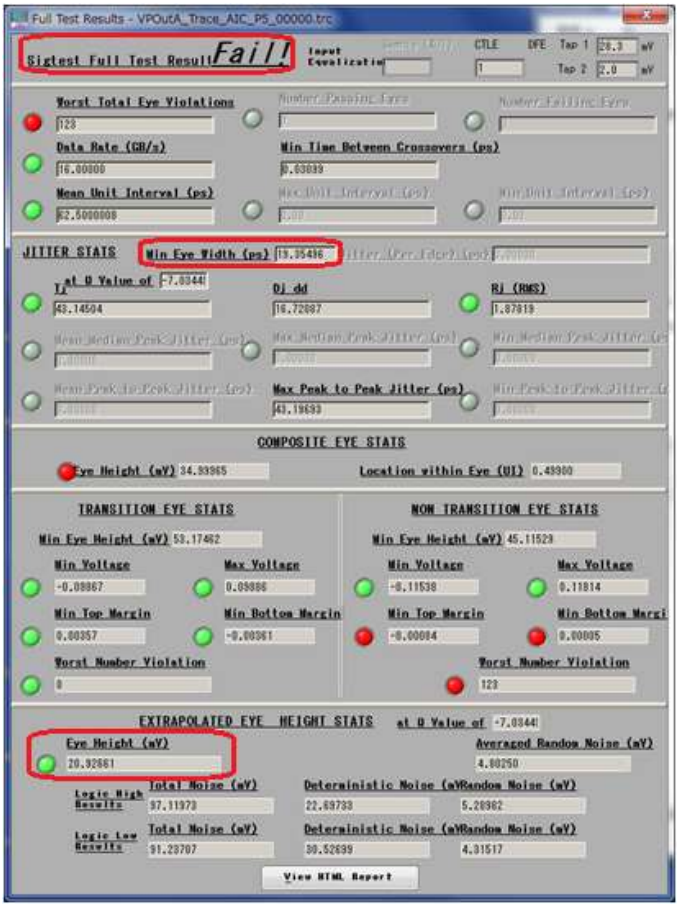
c) SigTest Settings:
   - Select a Data File
   - Select 'Load and Verify Data File'
   - Select Technology as 'PCIE_4_0_RX_CAL'
   - Select Template File as 'PCIe_4_16G_Rx_CAL_CTLE_x.xdB'
   - Select 'Test'

   (Note: Use the current version of SigTest, V4.0.38 with the PCIe_4_16G_Rx_CAL_CTLE_x.xdB.dat template file– 8 dB to 9.5 dB in ¼ dB steps CTLE curves allowed for each Tx preset.)



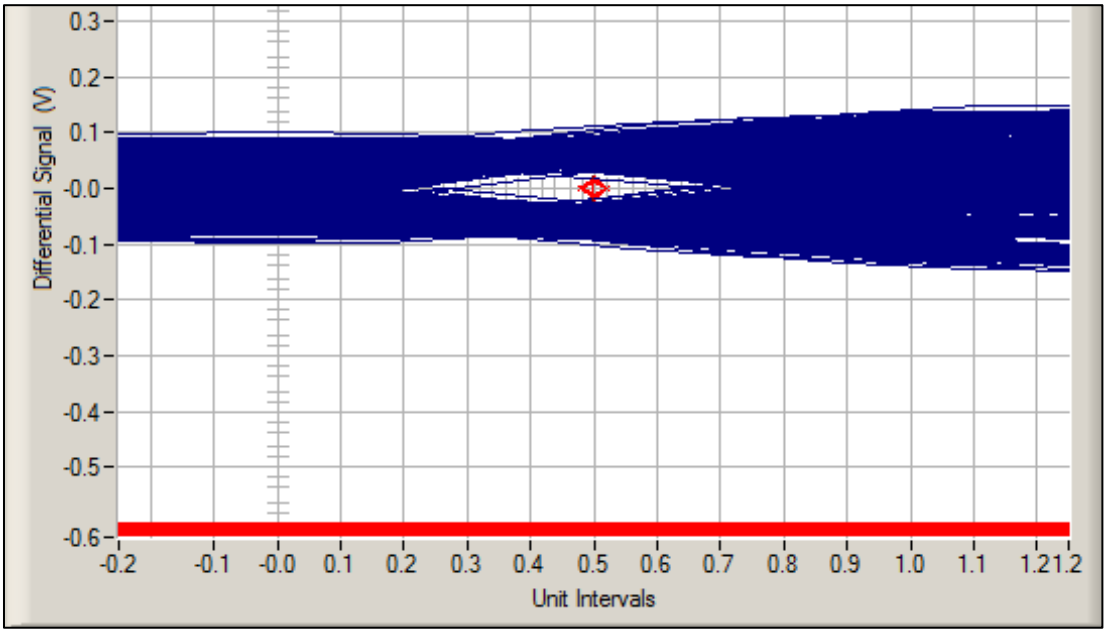
d) SigTest Results:

Note that the SigTest Full Test Result always shows 'Fail!' which can be ignored.



Min Eye Width: 18.25 to 19.25 ps

Eye Height: 13.5 to 16.5 mV



Notes:

- *Locate the largest loss channel (27 dB to 30 dB) where the Eye Width/Eye Height is above the calibration target value.*
- *Save more than five waveforms and obtain the average value.*

For final eye calibration, adjust Voltage Swing, SJ, and DM Amplitude until the target Eye Width and Eye Height are achieved.

5 Testing Using GRL-PCIE4-BASE-RXA Software

Once the final stressed eye has been calibrated successfully, receiver stress jitter voltage tolerance and margin testing can then be performed on the device under test (DUT). The DUT should have a Replica Channel of the same Insertion Loss as the Replica Channel used for calibration. The Replica Channel is removed when performing the DUT tests.

The GRL-PCIE4-BASE-RXA software automates the receiver compliance and jitter tolerance testing, at the spec-defined or user-defined jitter frequency steps. The GRL software also supports nested loop testing of multiple parameters to facilitate silicon PVT testing or testing across multiple test conditions. When testing is completed, the results will be logged in an aggregated test report which can be generated into a PDF format.

Receiver device compliance ensures the receiver DUT is able to correctly interpret data from a received signal with valid voltage and timing characteristics by achieving an acceptable bit error ratio (BER) of less than 1E-12. The signal used for verifying receiver tolerance must contain the maximum allowable jitter, noise, and signal loss. The stressed receiver tolerance test should include various differential mode sinusoidal interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

The receiver DUT can operate in the Common Clock (CC) Refclk and Independent Refclk (IR) clock modes. For the CC clock mode, a single Refclk source is applied for both the BERT signal generator and the DUT along with SSC and SJ mask.

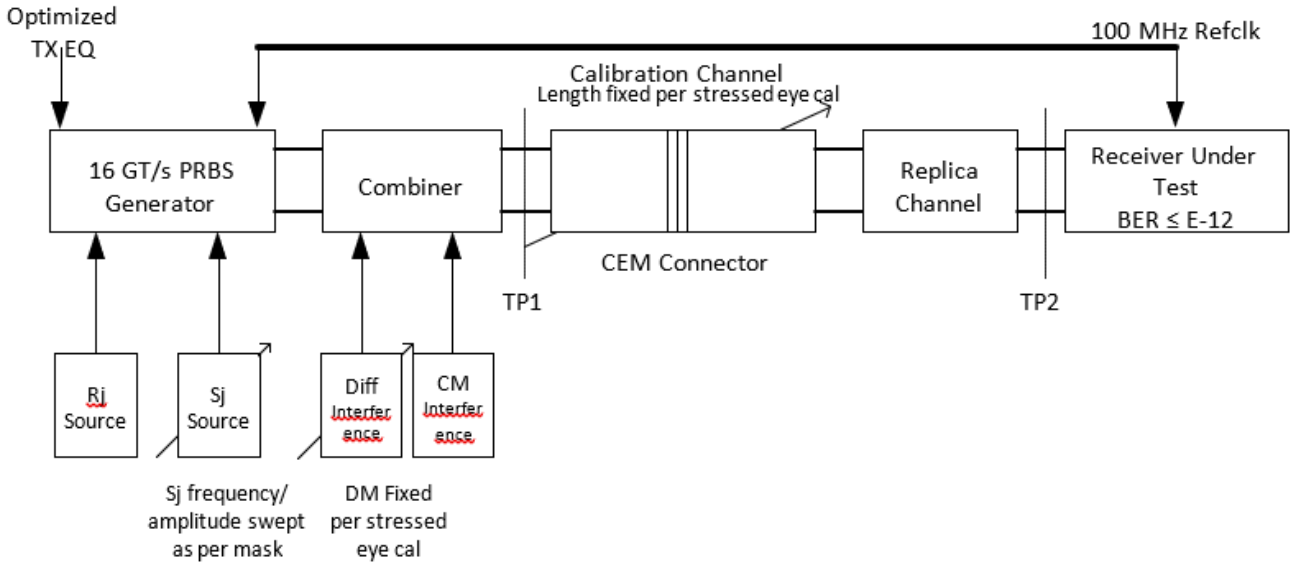


FIGURE 33. RX DUT STRESS JITTER TEST (CC MODE) BLOCK DIAGRAM FROM PCIE GEN 4 BASE SPECIFICATION

For the IR clock mode, two Refclk sources are applied for both the BERT signal generator and the DUT along with independent SSC and SJ mask.

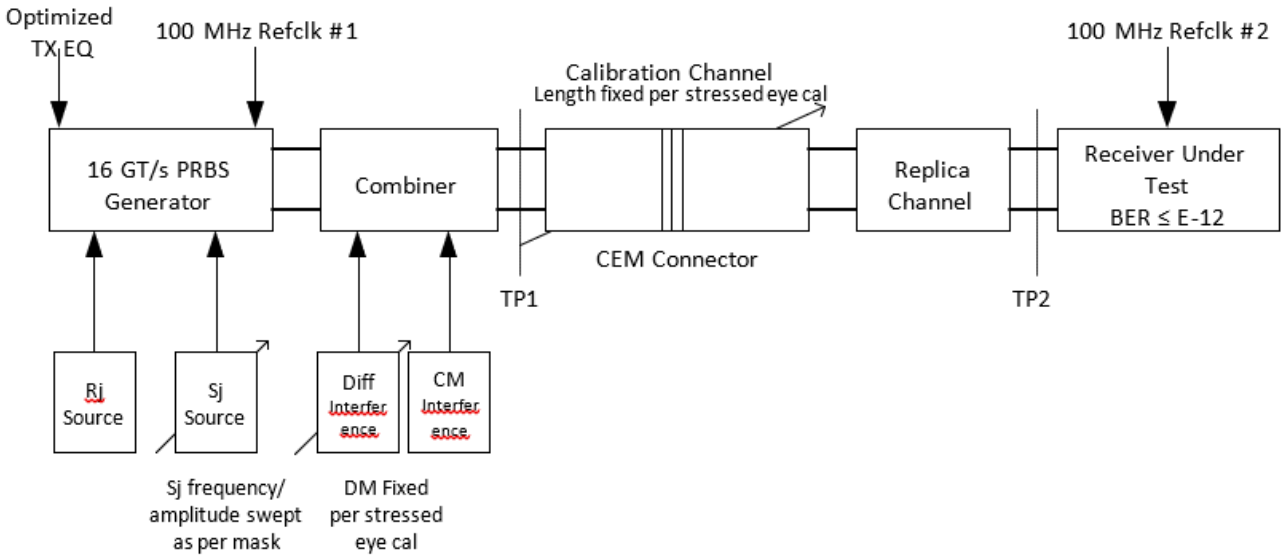


FIGURE 34. RX DUT STRESS JITTER TEST (IR MODE) BLOCK DIAGRAM FROM PCIE GEN 4 BASE SPECIFICATION

Once the stressed receiver tolerance test setup has been calibrated, the BERT will transmit a modified compliance pattern to the receiver and monitors the loopback pattern has a BER that is less than 1E-12.

5.1 Receiver DUT Compliance Test Setup

5.1.1 Test Setup Using MP1800A BERT

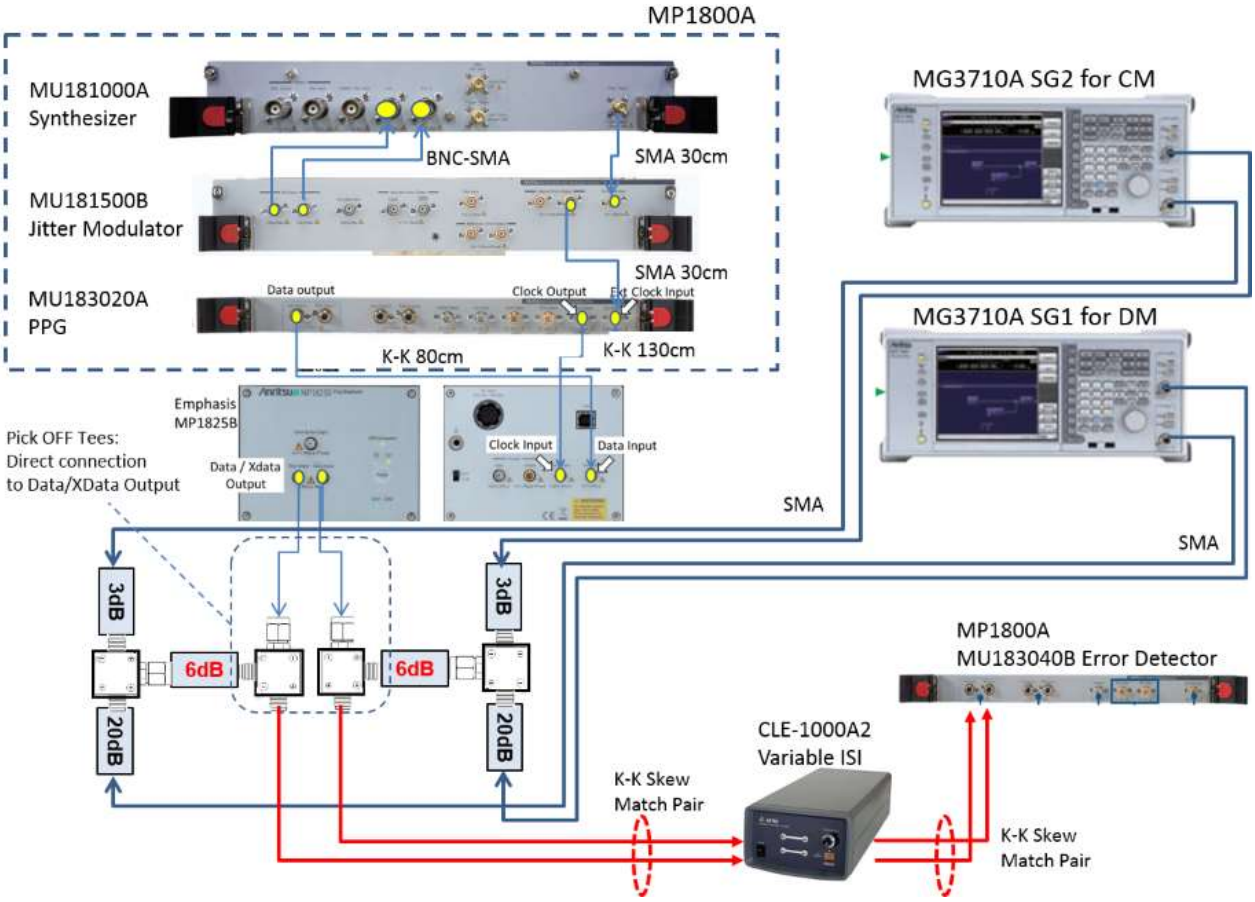


FIGURE 35. TYPICAL RECEIVER DUT TEST SETUP (USING MP1800A BERT)

Note: The Artek CLE Series Variable ISI Generator is used to replace the Calibration Channel + Breakout Channel.

Connection Steps:

1. Using the BNC-SMA Cable Pair (Anritsu J1508A), connect the MU181000A Synthesizer Ext I_Ext Q to the MU181500B Jitter Modulator I_Q output.
2. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181000A Synthesizer clock output to the MU181500B Jitter Modulator Ext clock input.
3. Using the 30cm SMA-SMA short cable (Anritsu J1349A), connect the MU181500B Jitter Modulator jittered clock output to the MU183020A PPG Ext clock input.
4. Using the 80cm K-K cable (Anritsu J1615A), connect the MU183020A PPG data output to the MP1825B De-emphasis Box data input.
5. Using the 130cm K-K cable (Anritsu J1615A), connect the MU183020A PPG clock output to the MP1825B De-emphasis Box clock input.
6. Connect the MP1825B data/Xdata output to the Pick-off Tees (Anritsu J1510A) with two 6dB attenuators (Anritsu 41KC-6).
7. Using a K-K skew matched cable pair, connect the outputs of the Pick-off Tees to the Artek Variable ISI Generator.

8. Connect the Artek outputs to the DUT's input.
9. Using a K-K skew matched cable pair, connect the DUT's Tx Out to the MU183040B Error Detector data input.
10. Connect both Pick-off Tees to the ends of the 6dB attenuators with a 3dB attenuator (Anritsu 41KC-3) attached on one side and a 20dB (Anritsu 41KC-20) attenuator on another side.
11. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 3dB attenuators to the outputs of the MG3710A SG (for CM).
12. Using the 100cm SMA-SMA long cables (Anritsu J1343A), connect both 20dB attenuators to the outputs of another MG3710A SG (for DM).

5.1.2 Test Setup Using MP1900A BERT

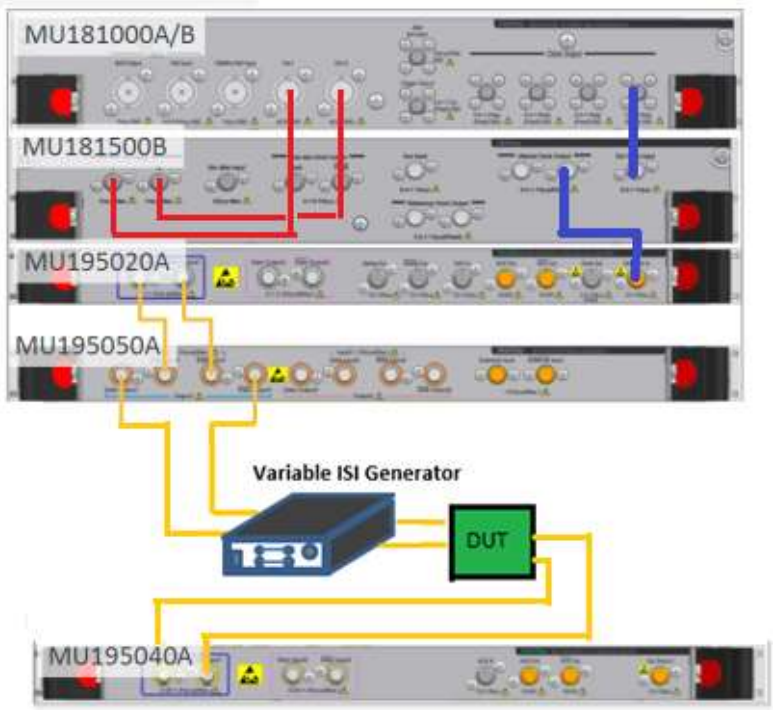


FIGURE 36. TYPICAL RECEIVER DUT TEST SETUP (USING MP1900A BERT)

Note: The Artek CLE Series Variable ISI Generator is used to replace the Calibration Channel + Breakout Channel.

Connection Steps:

1. Using back the same BERT connections from calibration, connect the MU195050A data outputs to the inputs of the variable ISI generator.
2. Using coaxial cables, connect the ISI generator outputs to the DUT Rx inputs.
3. Using phase matched K-K coaxial cables, connect the DUT Tx outputs to the MU195040A data inputs for loopback error detection.

5.1.3 Receiver Compliance Tests

In the following diagram, **Select Tests > Stress Jitter Voltage** tests are selected if tests at the Compliance Jitter Limits are to be performed.

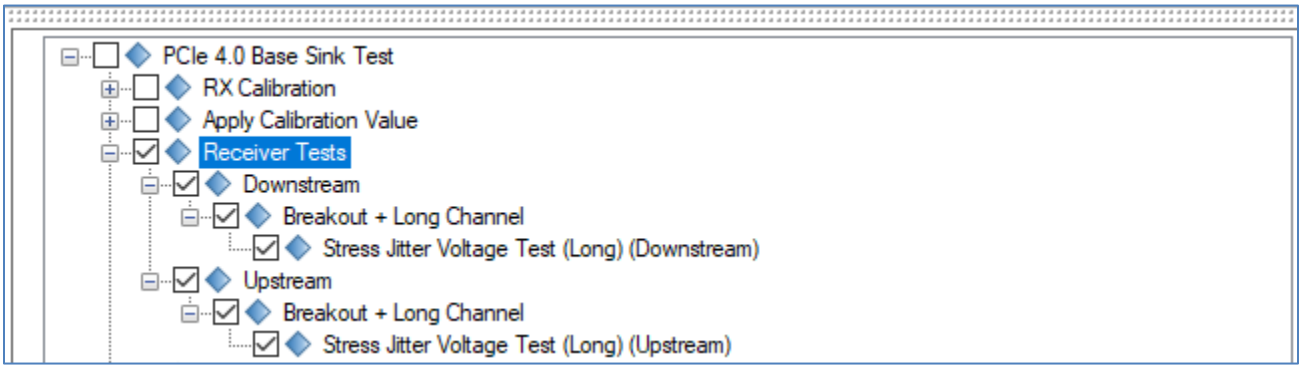


FIGURE 37. SELECTING RECEIVER COMPLIANCE TESTS

Once eye height and eye width have been calibrated, the Rx DUT will be connected to the far end of the calibration channel for testing. Optimization for the transmitter equalization will then be performed (equalization must also be optimized for the Rx DUT as well). SJ will be set to an initial value of 0.1 UI at 100 MHz that allows the receiver CDR to achieve lock which will then be swept over the frequency range as shown below, while maintaining fixed Tx equalization. The 100 MHz SJ initial tone will then be removed to perform testing for the appropriate swept SJ profile.

Note that an additional SJ tone at 210 MHz shall be present for all testing, while having the same amplitude as the 100 MHz SJ to achieve the target eye width minus 0.1 UI. This is not required if the SJ calibration is less than 0.1 UI.

The DUT must achieve a compliance BER of 10E-12 or lower for the entire swept SJ range. The Rx DUT is tested using an SJ mask in the 400 kHz to 1.0 MHz range and the 33 kHz single tone magnitude of 25 ns PP with 400 UI PP.

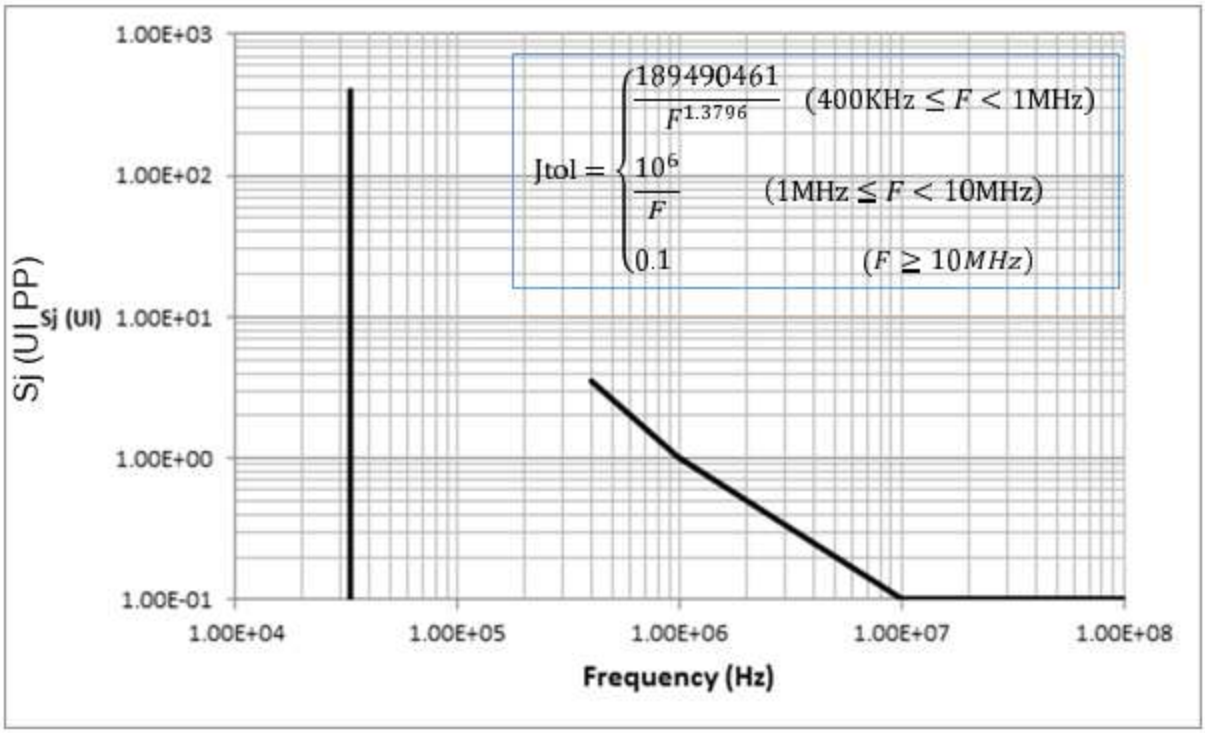


FIGURE 38. SJ MASK FUNCTION IN IR MODE FROM PCIE GEN 4 BASE SPECIFICATION

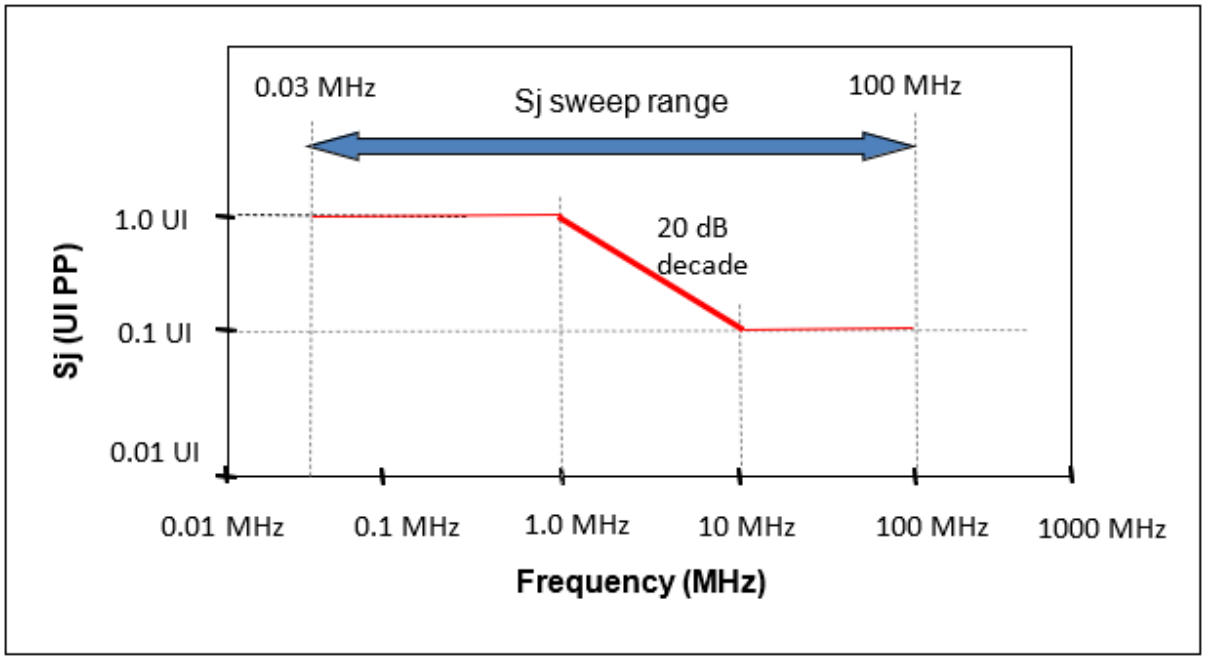


FIGURE 39. SJ MASK FUNCTION IN CC MODE FROM PCIE GEN 4 BASE SPECIFICATION

The stress jitter voltage tests are run from the same screen as shown in Figure 26.

5.1.4 Receiver Margin Tests

In the following diagram, **Select Tests > Stress Jitter Voltage Margin** tests are selected if Jitter Margin testing is to be performed.

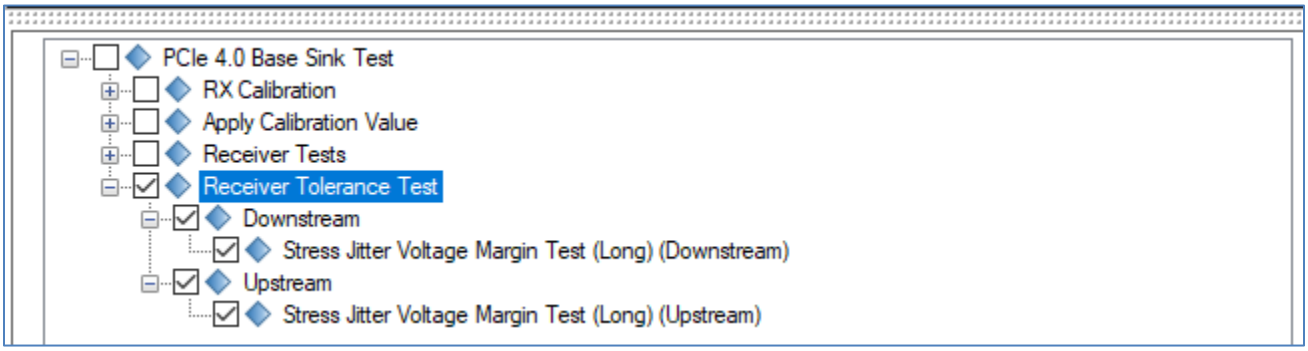


FIGURE 40. SELECTING RECEIVER MARGIN TESTS

The marginal tests are run from the same screen as shown in Figure 26.

5.1.5 Apply Calibrated Values for Testing

Calibrated values from the stressed jitter voltage calibration can be used in the DUT Rx tests. To apply these values, go to **Select Tests > Apply Stress Voltage Param**.

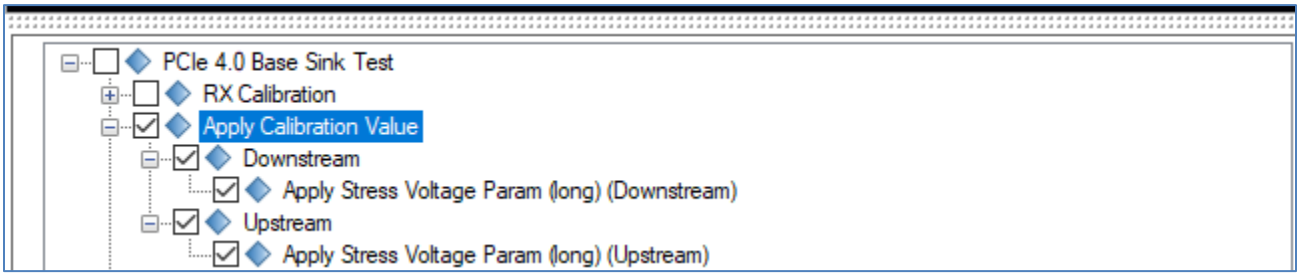


FIGURE 41. SELECTING TO APPLY CALIBRATION VALUES

5.2 Enable Loopback BER Test

To set up the GRL software to automate loopback testing for error detection, go to the Configurations page and set up the following settings. *Make sure that the Rx DUT is capable of supporting loopback mechanism for BER measurements.*

1. Under the Error Counter tab, select 'LoopBack' to enable loopback test mode for the DUT.

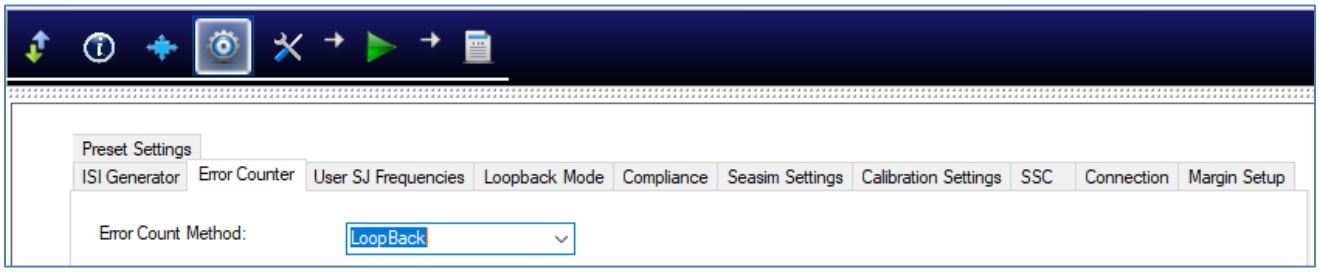


FIGURE 42. SELECT BER LOOPBACK TEST METHOD

2. Under the Loopback Mode tab, select 'Clock Recovery' in the Clock Recovery Method field to apply the clock data recovery function to process the modified compliance pattern generated by the DUT. Then, set the value for the Clock Recovery Loop Bandwidth.

   If using a user-defined pattern instead of the default test pattern for error checking, select the 'Custom Pattern for Error Detector' checkbox. Then, select the type of custom test pattern to be used.

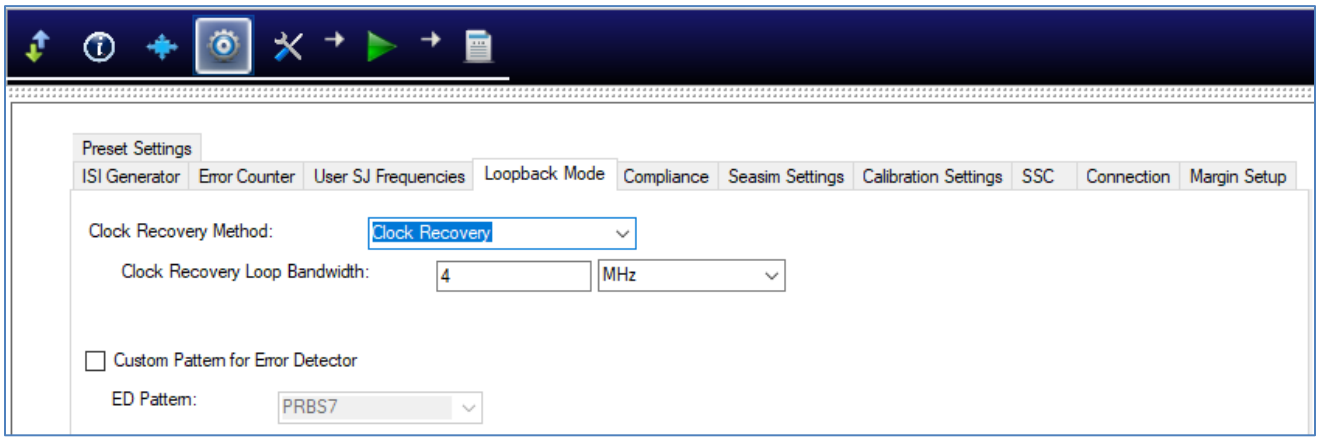


FIGURE 43. SET UP LOOPBACK TEST

3. If needed to change the default spec-defined limits for the target BER and maximum error allowed for BER measurements, then select the Compliance tab and enter new values.

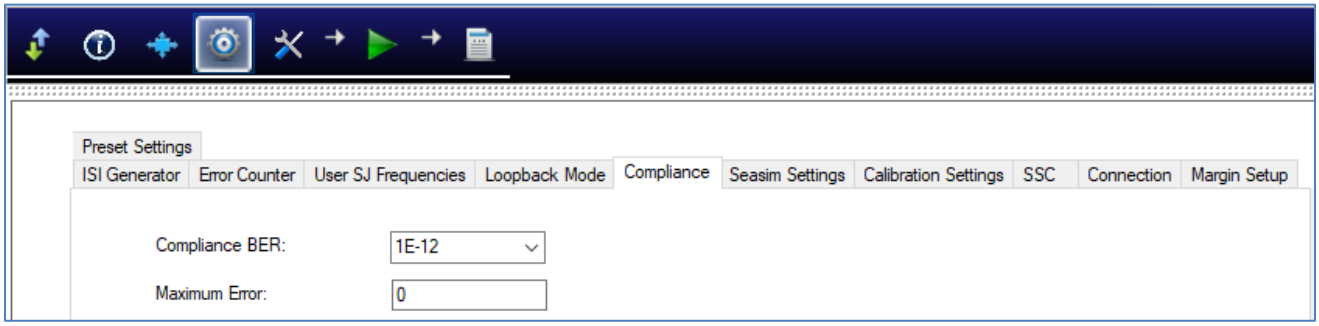


FIGURE 44. SET BER/ERROR LIMITS

6 Interpreting Test Report

The **Report** page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

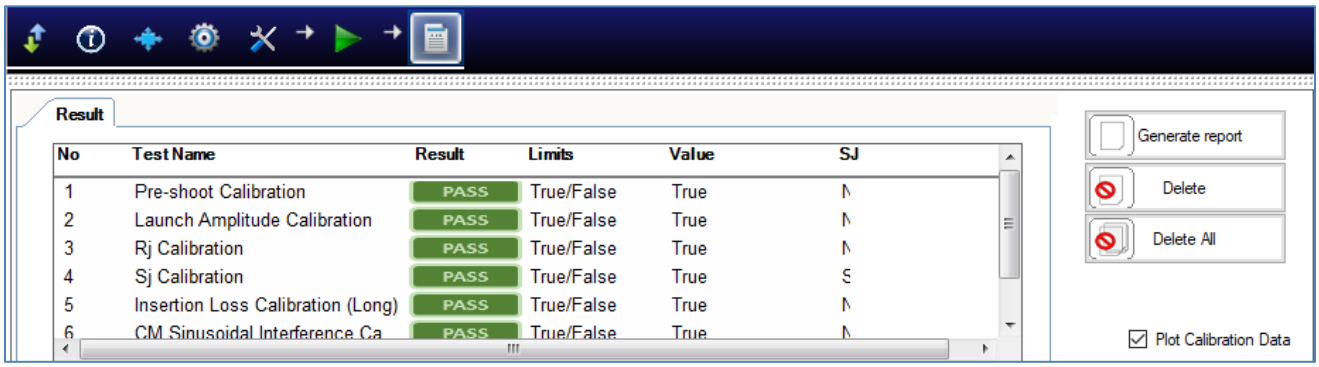


FIGURE 45. REPORT RESULTS PAGE

6.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.

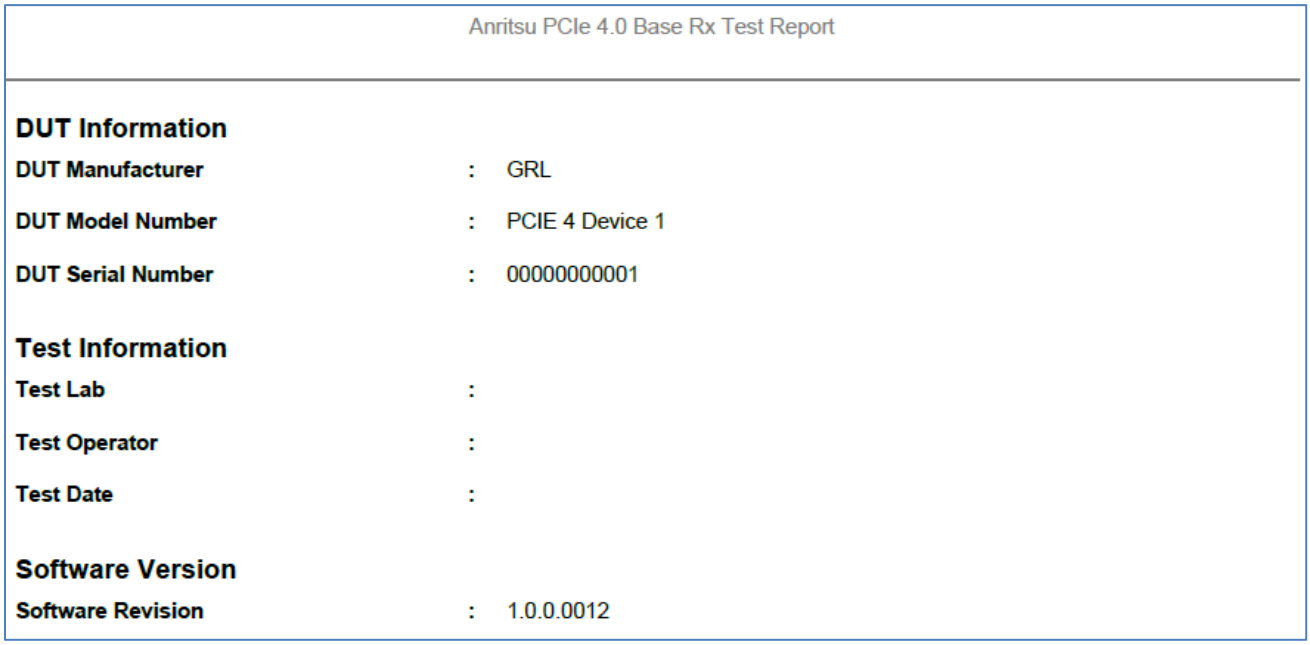


FIGURE 46. DUT INFORMATION

6.2 Summary Table

This portion is populated from the tests performed and its results. This gives an overall view of all the results and its test conditions.

No	TestName	Limits	Value	Results	SJ
1	PG Delay Calibration	True/False	True	Pass	
2	Pre-shoot Calibration	True/False	True	Pass	
3	De-emphasis Calibration	True/False	True	Pass	
4	Launch Amplitude Calibration	True/False	True	Pass	
5	Rj Calibration	True/False	True	Pass	
6	Sj Calibration	True/False	True	Pass	SJLF_2
7	Sj Calibration	True/False	True	Pass	SJLF_3
8	Sj Calibration	True/False	True	Pass	SJLF_4
9	Sj Calibration	True/False	True	Pass	SJLF_1
10	SJ Tone Calibration	True/False	True	Pass	
11	DM Phase Calibration	True/False	True	Pass	
12	CM Phase Calibration	True/False	True	Pass	
13	Insertion Loss Calibration (Long) (Downstream)	True/False	True	Pass	
14	CM Sinusoidal Interference Calibration (Long) (Downstream)	True/False	True	Pass	
15	DM Sinusoidal Interference Calibration (Long) (Downstream)	True/False	True	Pass	
16	Stressed Jitter Voltage Calibration (Long) (Downstream)	True/False	True	Pass	
17	Insertion Loss Calibration (Long) (Upstream)	True/False	True	Pass	
18	CM Sinusoidal Interference Calibration (Long) (Upstream)	True/False	True	Pass	
19	DM Sinusoidal Interference Calibration (Long) (Upstream)	True/False	True	Pass	
20	Stress Jitter Voltage Calibration (Long) (Upstream)	True/False	True	Pass	

FIGURE 47. SUMMARY TABLE

6.3 Calibration Data Results

If Plot Calibration Data checkbox is checked, then the plots are shown in this part of the report.

2. Pre-shoot Calibration

Test Limits	:	True/False
Result	:	True
Cal Parameter	:	PreShoot
Test completed time	:	05 January 2017 0:00:35 AM

PreShootCalibration Plot

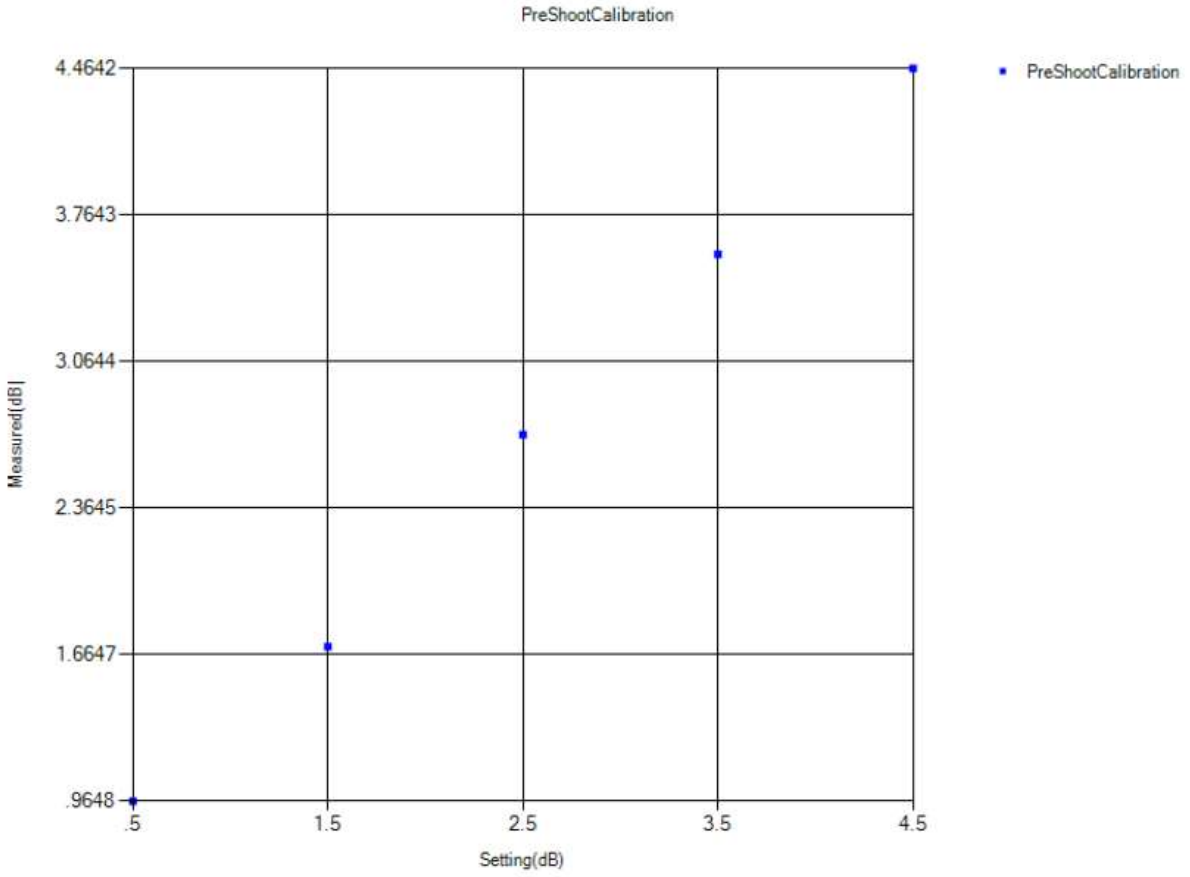


FIGURE 48. CALIBRATION RESULTS EXAMPLE

6.4 Compliance Test Results

27. Stress Jitter Voltage Test (Long) (Upstream) [SJLF_4]

Pass/Fail Stats	:	Pass
Test Limits	:	True/False
Result	:	True
Test Frequency	:	100 MHz
ISI Generator	:	Artek
Preshoot (dB)	:	0 (0)
DeEmphasis (dB)	:	-6 (-6.35)
RJ (ps RMS)	:	1 (0.24)
SJ (ps)	:	12.5 (0.17)
Amplitude (mV)	:	500 (330)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	11.06383039056 (26.2475834324656)
CM Freq (MHz)	:	120
CMSI (mV)	:	150 (169228.754408806)
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	12.5 (0.17229946287562)
Max Error Allowed	:	0
Error Counts	:	0
Test completed time	:	20 February 2018 22:47:36 PM

FIGURE 49. COMPLIANCE TEST RESULTS EXAMPLE

6.5 Margin Test Results

29. Stress Jitter Voltage Margin Test (Long) (Downstream) [SJLF_2]		
Pass/Fail Stats	:	Fail
Test Limits	:	True/False
Result	:	False
ISI Generator	:	Artek
Preshoot (dB)	:	0 (0)
DeEmphasis (dB)	:	-6 (-6.35)
RJ (ps RMS)	:	1 (0.24)
Amplitude (mV)	:	350 (230)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	16.3780929451514 (42.6636011745818)
CM Freq (MHz)	:	120
CMSI (mV)	:	150 (168440.228264395)
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	12.5 (0.17229946287562)
Sj Specs	:	125 UI
Max Error Allowed	:	0
Last Passing Sj	:	-900000000000000000000000000.0000 GUI
Test completed time	:	20 February 2018 22:06:29 PM

FIGURE 50. MARGIN TEST RESULTS EXAMPLE

7 Saving and Loading Test Sessions

The GRL-PCIE4-BASE-RXA software enables Calibration and Test Results to be created and maintained as a 'Live Session' in the application. This allows you to quit the application and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To save a session, with all of the parameter information, the test results, and any waveforms, use the "Options" command on the menu bar, then the "Save Session" command.

To load a session back into the software, including the saved parameter settings, use the "Options" command on the menu bar, then the "Load Session" command.

To create a New session and return the application back to a default configuration, use "Options" command on the menu bar, then the "New Session" command.

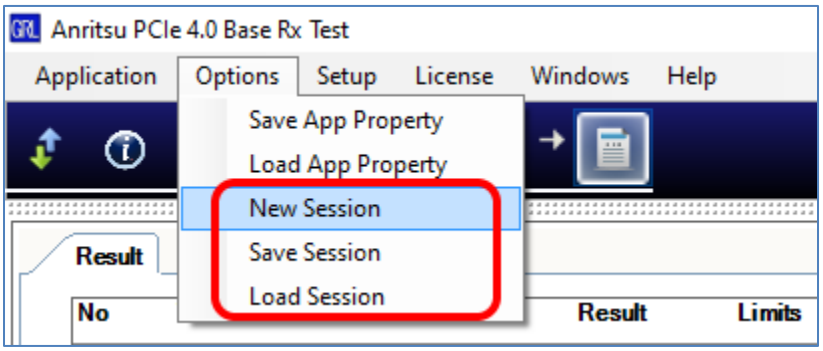


FIGURE 51. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

8 Appendix A: Method of Implementation (MOI) Using Automation

This section provides sample methodology to automate PCIe Gen 4 Base Rx calibration using GRL-PCIE4-BASE-RXA software at 16 GT/s. This procedure will ensure Receiver Impairment adjustments on the MP1800A/MP1900A BERT are accurate before running DUT compliance tests.

8.1 Perform Calibration at TP1

8.1.1 Pre-shoot Calibration

The **Caltable** method is used to calibrate pre-shoot:

1. Set 800mV (p-p) amplitude on BERT.
2. Set 0dB for De-emphasis on MP1825B/MP1900A.
3. Measure:

   1dB at MP1825B/MP1900A, then measure Pre-shoot, record
   2dB at MP1825B/MP1900A, measure again, record
   3dB at MP1825B/MP1900A, measure again, record
   .....
   5dB at MP1825B/MP1900A, measure again, record.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured Pre-shoot at 1dB Min and Max 4dB.

8.1.2 De-emphasis Calibration

The Caltable method is used to calibrate De-emphasis:

1. Set 800mV (p-p) amplitude on BERT.
2. Set 0dB for Pre-shoot on MP1825B/MP1900A.
3. Measure:

   -8dB at MP1825B/MP1900A, then measure De-emphasis, record
   -7dB at MP1825B/MP1900A, measure again
   -6dB at MP1825B/MP1900A, measure again
   .....
   0dB.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured De-emphasis at -1dB Min and Max -6dB.

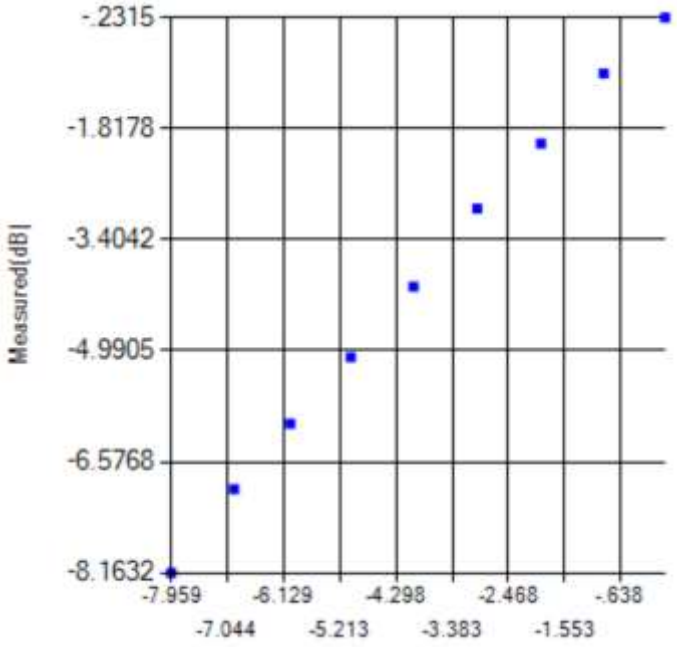


FIGURE 52. DE-EMPHASIS CALIBRATION CALTABLE GRAPH

8.1.3 Launch Amplitude Calibration

The Caltable method is used to calibrate Launch Amplitude:

1. Initialize BERT.
2. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
3. Set 300mV Amplitude at BERT, then measure the amplitude in scope, record it.
4. Increase 100mV on each iteration, measure the amplitude in scope, until measured amplitude meets or exceeds 1200mV.
5. Plot a Caltable graph.
6. Passing criteria is to obtain MEAN value of Launch Amplitude measurement at 720-800mV.

8.1.4 RJ Calibration

The Caltable method is used to calibrate RJ:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set Initial RJ value to 0.04UI(p-p) on BERT.
7. Measure RJ (in ps (RMS)) from scope using EZJIT, record the measured value.
8. Increase 0.1UI (p-p) on each iteration, measure RJ from scope, until measured RJ meets or exceeds 1.0ps (RMS).
9. Plot a Caltable graph.
10. Passing criteria is to obtain measured RJ at 1.0 ps (RMS).

8.1.5 SJ Calibration

The Caltable method is used to calibrate SJ:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set the SJ Frequency of the first Permutation (30KHz, 1MHz, 10MHz, 100MHz).
7. Set 0 (%UI (p-p)) as base value in SJ, measure SJ (in ps (p-p)) from scope using EJZIT, record.
8. Increase 0.1UI (p-p) on each iteration for SJ Frequency 1MHz, 10MHz, 100MHz; Increase 0.2UI (p-p) on each iteration for SJ Frequency 30KHz.
9. Measure SJ from scope until measured SJ meets or exceeds 62.5ps for 30KHz SJ Frequency or 20.0ps for SJ Frequency 1MHz, 10MHz, 100MHz.
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 6ps (p-p) and Max 62.5ps (p-p) for 30KHz, 20.0ps (p-p) for 1MHz, 10MHz, 100MHz.
12. Proceed to next permutation.

8.1.6 SJ Tone (33KHz SSC) Calibration

The Caltable method is used to calibrate SJ Tone:

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set 1100 Pattern on BERT.
6. Set SJ2 Frequency (210MHz).
7. Set 0 (%UI (p-p)) as base value in SJ2, measure SJ (in ps (p-p)) from scope using EJZIT, record.
8. Increase 0.1UI (p-p) on each iteration.
9. Measure SJ from scope until measured SJ meets or exceeds 10ps (p-p).
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 5ps (p-p) and Max 10ps (p-p).

8.2 Perform Calibration at TP2

Calibration at TP2 can be performed for Downstream (for Host) or Upstream (for Device).

8.2.1 Insertion Loss Calibration *(Applicable only if CTS version '0.7' is being used as the measurement reference method)*

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set Clk/256 Pattern on BERT.
6. Set Artek to base % of ISI (if long, set 15%).
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (start from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain .log file and .csv file from Seasim.
13. Read insertion plot from .csv. Check against upper and lower limit of specifications.
14. Use GRL script to plot output of insertion loss curve with specifications.
15. If failed, loop, increase 1% on Artek. Repeat insertion loss measurement.
16. Passing criteria is to ensure that 60% of the curve is within the upper and lower limits.

8.2.2 ISI Calibration (CEM Connector Channel + Replica Channel) *[Applicable only if CTS version '1.0' is being used as the measurement reference method AND supported ISI Generator of either PCIe ISI Board or Artek is used.]*

1. Initialize BERT.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set Clk/256 Pattern on BERT.
6. Start with PCIe CEM Variable ISI board Lane 3.
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (start from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain .log file and .csv file from Seasim.
13. Record insertion loss at 8GHz in dB from .csv file. Check against upper and lower specification limits.
14. If insertion loss at 8GHz is above 27dB, decrease Lane number and repeat steps 7 to 13.
15. If insertion loss at 8GHz is below 30dB, increase Lane number and repeat steps 7 to 13.
16. Insertion loss (IL) profile curve will be generated to determine Lane number that corresponds to 27dB, 27.5dB, 28dB, 28.5dB, 29.5dB and 30dB losses for use in next step of calibration.

8.2.3 Common Mode (CM) Sinusoidal Interference Calibration

Note: For the MG3710A (used in this test with the MP1800A BERT), every time the equipment is powered off or turned on, phase calibration needs to be run again before running CM-SI noise calibration.

The Caltable method is used to calibrate CM-SI:

1. Insert ISI trace at 28dB loss from previous calibration step.
2. Initialize BERT.
3. Initialize MG3710A.
4. Set 0mV (p-p) amplitude.
5. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
6. Set All Stress to 0mV.
7. Set Frequency on MG3710A/MP1900A for Common Mode to 120MHz.
8. Set Output on MG3710A/MP1900A for Common Mode to 7dBm/20mV, turn On Output.
9. Turn Off Output on MG3710A/MP1900A for Differential Mode.
10. Initialize scope.
11. Set up Func1 on scope to (Chan1 + Chan2)/2.
12. Measure Vp-p on Func1.

13. If MP1800A/MG3710A combination is used, increase Phase on MG3710A for Common Mode by 10%, measure Vp-p on scope until Max value.
14. Record measured Phase.
15. Set 800mV (p-p) amplitude (based on calibrated value).
16. Set All Zero Pattern on BERT.
17. Set ISI % value based on above calibrated data.
18. Set MG3710A/MP1900A (Common Mode) to Sine Wave.
19. Set -5dBm as base value on MG3710A.
20. Measure Amplitude (in mV) from scope, record.
21. Increase 0.174dBm/20mV on each iteration, measure Amplitude from scope until measured value meets or exceeds 150mV.
22. Plot a Caltable graph.
23. Passing criteria is to obtain measured CM-SI at Min 100mV and Max 150mV.

8.2.4 Differential Mode (DM) Sinusoidal Interference Calibration

This calibration is to ensure that the waveform achieves the calibrated eye height.

The Caltable method is used to calibrate DM-SI:

1. Insert ISI trace at 28dB loss from calibration step of 8.2.2 ISI Calibration (CEM Connector Channel + Replica Channel).
2. Initialize BERT.
3. Initialize MG3710A.
4. Set 0mV (p-p) amplitude.
5. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
6. Set All Stress to 0mV.
7. Set Frequency on MG3710A/MP1900A for Differential Mode to 2.1GHz.
8. Set Output on MG3710A/MP1900A for Differential Mode to 7dBm/15mV, turn On Output.
9. Turn Off Output on MG3710A/MP1900A for Common Mode.
10. Initialize scope.
11. Set up Func1 on scope to (Chan1 – Chan3).
12. Measure Vp-p on Func1.
13. If MP1800A/MG3710A combination is used, increase Phase on MG3710A for Differential Mode by 10%, measure Vp-p on scope until Max value.
14. Record measured Phase.
15. Set 800mV (p-p) amplitude (based on calibrated value).
16. Set All Zero Pattern on BERT.
17. Set ISI % value based on above calibrated data.
18. Set 0.89dBm as base value on MG3710A (Differential Mode).
19. Measure Amplitude (in mV) from scope, record.
20. Increase 0.174dBm/10mV on each iteration, measure Amplitude from scope until measured value meets or exceeds 30mV.
21. Plot a Caltable graph.
22. Passing criteria is to obtain measured DM-SI at Min 15mV and Max 40mV.

8.2.5 Optimized Preset/Final ISI Calibration

This calibration is to determine the optimum Preset, Equalization (EQ) gain, and final ISI trace to be used for final eye calibration in the next step.

1. Initialize BERT.
2. Set 500mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stress to 0mV.
5. Set Clk/256 Pattern on BERT.
6. Change to ISI trace at 27dB loss.
7. Set Preset to P5.
8. Trigger waveform on scope to display waveform.
9. Save waveform to .dat file (Y only).
10. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
11. Create Seasim config file with predefined values for Eye Opening calculation, starting with CTLE at 8.00dB gain.
12. Run Seasim with config file and step response.
13. Obtain .log file from Seasim.
14. Record eye height (EH) and eye width (EW) from .log file.
15. Calculate Area = EH x EW.
16. Repeat step 11 with CTLE DC gain of 0.25dB incremental up to 9.5dB. Record the DC gain for the maximum Area and EH and EW obtained.
17. Change Preset to P6. Repeat steps 8 to 16.
18. Determine optimized EH and EW with maximum Area from either P5 or P6 Preset.
19. If optimized EH is above 15mV and EW above 0.3UI, repeat step 6 by adding on 0.5dB ISI up to 30dB.
20. If optimized EH or EW falls below specification (15mV or 0.3UI), the last ISI trace and its associated optimized Preset and EQ shall be applied in the next step of calibration.
21. Once EH and EW at 0, 5, 10, 15mV are obtained, plot Caltable graph.

8.2.6 Stress Jitter Voltage Eye Calibration

This calibration is to ensure that the waveform achieves the calibrated eye width and eye height.

1. Initialize BERT.
2. Set 500mV (p-p) amplitude (based on calibrated value).
3. Set MP1825B/MP1900A to optimized Preset obtained from previous calibration step.
4. Set All Stress to 0mV.
5. Set Clk/256 Pattern on BERT.
6. Change to ISI trace obtained from previous calibration step.
7. Trigger waveform on scope to display waveform.
8. Save waveform to .dat file (Y only).

9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for Eye Opening calculation, starting with 0mV DM-SI.
11. Run Seasim with config file and step response.
12. Obtain .log file from Seasim.
13. Read eye height (EH) and eye width (EW).
14. Record EH vs. DM, and EW vs. DM for 500mV.
15. Increase DM-SI (in Seasim config) to 5mV, run Seasim again, obtain EH and EW.
16. Once EH and EW at 0, 5, 10, 15mV are obtained, plot Caltable graph.
17. If EH and EW do not fall within 0.3UI and 15mV, increase SJ by 0.1UI. Repeat method to obtain EH and EW by adjusting DM.
18. If EH and EW do not fall within 0.3UI and 15mV after SJ variation, adjust Amplitude and repeat method to obtain EH and EW.
19. Repeat until EW and EW fall within specifications.
20. Record measured Amplitude, SJ, and DM.

8.2.7 DM Optimization and Final Eye Calibration Using SigTest

This calibration applies the SigTest post processing method to determine the final eye height and eye width. *(Note: SigTest Final Eye Calibration is applicable only if CTS version '1.0' is being used as the measurement reference method.)*

1. Initialize BERT.
2. Set to final amplitude obtained from previous calibration step.
3. Set MP1825B/MP1900A to optimized Preset obtained from calibration step of 8.2.5 Optimized Preset/Final ISI Calibration.
4. Set DM and SJ to calibrated values obtained from previous calibration step.
5. Set RJ to calibrated value from 8.1.4 RJ Calibration step.
6. Change Pattern on BERT to PCIe Compliance Pattern.
7. Change to ISI trace obtained from calibration step of 8.2.5 Optimized Preset/Final ISI Calibration.
8. Trigger waveform on scope and capture waveform.
9. Run Sigtest (current version 4.0.38) using *'PCIE_4_0_RX_CAL\PCIe_4_16G_Rx_CAL_CTLE_XdB'* template, where XdB is the DC gain obtained from calibration step of 8.2.5 Optimized Preset/Final ISI Calibration.
10. Record eye height (EH) and eye width (EW).
11. If EH and EW are not within specifications, adjust amplitude and SJ until EH and EW achieve target specs.

9 Appendix B: Artek CLE Model Series Installation

9.1 ISI Generator Driver Installation

If using a Artek CLE Model unit for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the Artek unit to the PC being used as the controller using a USB 2.0 cable.
2. Turn on the front panel power switch on the Artek unit.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for Artek has been installed, you will see a 'bang' in the Device Manager.

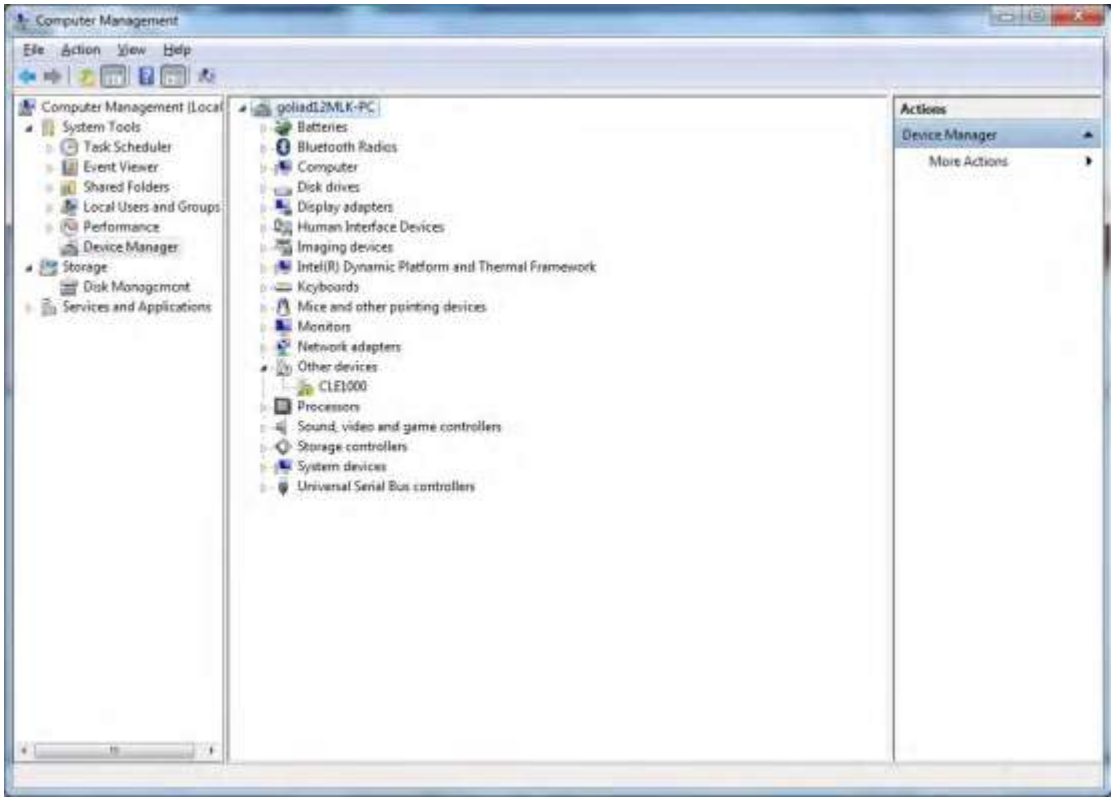


FIGURE 53. DEVICE MANAGER WINDOW

4. To install the Artek driver, go to http://www.aceunitech.com/support.html and download the Control Software package for the Artek CLE Series.
5. Unpack the CLE Series Software .zip file.
6. Install the CLE Series Driver:
   a) In Device Manager, right-click on **CLExxxx** > **Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 54.
   c) Browse to the root directory of the unzipped CLE Series Software folder.
   d) Click **Next**. You will be asked to confirm your request to install a driver. See Figure 55.
   e) Click **Install**. The driver software will complete the installation.
7. Once installation has completed, the Device Manager should look like Figure 56.

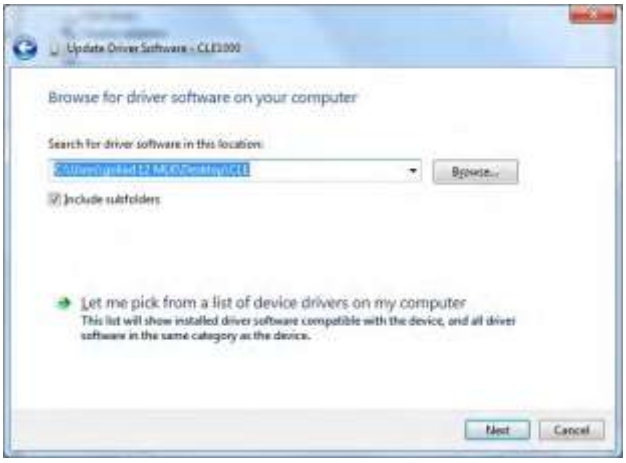


FIGURE 54. UPDATE DRIVER WINDOW

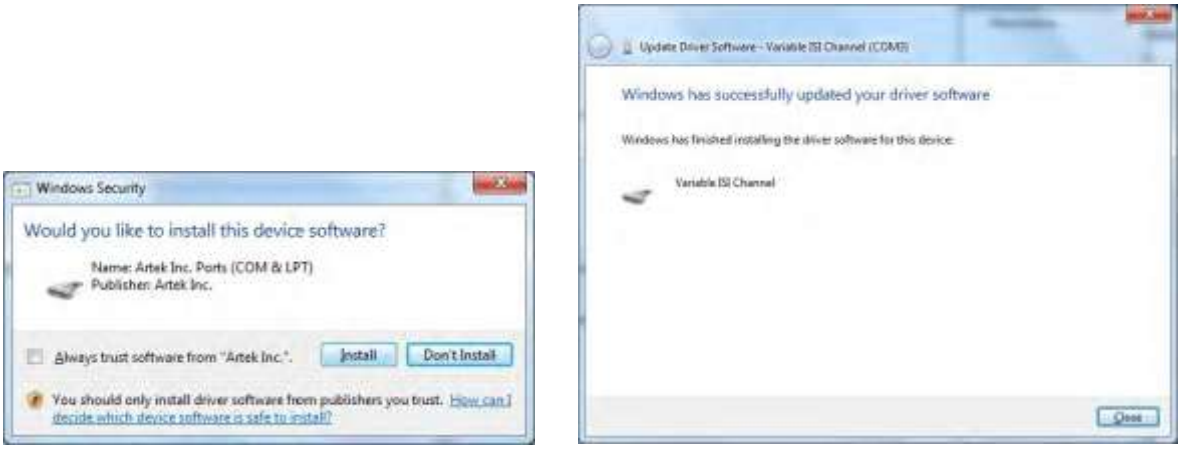


FIGURE 55. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

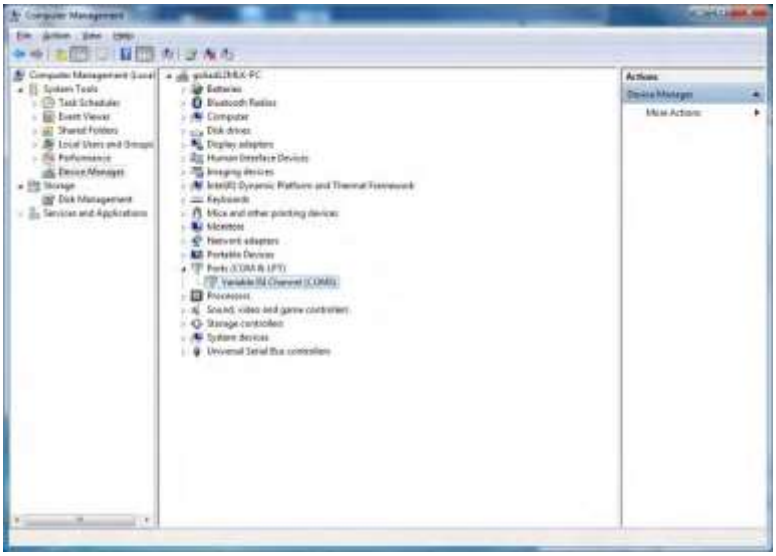


FIGURE 56. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE Series software driver is now installed and the Artek unit can now be selected for use remotely using the GRL software.

9.2 CLE Series GUI Installation

It may also be useful to install the CLE Series GUI, so that the ISI channel can also be controlled manually from the PC. To install the software, do the following:

1. In the CLE Series Software folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you do not want to have manual control.

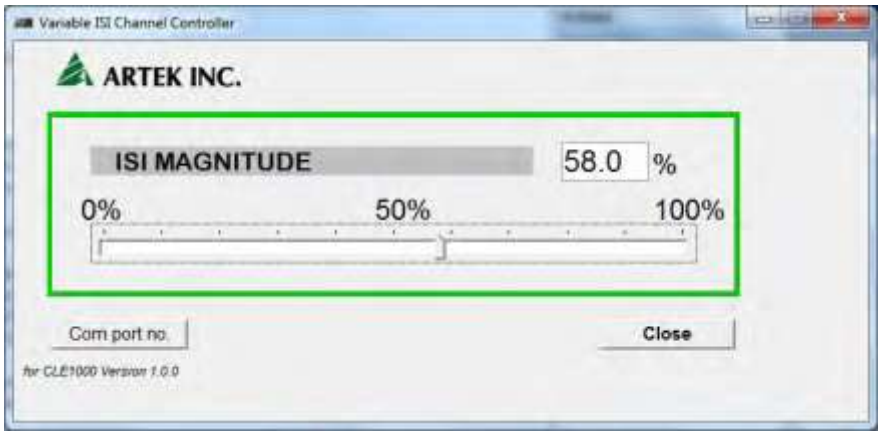


FIGURE 57. CLE SERIES GUI

10 Appendix C: Receiver Return Loss

The PCIe 4.0 Base Specification requires return loss to be measured at the end of the respective breakout channels with de-embedding performed for the breakout channel's contribution to RL to associate it with the Tx or Rx pin.

To measure return loss, the receiver must be powered up with its termination circuits turned on. For accurate RL measurements, microprobing may be performed on the Rx behavioral package.

The pass/fail mask for differential mode return loss over a 50 MHz to 8.0 GHz frequency range is shown in Figure 58 below.

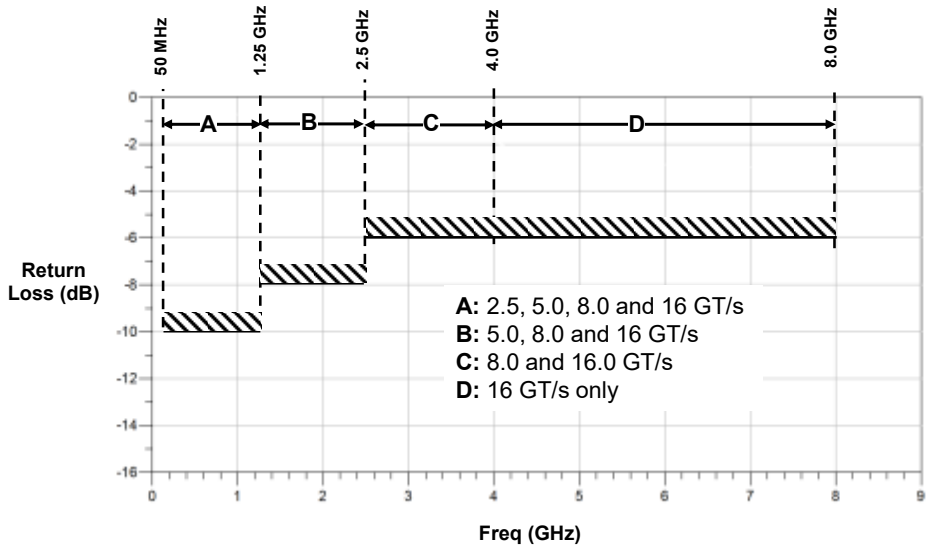


FIGURE 58. Differential Mode Return Loss Mask

FIGURE 59 shows the pass/fail mask for common mode return loss over the same frequency range as the differential mode.

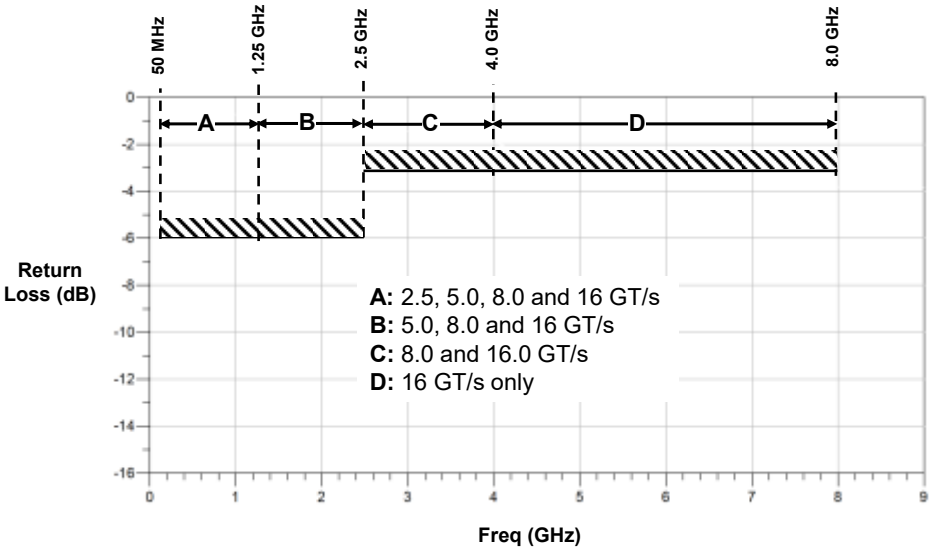
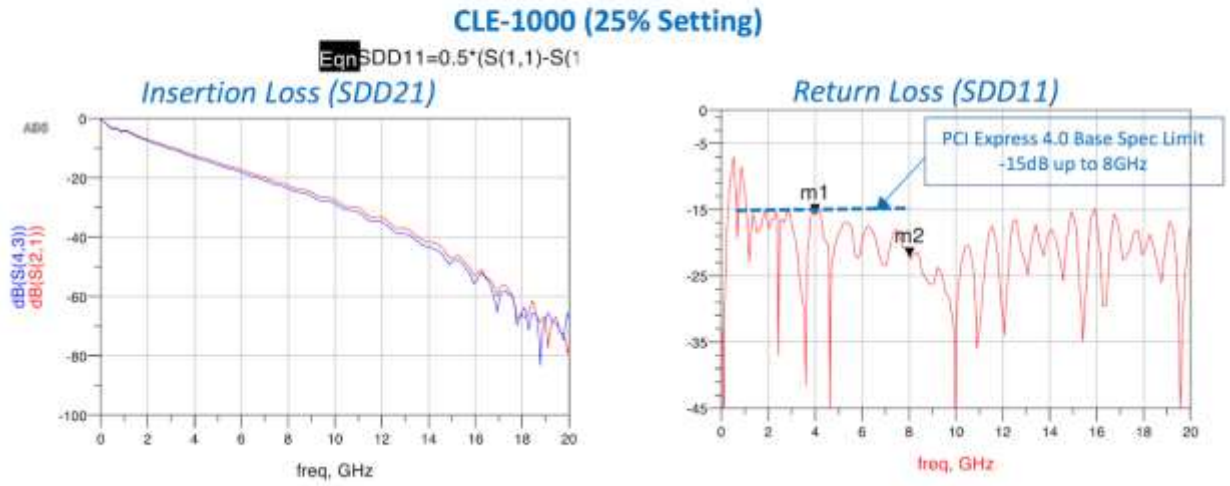


FIGURE 59. Common Mode Return Loss Mask

In the PCIe 3.0 Base Specification, the return loss limit was -18dB but the value was decreased to -15dB in PCIE4.0. The following diagram defines the insertion loss and return loss measured at 25% setting using the Artek CLE Series ISI generator.

IL and RL at 25% Setting



11 Appendix D: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

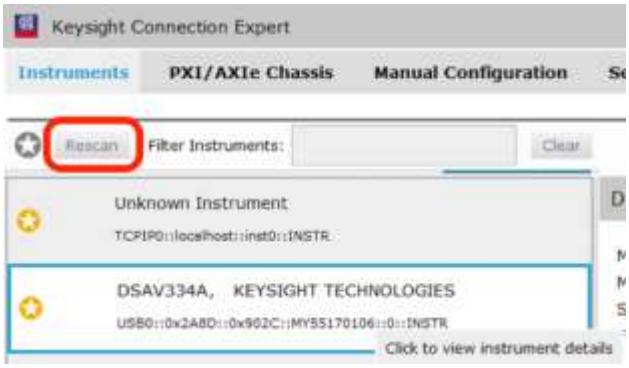


FIGURE 60. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

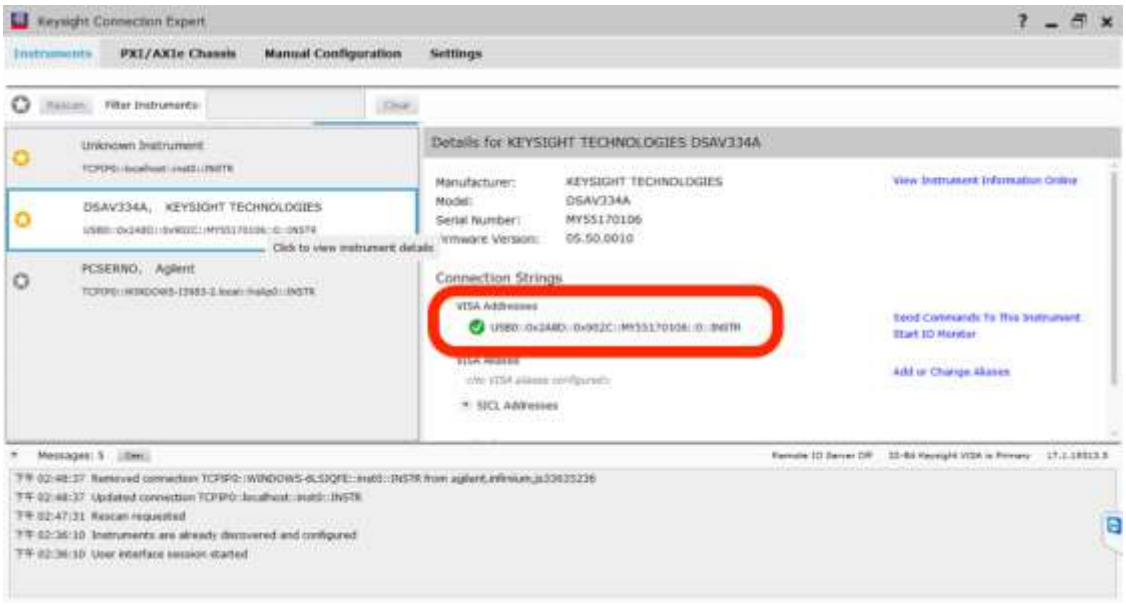


FIGURE 61. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe 4.0 Base Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

12 Appendix E: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

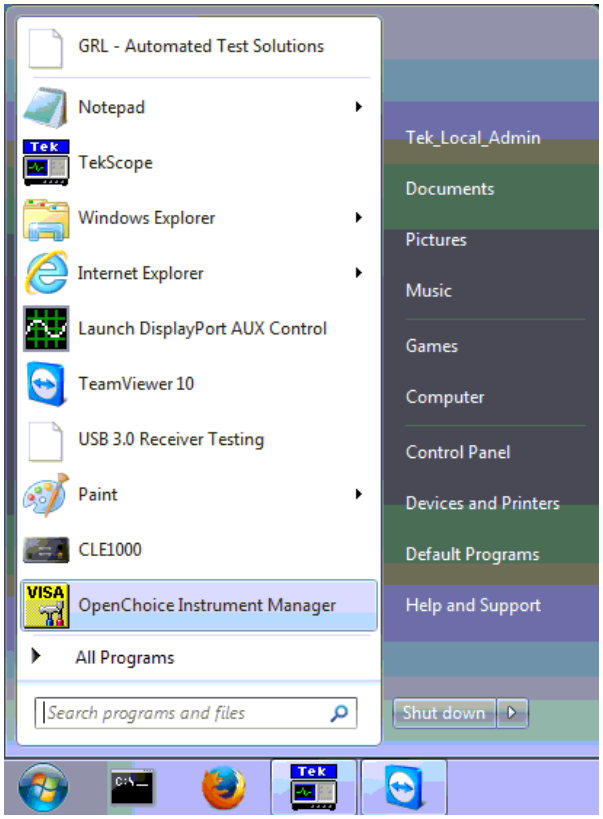


FIGURE 62. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

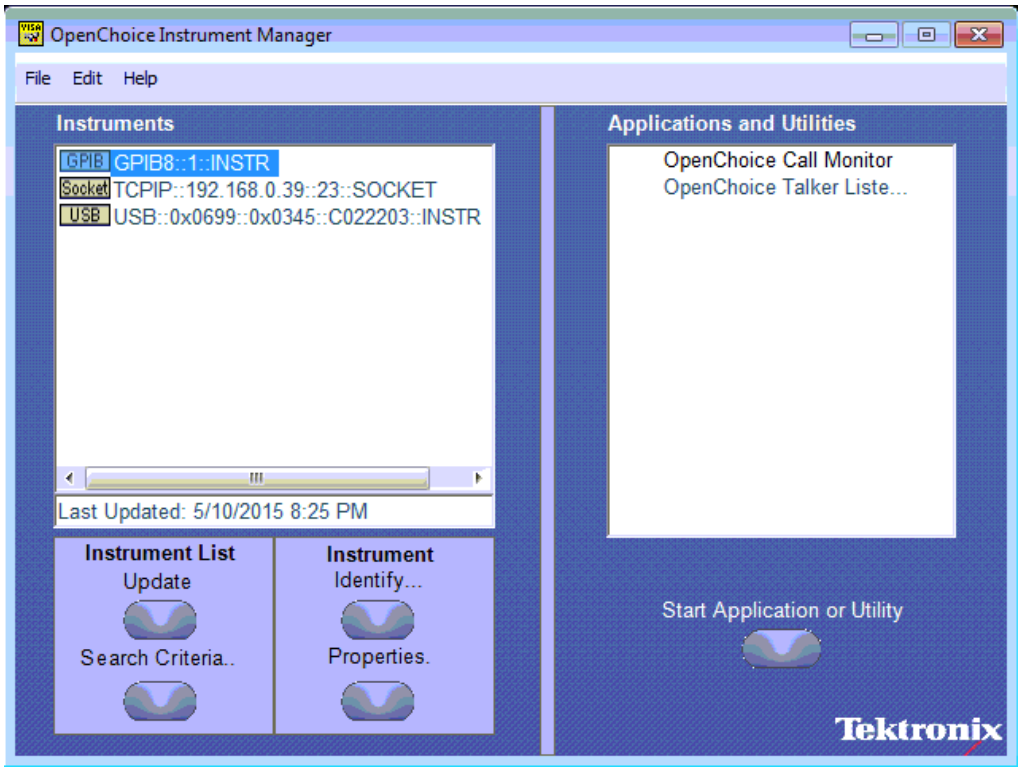


FIGURE 63. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe 4.0 Base Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe 4.0 Base Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

13 Appendix F: Scope and Cable De-skew

Before beginning any test or data acquisition, the oscilloscope must be warmed, calibrated, and cables de-skewed. This section describes the procedure for calibrating the Oscilloscope, and de-skewing the cables.

The DSO/DSA and DSAX/DSOX series Oscilloscopes must be calibrated manually, and this is recommended after a 30- to 60-minute warm-up period.

FIGURE 64. SCOPE DESKEW SETUP

Perform the following steps, with reference to Figure 68.

1. Select the **File → Open → Setup...** menu to open the **Open Setup File** window.
2. Navigate to the directory location that contains the deskew setup file (.set).
3. Select the deskew setup file by clicking on it.
4. Click the **Open** button to configure the oscilloscope from this setup file.

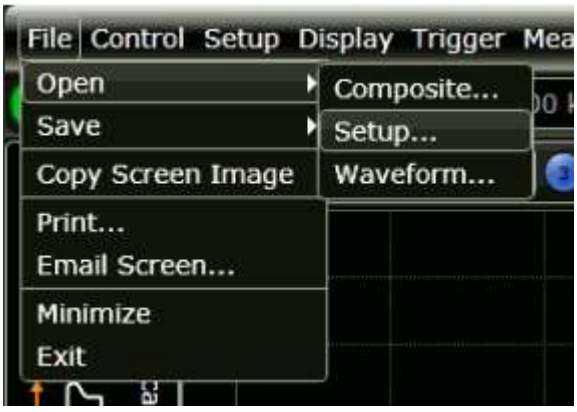


FIGURE 65. OPEN SCOPE DE-SKEW SETUP FILE WINDOW

FIGURE 66. SCOPE DE-SKEW SETUP FILE EXAMPLE

An example of the oscilloscope display is shown in Figure 67. A rising edge of the square wave is shown in a 100ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (blue trace) superimposed on one another. The lower portion of the screen is the differential signal (white trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure below is an example of exaggerated skew between channel 1 and channel 3.

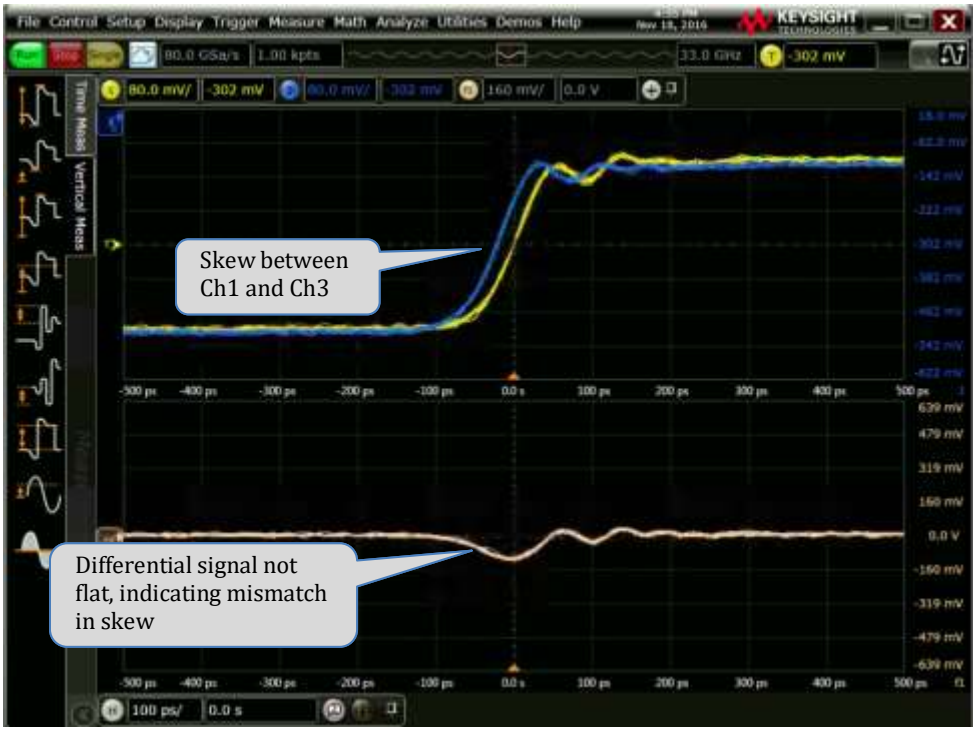


FIGURE 67. SCOPE DE-SKEW OSCILLOSCOPE DISPLAY

Figure 68 shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace) and channel 3 (blue trace) traces overlap, and the differential signal (white trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

FIGURE 68. SCOPE DE-SKEW OSCILLOSCOPE DISPLAY DE-SKEWED

Referring to Figure 69 and Figure 70, perform the following steps to de-skew the channels:

1. Click on the **Setup → Channel 1…** menu to open the **Channel** window.
2. Move the **Channel** window to the left so you can see the traces.
3. Adjust the **Skew** by clicking on the ← or → arrows, to achieve the flattest response on the differential signal (white trace).
4. Close the Channel window.
5. The de-skew operation is now complete.
6. Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

FIGURE 69. SCOPE DE-SKEW PROCESS – OPEN CHANNEL WINDOW

FIGURE 70. SCOPE DE-SKEW PROCESS – ADJUST SKEW

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