Granite River Labs

PCI Express® Gen 3.0 Base PCIe3-BASE & PCIe4-BASE (8 GT/s) Receiver Compliance Test Automation Solution User Guide & MOI

Using Anritsu MP1900A BERT, Tektronix DPO/MSO70000 Series Oscilloscope, and GRL-PCIE4-BASE-RXA Automation Test Software

Published on 15 April 2021

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TABLE OF CONTENTS

List of Figures

List of Tables

1 Introduction

This user manual provides information using the GRL PCIe3-BASE & PCIe4-BASE (8 GT/s) Rx test automation solution, GRL-PCIE4-BASE-RXA to set up and test an electrical receiver (Rx) device to meet PCI Express Base compliance at 8 GT/s as per PCI Express (PCI-SIG) Standards.

The main body of this documentation first describes how to configure the GRL-PCIE4-BASE-RXA test software to calibrate the stressed eye at the receiver of the device under test (DUT) in a PCIe Gen 3.0 (8 GT/s) system. This includes calibration to be performed at the following test points: TP1, TP2, and TP2P. The GRL software will automate calibration without channel effect at TP1 before measuring the eye opening due to trace length at TP2. The software also supports PCI-SIG Seasim application to perform calculation for TP2P to simulate the eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

After completing calibration, the GRL software will automate compliance testing for the receiver using Bit Error Ratio (BER) as a metric. The receiver path is tested with worst case eye to ensure a BER of less than 1E-12 can be achieved. The signal used to measure receiver tolerance should include the maximum allowable jitter, noise, and signal loss. The receiver tolerance test includes various differential mode sinusoidal interference, minimum transmitter voltage amplitude, and jitter which includes random jitter including a sinusoidal periodic jitter component that is swept across specific frequency intervals. The GRL software also provides an optional stress margin search test for the DUT.

The GRL-PCIE4-BASE-RXA software performs test automation according to PCI-SIG-approved Methods of Implementation (MOI's) using a high performance real-time oscilloscope, Anritsu BERT signal generator and error detector, and a compliant variable ISI generator. The GRL software is run from the computer or oscilloscope to provide automation control to test the DUT for PCIe Gen 3.0 Base Rx electrical compliance. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

Note: See Appendix of this documentation for test methodology example using automation or refer to PCI-SIG for approved Method of Implementation (MOI's) as technical reference.

1.1 Reference Documents

[1] PCI Express Base Specification, Rev. 3.1a, December 7, 2015

[2] PCI Express Base Specification, Rev. 4.0, Version 1.0, September 27, 2017

Note: The most current versions of above documents and ECNs are available to PCI-SIG Working Group members at: http://www.pcisig.com/specifications/pciexpress/

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT connector type. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description/Key Spec Requirement
Keysight/Tektronix High Performance Real-time Oscilloscope [a]	1	≥ 20 GHz bandwidth [b], with Windows 7+ OS and DPOJET (Jitter and Eye Analysis Tools) software
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator • MU195040A 21G/32G bit/s SI Error Detector • MU195050A Noise Generator
ISI Generator	1	PCIe-4 Base Spec compliant Fixed or Variable ISI Channel [c]
V(m) - K(f) Adapter	*2*	*34VKF50A Coaxial Adapter, only required if using a PAM4 Pulse Pattern Generator*
Computer (laptop or desktop)	1	For automation control (Windows 7+ OS)

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

[c] The Artek CLE Model Series is supported for variable ISI generation. Refer to Appendix of this document for the Artek CLE Series driver installation procedure.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable[a]	Qty.
SMA-to-SMA cables	2
Coaxial cables	2 pairs
Phase matched K-K coaxial cables	2 pairs

[a] Based on the standard test configuration. May require more or less cables depending on the DUT connector type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
GRL-PCIE3-BASE-RXA[a]	Granite River Labs PCIe® 4.0 (16 GT/s and 8 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com Included with Node Locked License to single oscilloscope or PC OS
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL PCIe Gen 3 Base Rx software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
Seasim	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software at TP2P) – www.pcisig.com
MX183000A	Anritsu High-Speed Serial Data Test Software – For loopback BER testing of the PCIe Gen 3 Base Rx DUT. This software is located in the MP1900A BERT.

[a] PCIe3-BASE and PCIe4-BASE will need to be installed to test at both 16 GT/s and 8 GT/s data rates. If the GRL-PCIE4-RXA test solution is purchased, the user will need to install the GRL-PCIE4-BASE-RXA and GRL-PCIE4-CEM-RXA solutions included in the package to perform testing for PCIe4-BASE and PCIe4-CEM at 16 GT/s and 8 GT/s.

3 General Overview of PCIe Base Rx CTS Requirements

This section extracts the general specifications from CTS to show the main differences between existing PCIe Base Rx data rates.

(Note: It is recommended to refer to the latest PCI-SIG released CTS for full measurement details.)

Table 8-11: Common Receiver Parameters

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	**124.9625 (min) 125.0375 (max)**	62.48125 (min) 62.51875 (max)	ps	UI is tolerance is equivalent to ±300 ppm and does not include SSC effects
$BW_{RX-PKG-PLL1}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL1}$	22 (max), 1.5 (min)	16 (max), 8 (min)	**4.0 (max), 2.0 (min)**	4.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$BW_{RX-PKG-PLL2}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL2}$	Not Specified	16 (max), 5.0 (min)	**5.0 (max), 2.0 (min)**	5.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$PKG_{RX-PLL1}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL1}$	3.0 (max)	3.0	**2.0**	2.0	dB	Second order PLL transfer bounding function
$PKG_{RX-PLL2}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL2}$	Not specified	1.0	**1.0**	1.0	dB	Second order PLL transfer bounding function
$RL_{RX-DIFF}$	Differential receiver return loss	See Figure 8-19	See Figure 8-19	See Figure 8-19	See Figure 8-19	dB	
RL_{RX-CM}	Common mode receiver return loss	See Figure 8-20	See Figure 8-20	See Figure 8-20	See Figure 8-20	dB	
$RX_{GND-FLOAT}$	Rx termination float time	500 (max)	500 (max)	500 **(max)**	500 (max)	ns	Limits added for 2.5 GT/s and 5.0 GT/s that match those for 8.0 GT/s
$V_{RX-CM-AC-P}$	Rx AC common Mode Voltage	150 (max)	150 (max)	**75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP**	75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP	mVP	Measured at Rx pins into a pair of 50Ω terminations to ground
Z_{RX-DC}	Receiver DC single ended impedance	40 (min) 60 (max)	40 (min) 60 (max)	Not specified	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. For 8.0 and 16.0 GT/s is bounded by RLRX-CM. See Note 5.
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V≥0 during Reset or power-down	≥10K (0-200 mV) ≥20K (> 200 mV)	≥10K (0-200 mV ≥20K (> 200 mV)	**≥10K (0-200 mV ≥20K (> 200 mV)**	**≥10K (0-200 mV ≥20K (> 200 mV)**	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during Reset or power-down	1.0K (min)	1.0K (min)	**1.0K (min)**	1.0K (min)	Ω	Parameters may not scale with process technology.

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect threshold	65 (min) 175 (max)	65 (min) 175 (max)	**65 (min)** **175 (max)**	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$. Measured at the package pins of the Receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	10 (max)	10 (max)	**10 (max)**	10 (max)	ms	An unexpected Electrical Idle ($V_{RX-DIFF-PP} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Lane to Lane skew	20 (max)	8 (max)	**6 (max)**	5 (max)	ns	Across all Lanes on a Port. $L_{RX-SKEW}$ comprehends Lane-Lane variations due to channel and repeater delay differences.

Notes:

1. Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in.
2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.
3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.
4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.
5. The Rx DC single ended impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance is permitted to start immediately and the Rx Common Mode Impedance (constrained by RL_{RX-CM} to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V_{-CMDC}|}.
7. $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.
8. Defines the time for the Receiver's input pads to settle to new common-mode on 2.5/5.0 GT/s transition to 8.0 GT/s.

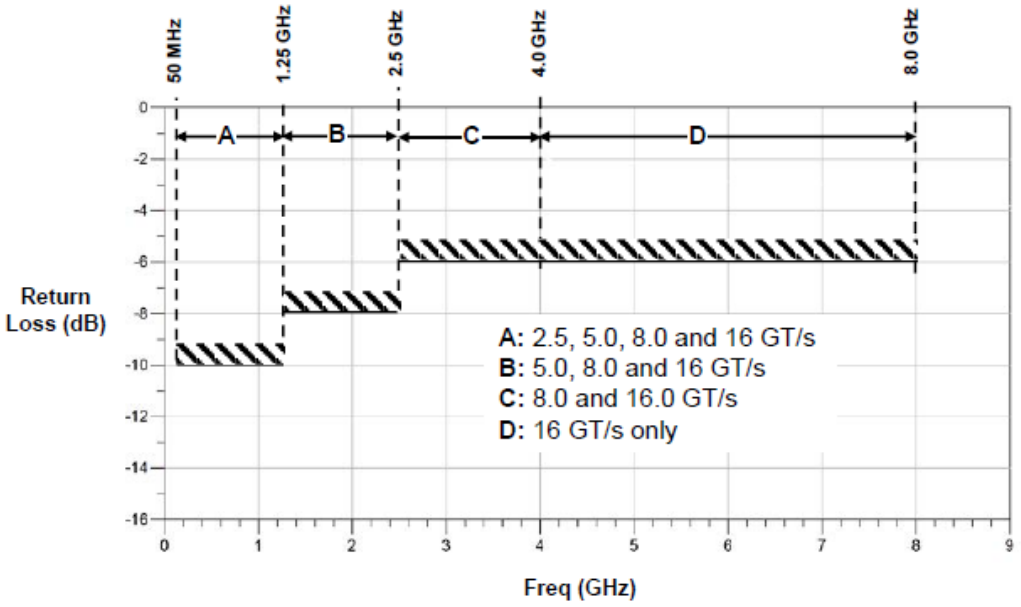


Figure 8-19: Tx, Rx Differential Return Loss Mask

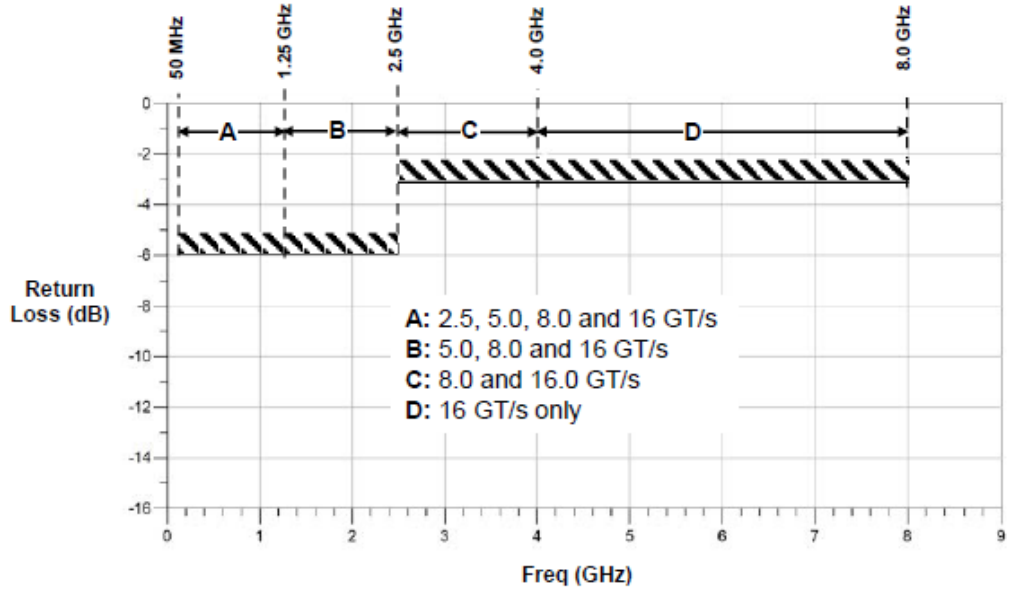


Figure 8-20: Tx, Rx Common Mode Return Loss Mask

Table 8-9: Calibration Channel IL Limits

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
2.5 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	4.7 dB @ 1.25 GHz	5.2 dB @ 1.25 GHz
5.0 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	10.0 dB @2.5 GHz	11.0 dB @2.5 GHz
8.0 GT/s	5 dB @ 1 GHz	8 dB @ 1 GHz	~20 dB @ 4 GHz	~22 dB @ 4 GHz
16.0 GT/s Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~22.5 dB @ 8 GHz	~23.5 dB @ 8 GHz
16.0 GT/s Non-Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~24.5 dB @ 8 GHz	~25.5 dB @ 8 GHz

Note: Calibration channel plus Rx package is 28 dB nominally (informative) for 16.0 GT/s.

Note: Different reference packages are defined for devcies containing Root Ports and all other device types at 16.0 GT/s.

Note: It is recommeded that some validation be done with shorter channels at 16.0 GT/s.

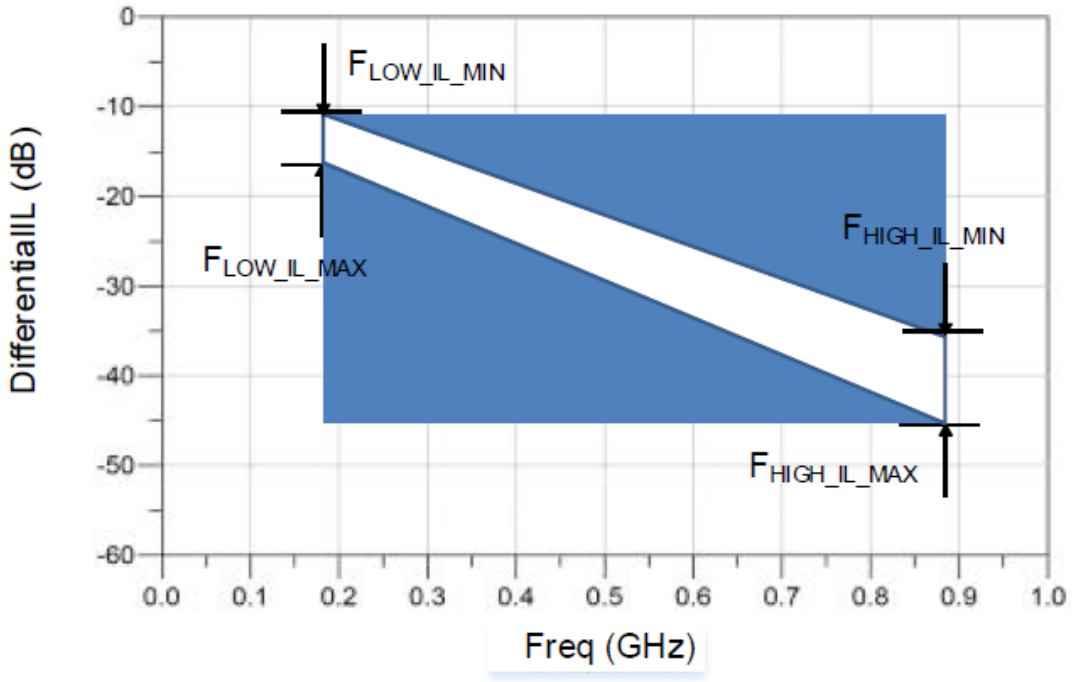


Figure 8-22: Calibration Channel IL Mask Excluding Rx Package

Table 8-10: Stressed Jitter Eye Parameters

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to1200	800-to 1200	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	ps	
T_{RX-ST}	Eye width	≤0.4	≤0.32	≤0.30	≤0.30	UI	Note 3, 4, 8,10
V_{RX-ST}	Eye height	≤175	≤100	≤25	≤15	mV PP	Note 2,4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	3.0 (max)	1.0	ps RMS	Note 6,7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	mV PP	Note 8
$V_{SSC-RES}$	SSC Residual	N/A	75	N/A	500	ps	Note 11, 13

Notes:

1. $V_{RX-LAUNCH}$ may be adjusted to meet V_{RX-ST} as long as the outside eye voltage at TP2 does not exceed 1300 mVPP for calibration at 2.5, 5.0 and 8.0 GT/s. $V_{RX-LAUNCH}$ is adjusted from 720 to 800 mV for 16 GT/s calibration.
2. Voltages shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
3. Eye widths shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
4. V_{RX-ST} and T_{RX-ST} are referenced to TP2P for 8.0 GT/s and 16.0 GT/s and TP2 for 2.5 GT/s and 5.0 GT/s. For 8.0 GT/s and 16.0 GT/s behavioral equalization are applied to the data at TP2.
5. $T_{RX-ST-SJ}$ may be measured at either TP1 or TP2. Only 8.0 GT/s and 16.0 GT/s Receivers are tested with Sj mask.
6. $T_{RX-ST-RJ}$ may be adjusted to meet the target value for T_{RX-ST} at 8.0 GT/s. Rj is measured at TP1 to prevent data-channel interaction from adversely affecting the accuracy of the Rj calibration. Rj is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
7. Both $T_{RX-ST-RJ}$ and $V_{RX-DIFF-INT}$ are limited to prevent the stressed eye from containing excessive amounts of jitter or noise distortion that are unrepresentative of a real channel. Too many of these distortion components produces a signal that cannot be equalized by an actual Receiver.
8. Defined as a single tone at 120 MHz. Measurement made at TP2 without post-processing. Common mode is turned off during T_{RX-ST} and V_{RX-ST} calibration and then turned on for the stressed eye jitter test.
9. For 2.5 GT/s and 5.0 GT/s Rx calibration variable channel loss is used to achieve the target eye height.
10. For 2.5 GT/s Rx calibration 100 MHz Sj is used to achieve the target eye width.
11. For 33 kHz SSC residual for common clock architecture testing only when testing at 5 GT/s.
12. Frequency for VRX-DIFF-INT is chosen to be slightly above the first pole of the reference CTLE.
13. Applied for CC testing only as a triangular phase modulation with a frequency between 30 kHz to 33 kHz when testing at 16 GT/s.

4 Setting Up GRL-PCIE4-BASE-RXA Automation Software

This section provides the procedures to start up and pre-configure the GRL-PCIE4-BASE-RXA automation software before running tests at 8 GT/s. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the software, follow the procedures in the following sections.

4.1 Download GRL-PCIE4-BASE-RXA Software

Download and install the GRL software as follows:

1. If the GRL-PCIE4-BASE-RXA software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **AnritsuPCIe3_0_BasePatternFilesInstallationxxxxxxxxxSetup.exe** – Run this on the Anritsu Signal Quality Analyzer to install the test pattern setup files.
   - **AnritsuPCIe3_0_BaseRxTestApplicationxxxxxxxxxSetup.exe** – Run this on the controller PC or oscilloscope to install the GRL-PCIE4-BASE-RXA application.
   - **AnritsuPCIe3_0_BaseRxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

4.2 Launch and Set Up Software

1. Once the software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

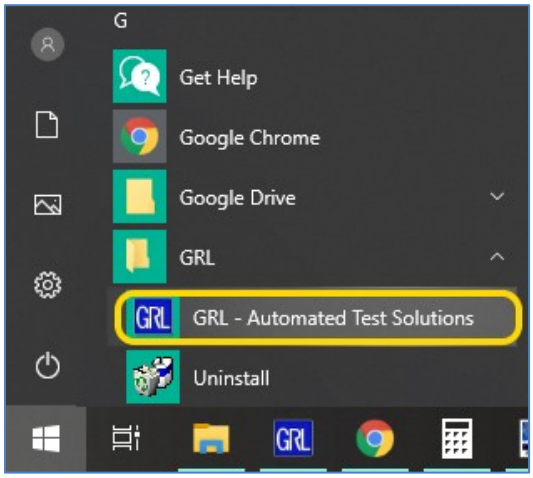


FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

2. From the Application→Rx Test Solution drop-down menu, select 'Anritsu PCIe 3.0 Base Rx Test' to start the PCIe 3.0 Base Rx Test Application. If the selection is grayed out, it means that your license has expired.

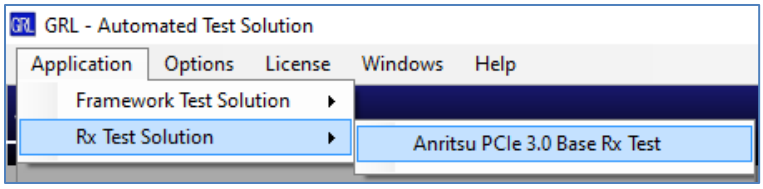


FIGURE 2. START PCIE 3.0 BASE RX TEST APPLICATION

3. To enable license, go to License→License Details.

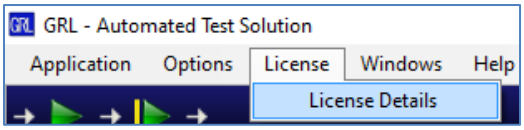


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

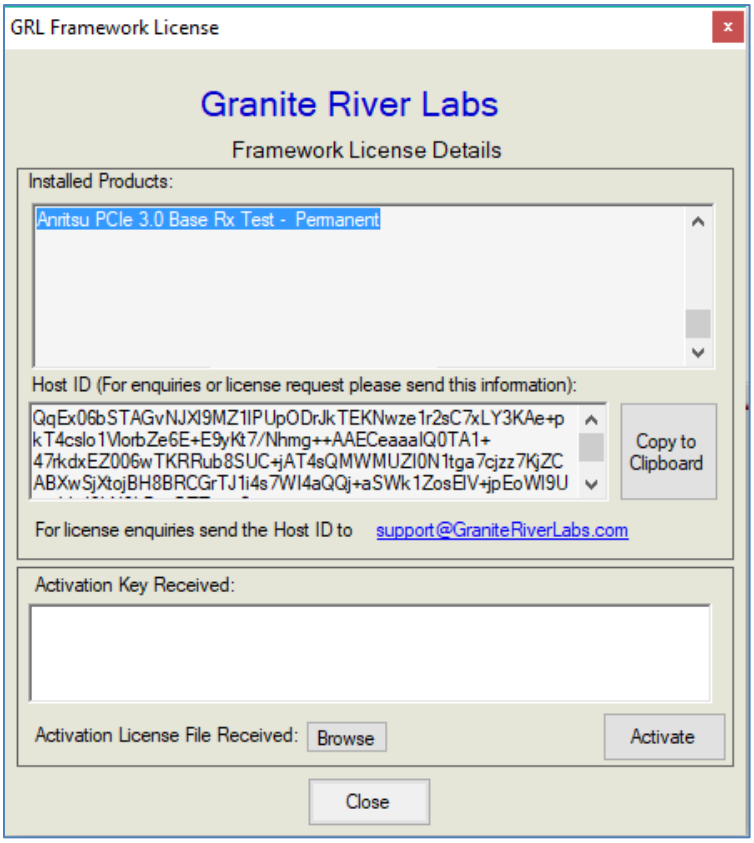


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select "Activate".
- If you do not have an Activation Key, select "Close" to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo*

version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.

4. Select the Equipment Setup icon on the PCIe 3.0 Base Rx Test Application menu.
5. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC.
6. If using a Artek CLE Model Series as the ISI generator, connect via USB to the GRL automation control enabled scope/PC and enter the Controller Serial (COM) address of the ISI generator. Also refer to Appendix of this document on how to install the CLE Series.
7. On the Scope or PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.
8. On the Equipment Setup page of the GRL PCIe 3.0 Base Rx Test Application, type in the address of each connected instrument into the 'Address' field.

   *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR".)*

   If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to **omit** the Port number from the address.

   *(Note: If the GRL software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".)*
9. Then select the "lightning" button ( ) for each connected instrument.

   The "lightning" button should turn green ( ) once the software has successfully established connection with each instrument.

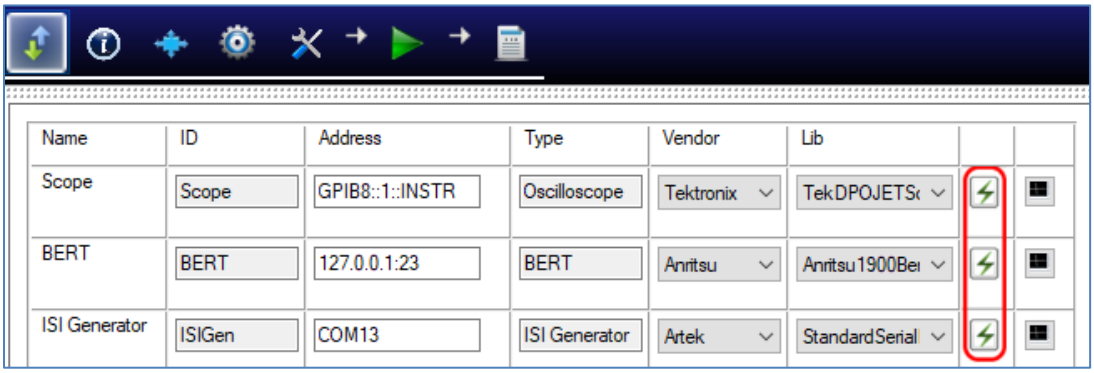


FIGURE 5. CONNECT INSTRUMENTS WITH GRL SOFTWARE

(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the PC is provided in the Appendix of this User Guide & MOI.)

4.3 Pre-Configure Software Before Calibration/Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced measurement setup.

4.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

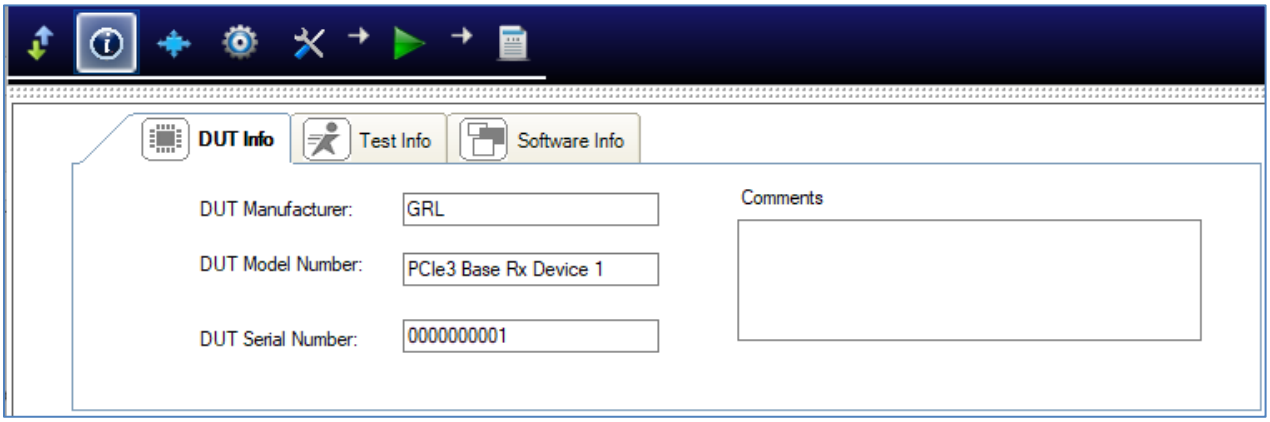


FIGURE 6. SESSION INFO PAGE

4.3.2 Set Measurement Conditions

Select  from the menu to access the **Conditions** page to set the conditions for calibration and testing.

Recommended procedure:

- *Step 1*: When calibrating, select all required conditions and perform the calibration.
- *Step 2*: Once calibration is completed and ready for testing, re-select the conditions that will be used for specific tests.

SJ tab: Select SJ Frequencies as defined by the Specification for calibration or testing.

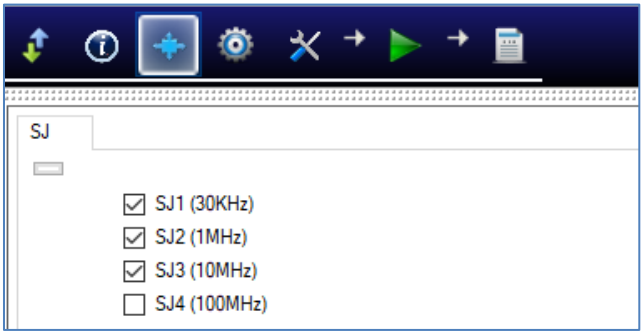


FIGURE 7. SELECT SJ FREQUENCIES

5 Calibrating Using GRL-PCIE4-BASE-RXA

The GRL-PCIE4-BASE-RXA test solution supports automated receiver calibration using the stressed eye method for PCIe Gen 3 base receivers at 8 GT/s. To perform calibration, the GRL software is run from the PC or oscilloscope to enable automation control for each step of pre and post processing measurement sequence.

Calibration for the PCIe3-Base & PCIe4-Base (8 GT/s) Rx electrical specification will basically be performed at three test points: TP1, TP2 and TP2P. Test Point 1 (TP1) is a physical test point for calibration without the effect of breakout channel length. TP2 is a physical test point that will affect the eye opening due to trace length. TP2P is a test point calculated by the PCI-SIG Seasim application to simulate the eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

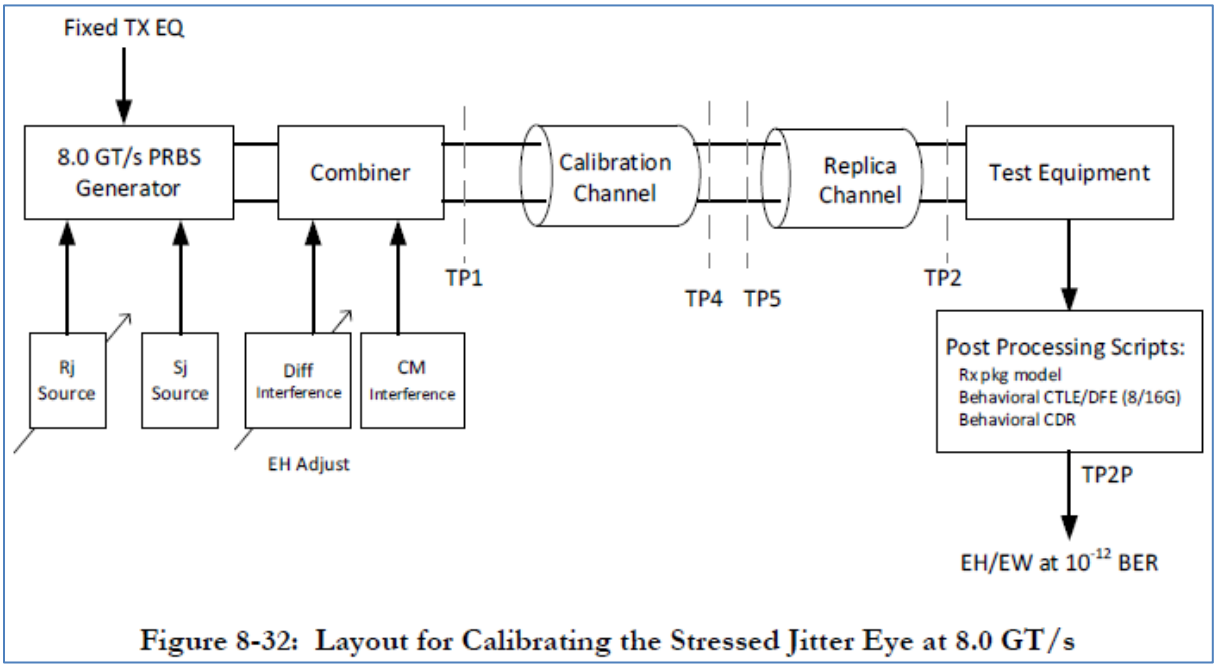


FIGURE 8. RX CALIBRATION BLOCK DIAGRAM FROM PCIE GEN 3 BASE SPECIFICATION

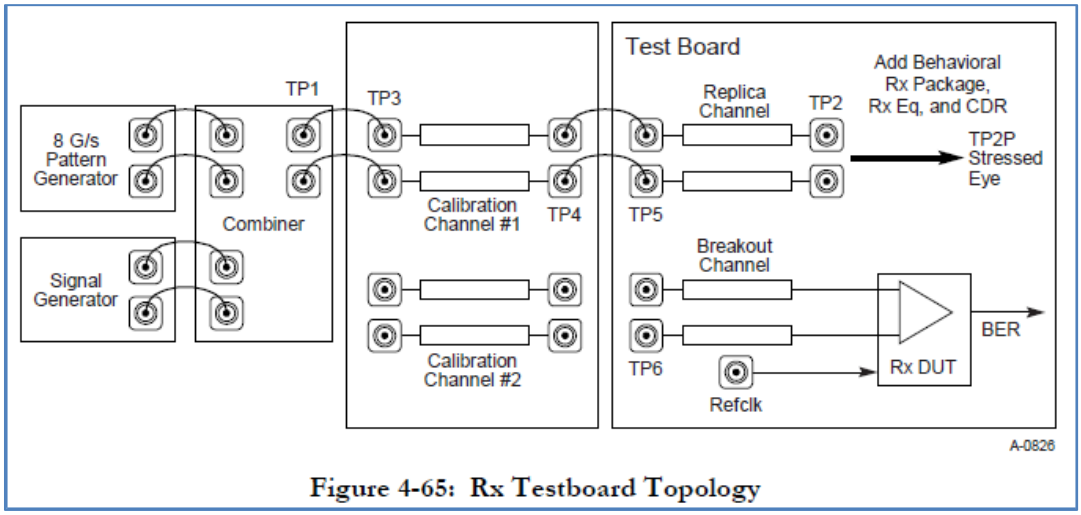


FIGURE 9. RX TEST SETUP SCHEMATIC FROM PCIE GEN 3 BASE SPECIFICATION

5.1 TP2 Channel Calibration Insertion Loss

The PCIe3-Base (8 GT/s) Rx Specification defines three types of calibration channel at TP2: None, Short and Long. The PCIe4-Base (8 GT/s) Rx Specification defines only the Long calibration channel at TP2.

Defined by the following figure, each channel insertion loss must meet the mask depending on its channel type. Variable and programmable ISI injector is needed to simulate the trace length to achieve the target loss for each channel.

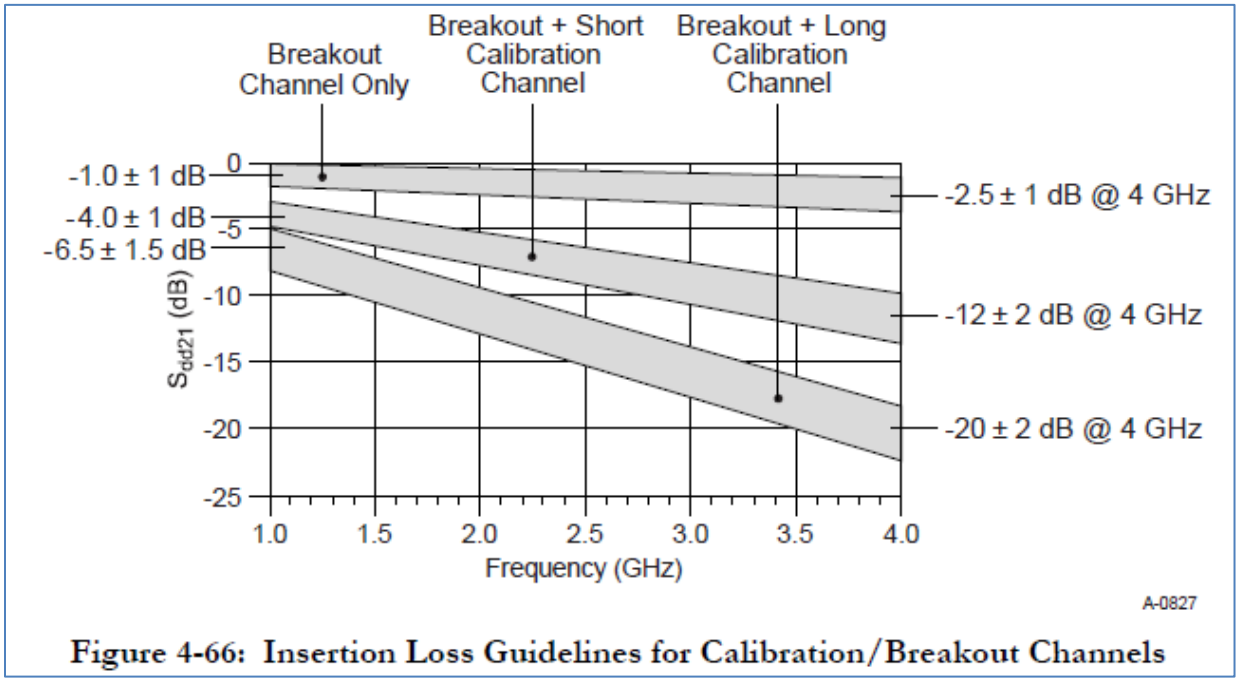


Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels

FIGURE 10. CHANNEL INSERTION LOSS MASK BY CHANNEL TYPE FROM PCIE GEN 3 BASE SPECIFICATION

Insertion loss is measured by differentiating step response and performing the FFT of the resulting impulse response. The Seasim application provides the method to calculate the insertion loss given the step response.

5.2 TP2P Post Processing Calibration

TP2P calibration consists of two methods for calibrating the stressed eye — one to determine the minimum eye height (voltage), and another for the minimum eye width (jitter).

5.2.1 TP2P Stressed Voltage Calibration

The configuration for calibrating a stressed voltage eye for Rx testing is shown below where the calibration procedure is performed for all calibration/breakout channel combinations. RJ and SJ are added as defined below and common mode and differential mode noise sources are added simultaneously.

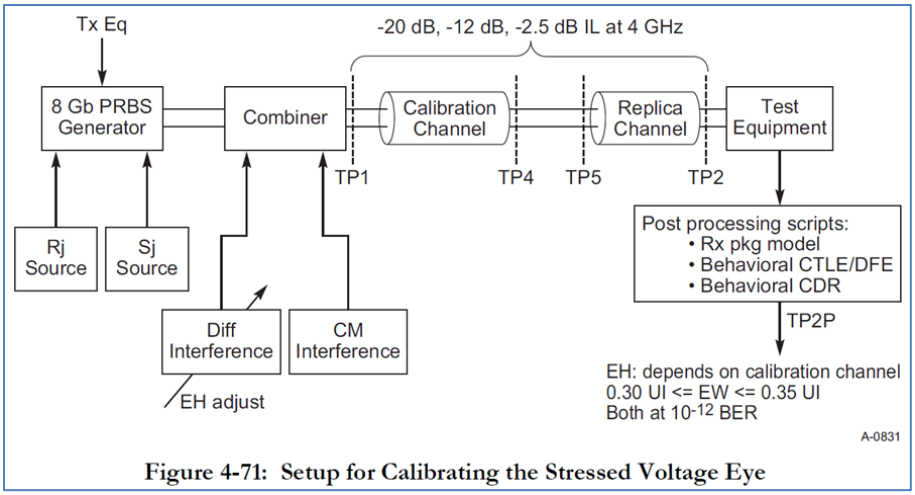


Figure 4-71: Setup for Calibrating the Stressed Voltage Eye

FIGURE 11. RX STRESSED VOLTAGE EYE CALIBRATION BLOCK DIAGRAM FROM PCIE GEN 3 BASE SPECIFICATION

Table 4-22: Stressed Voltage Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800	mVPP	Measured at TP1 Figure 4-65. $V_{RX-LAUNCH-8G}$ may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mVPP.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mVPP	Eye height @ BER=10^{-12}. Notes 1,2.
$T_{RX-SV-8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER=10^{-12}. Note 2
$V_{RX-SV-DIFF-8G}$	Differential mode interference	14 or greater	mVPP	Adjusted to set EH. Frequency = 2.10 GHz. Note 3.
$V_{RX-SV-CM-8G}$	Rx AC Common mode voltage at TP2P	150 (EH < 100 mVPP) 250 (EH ≥ 100 mVPP)	mVPP	Defined for a single tone at 120 MHz. Note 3.
$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.
$T_{RX-SV--RJ-8G}$	Random Jitter	2.0	ps RMS	Rj spectrally flat before filtering. Notes 4,5.
$V_{RX-MAX-SE-SW}$	Max single-ended swing	±300	mVP	Note 6.

Notes:

1. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the Rx DUT is capable of equalizing over a range of channel loss profiles. The test also guarantees the Rx is capable of operating over a sufficient dynamic range of eye heights. The "SV" in the parameter names refers to stressed voltage.
2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ are referenced to TP2P and are obtained after post processing data captured at TP2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.
3. $V_{RX-SV-DIFF-8G}$ measurement is made at TP2 without post processing. $V_{RX-SV-CM-8G}$ may be made at either TP1 or TP2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
4. $T_{RX-SV-SJ-8G}$ and $T_{RX-SV-RJ-8G}$ measurements are made at TP1 without post processing.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 4-74 for details.

6. $V_{RX-MAX-SE-SW}$ sets the maximum outer, single-ended eye voltage limit in the presence of differential and CM noise applied to the Rx, as observed at TP2 relative to ground with no behavioral RxEq post processing.

FIGURE 12. RX STRESSED VOLTAGE EYE LIMITS FROM PCIE GEN 3 BASE SPECIFICATION

Eye width and eye height are evaluated at TP2P after applying post processing. Both CTLE and DFE are applied when calibrating the long channel, and only CTLE for the medium and short channels calibration channels.

Eye height is determined by tuning the differential noise to meet the target $V_{RX-SV-8G}$ value. If this method is not able to maintain a sufficient eye width, less differential noise can be injected and the generator launch voltage can be adjusted.

Seasim application is used to post process the receiver eye at TP2P. This involves providing RJ, SJ, and DM-SI sources to Seasim, while combining CM-SI with clk/256 pattern source from BERT and captured in scope.

A sample of eye opening diagram simulated by Seasim is shown below.

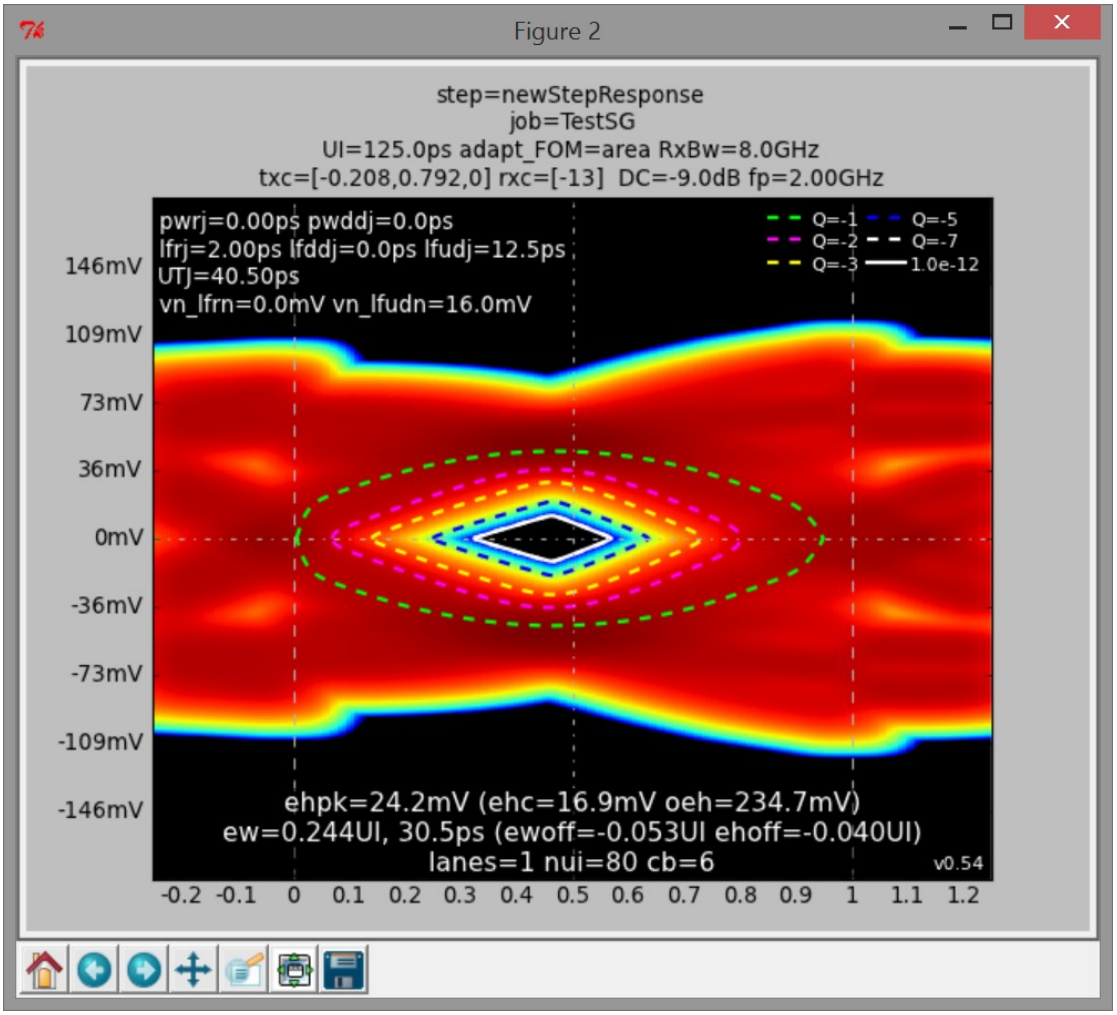


FIGURE 13. SEASIM SIMULATED EYE DIAGRAM EXAMPLE

5.2.2 Stressed Jitter Calibration (For Long Channel Only @PCIe3-Base Rx Specs)

The stressed jitter eye calibration only applies for the long calibration channel (-20 dB) as per the PCIe3-Base Rx specifications, which is also performed similarly to the stressed voltage eye calibration and using the same post processing scripts. Eye width is determined by adjusting the RJ source, while eye height can be obtained by adjusting the generator launch voltage.

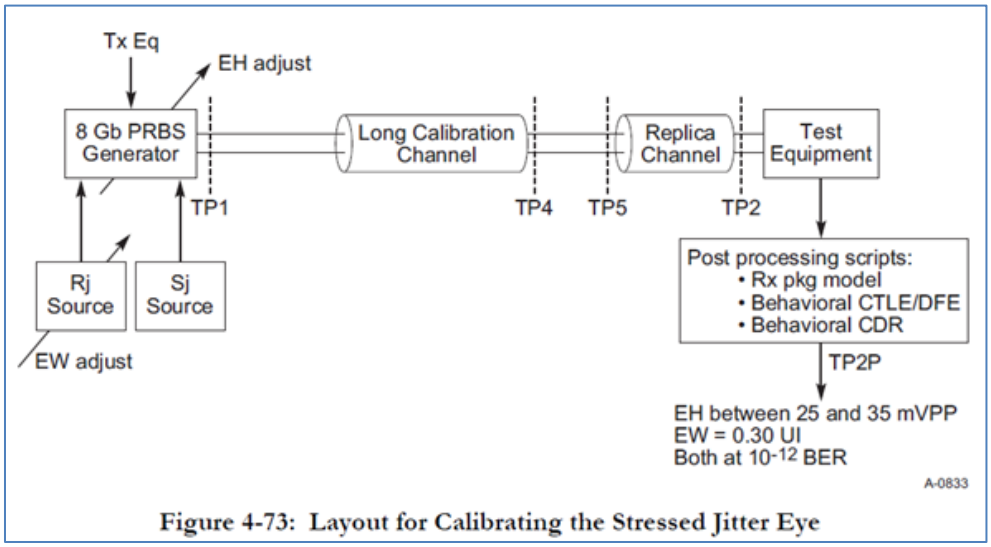


Figure 4-73: Layout for Calibrating the Stressed Jitter Eye

FIGURE 14. RX STRESSED JITTER EYE CALIBRATION BLOCK DIAGRAM FROM PCIE GEN 3 BASE SPECIFICATION

Table 4-23: Stressed Jitter Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800 (nominal)	mVPP	Measured at TP1, see Figure 4-65. See Note 1.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-ST-8G}$	Eye height at TP2P	25 (min) 35 (max)	mVPP	At BER=10^{-12}. See Note 2.
$T_{RX-ST-8G}$	Eye width at TP2P	0.30	UI	At BER=10^{-12}. See Note 2.
$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.
$T_{RX-ST--RJ-8G}$	Random Jitter	3.0	ps RMS	Rj spectrally flat before filtering. Measured at TP1. See Note 4.

Notes:

1. $V_{RX-LAUNCH-8G}$ may be adjusted to meet $V_{RX-ST-8G}$ as long as the outside eye voltage at TP2 does not exceed 1300 mVPP.
2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ are referenced to TP2P and are obtained after post processing data captured at TP2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.
3. $T_{RX-ST-SJ-8G}$ may be measured at either TP1 or TP2.
4. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the 0.3 UI value for $T_{RX-ST-8G}$. Rj is measured at TP1 to prevent data-channel interaction from adversely affecting the accuracy of the Rj calibration.

   Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.

FIGURE 15. RX STRESSED JITTER EYE LIMITS FROM PCIE GEN 3 BASE SPECIFICATION

The calibration setups as described in the following sections will use the Anritsu BERT and appropriate accessories to provide the necessary test patterns with jitter, ISI, crosstalk, and transmitter equalization.

When calibration is completed, the GRL software will generate a test report detailing all results obtained from the calibration.

5.3 Set Up Automated Rx Calibration for TP1

Once pre-configuration has been completed from previous section, continue with the following calibration setup at TP1 (output of the BERT generator) using a GRL automation control enabled oscilloscope and MP1900A BERT.

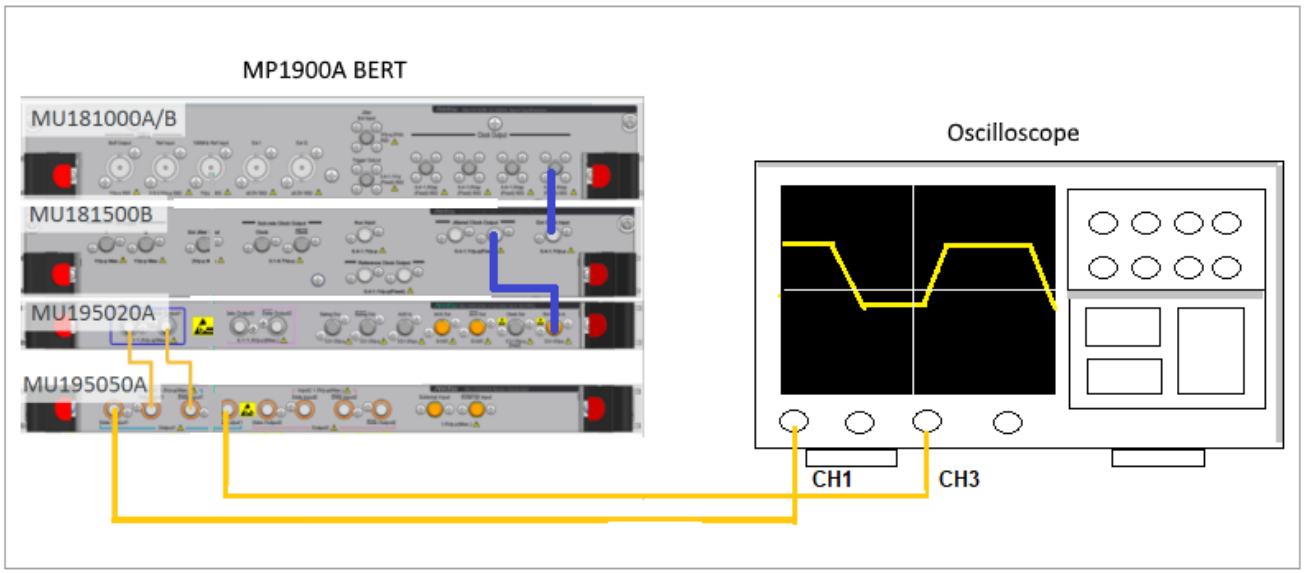


FIGURE 16. RECOMMENDED SETUP FOR TP1 RX CALIBRATION

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A Ext clock input.
3. Using coaxial cables, connect the MU195020A data outputs to the MU195050A data inputs.
4. Using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 3 on the oscilloscope.

5.4 Set Up Automated Rx Calibration for TP2

The next step is to calibrate the TP1-TP2 Channel (output of the breakout channel length) with the following calibration setup using a GRL automation control enabled oscilloscope, MP1900A BERT, and variable ISI source.

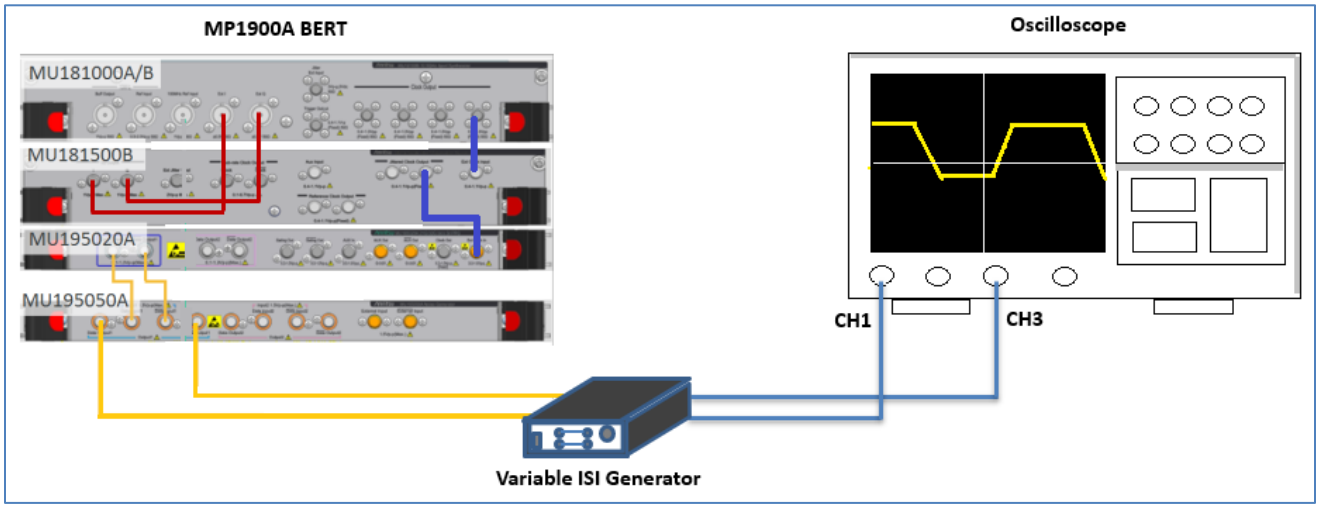


FIGURE 17. RECOMMENDED SETUP FOR TP2 CHANNEL RX CALIBRATION

1. Using back the same BERT connections from the TP1 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to the inputs of the variable ISI generator.
3. Connect the ISI generator outputs to Channels 1 and 3 on the oscilloscope.

5.5 Set Up Calibration Requirements

After setting up the physical equipment, select  from the GRL PCIe 3.0 Base Rx Test Application menu to access the Setup Configuration page. Use this page to configure the necessary measurement-related settings prior to running calibration.

5.5.1 ISI Generator Tab

Select the type of supported ISI generators to be used:

- "None": This is the recommended method which is used to provide -18 dB physical channel Insertion Loss for calibration and testing. A PCIe 3.0 CEM Fixture can be used in the setup for this method.
- "Artek": This is provided as an Option. The Artek CLE1000-S2 ISI channel and an additional ISI board can be used in the setup for ISI automation. *(Also see Appendix for more information on installing the Artek CLE Series.)*

The ISI Generator will be used for both calibration and testing.

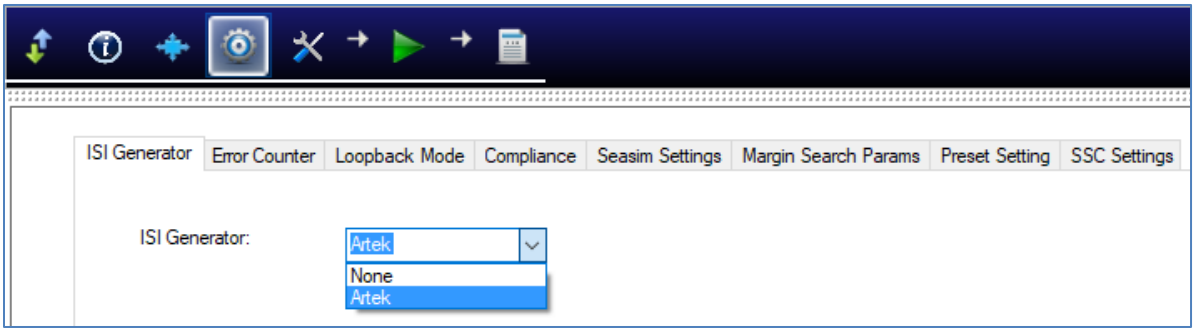


FIGURE 18. SELECT ISI GENERATOR

If the Artek CLE1000-A2 is being used, take note that the insertion loss specification of the CLE1000-A2 does not meet the PCI Express 3.0 Base Specification Requirement of -18 dB from 500 MHz to 5 GHz. Refer to Appendix B, Section 10.3: Return Loss Limitations of the Artek CLE1000-A2 for more information.

5.5.2 Seasim Settings Tab

Set up the Seasim parameters if using the Rx Behavioral package during Eye Height and Eye Width calibration. Also set the intrinsic jitter (if required) to be used in the Seasim calculation.

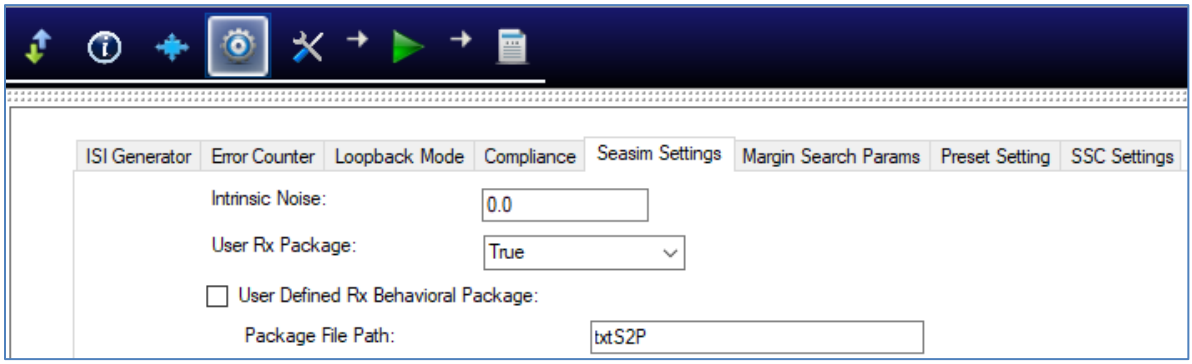


FIGURE 19. CONFIGURE SEASIM

5.5.3 Preset Setting Tab

Select a pre-defined preset to be used, or select the checkbox to use a custom preset. If using a custom preset, enter the Pre-shoot and De-emphasis values for the preset.

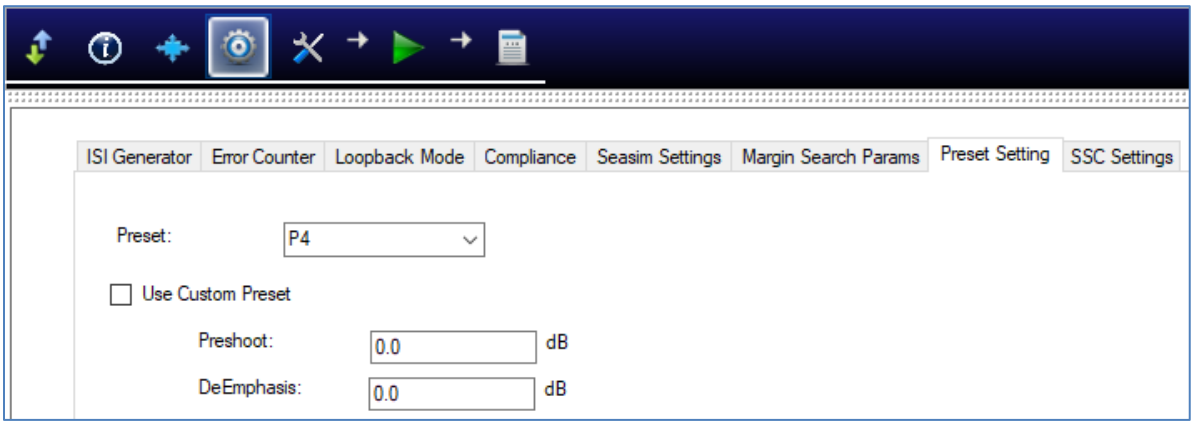


FIGURE 20. CONFIGURE PRESET

5.5.4 SSC Settings Tab

Select 'True' to enable Spread Spectrum Clock (SSC) capabilities for calibration and receiver testing (if supported by the DUT) for informative purpose. Set the Frequency and Deviation values for SSC.

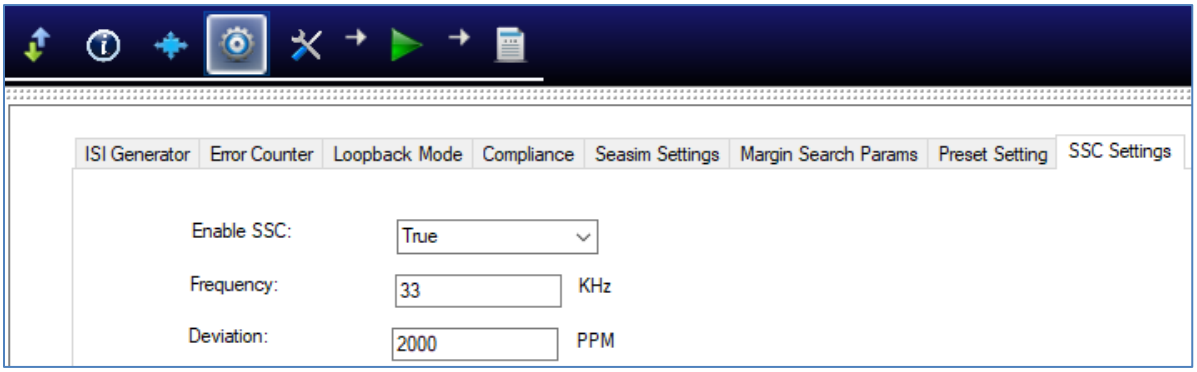


FIGURE 21. SET UP SSC

5.6 Select PCIe Gen 3 Base Rx Calibration

After setting up the calibration requirements, access the **Select Tests** page on the left panel to select available Rx calibration. Select the check boxes of the respective calibration to be performed.

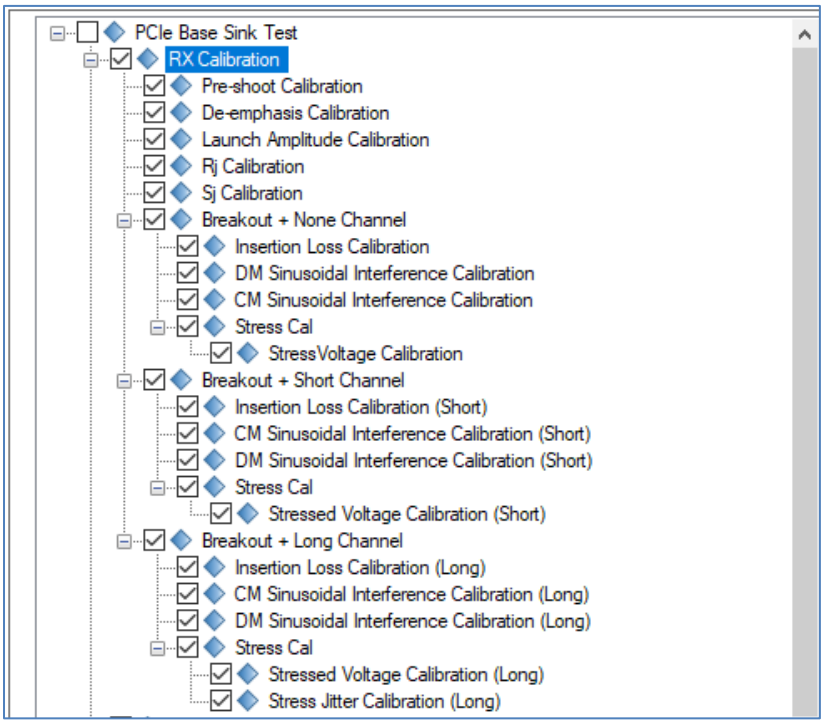


FIGURE 22. SELECT RX CALIBRATION

*[Note: The calibration list can be toggled as per PCIe3-Base & PCIe4-Base (8 GT/s) Rx specs using the **Test Methodology** selection field in the Configurations page. See Section 5.7 for details.]*

5.6.1 Select to Perform TP1 Calibration

At TP1, select to calibrate for BERT de-emphasis and pre-shoot (which form a linear curve fit), launch amplitude, random jitter (RJ), and sinusoidal jitter (SJ) (for PCIe Gen 3 frequencies as per PCIe3-Base & PCIe4-Base (8 GT/s) Rx specs and forms a linear curve fit for each SJ frequency).

The GRL software will automatically run the selected calibration when initiated.

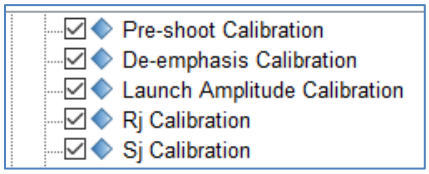


FIGURE 23. SELECT TP1 CALIBRATION

5.6.2 Select to Perform TP2-TP2P Channel Calibration

At TP2-TP2P, select to calibrate for channel insertion loss, differential mode (DM) and AC common mode (CM) SI, and final stressed voltage/jitter eye to achieve calibrated eye height and width to produce a final stressed eye diagram for all calibration/breakout channel combinations.

The GRL software will automatically run the selected calibration when initiated.

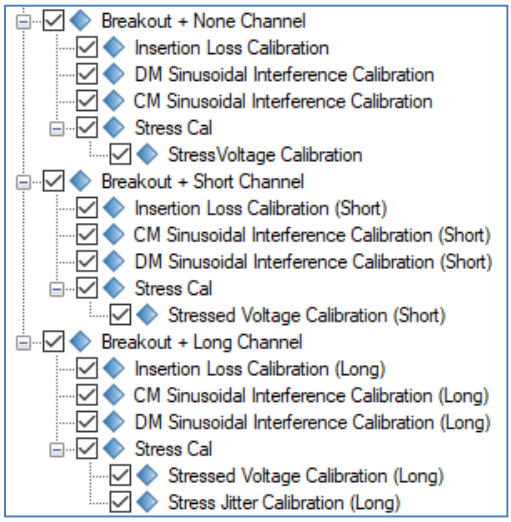


FIGURE 24. SELECT TP2-TP2P CALIBRATION (FOR PCIE3-BASE (8 GT/S) RX SPECS)

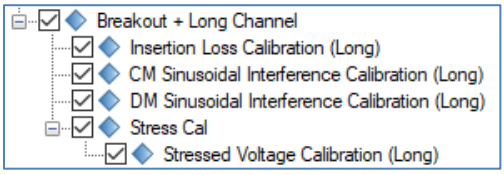


FIGURE 25. SELECT TP2-TP2P CALIBRATION (FOR PCIE4-BASE (8 GT/S) RX SPECS)

5.7 Configure Rx Calibration Parameters

Select  from the menu to access the Configurations page. Select the PCIe3-Base or PCIe4-Base (8 GT/s) Rx specs to be applied for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

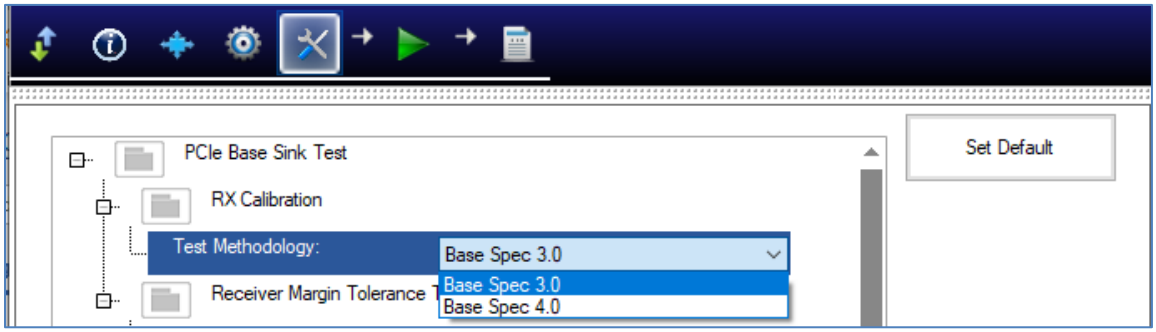


FIGURE 26. RX CALIBRATION CONFIGURATION PAGE

TABLE 4. RX CALIBRATION PARAMETER DESCRIPTION

Parameter	Description
Test Methodology	Select the PCIe3-Base or PCIe4-Base (8 GT/s) Rx specs to be applied for calibration. *[Note: This will cause the Rx calibration list to change as per the selected PCIe-Base specs.]*

5.8 Run Automation Calibration

Once calibration have been selected and set up from the previous sections, the calibration are ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE4-BASE-RXA software automatically runs the selected calibration when initiated.

Before running the calibration, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration exist, the software will *skip* those calibration.
- **Replace if Result Exists** – If results from previous calibration exist, the software will *replace* those calibration with new results.

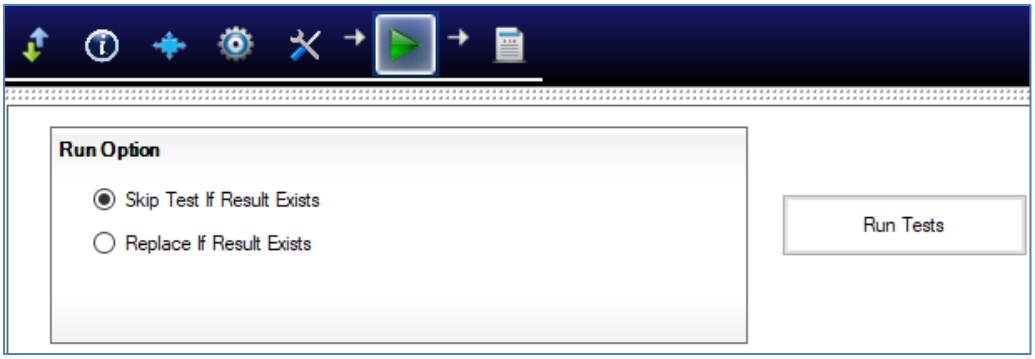


FIGURE 27. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration. The connection diagram for the calibration being run will initially appear to allow the user to make sure that the calibration environment has been properly set up before calibration can proceed. Below shows an example of the connection diagram pop-up for the TP1 calibration.

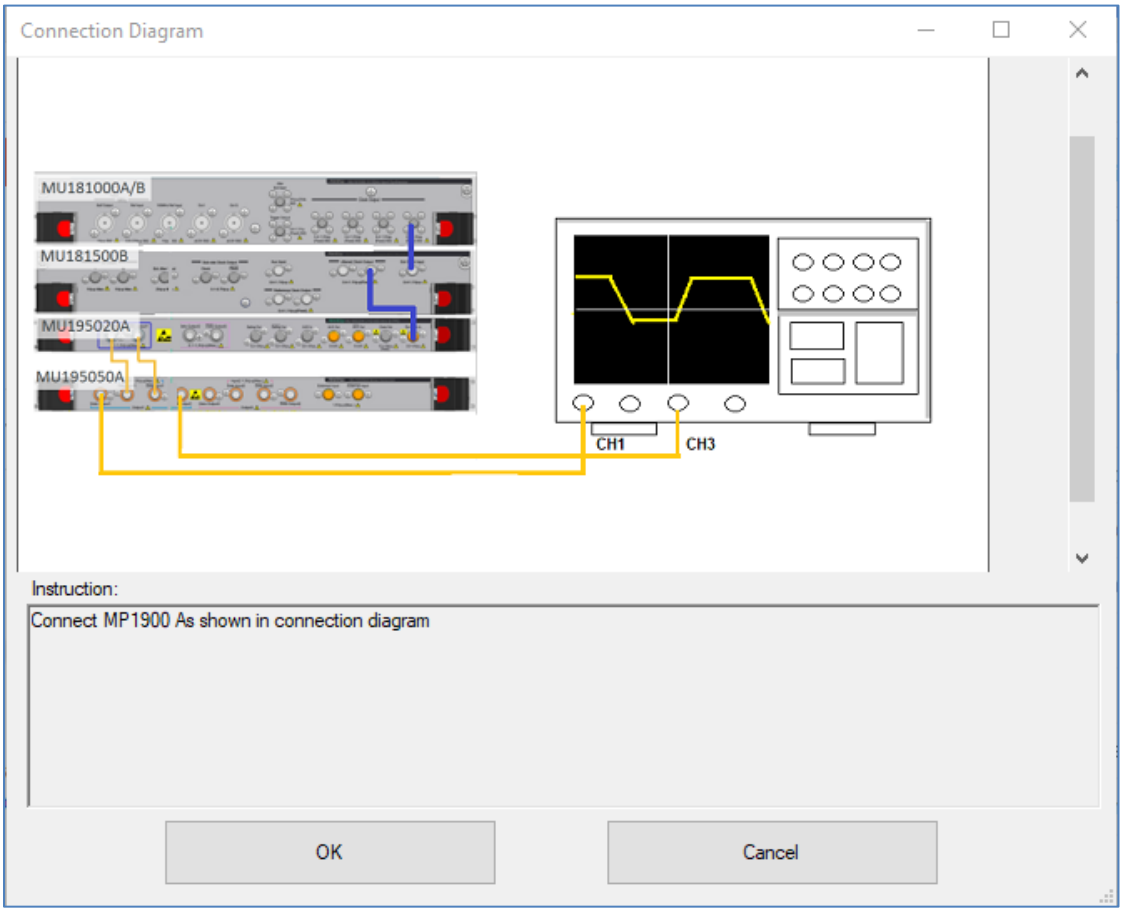


FIGURE 28. EXAMPLE CONNECTION POP-UP DIAGRAM FOR TP1 CALIBRATION

6 Testing Using GRL-PCIE4-BASE-RXA

The GRL-PCIE4-BASE-RXA test solution supports automated Rx compliance testing as well as optional margin tolerance testing for PCIe Gen 3 base receivers at 8.0 GT/s. Receiver compliance is tested for stress tolerance with and without the effect of breakout channel length at 8.0 GT/s. Receiver margin tolerance is an optional test which measures the stress margins with and without applying trace length.

Receiver device compliance ensures the receiver DUT is able to correctly interpret data from a received signal with valid voltage and timing characteristics by achieving an acceptable bit error ratio (BER) of less than 1E-12. The signal used for verifying receiver tolerance must contain the maximum allowable jitter, noise, and signal loss. The stressed receiver tolerance test should include various differential mode sinusoidal interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver tolerance test setup has been calibrated, the BERT will transmit a modified compliance pattern to the receiver and monitors the loopback pattern has a BER that is less than 1E-12 with a confidence level of 95%.

When testing is completed, the GRL software will generate a test report detailing all results obtained from the test runs.

6.1 Stressed Voltage Receiver Test

Once eye height and eye width have been calibrated, the Rx DUT will be connected to the far end of calibration channel for testing. Optimization for the transmitter equalization will then be performed in a similar way as for the stressed voltage eye calibration (equalization must also be optimized for the Rx DUT as well). SJ will be set to an initial value that allows the receiver CDR to achieve lock.

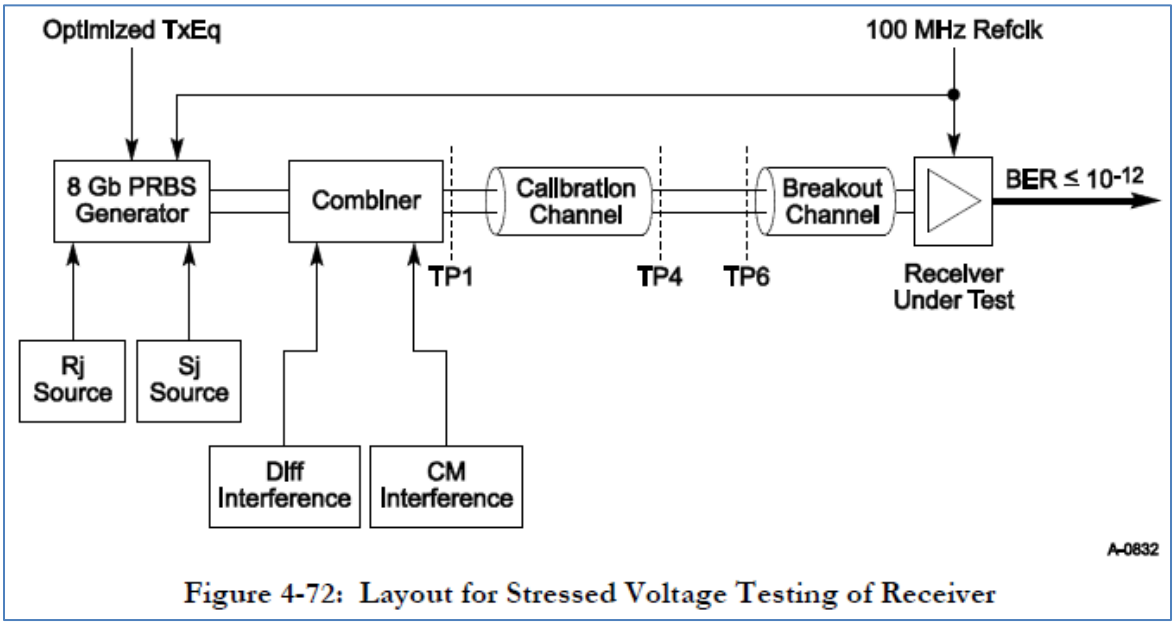


FIGURE 29. RX DUT STRESSED VOLTAGE TEST BLOCK DIAGRAM FROM PCIE GEN 3 BASE SPECIFICATION

6.2 Stressed Jitter Receiver Test (For Long Channel Only @PCIe3-Base Rx Specs)

The stressed jitter receiver test only applies for the long channel as per the PCIe3-Base Rx specs. Once eye height and eye width have been calibrated, the Rx DUT will be connected to the far end of the long calibration channel for testing. Optimization for the transmitter equalization will then be performed in a similar way as for the stressed voltage eye calibration (equalization must also be optimized for the Rx DUT as well). SJ will be set to an initial value that allows the receiver CDR to achieve lock which will then be swept over the frequency range as shown below, while maintaining fixed Tx equalization. The DUT must achieve a compliance BER of 1E-12 or lower for the entire swept SJ range.

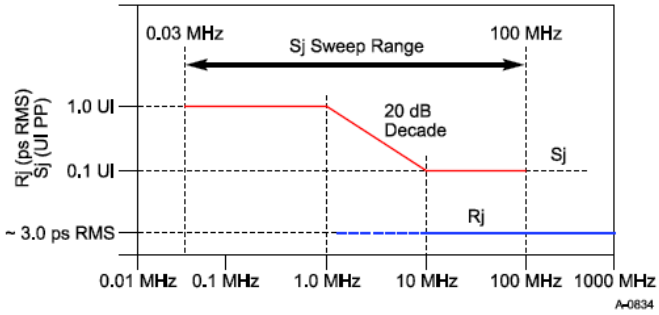


Figure 4-74: Swept Sj Mask

FIGURE 30. RX DUT STRESSED JITTER TEST SWEPT SJ MASK FROM PCIE GEN 3 BASE SPECIFICATION

6.3 Set Up Automated DUT Rx Compliance Test

Once calibration has been completed from Section 5, continue with the following test setups for DUT Rx compliance using the MP1900A BERT (including the MU195040A SI Error Detector) and variable ISI generator (for Short and Long Channels only).

6.3.1 Connect Equipment for No Breakout Channel Length Effect

The following setup is used to test the Rx DUT for 'None' channel stressed voltage compliance.

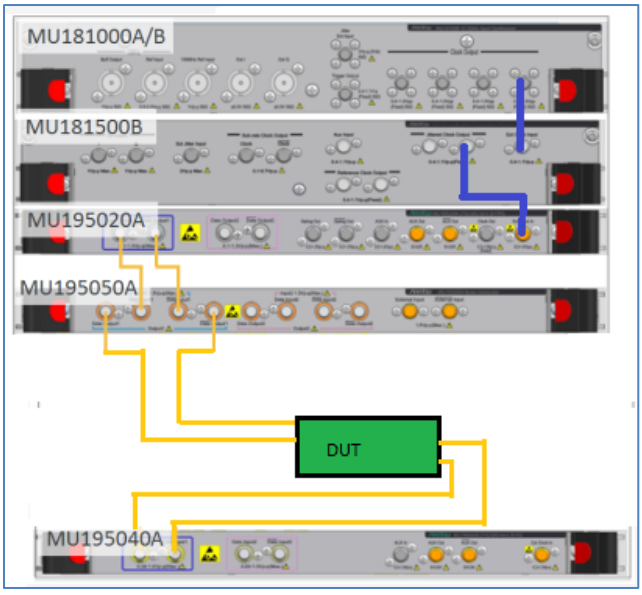


FIGURE 31. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (NONE CHANNEL)

1. Using back the same BERT connections from calibration, connect the MU195050A data outputs to the DUT Rx inputs.
2. Using phase matched K-K coaxial cables, connect the DUT Tx outputs to the MU195040A data inputs for loopback error detection.

6.3.2 Connect Equipment for Short/Long Breakout Channel Length Effect

The following setup is used to test the Rx DUT for Short/Long channel stressed voltage compliance as well as for Long channel stressed jitter compliance.

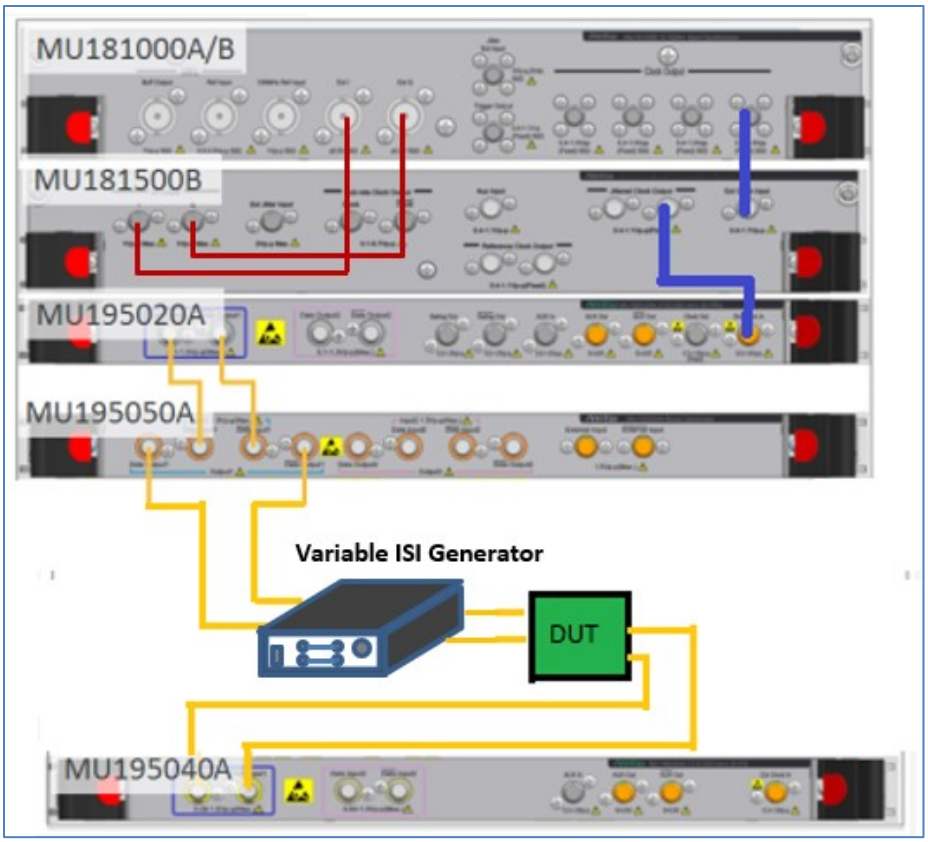


FIGURE 32. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (SHORT/LONG CHANNEL)

1. Using back the same BERT connections from calibration, connect the MU195050A data outputs to the inputs of the variable ISI generator.
2. Using coaxial cables, connect the ISI generator outputs to the DUT Rx inputs.
3. Using phase matched K-K coaxial cables, connect the DUT Tx outputs to the MU195040A data inputs for loopback error detection.

6.4 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL PCIe 3.0 Base Rx Test Application menu to access the Setup Configuration page. Use this page to configure the necessary measurement-related settings prior to running DUT tests.

6.4.1 Error Counter Tab

Select the DUT receiver base loopback capability for error detection. If the DUT can be configured for the loopback mode, select 'LoopBack', or otherwise select 'Manual'.

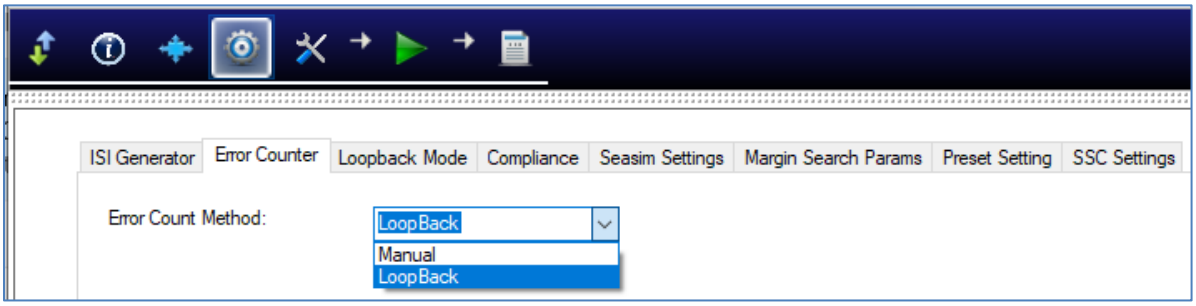


FIGURE 33. SELECT ERROR DETECTION MODE

6.4.2 Loopback Mode

If the 'LoopBack' mode has been selected from the Error Counter tab, then select 'Clock Recovery' in the Clock Recovery Method drop-down and set the clock recovery loop bandwidth. *Other options on the Clock Recovery Method drop-down are not yet supported.*

Optionally, a user-defined test pattern can also be used for error detection by selecting the 'Custom Pattern for Error Detector' checkbox. Then, select a supported pattern type to be used from the ED Pattern drop down field. If the checkbox is not selected, the default test pattern will be used.

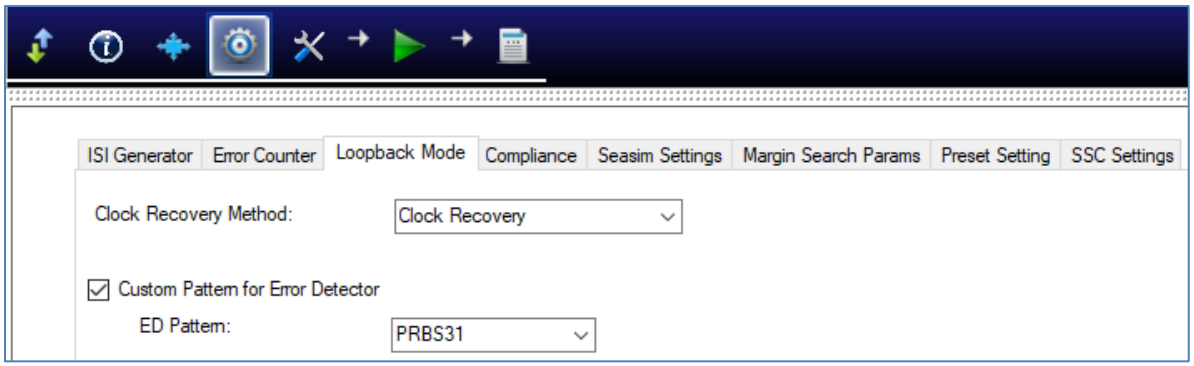


FIGURE 34. SET UP LOOPBACK TESTING

6.4.3 Compliance Tab

Set the target BER and Maximum Error limits allowed for compliance during testing. By default, the existing field values are based on Specification defined limits, however other values can also be set as required.

Note: The syntax '1e-12' indicates 1x10^{-12}, and is the only syntax supported in this field.

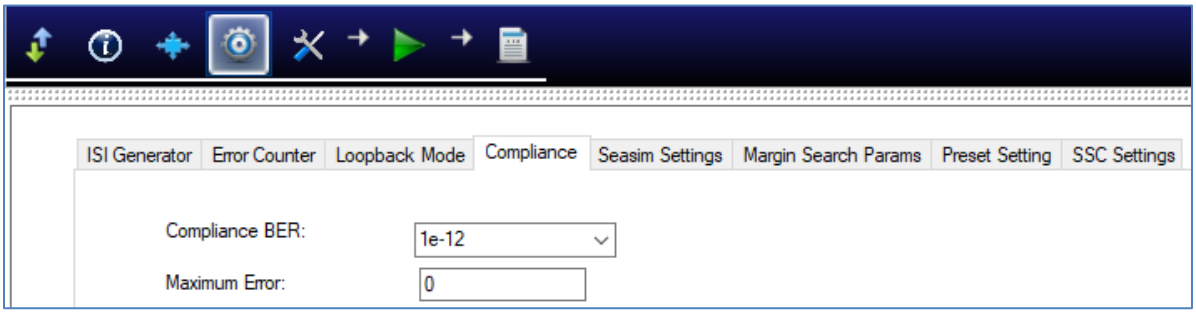


FIGURE 35. SET COMPLIANCE BER AND MAXIMUM ERROR LIMITS

6.4.4 Margin Search Parameters Tab

Set the target compliance BER, maximum error, step size, and maximum number of steps to be used when running optional margin tolerance tests.

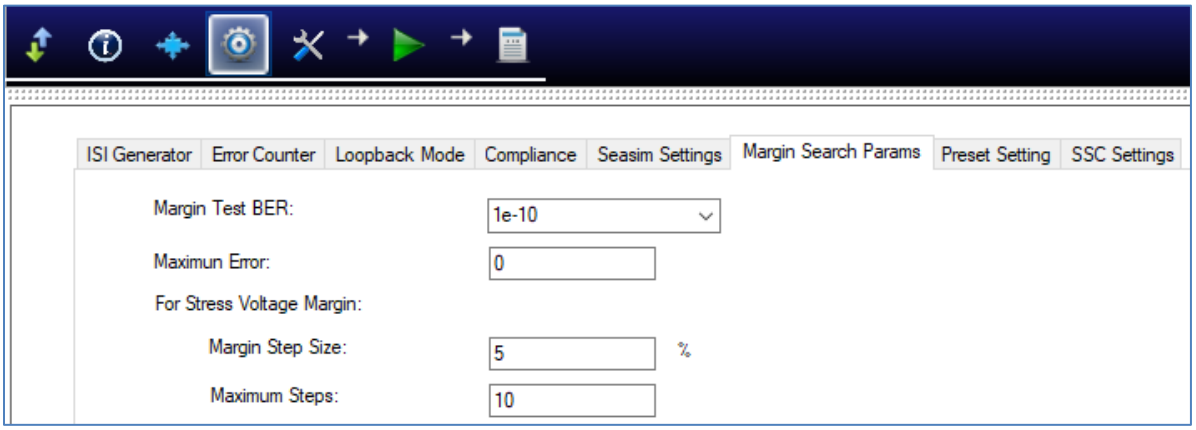


FIGURE 36. SET UP MARGIN SEARCH TEST

6.4.5 SSC Settings Tab

Select 'True' to enable Spread Spectrum Clock (SSC) capabilities for receiver testing (if supported by the DUT) for informative purpose. Set the Frequency and Deviation values for SSC.

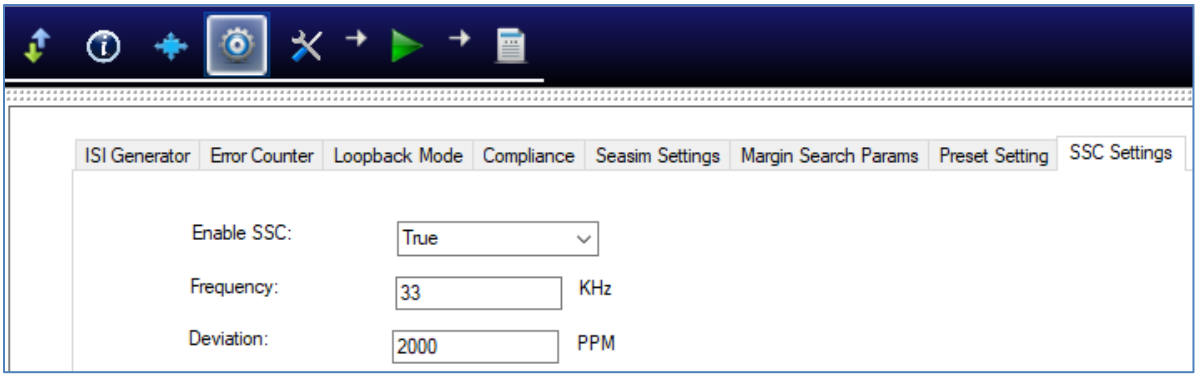


FIGURE 37. SET UP SSC

6.5 Select PCIe Gen 3 Base Rx DUT Tests

After setting up test requirements, access the **Select Tests** page on the left panel to select available Rx tests for the DUT. Select the check boxes of the respective tests to be run.

Note: When running tests for the first time or changing anything in the setup, it is suggested to perform calibration first. If calibration is not completed, attempting to run the Rx tests will produce errors.

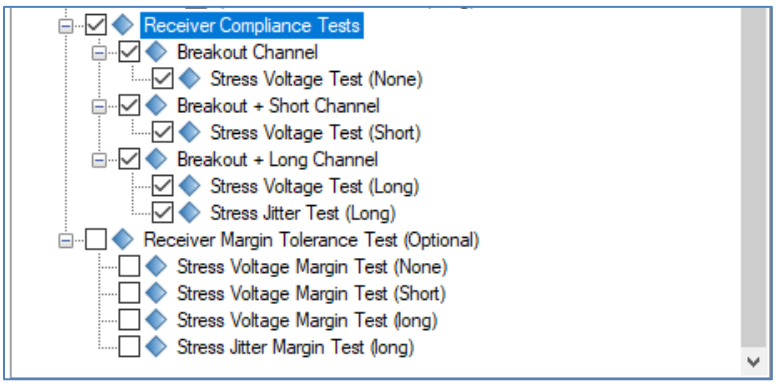


FIGURE 38. SELECT RX DUT TESTS

*[Note: The test list can be toggled as per PCIe3-Base & PCIe4-Base (8 GT/s) Rx specs using the **Test Methodology** selection field in the Configurations page. See Section 5.7 for details.]*

6.5.1 Select to Run Rx DUT Compliance Test

Select 'Receiver Compliance Test' to test the DUT for compliance with the PCIe3-Base & PCIe4-Base (8 GT/s) stress tolerance specs for all breakout channel lengths. Individual tests can also be selected to be performed as required.

The GRL software will automatically run the test sequence when initiated.

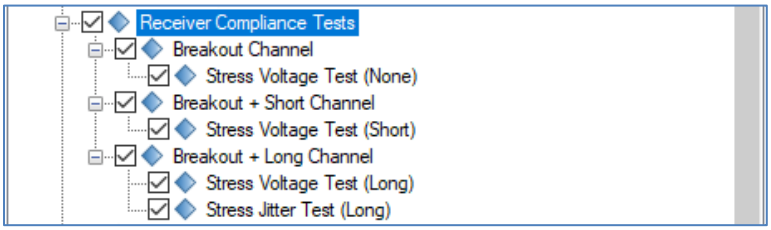


FIGURE 39. SELECT RX COMPLIANCE TEST (FOR PCIE3-BASE (8 GT/S) RX SPECS)

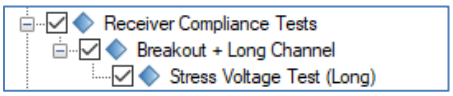


FIGURE 40. SELECT RX COMPLIANCE TEST (FOR PCIE4-BASE (8 GT/S) RX SPECS)

6.5.2 Select to Run Rx Margin Tolerance Test

Select 'Receiver Margin Tolerance Test' to perform an optional test to conduct a stressed margin search for jitter tolerance for all breakout channel lengths. Individual tests can also be selected to be performed as required.

The GRL software will automatically run the selected test when initiated.

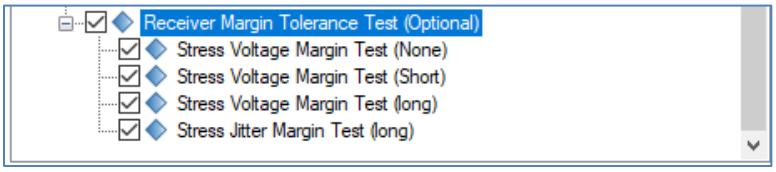


FIGURE 41. SELECT RX MARGIN TOLERANCE TEST (FOR PCIE3-BASE (8 GT/S) RX SPECS)

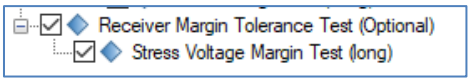


FIGURE 42. SELECT RX MARGIN TOLERANCE TEST (FOR PCIE4-BASE (8 GT/S) RX SPECS)

6.6 Configure Margin Tolerance Test Parameters

If the Rx margin tolerance tests are selected to be performed, select  from the menu to access the Configurations page. Set the necessary margin test parameters for each SJ frequency as described below.

To return all parameters to their default values, select the 'Set Default' button.

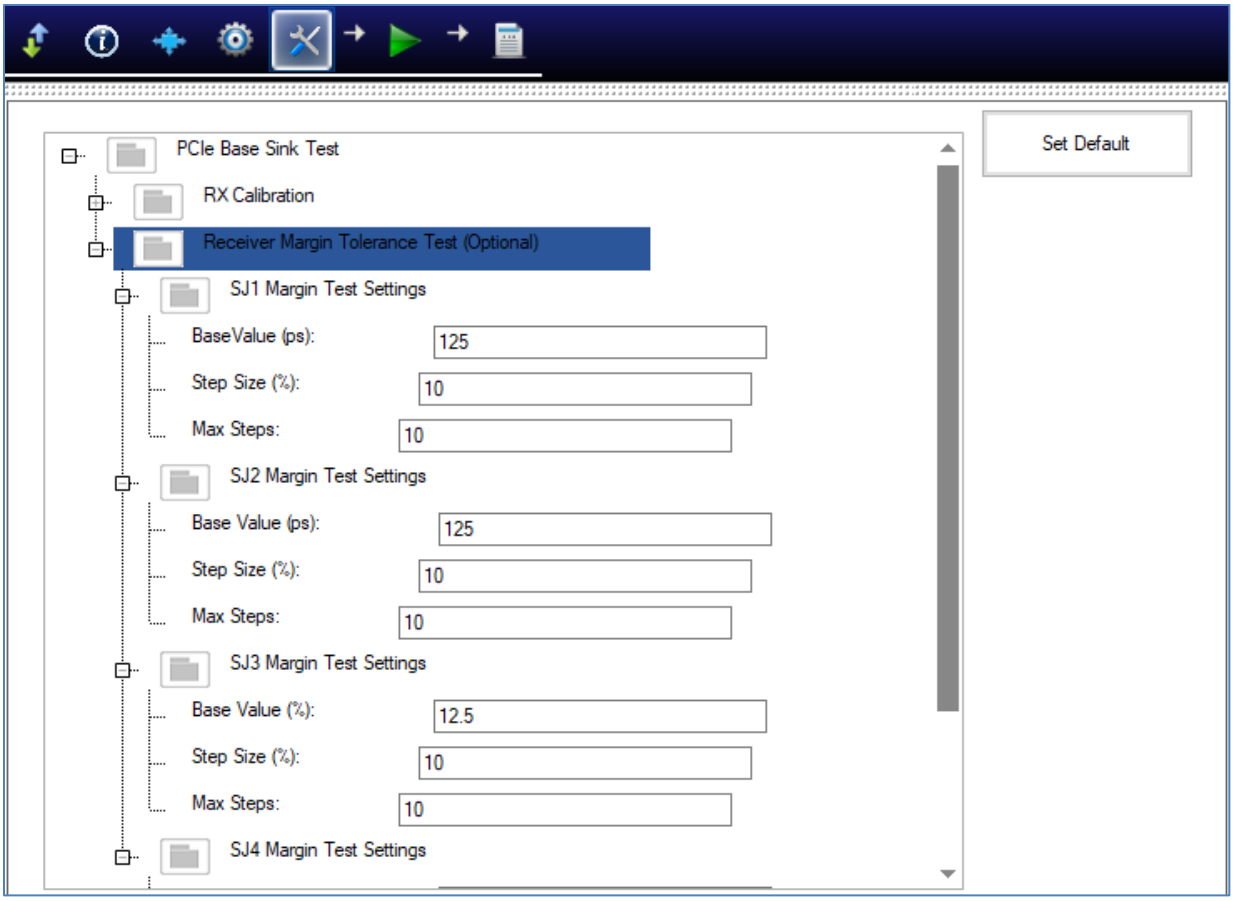


FIGURE 43. MARGIN TEST CONFIGURATION PAGE

TABLE 5. TEST PARAMETERS DESCRIPTION

Parameter	Description
SJ# Margin Test Settings – Base Value (ps)	Set the duration in picoseconds for running margin search tests for each respective SJ margin.
SJ# Margin Test Settings – Step Size (%)	Set the step size in percentage for stepping through each respective SJ margin when running margin search tests.
SJ# Margin Test Settings – Max Steps	Set the maximum number of steps for stepping through each respective SJ margin during margin search tests.

6.7 Enable Loopback BER Test

To set up the GRL software to automate loopback testing for error detection, go to the Configurations page and set up the following settings. *Make sure that the Rx DUT is capable of supporting loopback mechanism for BER measurements.*

1. Under the Error Counter tab, select 'LoopBack' to enable loopback test mode for the DUT.

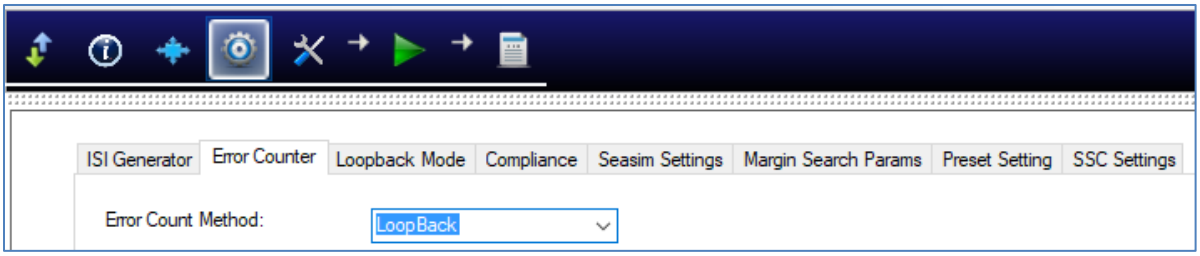


FIGURE 44. SELECT BER LOOPBACK TEST METHOD

2. Under the LoopBack Mode tab, select 'Clock Recovery' in the Clock Recovery Method field to apply the clock data recovery function to process the modified compliance pattern generated by the DUT.

   If using a user-defined pattern instead of the default test pattern for error checking, select the 'Custom Pattern for Error Detector' checkbox. Then, select a supported custom test pattern from the ED Pattern drop down field to be used.

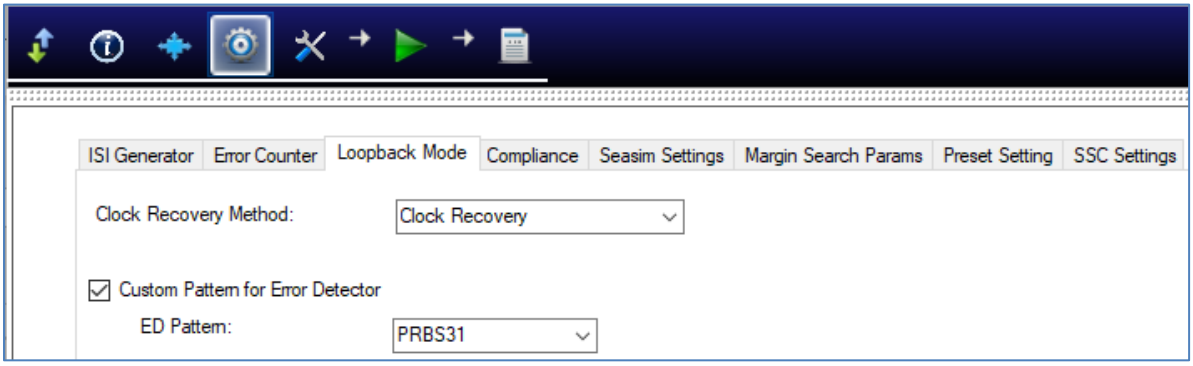


FIGURE 45. SET UP LOOPBACK TEST

3. If necessary to change the default spec-defined limits for the target BER and maximum error allowed for BER measurements, then select the Compliance tab and enter new values.

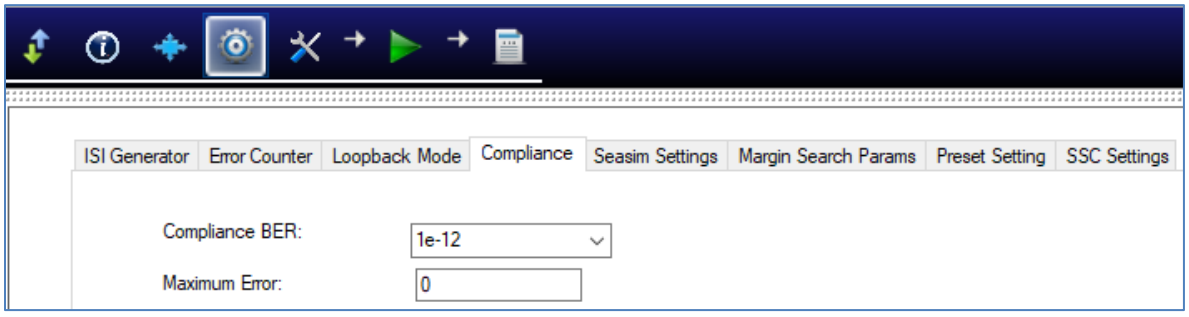


FIGURE 46. SET BER/ERROR LIMITS

6.8 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run for the DUT.

Select  from the menu to access the Run Tests page. The GRL-PCIE4-BASE-RXA software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

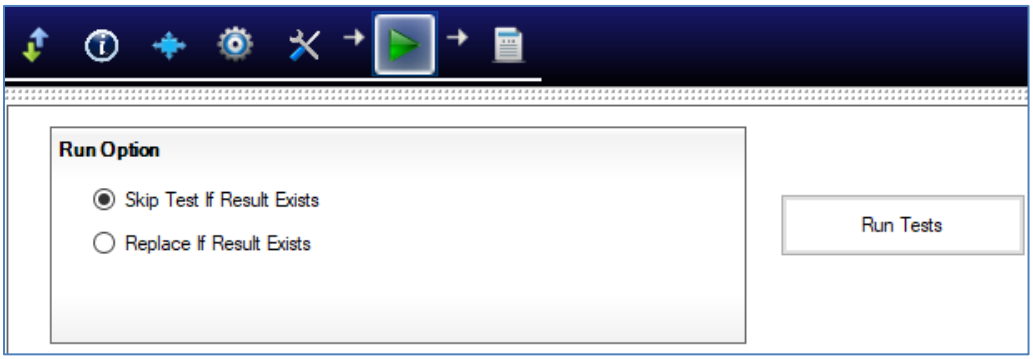


FIGURE 47. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed. Below shows an example of the connection diagram pop-up for the Rx DUT compliance test.

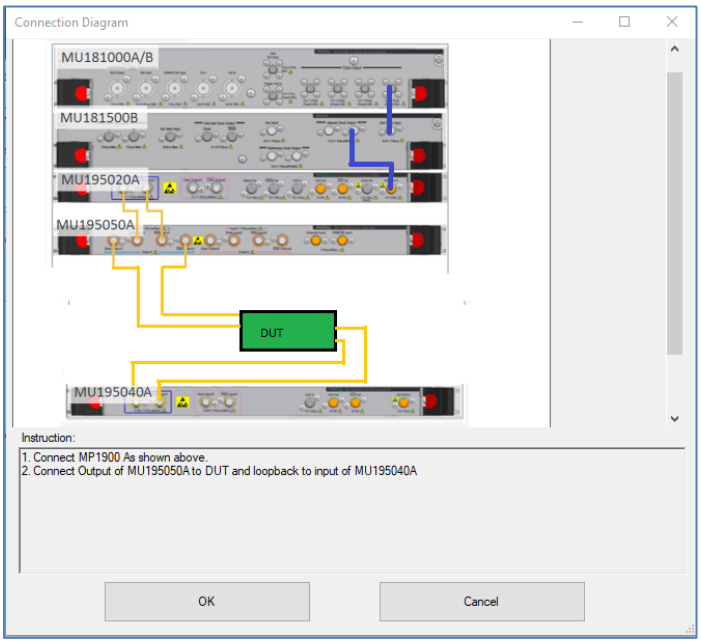


FIGURE 48. EXAMPLE CONNECTION POP-UP DIAGRAM FOR RX COMPLIANCE TEST

7 Interpreting GRL-PCIE4-BASE-RXA Test Report

When all calibration and test runs have completed from the previous section, the GRL-PCIE4-BASE-RXA software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

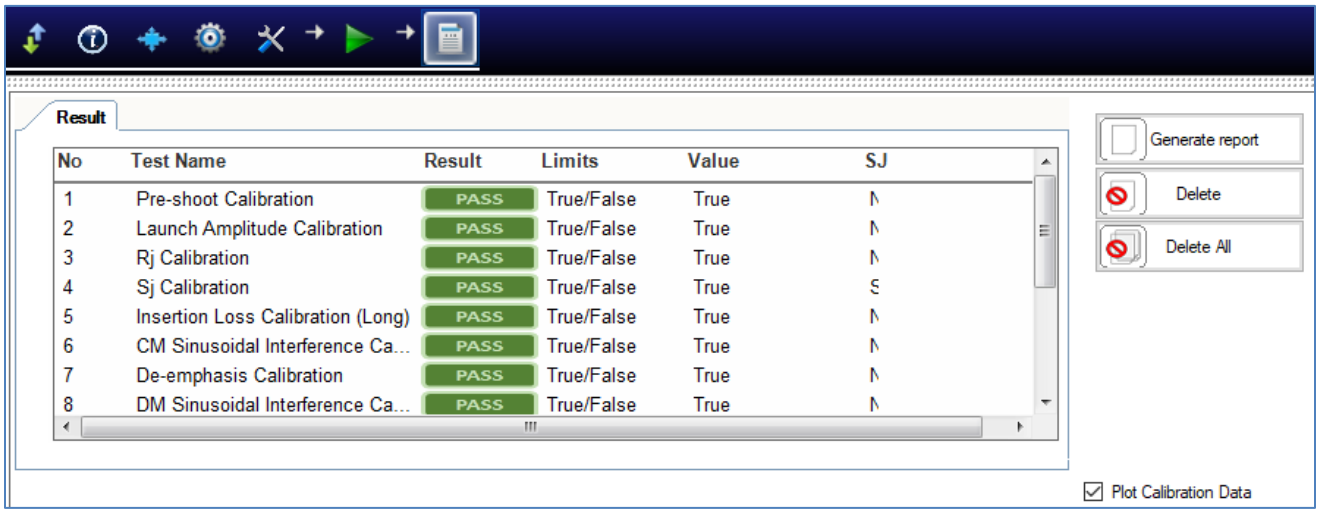


FIGURE 49. TEST REPORT PAGE

7.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

7.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.

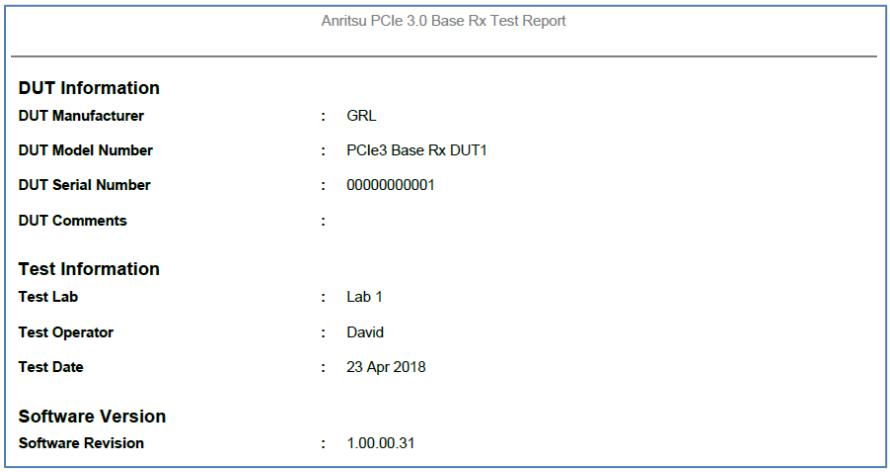


FIGURE 50. TEST SESSION INFORMATION EXAMPLE

7.1.2 Test Summary Table

This table provides an overall view of all the calibration and tests performed along with their conditions and results.

No	TestName	Limits	Value	Results	SJ
1	Pre-shoot Calibration	True/False	True	Pass	
2	De-emphasis Calibration	True/False	True	Pass	
3	Launch Amplitude Calibration	True/False	True	Pass	
4	Rj Calibration	True/False	True	Pass	
5	Sj Calibration	True/False	True	Pass	SJLF_1
6	Sj Calibration	True/False	True	Pass	SJLF_2
7	Sj Calibration	True/False	True	Pass	SJLF_3
8	Insertion Loss Calibration	True/False	True	Pass	
9	DM Sinusoidal Interference Calibration	True/False	True	Pass	
10	CM Sinusoidal Interference Calibration	True/False	True	Pass	
11	StressVoltage Calibration	True/False	True	Pass	
12	Insertion Loss Calibration (Short)	True/False	True	Pass	
13	CM Sinusoidal Interference Calibration (Short)	True/False	True	Pass	
14	DM Sinusoidal Interference Calibration (Short)	True/False	True	Pass	
15	Stressed Voltage Calibration (Short)	True/False	True	Pass	
16	Insertion Loss Calibration (Long)	True/False	True	Pass	
17	CM Sinusoidal Interference Calibration (Long)	True/False	True	Pass	
18	DM Sinusoidal Interference Calibration (Long)	True/False	True	Pass	
19	Stressed Voltage Calibration (Long)	True/False	True	Pass	
20	Stress Jitter Calibration (Long)	True/False	True	Pass	

FIGURE 51. TEST SUMMARY TABLE EXAMPLE

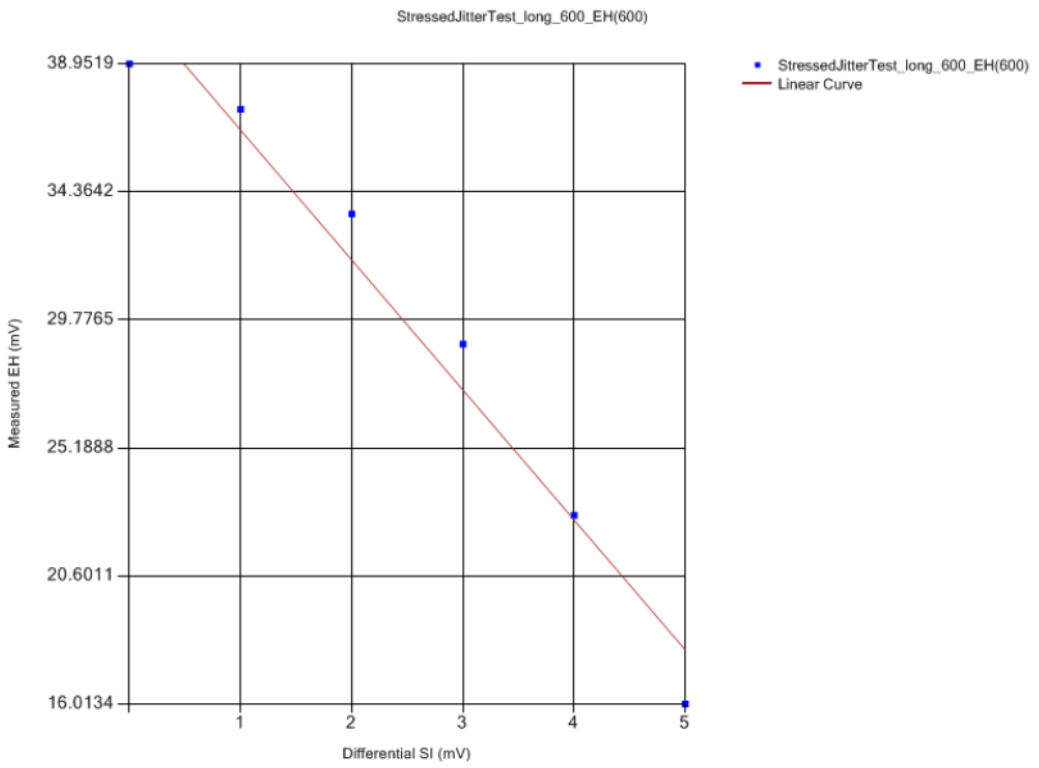
7.1.3 Test Results

This portion displays the results in detail along with supporting data points and screenshots for each calibration/test run.

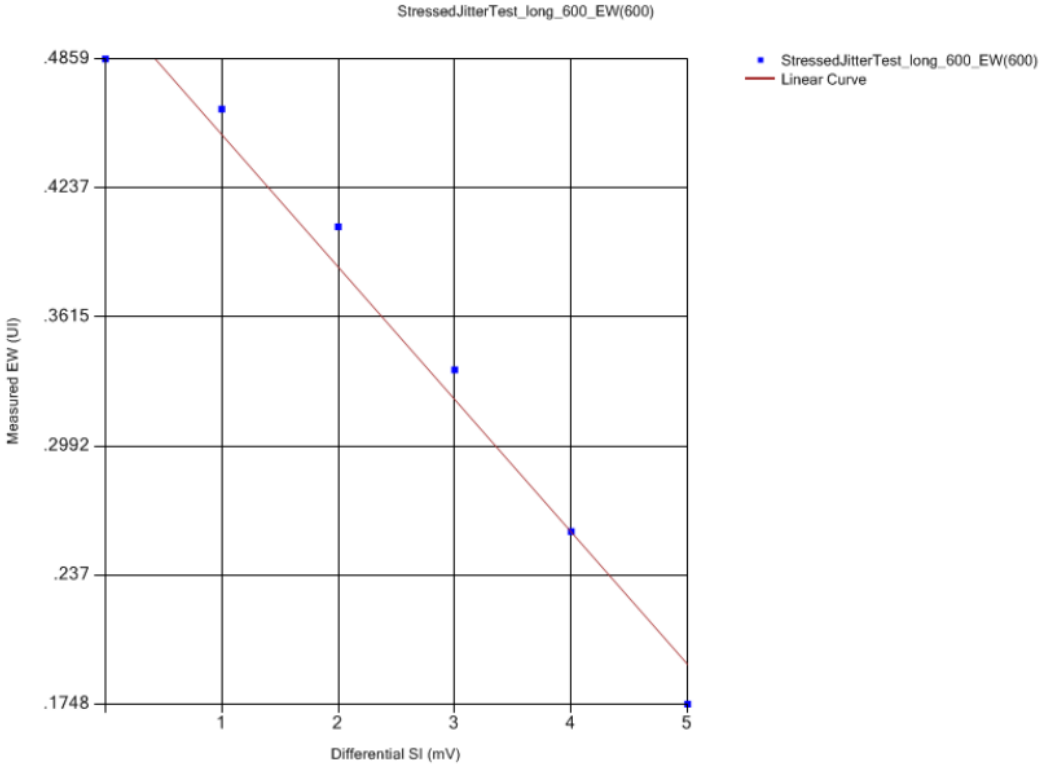
20. Stress Jitter Calibration (Long)

Pass/Fail Stats	:	Pass
Test Limits	:	True/False
Result	:	True
ISI Generator Type:	:	Artek
Level (V)	:	0.6
SJ (UI)	:	0.1
RJ (ps)	:	3.31723192004739
Test completed time	:	27 February 2018 23:46:17 PM

StressedJitterTest_long_600_EH(600) Plot



StressedJitterTest_long_600_EW(600) Plot



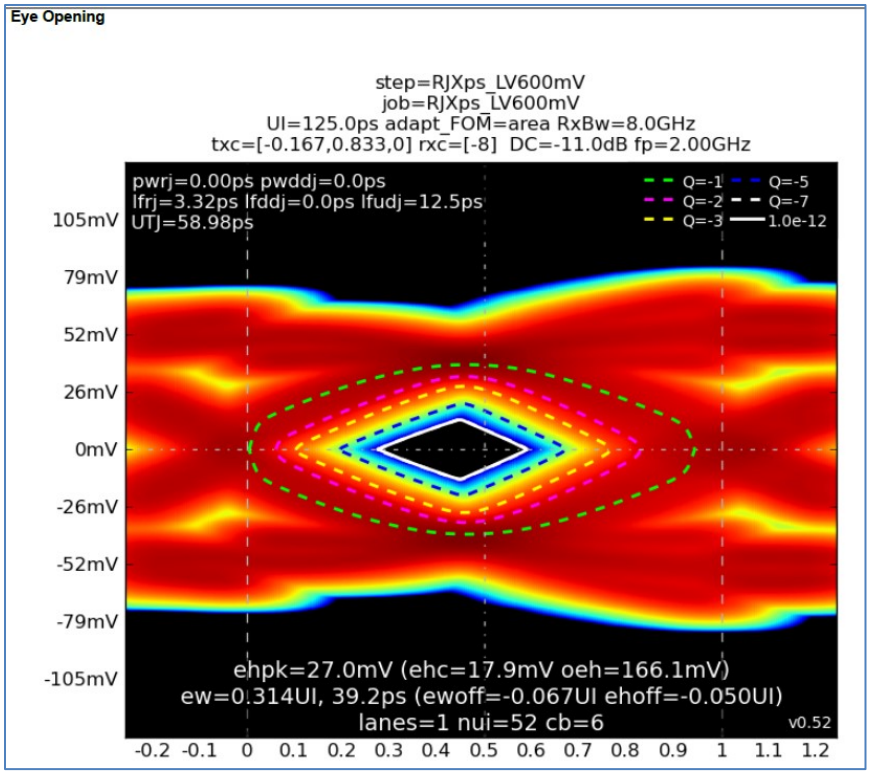


FIGURE 52. TEST RESULTS EXAMPLE

7.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

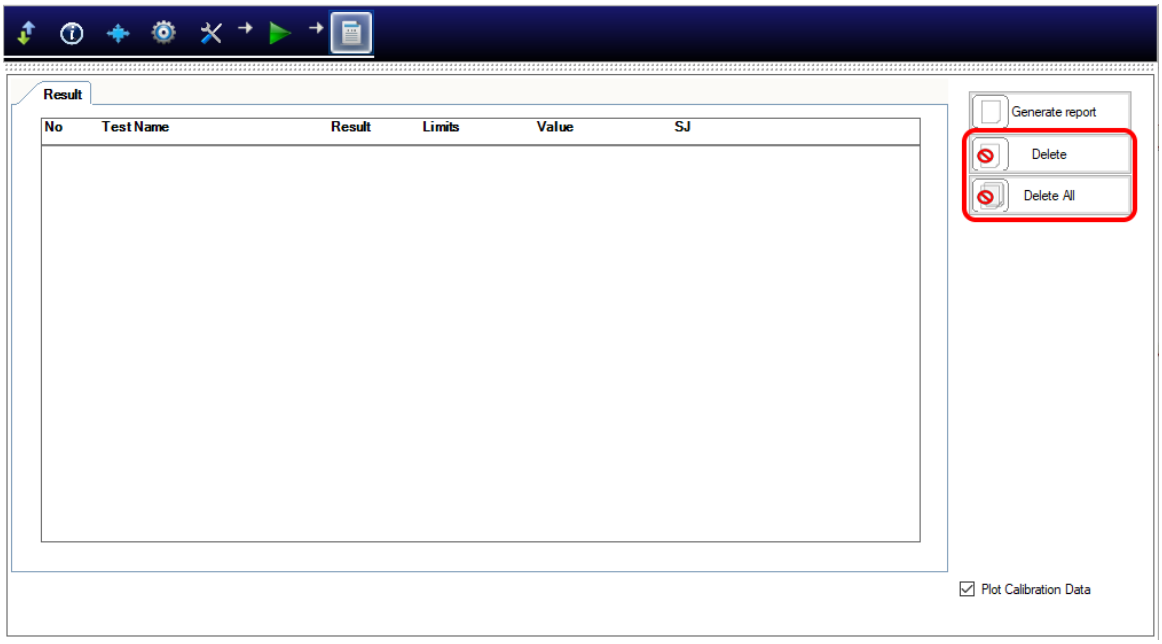


FIGURE 53. DELETE TEST RESULTS

8 Saving and Loading GRL-PCIE4-BASE-RXA Test Sessions

The usage model for the GRL-PCIE4-BASE-RXA software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To ***create a new test session*** and return the application back to the default configuration, select Options → 'New Session'.

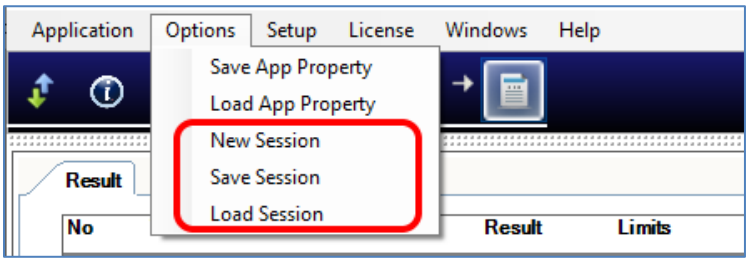


FIGURE 54. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

9 Appendix A: Method of Implementation (MOI) Using Automation

This section provides sample methodology to automate PCIe Gen 3 Base Rx calibration using GRL-PCIE4-BASE-RXA software at 8 GT/s. This procedure will ensure Receiver Impairment adjustments on the BERT are accurate before running DUT compliance tests.

9.1 Perform Calibration at TP1

9.1.1 Pre-shoot Calibration

Pre-shoot is calibrated for target dB of 3.5 for each preset for different trace lengths of the breakout board. The Caltable method is used to calibrate pre-shoot:

1. Set 800 mV (p-p) amplitude on BERT.
2. Disable all stresses (RJ, SJ, etc.)
3. Set 0 dB for De-emphasis.
4. Measure:

   1 dB, then measure pre-shoot, record
   2 dB, measure again, record
   …..
   4 dB, measure again, record.

5. Plot a Caltable graph.
6. Passing criteria is to obtain measured pre-shoot at 3.5 dB.

9.1.2 De-emphasis Calibration

De-emphasis is calibrated for target dB of -6.0 for each preset for different trace lengths of the breakout board. The Caltable method is used to calibrate de-emphasis:

1. Set 800 mV (p-p) amplitude on BERT.
2. Disable all stresses (RJ, SJ, etc.)
3. Set 0 dB for Pre-shoot.
4. Measure:

   -8 dB, then measure de-emphasis, record
   -7 dB, measure again, record
   -6 dB, measure again, record
   …..
   0 dB.

5. Plot a Caltable graph.
6. Passing criteria is to obtain measured de-emphasis at -6 dB.

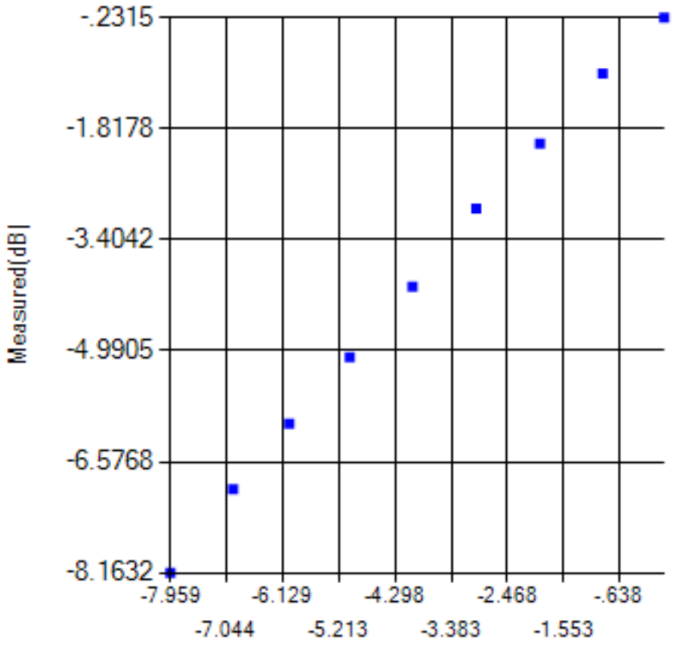


FIGURE 55. DE-EMPHASIS CALIBRATION CALTABLE GRAPH

9.1.3 Launch Amplitude Calibration

Launch amplitude is calibrated for target minimum peak-to-peak amplitude of 800 mVpp. The Caltable method is used to calibrate launch amplitude:

1. Initialize BERT.
2. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
3. Set 300 mV Amplitude on BERT, then measure the amplitude in scope, record it.
4. Increase 100 mV on each iteration, measure the amplitude on scope, until measured amplitude meets or exceeds 1300 mV.
5. Plot a Caltable graph.
6. Passing criteria is to obtain MEAN value of amplitude measurement at 800 mV.

9.1.4 RJ Calibration

Random jitter (RJ) is calibrated for target value of 2 to max 3 ps (RMS). The Caltable method is used to calibrate RJ:

1. Initialize BERT.
2. Set 800 mV (p-p) amplitude (based on calibrated value).
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set all stresses to 0 mV.
5. Set Clock Pattern 1100 on BERT.
6. Set Initial RJ value to 0.04 UI(p-p) on BERT.
7. Measure RJ (in ps (RMS)) from scope using EZJIT, record the measured value.
8. Increase 0.1 UI (p-p) on each iteration, measure RJ from scope, until measured RJ meets or exceeds 3 ps (RMS).
9. Plot a Caltable graph.
10. Passing criteria is to obtain measured RJ at Min 2 ps (RMS) and Max 3 ps (RMS).

9.1.5 SJ Calibration

Sinusoidal Jitter (SJ) is calibrated (with Clock pattern 1100) for four SJ frequencies: 30 kHz, 1 MHz, 10 MHz and 100 MHz.

Stressed Voltage Test:

$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.

Stressed Jitter Test:

$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.

The Stressed Jitter test requires the test to pass each and every frequency, with its respective SJ amplitude at 30 kHz, 1 MHz, 10 MHz, and 100 MHz.

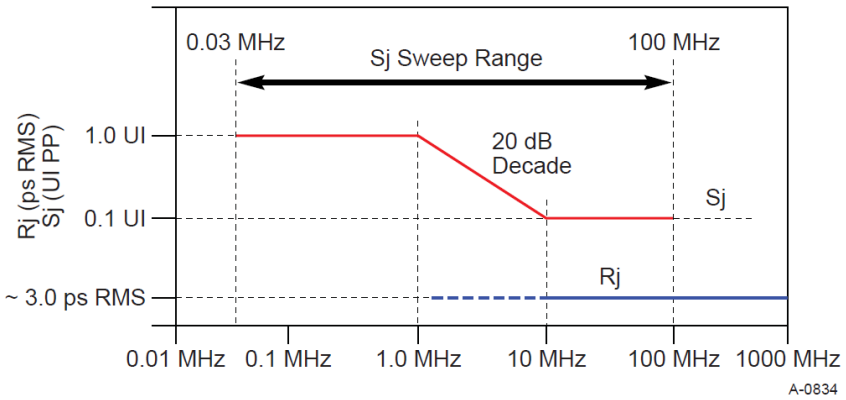


Figure 4-74: Swept Sj Mask

FIGURE 56. SWEEP JITTER RANGE AND MASK

The Caltable method is used to calibrate SJ:

1. Initialize BERT.
2. Set 800 mV (p-p) amplitude (based on calibrated value).
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set all stresses to 0 mV.
5. Set Clock Pattern 1100 on BERT.
6. Set the SJ Frequency of the first Permutation (30 kHz, 1 MHz, 10 MHz, 100 MHz).
7. Set 0 (%UI (p-p)) as base value in SJ, measure SJ (in ps (p-p)) from scope using EJZIT, record.
8. Increase 0.1 UI (p-p) on each iteration for SJ Frequency 1 MHz, 10 MHz, 100 MHz; Increase 0.2 UI (p-p) on each iteration for SJ Frequency 30 kHz.
9. Measure SJ from scope until measured SJ meets or exceeds 62.5 ps for 30 kHz SJ Frequency or 20.0 ps for SJ Frequency 100 kHz, 1 MHz, 100 MHz.
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 6 ps (p-p) and Max 62.5 ps (p-p) for 30 kHz, 20.0 ps (p-p) for 100 kHz, 1 MHz, 100 MHz.
12. Proceed to next permutation.

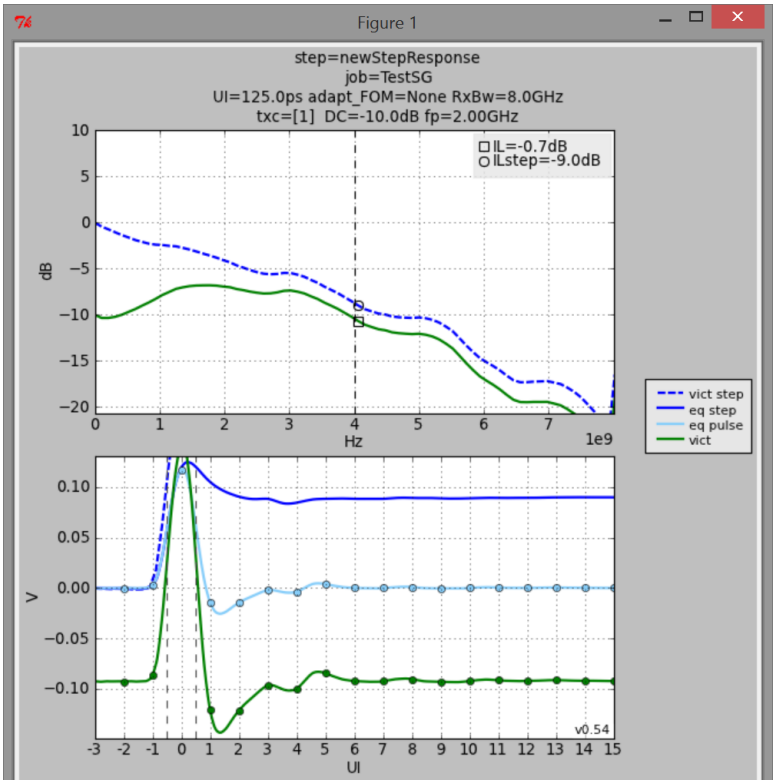
9.2 Perform Calibration at TP2

Calibration at TP2 is performed for the None, Short or Long breakout calibration channels.

9.2.1 Insertion Loss Calibration

1. Initialize BERT.
2. Set 800 mV (p-p) amplitude (based on calibrated value).
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set all stresses to 0 mV.
5. Set Clk/256 Pattern on BERT.
6. Set ISI % on Artek to 0.0 (if long, set 15%).
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (start from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain .log file and .csv file from Seasim.
13. Read insertion plot from .csv. Check against upper and lower limit of specifications.
14. Use GRL script to plot output of insertion loss curve with specifications.
15. If failed, loop, increase 1% on Artek. Repeat insertion loss measurement.
16. Passing criteria is to ensure that 60% of the curve is within the upper and lower limits for the respective channel type.

Below shows a sample graph output by Seasim indicating insertion loss of -9dB at 4 GHz.



9.2.1.1 Example Insertion Loss Results

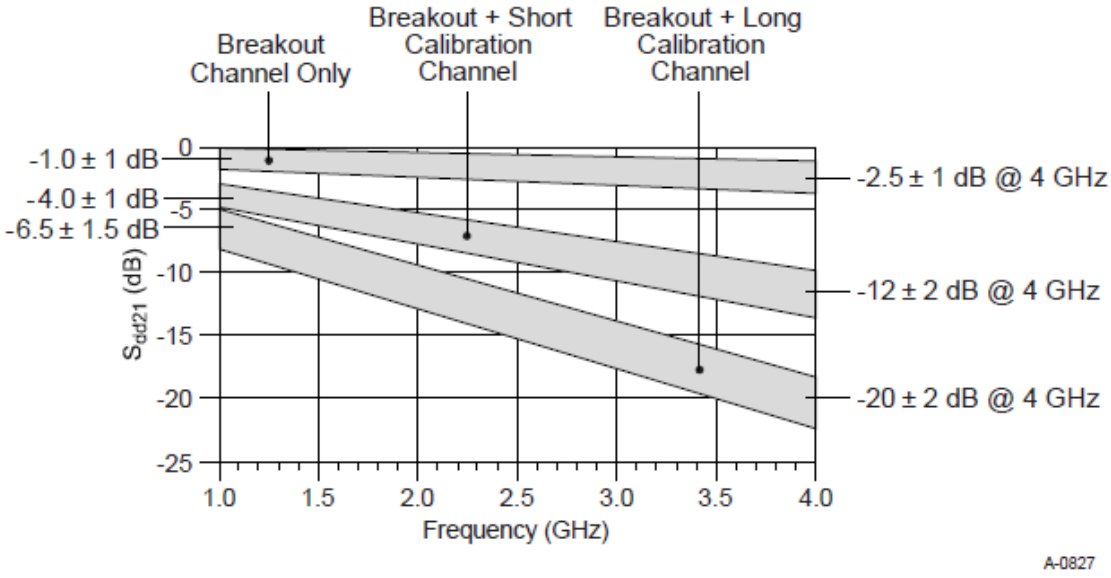


Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels

FIGURE 57. SPECIFICATION MASK

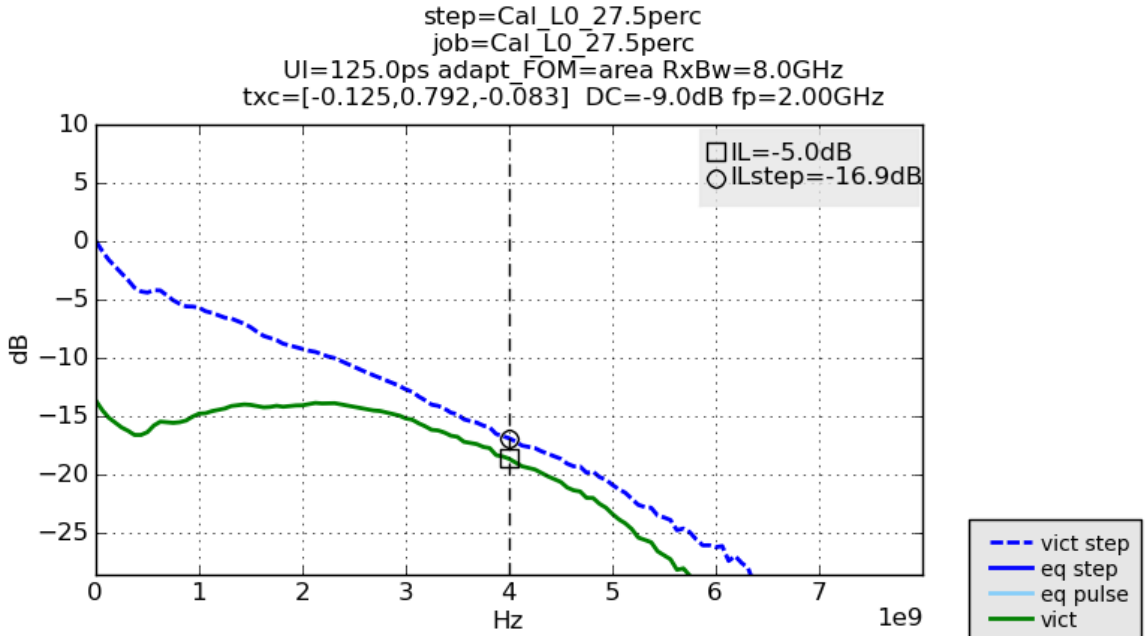


FIGURE 58. INSERTION LOSS AT 27.5% ISI (-16.9 DB)

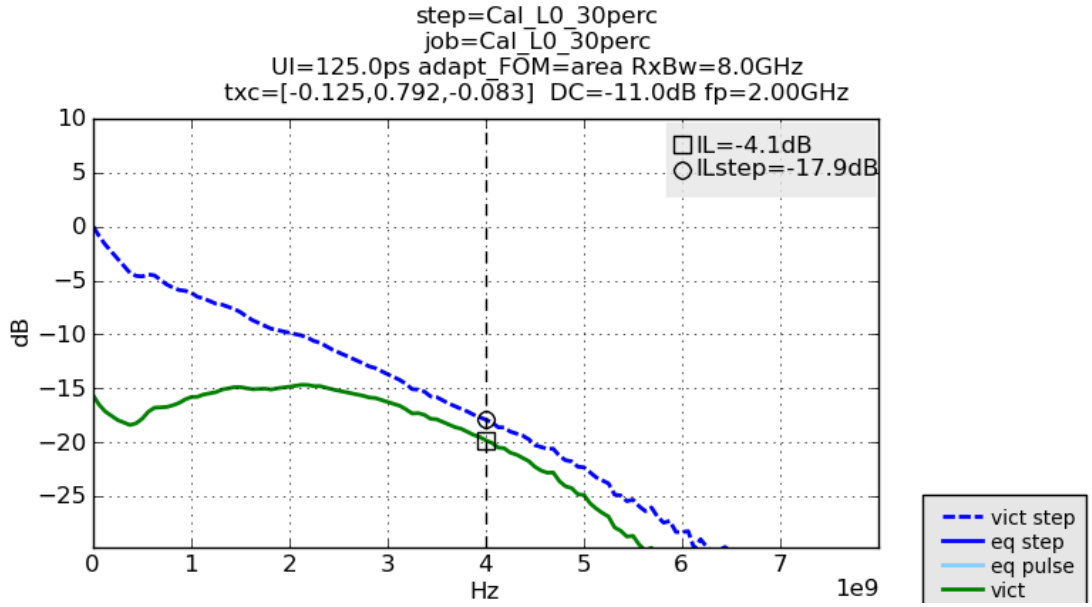


FIGURE 59. INSERTION LOSS AT 30% ISI (-17.9 DB)

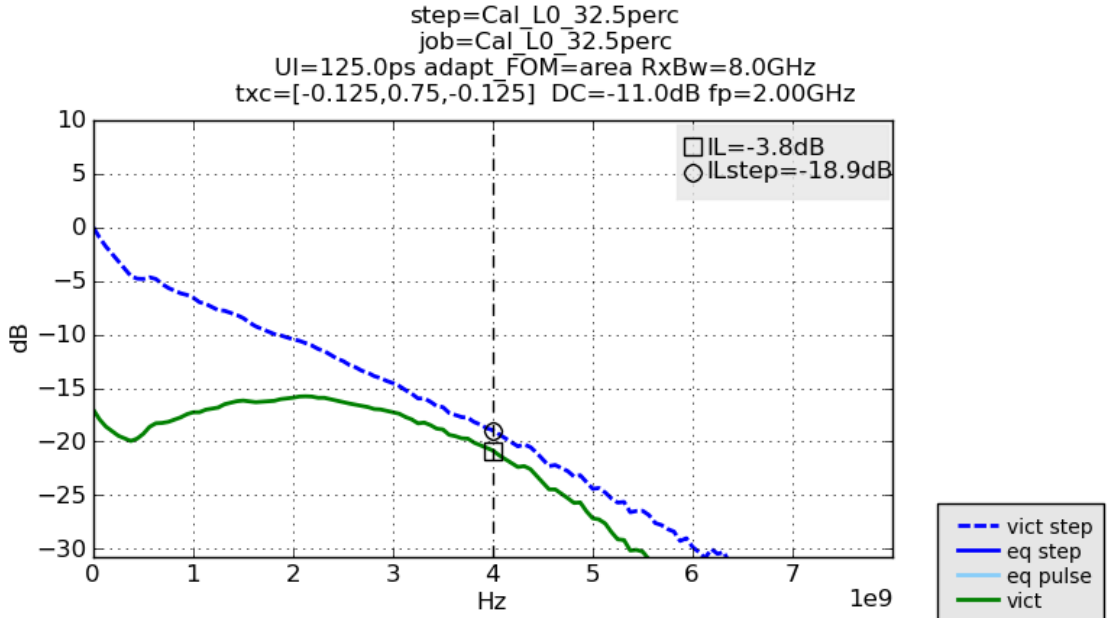


FIGURE 60. INSERTION LOSS AT 32.5% ISI (-18.9 DB) WITHIN TARGET

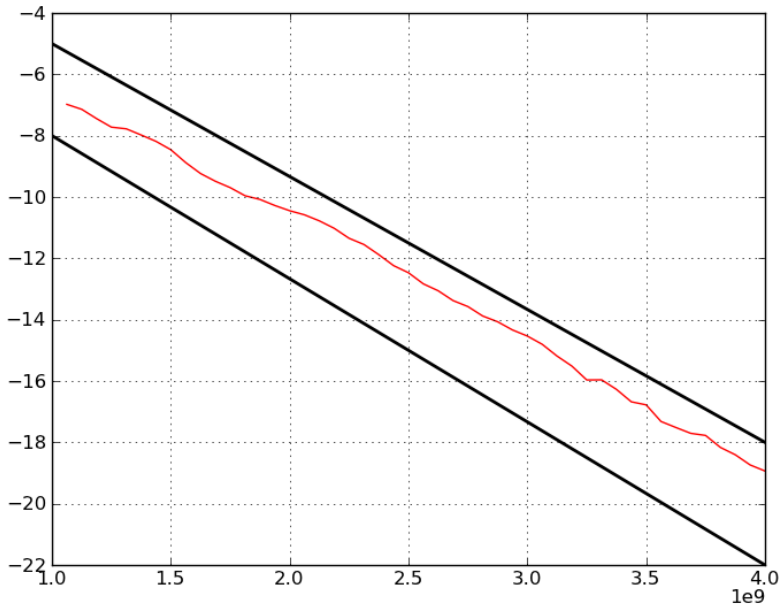


FIGURE 61. INSERTION LOSS CALIBRATION FOR LONG CHANNEL – IL FALLS BETWEEN REQUIRED MASK

9.2.2 AC Common Mode (CM) Sinusoidal Interference Calibration

The Caltable method is used to calibrate CM-SI:

1. Initialize BERT.
2. Set 0 mV (p-p) amplitude.
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set all stresses to 0 mV.
5. Set Frequency for Common Mode to 120 MHz.
6. Set Output for Common Mode to 7 dBm, turn On Output.
7. Turn Off Output for Differential Mode.
8. Initialize scope.
9. Set up Func1 on scope to (Chan1 + Chan2)/2.
10. Measure Vp-p on Func1.
11. Increase Phase for Common Mode by 10%, measure Vp-p on scope until Max value.
12. Record measured Phase.
13. Set 800 mV (p-p) amplitude (based on calibrated value).
14. Set All Zero Pattern on BERT.
15. Set ISI % value based on above calibrated data.
16. Set Common Mode to Sine Wave.
17. Set -5 dBm as base value.
18. Measure Amplitude (in mV) from scope, record.
19. Increase 0.174 dBm on each iteration, measure Amplitude from scope until measured value meets 150 mV (for Long Channel).
20. Plot a Caltable graph.
21. Passing criteria is to obtain measured CM-SI at 150 mV for Long Channel or 250 mV for Short and None Channel.

9.2.3 Differential Mode (DM) Sinusoidal Interference Calibration

This calibration ensures that the waveform achieves the calibrated eye height. The Caltable method is used to calibrate DM-SI:

1. Initialize BERT.
2. Set 0 mV (p-p) amplitude.
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set all stresses to 0 mV.
5. Set Frequency for Differential Mode to 2.1 GHz.
6. Set Output for Differential Mode to 7 dBm, turn On Output.
7. Turn Off Output for Common Mode.
8. Initialize scope.
9. Set up Func1 on scope to (Chan1 – Chan3).
10. Measure Vp-p on Func1.
11. Increase Phase for Differential Mode by 10%, measure Vp-p on scope until Max value.
12. Record measured Phase.
13. Set 800 mV (p-p) amplitude (based on calibrated value).
14. Set All Zero Pattern on BERT.
15. Set ISI % value based on above calibrated data.
16. Set 0.89 dBm as base value (Differential Mode).
17. Measure Amplitude (in mV) from scope, record.
18. Increase 0.174 dBm on each iteration, measure Amplitude from scope until measured value meets or exceeds 14 mV.
19. Plot a Caltable graph.
20. Passing criteria is to obtain measured DM-SI at 14 mVpp or greater.

9.3 Perform Calibration at TP2P

9.3.1 Stress Jitter Voltage Eye Calibration

This calibration verifies that the waveform achieves the calibrated eye width and eye height. Seasim is used to post process the receiver eye at TP2P, where RJ, SJ, and DM-SI sources are input to Seasim while CM-SI is combined with clk/256 pattern source from BERT and captured in scope.

1. Initialize BERT.
2. Set 800 mV (p-p) amplitude (based on calibrated value).
3. Set to 0 dB Pre-shoot and De-emphasis obtained from Caltable as measured above (for the Short and None channels). Use “Preset 7” values for the Long channel.
4. Set all stresses to 0 mV.
5. Set Clk/256 Pattern on BERT.
6. Set Artek to calibrated ISI %.
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].

10. Create Seasim config file with predefined values for Eye Opening Calculation, starting with 0 mV DM-SI.
11. Run Seasim with config file and step response.
12. Obtain .log file from Seasim.
13. Read eye height (EH) and eye width (EW).
14. Record EH vs. DM, and EW vs. DM for 800 mV.
15. Increase DM-SI (in Seasim config) to 5 mV, run Seasim again, obtain EH and EW.
16. After obtained EH and EW from 0, 5, 10, 15, 20, 25 mV, plot Caltable graph.
17. If EH and EW do not fall within 0.3 UI and 25 mV (for Long Channel), increase SJ by 0.1 UI. Repeat method to obtain EH and EW by adjusting DM.
18. If EH and EW do not fall within 0.3 UI and 25 mV after SJ variation, adjust Amplitude and repeat method to obtain EH and EW.
19. Repeat until EH and EW fall within specs for each channel type.
20. Record measured Amplitude, SJ, and DM.

10 Appendix B: Artek CLE Model Series Installation

10.1 ISI Generator Driver Installation

If using a Artek CLE Model unit for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the Artek unit to the PC being used as the controller using a USB 2.0 cable.
2. Turn on the front panel power switch on the Artek unit.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for Artek has been installed, you will see a 'bang' in the Device Manager.

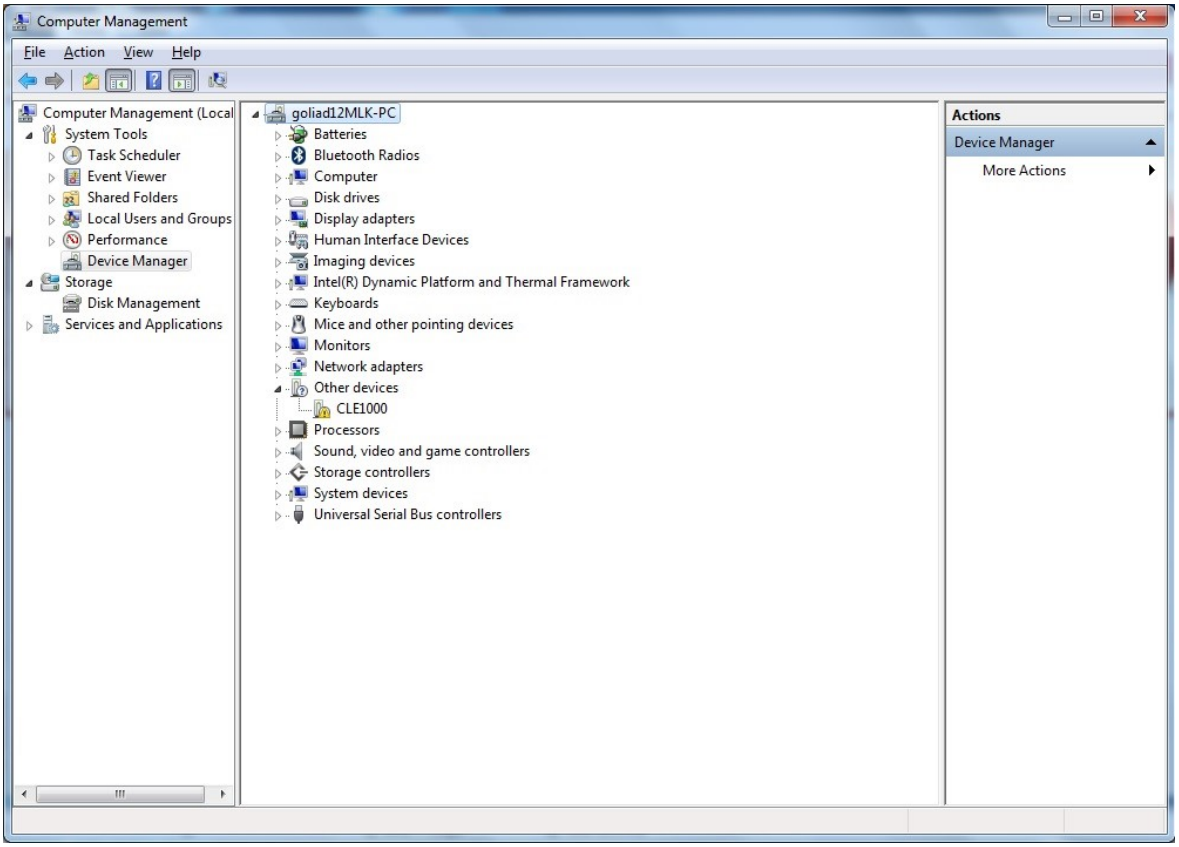


FIGURE 62. DEVICE MANAGER WINDOW

4. To install the Artek driver, go to http://www.aceunitech.com/support.html and download the Control Software package for the Artek CLE Series.
5. Unzip the CLE Series Software folder and install the driver as follows:

   a) In Device Manager, right-click on **CLExxxx > Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 63.
   c) Browse to the root directory of the unzipped CLE Series Software folder.
   d) Click **Next** and then click **Install** to complete installation for the driver software. See Figure 64.

   Once installation has completed, the Device Manager window should look like the example in Figure 65.

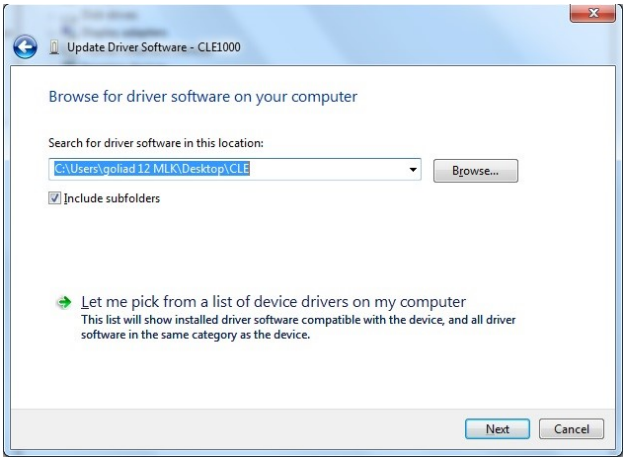


FIGURE 63. UPDATE DRIVER WINDOW

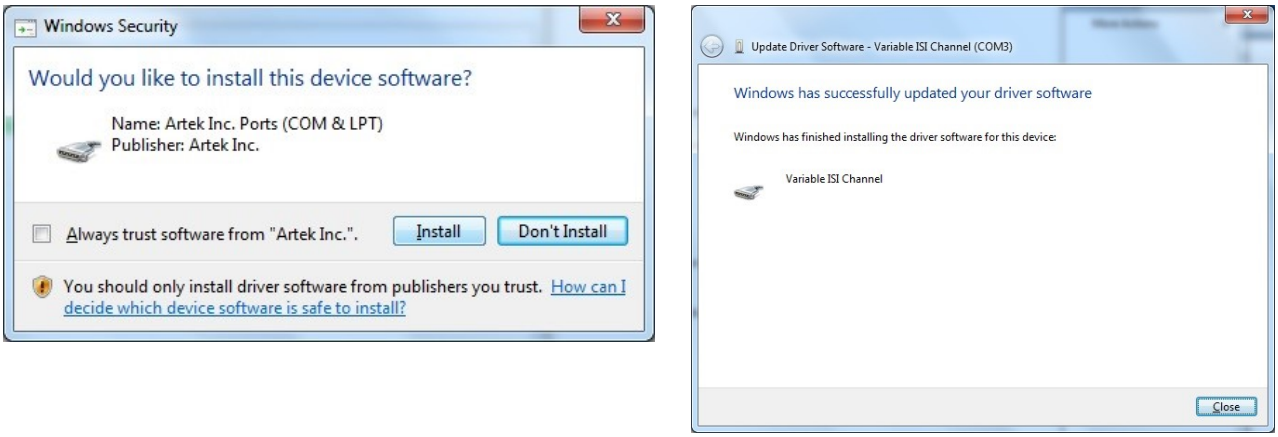


FIGURE 64. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

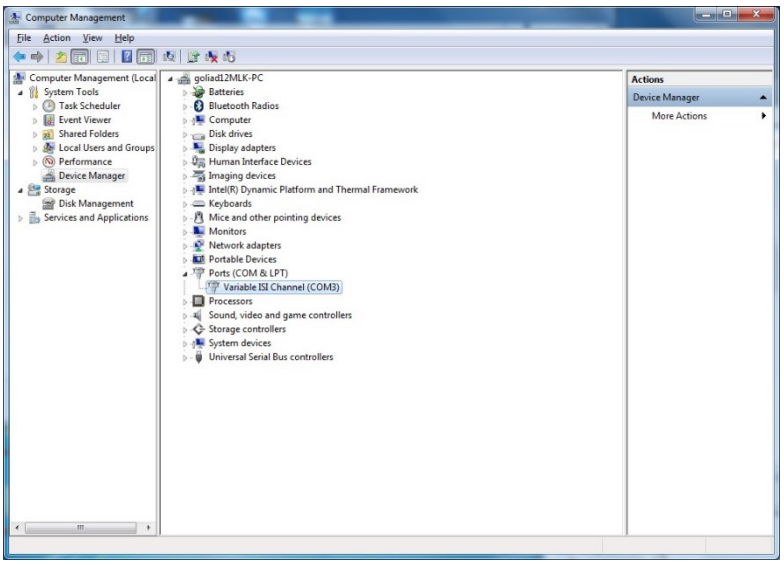


FIGURE 65. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE Series software driver is now installed and the Artek unit can now be selected for use remotely using the GRL software.

10.2 CLE Series User Interface (UI) Installation

It may also be useful to install the CLE Series UI, so that the ISI channel can also be controlled manually from the computer. To install the UI, follow these steps:

1. In the CLE Series Software folder, select and install the Setup.exe file. Upon successful installation, the following UI window will appear.
2. Close this window if manual control is not required.

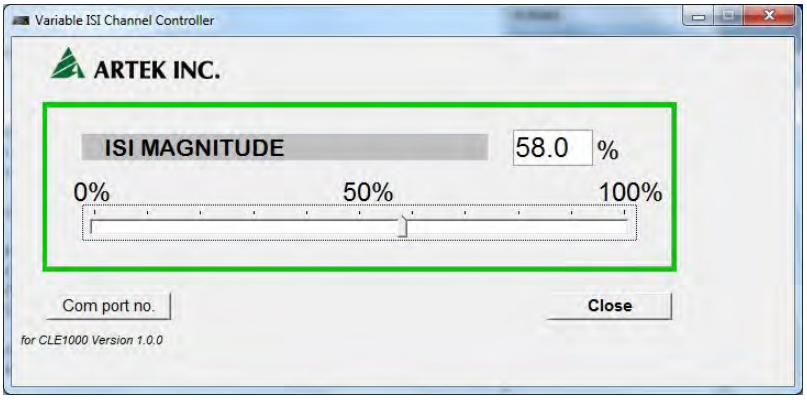


FIGURE 66. CLE SERIES UI

10.3 Return Loss Limitations of the Artek CLE1000-A2

If using the Artek CLE1000-A2 for Insertion Loss, it should be understood that the Return Loss Specifications of the CLE1000 does not meet the specific requirements of the PCI Express 3.0 Base Specification. The return loss of the CLE1000 varies with the % of ISI that is provided. The following two plots show the return loss of the CLE1000 at Channel lengths of 10% to 50%, which would be the typical range of a PCIe3 Calibrated Channel.

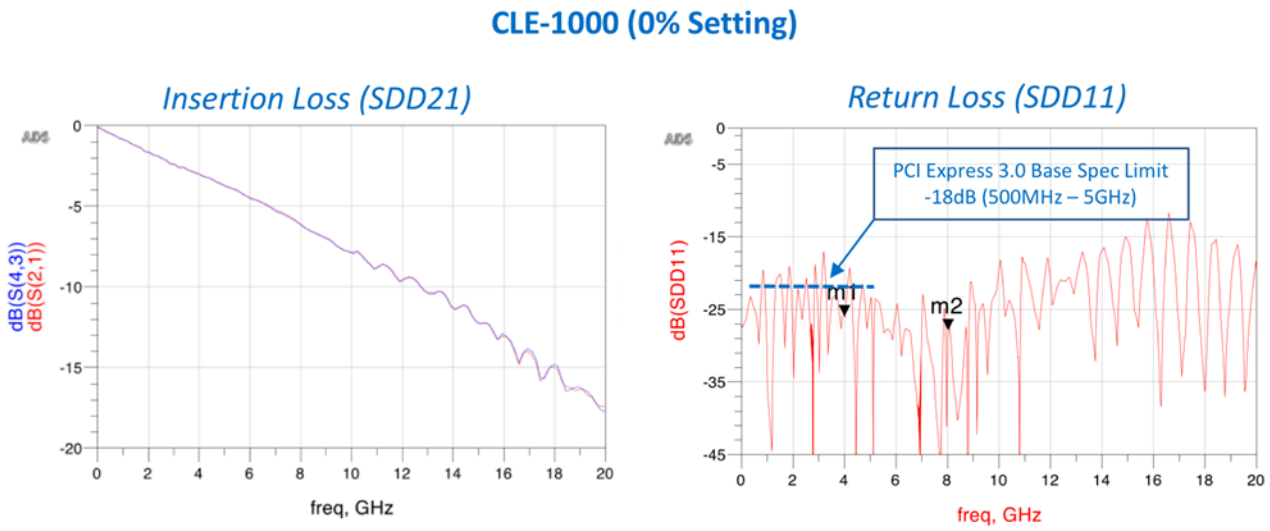


FIGURE 67. CLE1000-A2 VARIABLE ISI GENERATOR IL, RL AT 0% SETTING

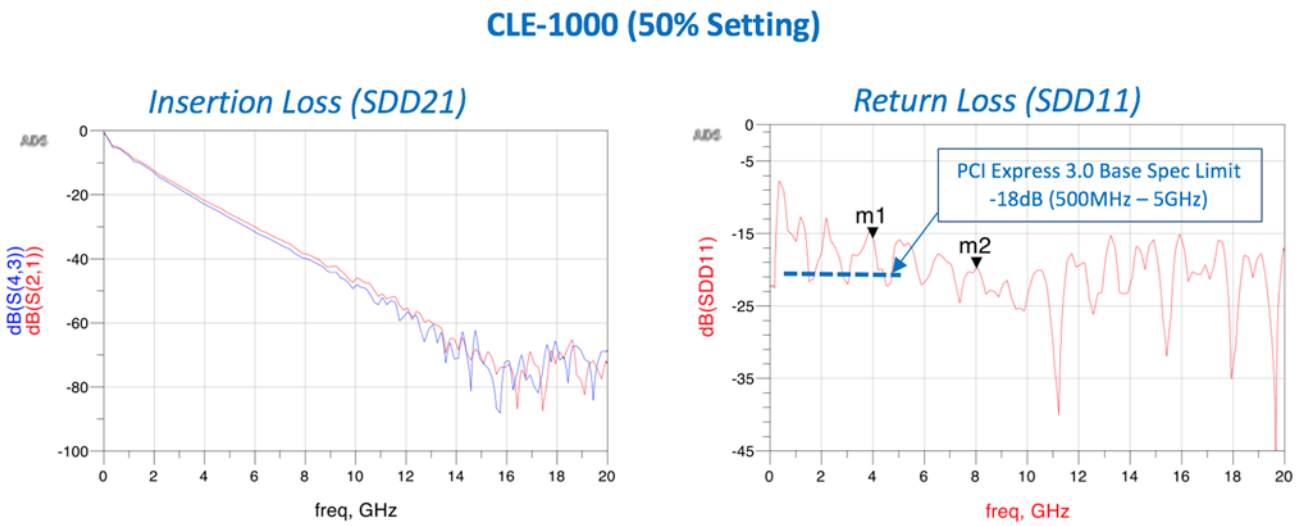


FIGURE 68. CLE1000-A2 VARIABLE ISI GENERATOR IL, RL AT 50% SETTING

11 Appendix C: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

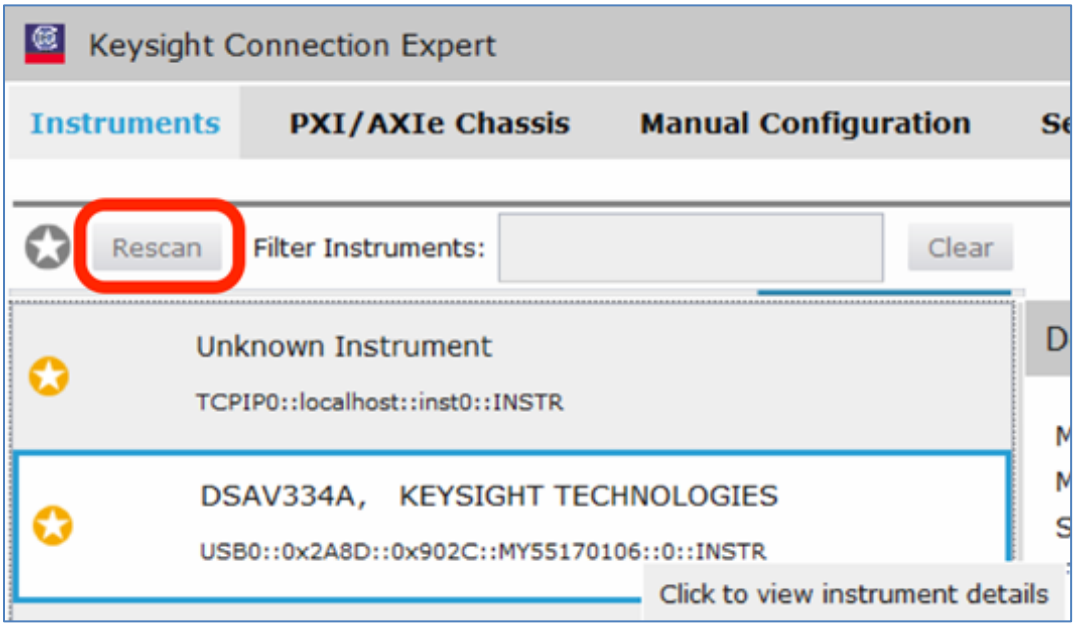


FIGURE 69. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

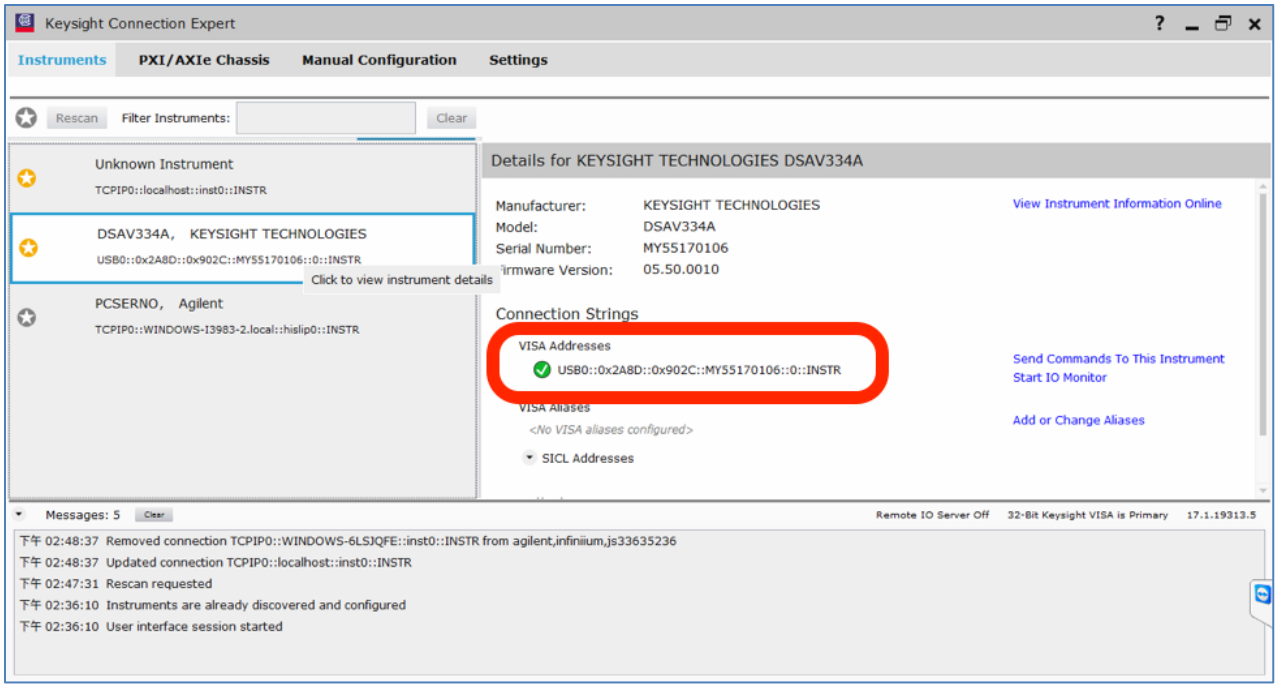


FIGURE 70. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe CEM 4.0 Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

   If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".

12 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

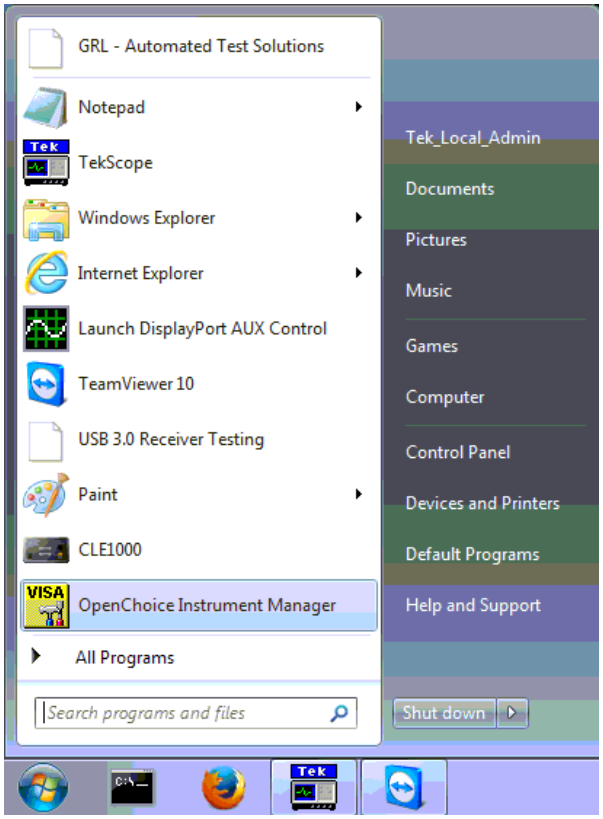


FIGURE 71. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

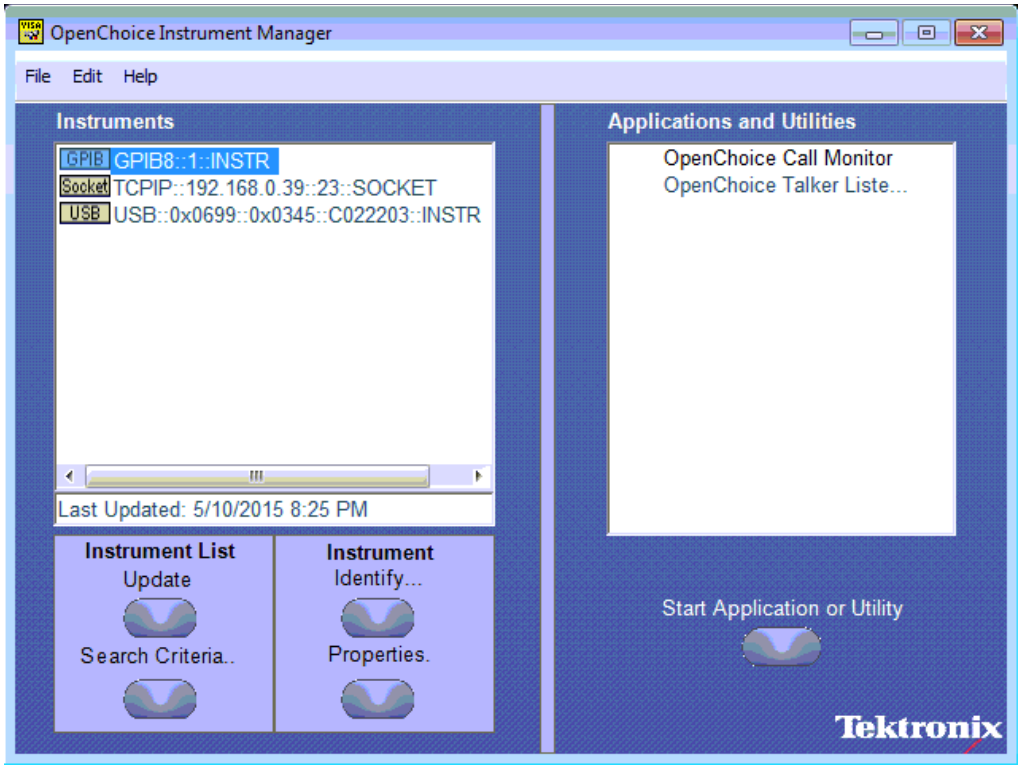


FIGURE 72. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe 3.0 Base Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe 3.0 Base Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

13 Appendix E: Scope and Cable De-skew

Before beginning any test or data acquisition, the oscilloscope must be warmed, calibrated, and cables de-skewed. This section describes the procedure for calibrating the Oscilloscope, and de-skewing the cables.

The DSO/DSA and DSAX/DSOX series Oscilloscopes must be calibrated manually, and this is recommended after a 30- to 60-minute warm-up period.

FIGURE 73. SCOPE DESKEW SETUP

Perform the following steps, with reference to Figure 77.

1. Select the **File → Open → Setup...** menu to open the **Open Setup File** window.
2. Navigate to the directory location that contains the deskew setup file (.set).
3. Select the deskew setup file by clicking on it.
4. Click the **Open** button to configure the oscilloscope from this setup file.

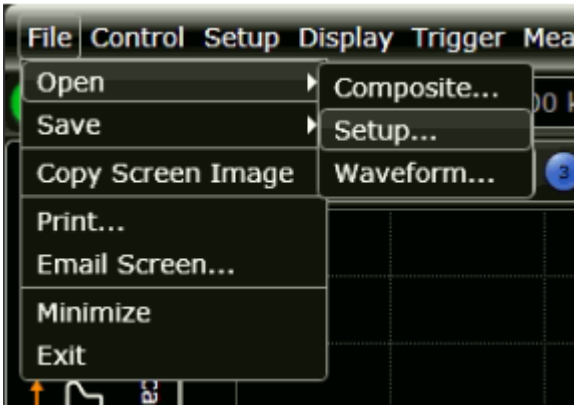


FIGURE 74. OPEN SCOPE DE-SKEW SETUP FILE WINDOW

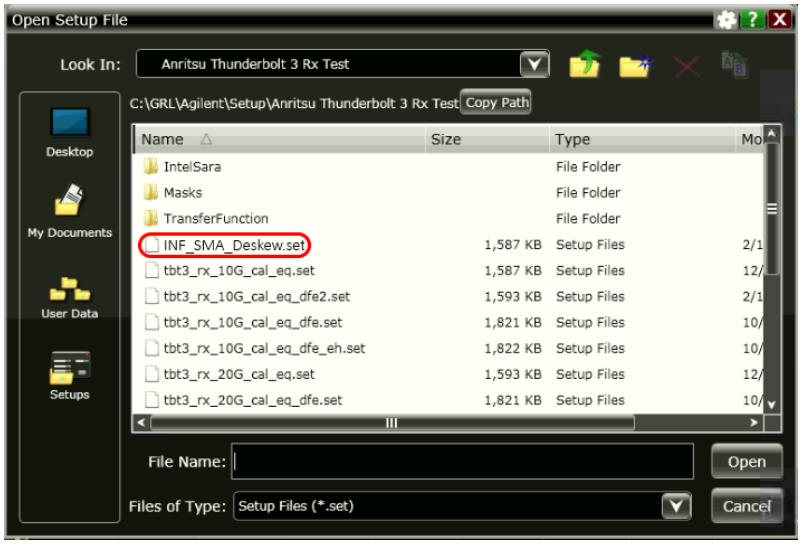


FIGURE 75. SCOPE DE-SKEW SETUP FILE EXAMPLE

An example of the oscilloscope display is shown in Figure 76. A rising edge of the square wave is shown in a 100ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (blue trace) superimposed on one another. The lower portion of the screen is the differential signal (white trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure below is an example of exaggerated skew between channel 1 and channel 3.

FIGURE 76. SCOPE DE-SKEW OSCILLOSCOPE DISPLAY

Figure 77 shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace) and channel 3 (blue trace) traces overlap, and the differential signal (white trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

FIGURE 77. SCOPE DE-SKEW OSCILLOSCOPE DISPLAY DE-SKEWED

Referring to Figure 78 and Figure 79, perform the following steps to de-skew the channels:

5. Click on the **Setup → Channel 1…** menu to open the **Channel** window.
6. Move the **Channel** window to the left so you can see the traces.
7. Adjust the **Skew** by clicking on the ← or → arrows, to achieve the flattest response on the differential signal (white trace).
8. Close the Channel window.
9. The de-skew operation is now complete.
10. Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

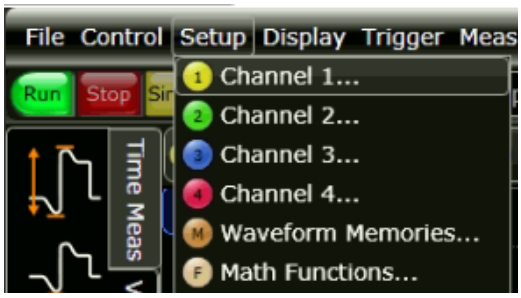


FIGURE 78. SCOPE DE-SKEW PROCESS – OPEN CHANNEL WINDOW

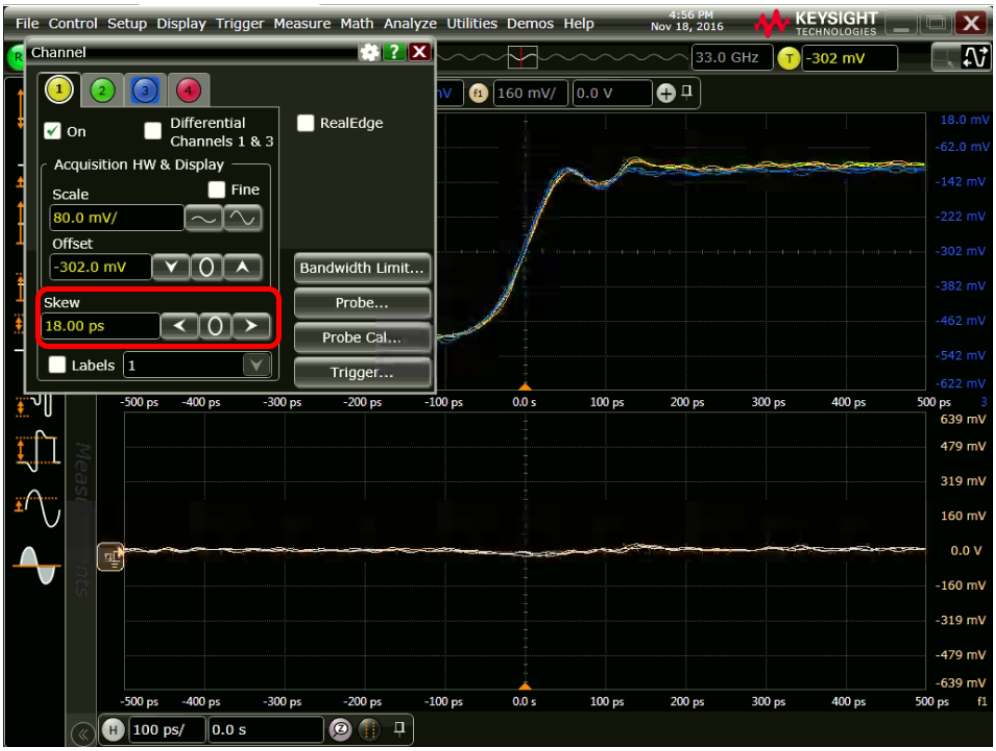


FIGURE 79. SCOPE DE-SKEW PROCESS – ADJUST SKEW

END_OF_DOCUMENT