Granite River Labs

PCI Express® 4.0 Base Specification (16 GT/s)

Receiver Test Method of Implementation (MOI)

for Tektronix BSX Series BERTScope and Real Time Oscilloscope

Using GRL-BSXPCI4BSE Receiver Calibration and Test Automation Software

All product names are trademarks, registered trademarks, or service marks of their respective owners.

The GRL disclaims all warranties and liability for the use of this document and the information contained herein and assumes no responsibility for any errors that may appear in this document, nor does the GRL make a commitment to update the information contained herein.

Contact the GRL office to obtain the latest revision of this document

Questions regarding this document in the GRL may be forwarded to:

Granite River Labs 3500 Thomas Road, Suite A, Santa Clara, CA 95054

Phone: 408-627-7608 Fax: 408-912-1810

E-mail: info@graniteriverlabs.com

http://www.graniteriverlabs.com

DISCLAIMER

This document is provided "as is" with no warranties whatsoever, including any warranty of merchantability, no infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample. The GRL disclaims all liability for infringement of proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

All product names are trademarks, registered trademarks, or service marks of their respective owners.

TABLE OF CONTENTS

List of Figures

List of Tables

Revision Record

Revision	Date	Change Log	Author(s)
0.5	4/2016	GRL-PCIE4-MOI Add Software Guide. Add Advanced Features.	Bill Altmann (GRL) baltmann@graniteriverlabs.com
0.7R	8/2016	Update for Rev1.0 GRL SW Release in support Rev0.7 of PCIE4 Base Specification	Mike Engbretson (GRL) mikeen@graniteriverlabs.com Bill Altmann (GRL) baltmann@graniteriverlabs.com
0.7	9/5/16	Update for Rev1.0 GRL SW Reviewed by Joe	Ganesh Baht (GRL) gbhat@graniteriverlabs.com
1.00	12/2017	Update for GRL SW V1.00.0003	Ong Gaik Pheng gpong@graniteriverlabs.com
1.10	01/2018	Update for GRL SW V1.00.0004	Ong Gaik Pheng gpong@graniteriverlabs.com
1.20	03/2018	Update for BSX BERTScope support and CTS V1.0	Ong Gaik Pheng gpong@graniteriverlabs.com
1.22	07/2018	Update for GRL SW V1.4.906	Ong Gaik Pheng gpong@graniteriverlabs.com
1.23	07/2018	Update for GRL SW V1.4.907	Ong Gaik Pheng gpong@graniteriverlabs.com
1.24	08/2018	Update equipment connection	Ong Gaik Pheng gpong@graniteriverlabs.com
1.25	09/2018	Update for GRL SW V1.4.924	Ong Gaik Pheng gpong@graniteriverlabs.com
1.26	10/2018	Update Appendix D to connect Scope via GPIB if GRL SW is installed on Scope	Ong Gaik Pheng gpong@graniteriverlabs.com
1.3x	04/2019 - 05/2019	Update Setup Configuration and Additional Parameters Configuration sections for GRL SW V1.04.945	Ong Gaik Pheng gpong@graniteriverlabs.com
1.4	06/2019	Update Conditions for Testing and Calibration for GRL SW V1.04.948	Ong Gaik Pheng gpong@graniteriverlabs.com

Reference Documents

[1] PCI Express® Base Specification, Rev. 4.0; Version 0.7; March 3, 2016

[2] PCI Express® Base Specification, Rev. 4.0; Version 1.0; September 27, 2017

1 Introduction

Receiver device compliance ensures correct data detection by the receiver for an acceptable bit error ratio (BER). PCIe Base Gen 4 devices shall support a BER that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits) when a signal with valid voltage and timing characteristics are delivered to the receiver compliance point [1]. The corresponding signal properties for verifying receiver tolerance should include the maximum allowable jitter, noise, and signal loss.

This document describes the procedures for receiver calibration and jitter tolerance testing based on the PCIe Base 4.0 (ASIC) Specification for 16 GT/s, using the GRL-BSXPCI4BSE PCIe 4.0 Base Specification Receiver Calibration and Test Software to automate the Tektronix BSX Model BERTScope and real-time oscilloscope to calibrate the stressed eye opening and test receiver conformance and jitter tolerance. The GRL-BSXPCI4BSE software uses Seasim statistical data eye simulator to establish the calibrated test channel DDJ. The final calibrated eye diagram uses both Seasim and SigTest software to achieve the final stressed eye calibration.

The BERTScope and appropriate accessories provide the necessary test patterns with jitter, ISI, and crosstalk. Additionally, the BERTScope is used to add the required transmitter equalization. The receiver jitter tolerance test includes various Differential Mode Sinusoidal Interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver eye opening has been calibrated, the receiver jitter tolerance and margin testing can then be performed on the device under test (DUT). The BERTScope is used to transmit a modified compliance pattern to the receiver DUT and monitors that the loopback pattern conforms to a BER that is less than 10^{-12} with a confidence level of 95%.

1.1 Glossary

SJ	Sinusoidal Jitter
ISI	Inter Symbol Interference
RJ	Random Jitter
CTLE	Continuous Time Linear Equalization
DFE	Decision Feedback Equalization
SDLA	Serial Data Link Analysis (Tektronix)
CDR	Clock / Data Recovery
BER	Bit Error Rate
BERT	Bit Error Rate Tester
EH	Eye Height
EW	Eye Width
Upstream	Reference to Host Test Setup (Calibrated with Device Channel)
Downstream	Reference to Device Test Setup (Calibrated with Host Channel)
PVT	Process, Voltage, Temperature

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT type. Below are the recommended lists of equipment for a typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS - SYSTEMS

System	Qty.	Description	Key Specification
Tektronix BSX Series	1	BERTScope Generator Set: • For 16 GT/s PCIe data rate: BSX240/CR175A (minimum) • For 8 GT/s PCIe data rate: BSX125/CR125A or BSA125/DPP125/CR125 (minimum)	• ≥ 28.6 Gb/s • Requires option STR for stress generation • 12.5 Gb/s clock recovery unit for DUT-sourced reference clock applications; not required for BERT-sourced reference
Tektronix DPO/MSO70000DX or 70000SX Series	1	Real-Time Oscilloscope with Tektronix DPOJET (Jitter and Eye Analysis) Software	• For 16 GT/s PCIe data rate: 25 GHz scope bandwidth (minimum) • For 8 GT/s PCIe data rate: 16 GHz scope bandwidth (minimum)
ISI Generator	1	PCIe-4 Base Spec compliant Fixed or Variable ISI Channel[a]	
Tektronix BSXSICOMB	2	Interference 40 GHz RF combiner kit for BSX Model BERTScope Used for combining Differential Mode (DM) SI and AC Common Mode (CM) SI with stressed Rx test pattern	
GRL-BSXPCI4BSE[b]	1	Granite River Labs PCIe® 4.0 (16 GT/s and 8 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com *(For BSX Model BERTScope only)* *– Included with Node Locked License to single oscilloscope or PC OS*	
Seasim	1	Seasim tool for post-processing analysis of the captured waveform (Eye Opening simulation software at TP2P) – www.pcisig.com Used for Channel (DDJ) calibration	
SigTest	1	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html SigTest used with Seasim for final eye calibration	
Computer (laptop or desktop)	1	For automation control (Windows 7+ OS)	

[a] The Artek CLE Model Series is supported for variable ISI generation. Refer to Appendix of this document for the Artek CLE Series driver installation procedure.

[b] PCIe3-BASE and PCIe4-BASE will need to be installed on the BSX BERTScope to test at both 16 GT/s and 8 GT/s data rates.

Note: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table 2 below is a recommended list. Please also refer to Tektronix's website for detailed cabling recommendations related to PCI Express.

TABLE 2. EQUIPMENT RECOMMENDATION – CABLES

Cable	Qty.	Tektronix P.N.
T+M SF104PE/11PC35/11PCC35/500mm 1.5ps Phase Matched	8	174-6663-00
T+M SF104PE/11PC35/11PCC35/1000mm 1.5ps Phase Matched	2	PMCABLE1M
T+M MF141/16SMA/16SMA/200mm SMA-to-SMA, Right Angle	4	174-6664-00
T+M MF141/16SMA/16SMA/300mm SMA-to-SMA, Right Angle	1	174-6665-00
T+M MF141/16SMA/16SMA/500mm SMA-to-SMA, Right Angle	1	174-6666-00
T+M MF141/11SMA/16SMA/1.829M SMA-to-SMA, Right Angle	2	174-6667-00
High-performance BNC	1	N/A

2.2 Extended Customization

GRL-BSXPCI4BSE can be further customized by the user or GRL Engineering using GRL's full KayaQ™ automation framework license. Contact GRL at support@graniteriverlabs.com or through your Tektronix Account Manager for further details.

3 GRL-BSXPCI4BSE Software Setup

3.1 Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL-BSXPCI4BSE PCIe 4.0 Base Receiver Test software for the 16 GT/s data rate. It also helps you familiarize yourself with the basic operation of the application.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

3.1.1 Launch and Set Up Software

3.1.1.1 On the BERTScope

1. Select View > System > Tools Tab.
2. Under Utilities Column, select the Remote button.
3. In Remote Window, select TCP/IP.
4. Change Terminator to “LF”. Select the Connect Button. See Figure 1.
   a) If you see an error pop-up when selecting the Connect button, try a different Port. For example, change Port 23 to 21.
5. Note the Address and Port number on Remote Client. They will be needed to connect the BERTScope to the automation software.
6. Minimize, but do not close, the *Remote Client* Window.

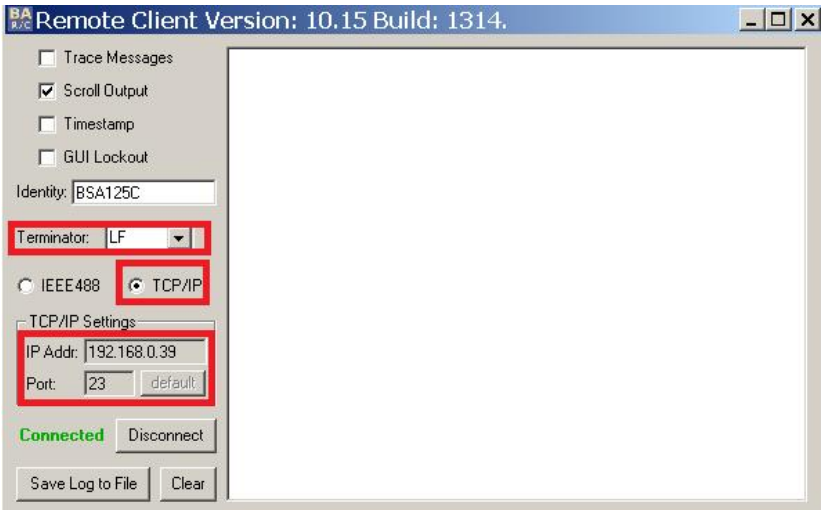

FIGURE 1. REMOTE CLIENT WINDOW

3.1.1.2 On the PC Used for GRL Framework Installation

1. Navigate to Start Menu > All Programs > GRL > GRL Automated Test Solutions.

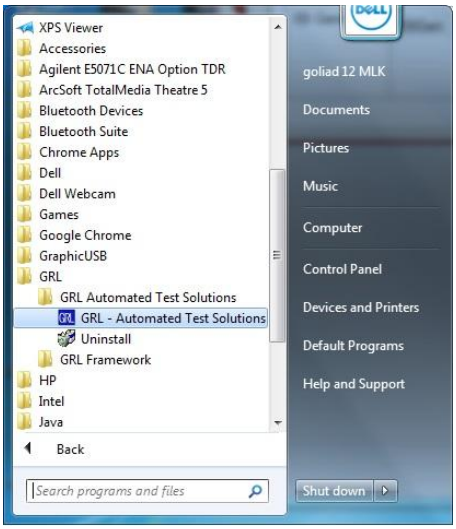

FIGURE 2. GRL AUTOMATED TEST SOLUTIONS IN START MENU

2. Click Application > Rx Test Solution > PCIe 4.0 Base Rx Test to open the application.

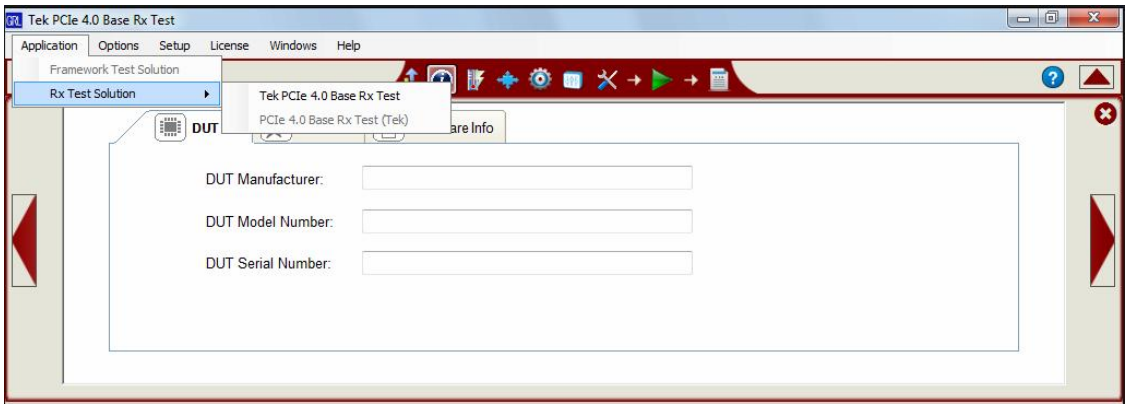

FIGURE 3. RX TEST SOLUTIONS IN GRL AUTOMATED TEST SOLUTIONS WINDOW

3. To enable license, go to License -> License Details. The dialog in Figure 4 will pop up.

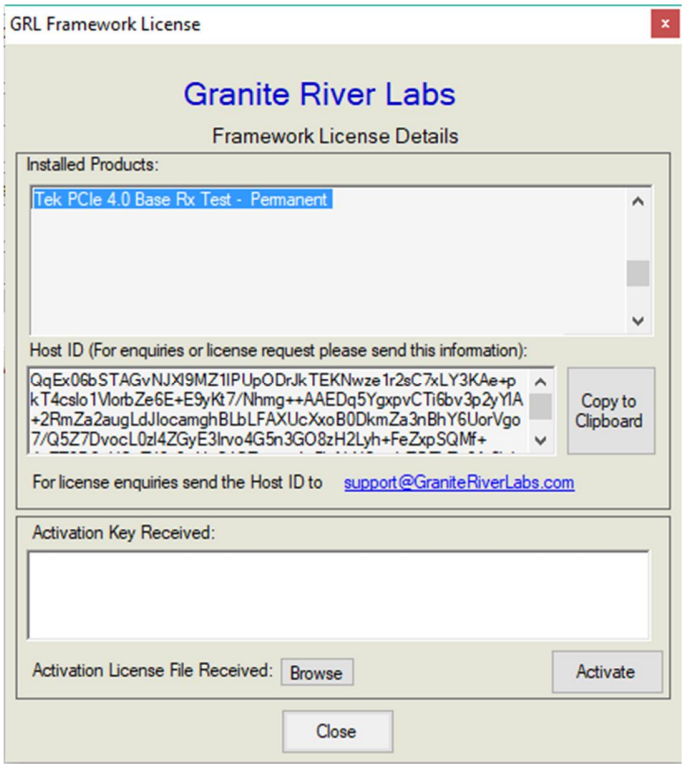

FIGURE 4. LICENSE DETAILS WINDOW

4. Activate License:
   a) If you have an Activation Key, please enter in the box provided and select **Activate**.
   b) If you do not have an Activation Key, select **Close** to use the software for 10 Days free of charge.

      Note: Once the 10-day trial times out, you will need to request an activation key for future usage on the same computer or oscilloscope. The demo SW is also limited in its capability in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request a License key by contacting support@graniteriverlabs.com.

5. Click on Equipment Setup icon  on the GRL Framework.
6. Enter the BERTScope IP address and Port number to match what is shown in the BERTScope *Remote Client* window in Step 4-5 of the previous section.

7. On the Scope, open the application **OpenChoice Instrument Manager** as shown below.

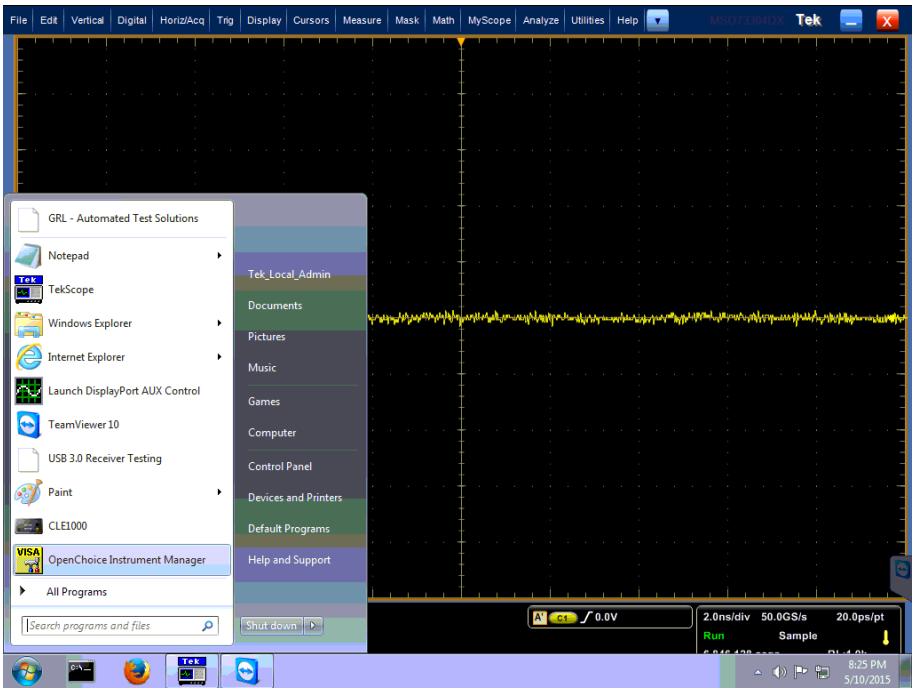

FIGURE 5. OPENCHOICE INSTRUMENT MANAGER IN START MENU

8. The Instrument Manager will display all the connected instruments on its list:
   a) GPIB8::1::INST (Scope)
   b) TCPIP::192.168.0.39::23::SOCKET (BERTScope)

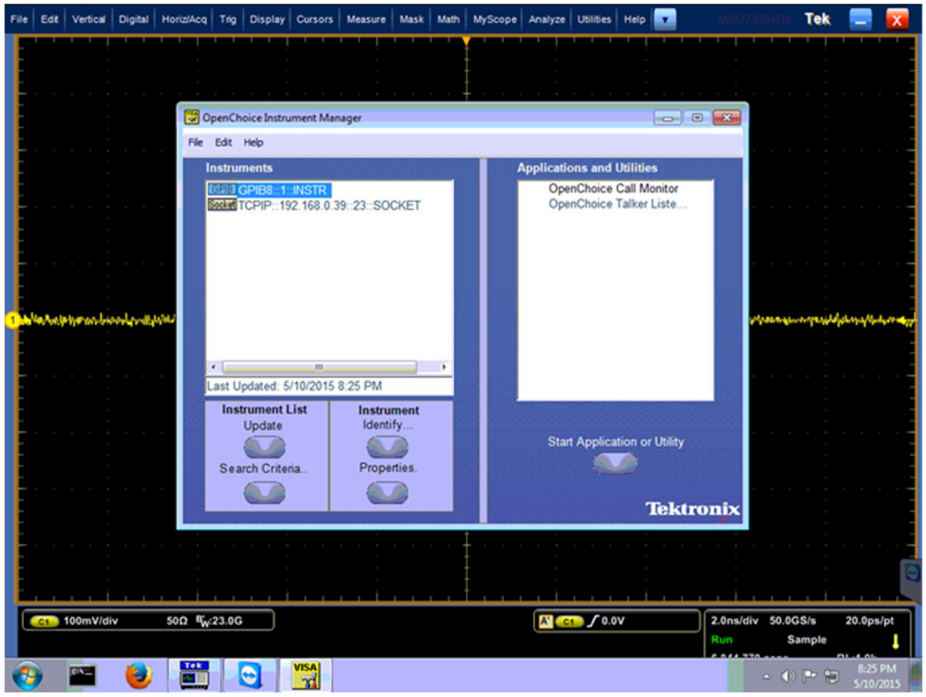

FIGURE 6. INSTRUMENT LIST IN INSTRUMENT MANAGER

9. Note these settings, as shown in Figure 7:

   a) Enter the Scope GPIB address.
   b) Enter the BERTScope IP address.

Note: If using an external ISI channel, enter the USB/Controller Serial (COM) address of the connected ISI Generator.

Note: If using an additional Arbitrary Function Generator (AFG), enter the USB/IP address of the connected AFG.

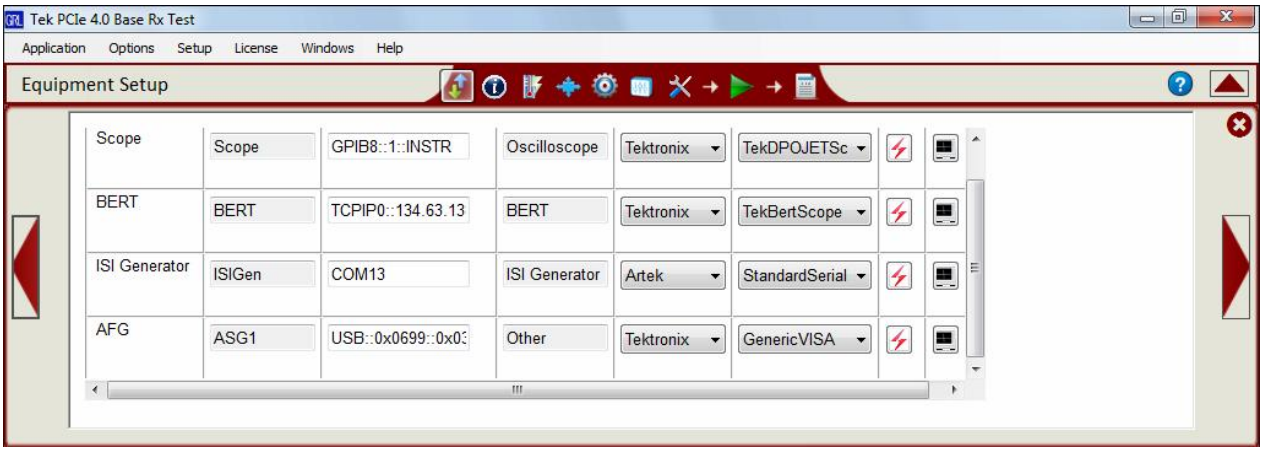

FIGURE 7. EQUIPMENT SETUP WINDOW

10. Verify the connection for each instrument by selecting the "lightning" button  , which should turn green if the connection is successful.

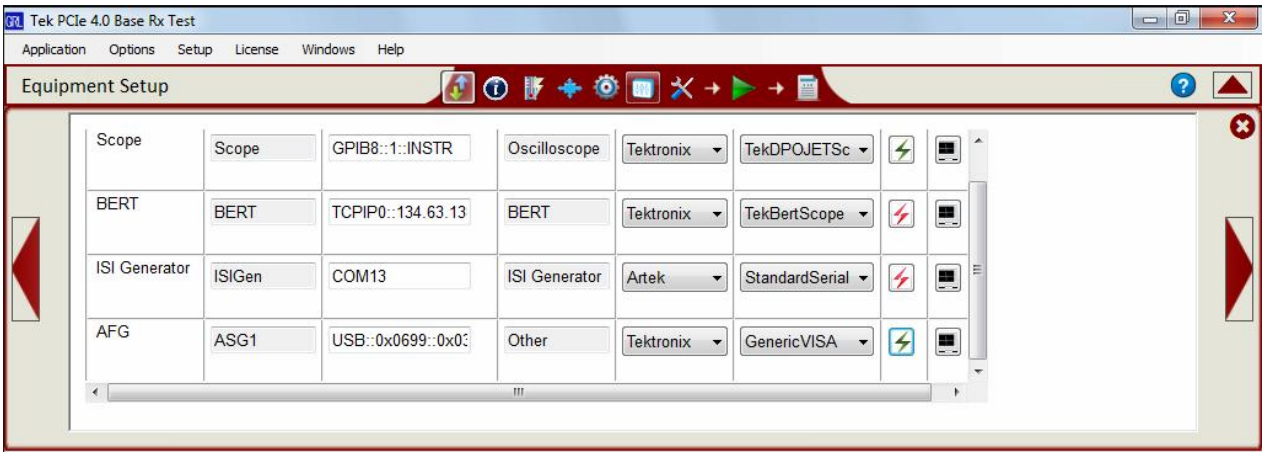

FIGURE 8. VERIFY INSTRUMENT CONNECTION

Note: If using the Scope with a controller PC, refer to Appendix for instructions on connecting the Scope to the PC.

3.2 Configuring the Software Before Calibration

3.2.1 Session Info

The information provided will be included in the report.

The **DUT Info** and **Test Info** are input by the user.

The **Software Info** is automatically populated.

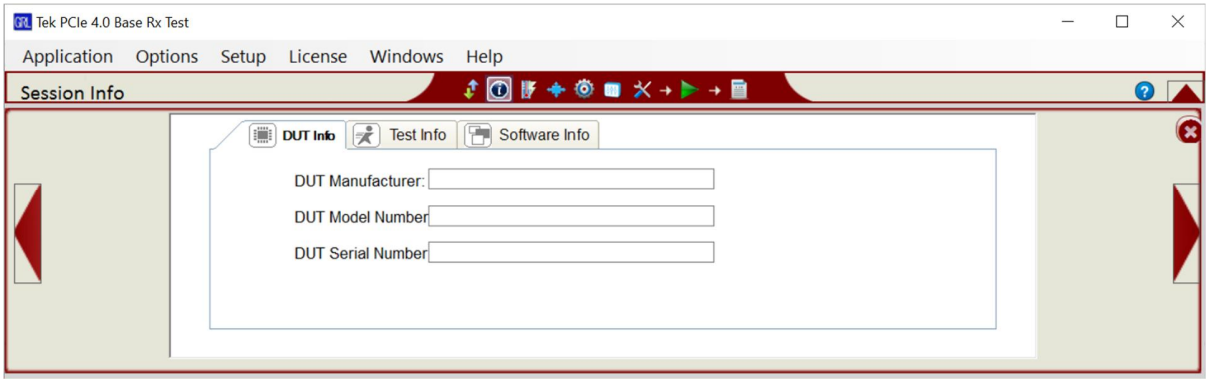

FIGURE 9. SESSION INFO

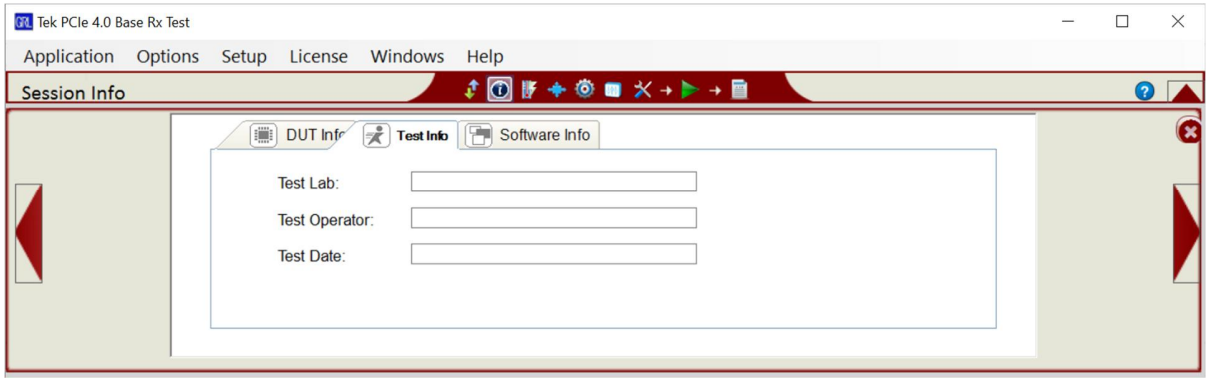

FIGURE 10. TEST INFO

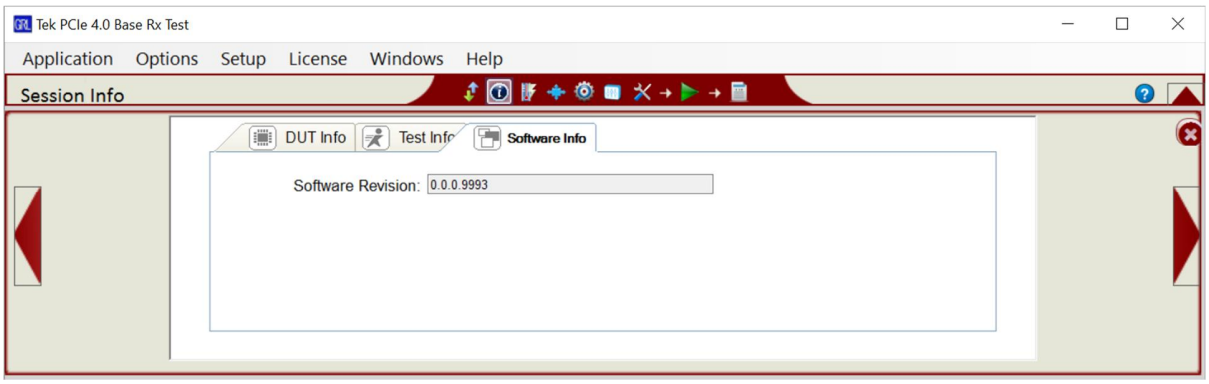

FIGURE 11. SOFTWARE INFO

3.2.2 Conditions for Testing and Calibration

In this section, Conditions ( ) for Testing and Calibration will need to be set.

When calibrating, the application will calibrate the selected range, SJ frequency, common mode voltage and differential voltage.

Recommended procedure:

1. When calibrating: select conditions for calibration and perform desired calibration.
2. When testing: re-select desired conditions for testing. For example, it may be only necessary to test range A at SJ frequency. The user would select the appropriate conditions for test.

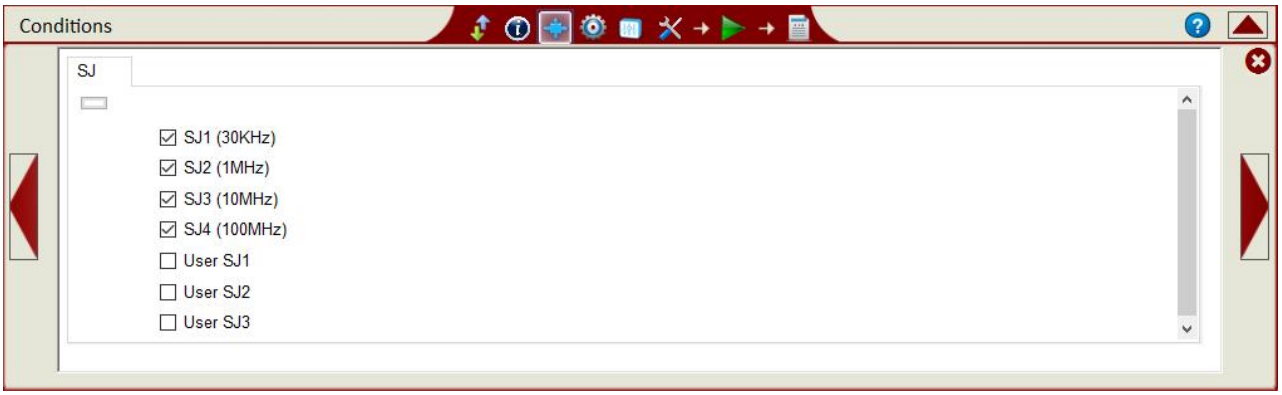

FIGURE 12. CONDITIONS FOR TESTING AND CALIBRATION

3.2.3 Setup Configuration

3.2.3.1 ISI Generator Tab

Select the type of supported ISI generators to be used:

- "None": This is the recommended method which is used to provide 22 to 27 dB physical channel Insertion Loss for calibration and testing. A PCIe 4.0 CEM Fixture can be used in the setup for this method.
- "Artek": This is provided as an Option. A compliant Artek CLE Model Series ISI channel and an additional ISI board can be used in the setup for ISI automation. *(Also see Appendix for more information on installing the Artek CLE Series.)*
- "PCIe ISI Board": This is provided as an Option which can be used to measure Insertion Loss when a Vector Network Analyzer is not available.

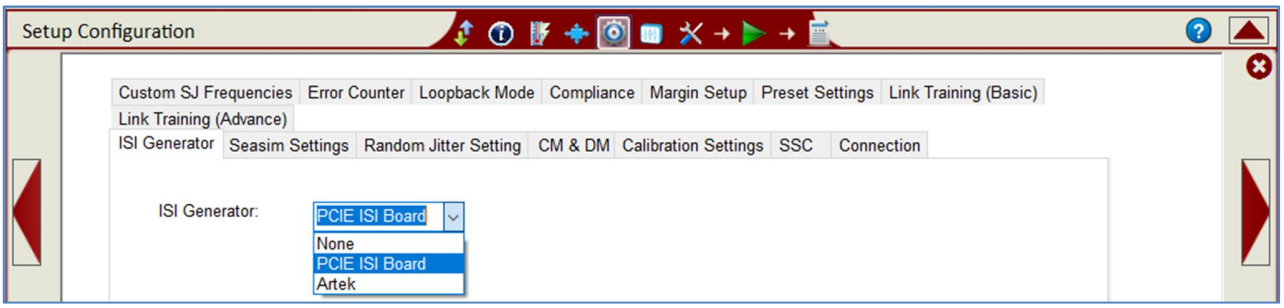

FIGURE 13. ISI GENERATOR SETUP

3.2.3.2 Seasim Settings Tab

Set up the Rx Behavioral package to be applied during post processing analysis for the Eye Height and Eye Width Calibration. Also set the intrinsic jitter (if required) to be used in the Seasim calculation.

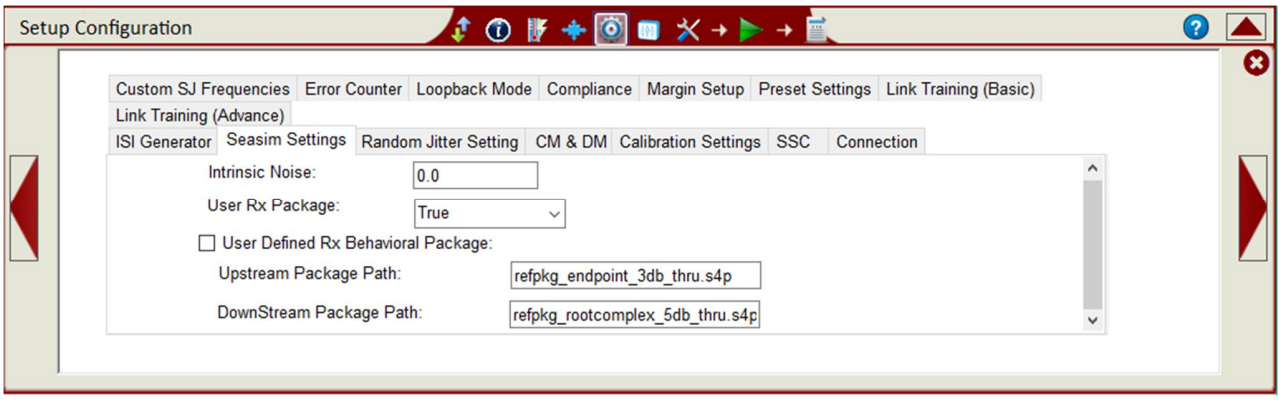

FIGURE 14. SEASIM SETUP

3.2.3.3 Random Jitter Setting Tab

Set the intrinsic RJ value in % unit interval for the BERTScope.

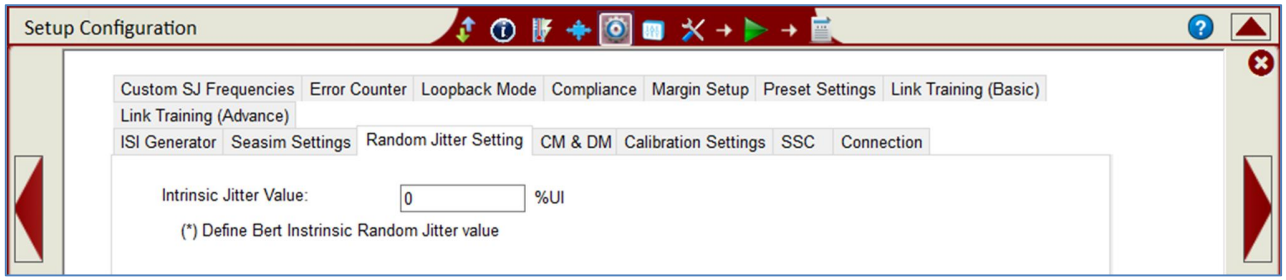

FIGURE 15. RANDOM JITTER SETTING

3.2.3.9 CM & DM Tab

Note: These settings are only applicable for the Tektronix BSX320 BERTScope version.

Select the BSX320 BERTScope channels to be used for the Common Mode and Differential Mode Sinusoidal Interference (SI) connections.

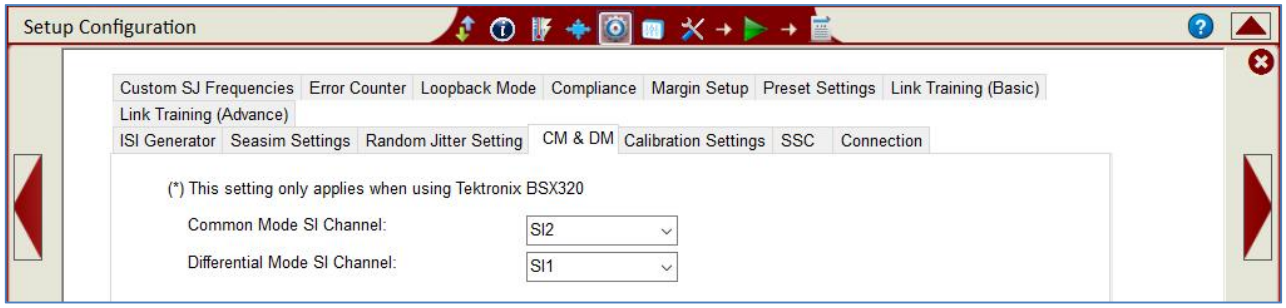

FIGURE 16. CM AND DM SI CHANNEL SETUP

3.2.3.10 Calibration Settings Tab

Specify or use the default frequency values for Differential Mode (DM) and Common Mode (CM) calibration.

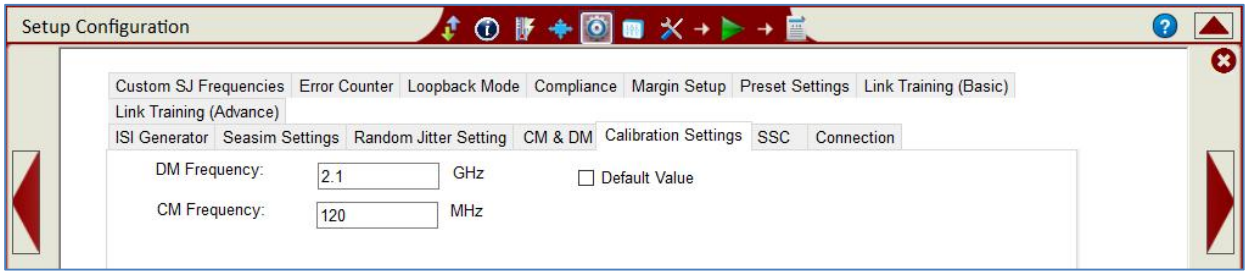

FIGURE 17. DM AND CM CALIBRATION SETTINGS

3.2.3.11 SSC Tab

Select the checkbox to enable Spread Spectrum Clock (SSC) capabilities for calibration and receiver testing (if supported by the DUT) for informative purpose. Set the Frequency and Deviation values for SSC.

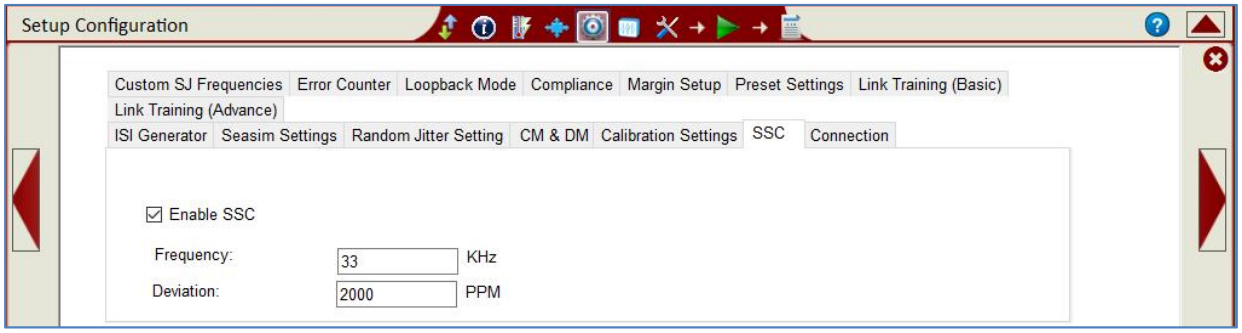

FIGURE 18. SSC SETUP

3.2.3.12 Connection Tab

Set up connection of Data+/- along with their Skew values on Scope. Scope channels shall be assigned according to how the scope cables are attached to the test setup.

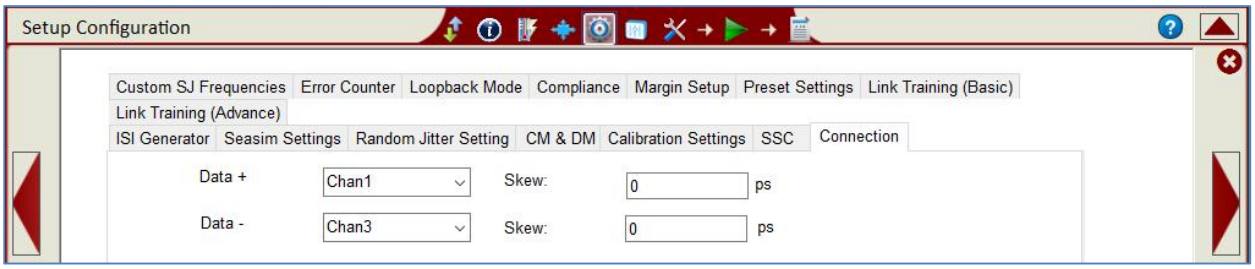

FIGURE 19. SCOPE CHANNEL CONNECTION SETUP

Note: To take best advantage of the Oscilloscope's Sample Rate, either the Chan1, Chan3 or Chan2, Chan4 pair should be used for the differential acquisition channel. The default is the Chan2, Chan4 pair as this provides the most convenient setup when the Scope is being connected to the Left of the BERTScope. This allows optimal cooling airflow to run through the Scope.

3.2.3.13 Custom SJ Frequencies Tab

Set the values for user-defined SJ frequencies that have been selected from the Conditions page.

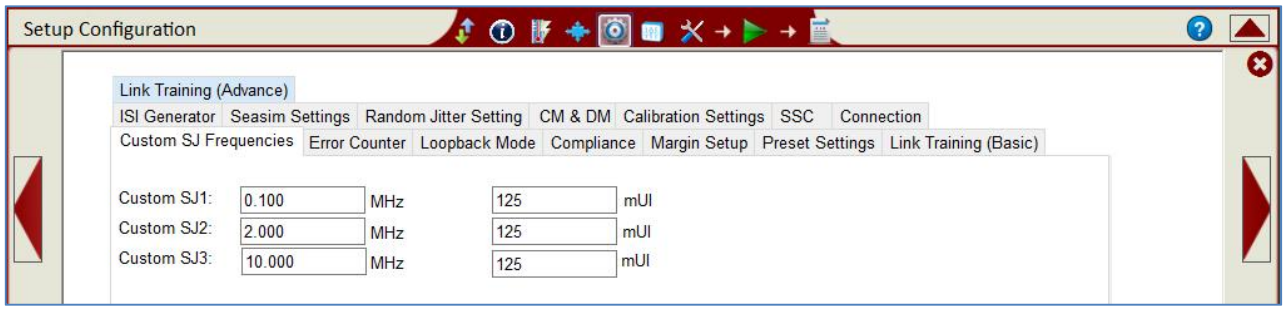

FIGURE 20. SET USER SJ FREQUENCIES

3.2.3.14 Error Counter Tab

Enable loopback test mode for the Rx base DUT for error detection. If the DUT can be configured to loopback mode, select 'LoopBack', if not select 'Manual'.

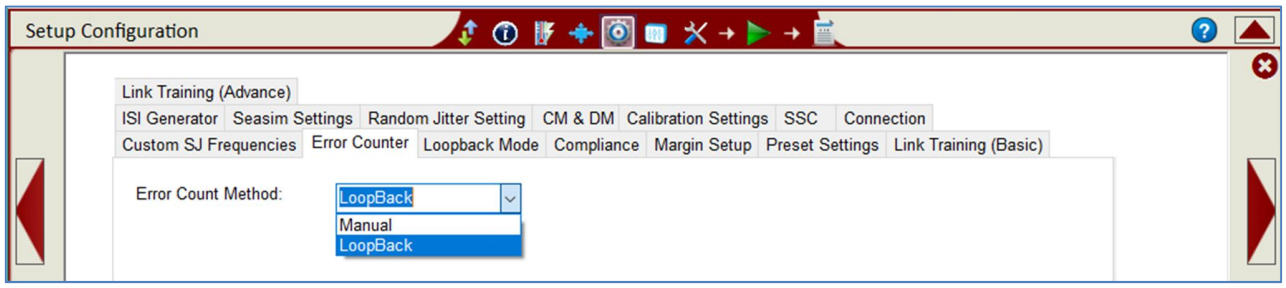

FIGURE 21. BER LOOPBACK TEST METHOD

3.2.3.15 Loopback Mode Tab

If "LoopBack" has been selected from the Error Counter tab, then select "Clock Recovery" in the Clock Recovery Method drop-down on the Loopback Mode tab. *Other options on the Clock Recovery Method drop-down are not yet supported.* Set the loop bandwidth as required for the Clock Recovery.

To perform clock synchronization which extracts the clock signal from the data to produce a synchronous clock signal, select the 'Grab and Go Sync' checkbox.

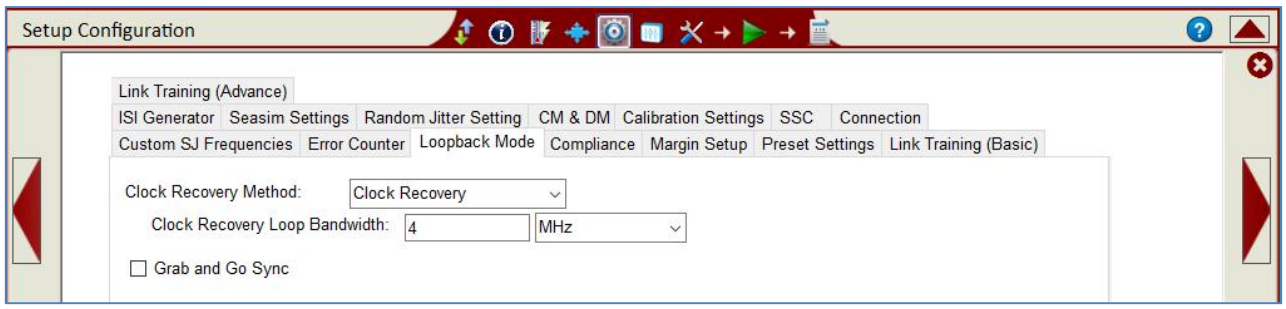

FIGURE 22. LOOPBACK MODE SETUP

3.2.3.16 Compliance Tab

Set the allowable BER and Maximum Error limits to be tested for compliance. By default, these limits are set to Specification, but can be defined by the user. The syntax '1e-12' indicates $1x10^{-12}$, and is the only syntax supported in this field. In normal circumstances, any error count above one constitutes a fail.

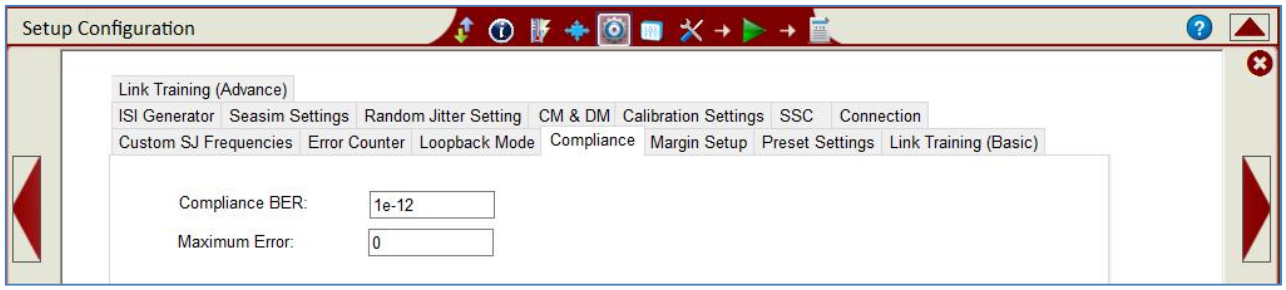

FIGURE 23. BER AND MAXIMUM ERRORS

3.2.3.17 Margin Setup Tab

Select the target BER, step size, and limits to be applied during marginal testing.

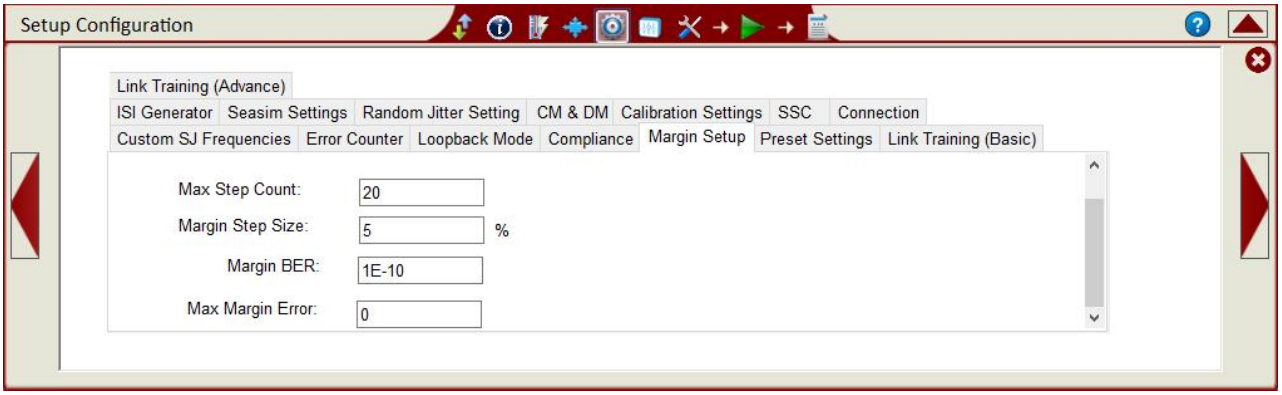

FIGURE 24. MARGIN SEARCH PARAMETERS SETUP

3.2.3.18 Preset Settings Tab

Select the preset and the preset hints for each Rx lane to use, and optionally custom Preshoot and Deemphasis settings.

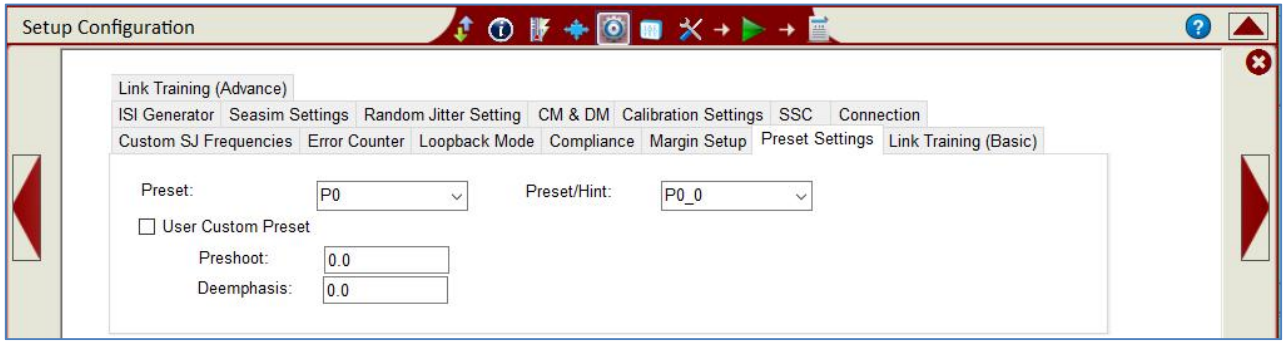

FIGURE 25. PRESET SETUP

3.2.3.19 Link Training (Basic) Tab

To perform link equalization, select the 'Use Link EQ' checkbox. Select the Lane and Link numbers along with the Fast Training Sequence (FTS) value required by the receiver from 0 to 255. FTS is used within an Ordered Set when transitioning from L0s to L0.

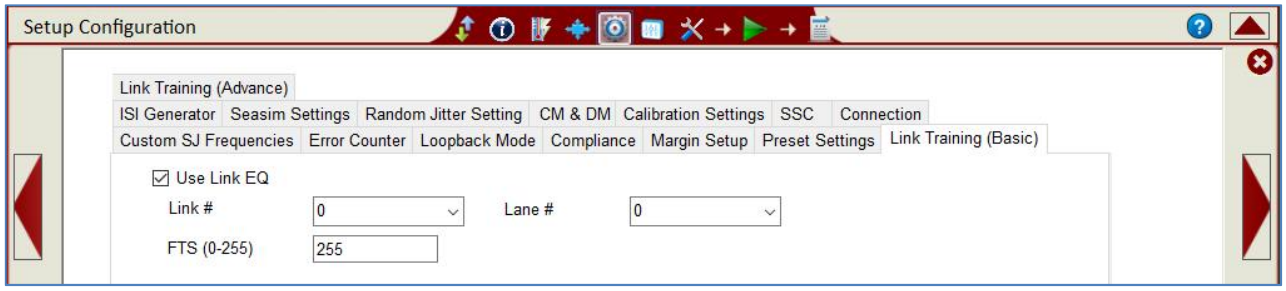

FIGURE 26. BASIC LINK TRAINING SETUP

3.2.3.20 Link Training (Advance) Tab

Set up advanced parameters for link training by entering the limit of extended synchronization bit, full swing (FS) and low frequency (LF) values as well as Electrical Idle length.

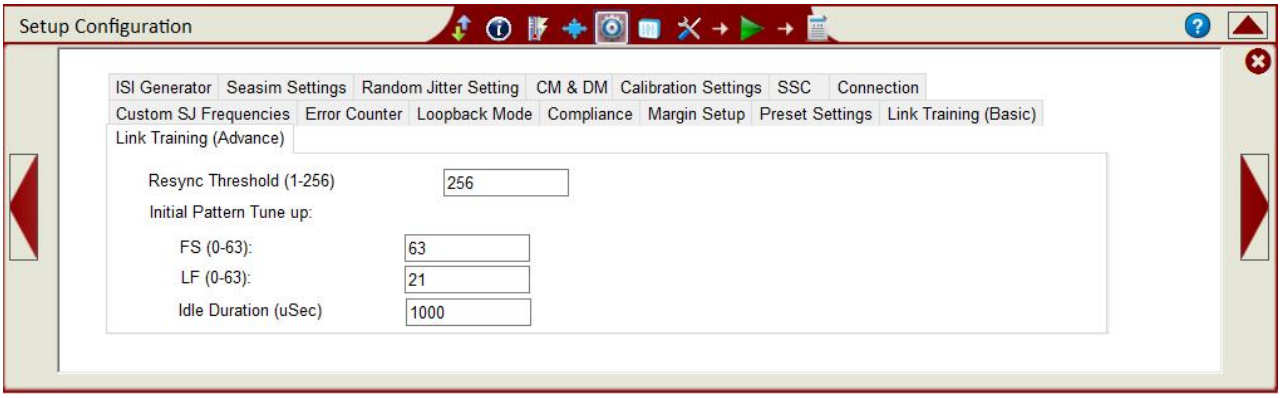

FIGURE 27. ADVANCE LINK TRAINING SETUP

4 Calibrating Using GRL-BSXPCI4BSE Software

Calibration for PCI Express 4.0 Base Specification are performed at two physical test points – TP1 and TP2. TP1 is a physical test point for calibration without the effect of a channel. An adjustable Calibrated CEM Connector is defined that is to be used along with the Replica Channel for the DUT for testing. TP2 is a test point that will affect the eye opening due to trace length. Post processing analysis of the signal is performed at the TP2P test point using the Seasim or SigTest application to simulate the stressed eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

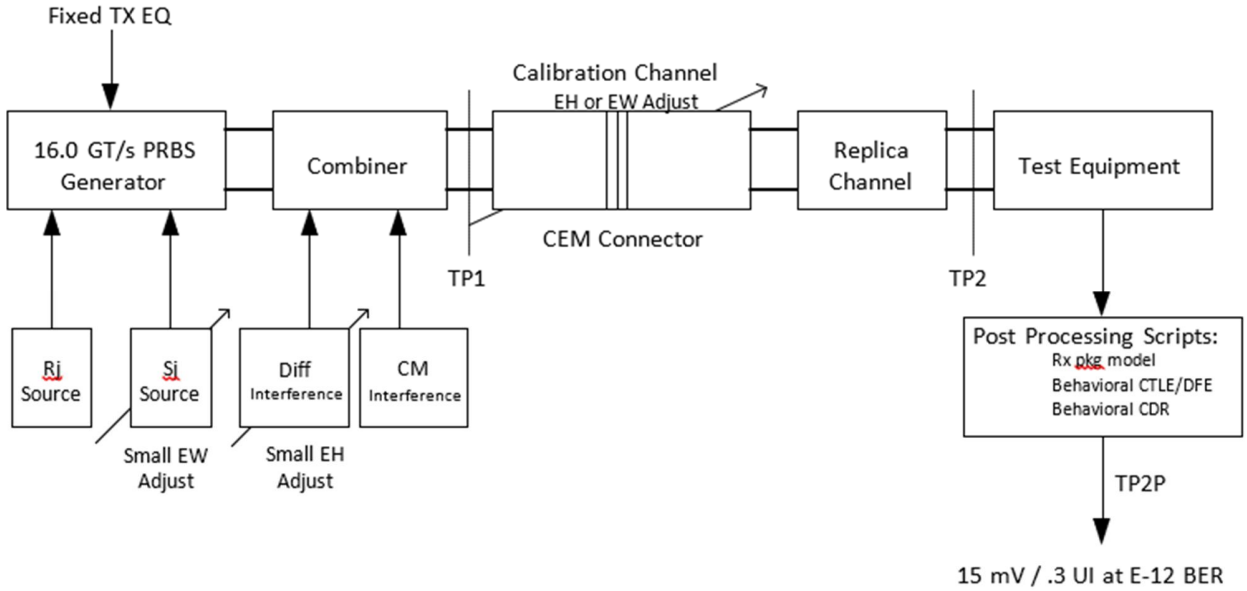

FIGURE 28. RX CALIBRATION BLOCK DIAGRAM FROM THE PCIE4.0 BASE SPECIFICATION

To calibrate the stressed eye at TP2, the calibration channel shall receive signals with appropriate test patterns generated by the signal source. After calibration, the signal source shall be used for testing Rx DUT compliance.

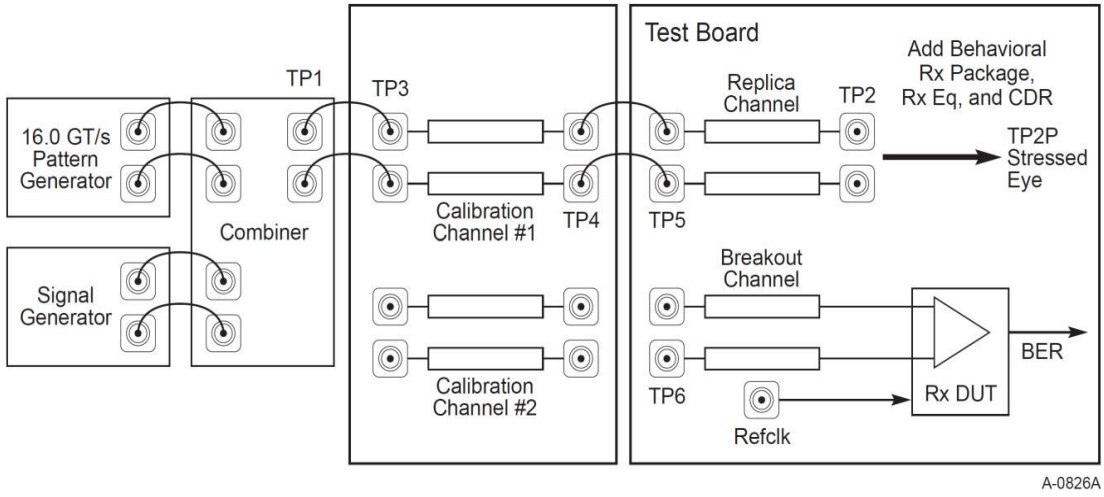

FIGURE 29. RX CALIBRATION/TEST SCHEMATIC OVERVIEW FROM THE PCIE4.0 BASE SPECIFICATION

4.1 Stressed Jitter Eye Parameters

The following table is an excerpt of the PCIe4.0 Base Specs showing the target measurement values for each calibration parameter.

TABLE 4-1: STRESSED JITTER EYE PARAMETERS FROM THE PCIE4.0 BASE SPECIFICATION

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to1200	800-to 1200	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	ps	
T_{RX-ST}	Eye width	≤0.4	≤0.32	≤0.30	≤0.30	UI	Note 3, 4, 8,10
V_{RX-ST}	Eye height	≤175	≤100	≤25	≤15	mV PP	Note 2,4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	3.0 (max)	1.0	ps RMS	Note 6,7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	mV PP	Note 8
$V_{SSC-RES}$	SSC Residual	N/A	75	N/A	500	ps	Note 11, 13

Notes:

1. $V_{RX-LAUNCH}$ may be adjusted to meet V_{RX-ST} as long as the outside eye voltage at TP2 does not exceed 1300 mV PP for calibration at 2.5, 5.0 and 8.0 GT/s. $V_{RX-LAUNCH}$ is adjusted from 720 to 800 mV for 16 GT/s calibration.
2. Voltages shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
3. Eye widths shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
4. V_{RX-ST} and T_{RX-ST} are referenced to TP2P for 8.0 GT/s and 16.0 GT/s and TP2 for 2.5 GT/s and 5.0 GT/s. For 8.0 GT/s and 16.0 GT/s behavioral equalization are applied to the data at TP2.
5. $T_{RX-ST-SJ}$ may be measured at either TP1 or TP2. Only 8.0 GT/s and 16.0 GT/s Receivers are tested with Sj mask.
6. $T_{RX-ST-RJ}$ may be adjusted to meet the target value for T_{RX-ST} at 8.0 GT/s. Rj is measured at TP1 to prevent data-channel interaction from adversely affecting the accuracy of the Rj calibration. Rj is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
7. Both $T_{RX-ST-RJ}$ and $V_{RX-DIFF-INT}$ are limited to prevent the stressed eye from containing excessive amounts of jitter or noise distortion that are unrepresentative of a real channel. Too many of these distortion components produces a signal that cannot be equalized by an actual Receiver.
8. Defined as a single tone at 120 MHz. Measurement made at TP2 without post-processing. Common mode is turned off during T_{RX-ST} and V_{RX-ST} calibration and then turned on for the stressed eye jitter test.
9. For 2.5 GT/s and 5.0 GT/s Rx calibration variable channel loss is used to achieve the target eye height.
10. For 2.5 GT/s Rx calibration 100 MHz Sj is used to achieve the target eye width.
11. For 33 kHz SSC residual for common clock architecture testing only when testing at 5 GT/s.
12. Frequency for $V_{RX-DIFF-INT}$ is chosen to be slightly above the first pole of the reference CTLE.
13. Applied for CC testing only as a triangular phase modulation with a frequency between 30 kHz to 33 kHz when testing at 16 GT/s.

4.2 Common Receiver Parameters

The following table is an excerpt of the PCIe4.0 Base Specs showing the target values for the common base Rx parameters. *Note: These parameters are not directly linked to the stressed eye measurement.*

TABLE 4-2: COMMON RECEIVER PARAMETERS

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	**124.9625 (min) 125.0375 (max)**	62.48125 (min) 62.51875 (max)	ps	UI is tolerance is equivalent to ±300 ppm and does not include SSC effects
$BW_{RX-PKG-PLL1}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL1}$	22 (max), 1.5 (min)	16 (max), 8 (min)	**4.0 (max), 2.0 (min)**	4.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$BW_{RX-PKG-PLL2}$	Rx PLL bandwidth corresponding to $PKG_{RX-PLL2}$	Not Specified	16 (max), 5.0 (min)	**5.0 (max), 2.0 (min)**	5.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function
$PKG_{RX-PLL1}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL1}$	3.0 (max)	3.0	**2.0**	2.0	dB	Second order PLL transfer bounding function
$PKG_{RX-PLL2}$	Maximum Rx PLL peaking corresponding to $BW_{RX-PKG-PLL2}$	Not specified	1.0	**1.0**	1.0	dB	Second order PLL transfer bounding function
$RL_{RX-DIFF}$	Differential receiver return loss	See Figure 8-19	See Figure 8-19	See Figure 8-19	See Figure 8-19	dB	
RL_{RX-CM}	Common mode receiver return loss	See Figure 8-20	See Figure 8-20	See Figure 8-20	See Figure 8-20	dB	
$RX_{GND-FLOAT}$	Rx termination float time	500 (max)	500 (max)	500 **(max)**	500 (max)	ns	Limits added for 2.5 GT/s and 5.0 GT/s that match those for 8.0 GT/s
$V_{RX-CM-AC-P}$	Rx AC common Mode Voltage	150 (max)	150 (max)	**75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP**	75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP	mVP	Measured at Rx pins into a pair of 50Ω terminations to ground

Symbol	Parameter	2.5 GT/s Value	5.0 GT/s value	8.0 GT/s Value	16.0 GT/s value	Units	Notes
Z_{RX-DC}	Receiver DC single ended impedance	40 (min) 60 (max)	40 (min) 60 (max)	Not specified	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. For 8.0 and 16.0 GT/s is bounded by RLRX-CM. See Note 5.
$Z_{RX-HIGH-IMP-DCPOS}$	DC input CM input impedance for V≥0 during Reset or power-down	≥10K (0200 mV) ≥20K (> 200 mV)	≥10K (0-200 mV ≥20K (> 200 mV)	**≥10K (0-200 mV** **≥20K (> 200 mV)**	**≥**10K **(0-200 mV** **≥20K (> 200 mV)**	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology.
$Z_{RX-HIGH-IMP-DCNEG}$	DC input CM input impedance for V<0 during Reset or power-down	1.0K (min)	1.0K (min)	**1.0K (min)**	1.0K (min)	Ω	Parameters may not scale with process technology.
$V_{RX-IDLE-DET-DIFFPP}$	Electrical Idle Detect threshold	65 (min) 175 (max)	65 (min) 175 (max)	**65 (**min**)** **175 (max)**	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2*|V_{RX-D+} - V_{RXD-}|. Measured at the package pins of the Receiver.
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	10 (max)	10 (max)	**10 (max)**	10 (max)	ms	An unexpected Electrical Idle ($V_{RX-DIFF-PP}$ < $V_{RXIDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Lane to Lane skew	20 (max)	8 (max)	**6 (max)**	5 (max)	ns	Across all Lanes on a Port. $L_{RX-SKEW}$ comprehends Lane-Lane variations due to channel and repeater delay differences.

Notes:

1. Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in.
2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.
4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.
5. The Rx DC single ended impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance is permitted to start immediately and the Rx Common Mode Impedance (constrained by RL_{RX-CM} to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V_{-CMDC}|}.
7. $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.
8. Defines the time for the Receiver's input pads to settle to new common-mode on 2.5/5.0 GT/s transition to 8.0 GT/s.

4.3 Calibration Parameters for TP1 (Output of BERTScope)

4.3.1 Setup for TP1 Calibration

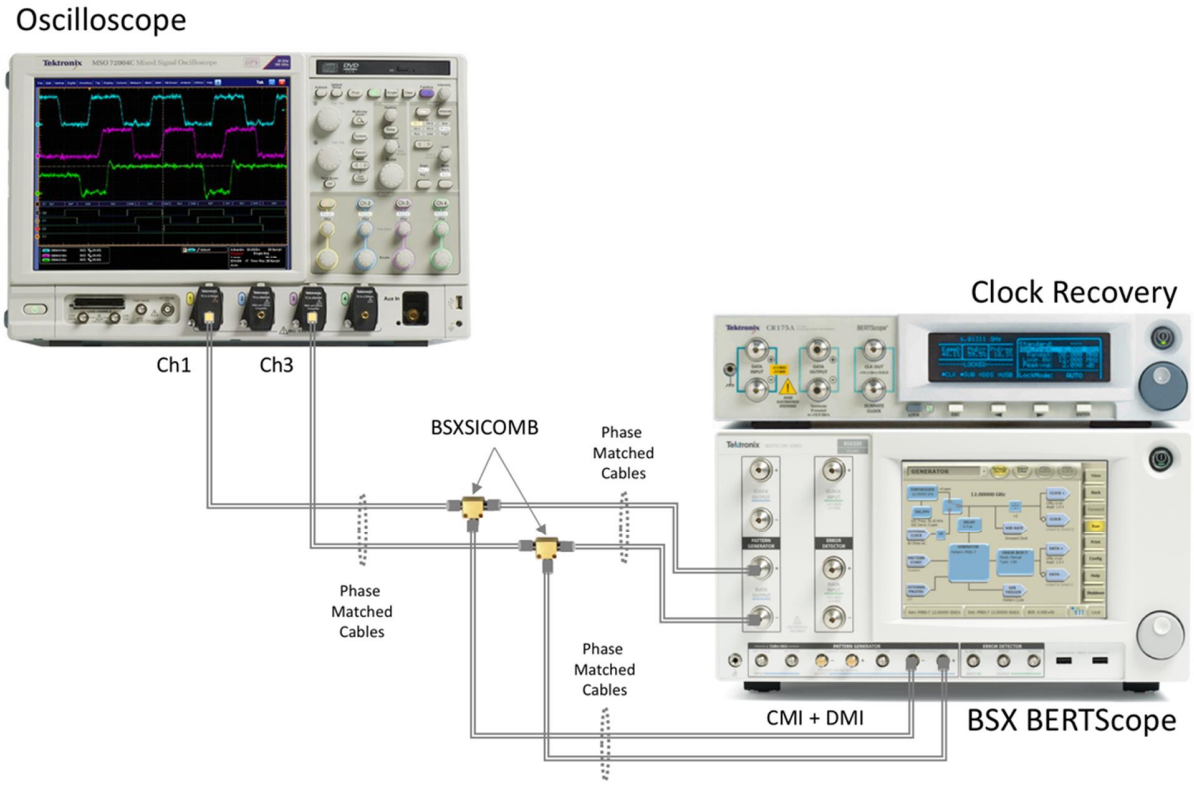

FIGURE 30. TYPICAL SETUP FOR TP1 CALIBRATION

Connection Steps:

1. Connect BERTScope Data (+/-) Out to BSXSICOMB In.
2. Connect BERTScope SI1-Out to BSXSICOMB CMI/DMI-In.
3. Connect BERTScope SI2-Out to BSXSICOMB CMI/DMI-In.
4. Connect BSXSICOMB Out to Scope Ch1, Ch3 (or Ch2, Ch4).

4.3.2 Selecting Calibration Steps

The following parameters are defined at TP1 and TP2 Test Points from Figure 28.

Calibrations at TP1:

1. Pre-shoot Calibration
2. De-emphasis Calibration
3. Launch Amplitude Calibration
4. RJ Calibration
5. SJ Calibration
6. SJ Tone Calibration

Calibrations at TP2, can be Downstream (for Host) or Upstream (for Device):

7. Downstream or Upstream:
   a. Insertion Loss Calibration *[Only applicable if CTS version '0.7' is selected from the Configurations page menu – see Section 7]*
   b. ISI Calibration (CEM Connector Channel + Replica Channel) *[Only applicable if CTS version '1.0' is selected from the Configurations page menu – see Section 7 AND ISI Generator other than "None" is selected from the Setup Configuration menu – see Section 3.2.3.1]*
   c. Common Mode (CM) Sinusoidal Interference Calibration
   d. Differential Mode (DM) Sinusoidal Interference Calibration (Achieves Calibrated Eye Height)
   e. Optimized Preset/Final ISI Calibration
   f. Stressed Jitter Voltage Calibration (Final stressed voltage and jitter eye adjustment to achieve Calibrated Eye Width)
   g. SigTest DM Optimization & Final Eye Calibration (Produces final stressed Eye Diagram if SigTest is used as post processing tool)

      [SigTest Final Eye Calibration is only applicable if CTS version '1.0' is selected from the Configurations page menu – see Section 7]

GRL-BSXPCI4BSE automatically calibrates these parameters when initiated. See Appendix for an implementation method with automation for the above calibration.

The **Select Tests** page is the place where the calibration/tests that need to be performed are selected. Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Rx Tests will throw an error when initiated.

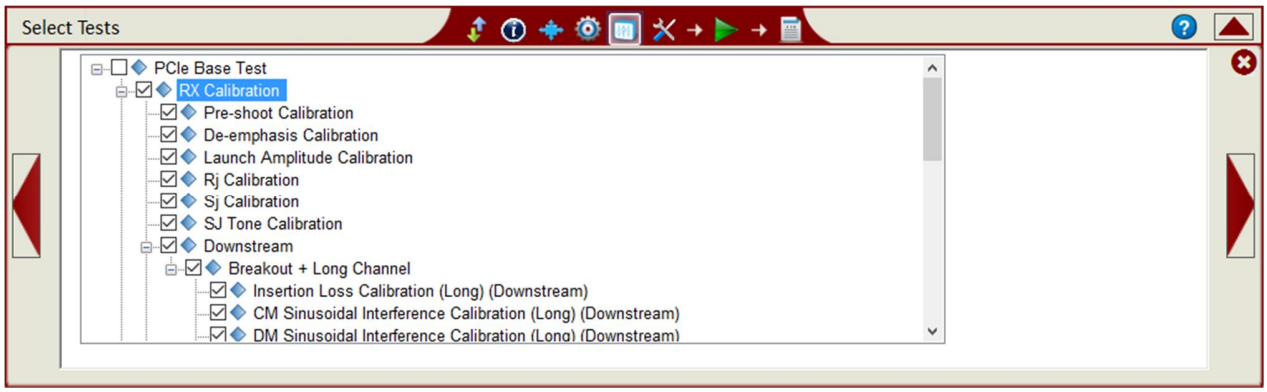

FIGURE 31. CALIBRATION SELECTION

4.3.3 Run Calibration Steps at TP1

Select the Run icon: 

1. Select any of these Options to Run the selected calibration:
   - **Skip Test if Result Exists –** If previous calibration results exist, then the software will *skip* the calibration steps that have existing reports.
   - **Replace if Result Exists –** If previous calibration results exist, then the software will *replace* each step in the calibration with new results.

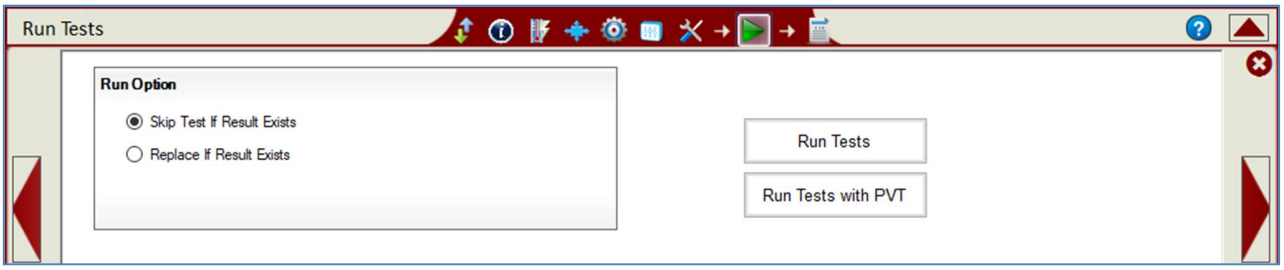

FIGURE 32. RUN TESTS PAGE

2. Select "Run Tests" to start running the selected calibration. To run calibration with Process, Voltage, Temperature (PVT) automation, select "Run Tests with PVT" (*see Appendix for details on using the Advanced PVT features.)*

When running Calibration at TP1, the connection diagram will be shown as a first step to help the user make sure all connections are made before the tests are run. See example below.

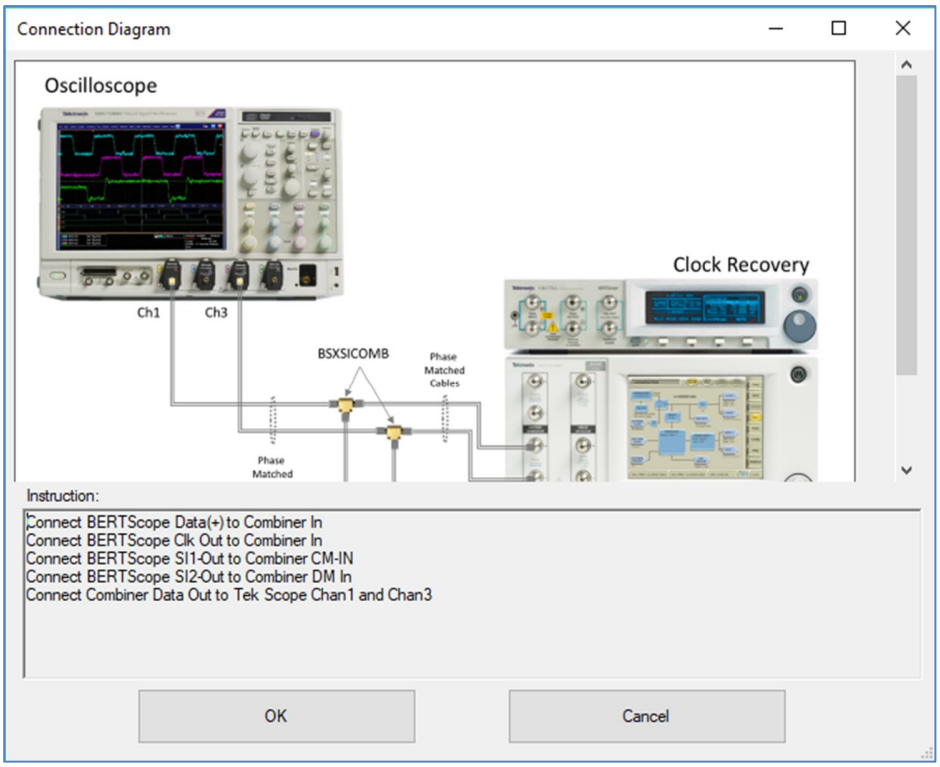

FIGURE 33. TP1 CONNECTION DIAGRAM DIALOG

4.4 Calibration Parameters for TP2 (Output of Long Channel)

The next step is to calibrate the TP1-TP2 Channel. As shown in Figure 28, the total TP1-TP2 calibration channel includes an Adjustable Calibration Channel, that requires the Insertion loss to fit within the limits called out in the PCI Express 4.0 Base specification. Figure 34 shows the limits for both Upstream (Host) and Downstream (Device) Channels.

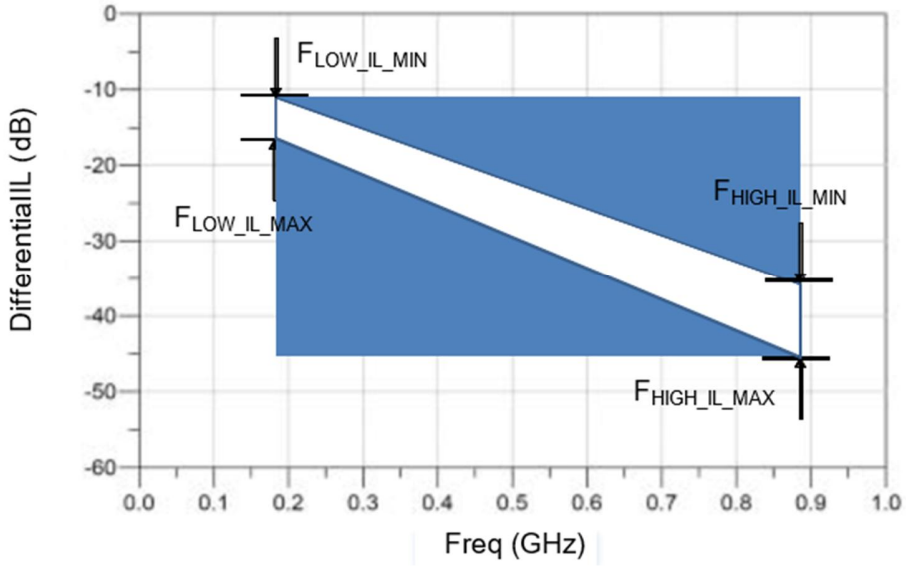

Table 2-1: Calibration Channel IL Limits

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
2.5 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	4.7 dB @ 1.25 GHz	5.2 dB @ 1.25 GHz
5.0 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	10.0 dB @2.5 GHz	11.0 dB @2.5 GHz
8.0 GT/s	5 dB @ 1 GHz	8 dB @ 1 GHz	~20 dB @ 4 GHz	~22 dB @ 4 GHz
16.0 GT/s Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~22.5 dB @ 8 GHz	~23.5 dB @ 8 GHz
16.0 GT/s Non-Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~24.5 dB @ 8 GHz	~25.5 dB @ 8 GHz

Note: Calibration channel plus Rx package is 28 dB nominally (informative) for 16.0 GT/s.

Note: Different reference packages are defined for devices containing Root Ports and all other device types at 16.0 GT/s.

Note: It is recommended that some validation be done with shorter channels at 16.0 GT/s.

FIGURE 34. INSERTION LOSS CALIBRATION LIMITS FROM THE PCIE4.0 BASE SPECIFICATION

The GRL-BSXPCI4BSE software uses a combination of a variable ISI channel, CEM connector, and replica channel to achieve the target IL profile. After calibrated using the GRL software, the calibrated channel IL should look like the example in Figure 36 after being analyzed with Seasim.

4.4.1 Setup for TP2 Calibration

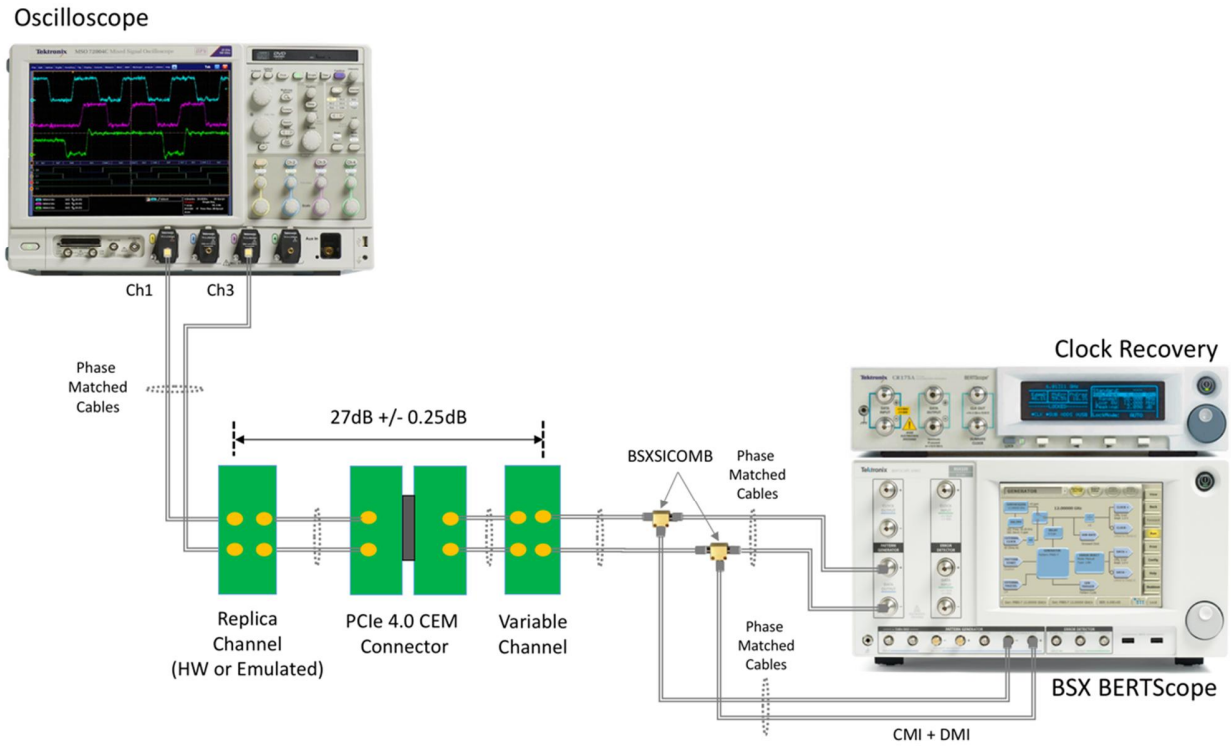

FIGURE 35. TYPICAL SETUP FOR TP2 CALIBRATION

Connection Steps:

1. Using back the same connections from the TP1 calibration setup, disconnect the BSXSICOMB Out from the Scope channels.
2. Connect the BSXSICOMB Out to a Variable ISI Channel inputs.
3. Connect the Variable ISI Channel outputs to a PCIe 4.0 CEM Connector Segment inputs.
4. Connect the CEM Connector Segment outputs to a Replica Channel inputs.
5. Connect the Replica Channel outputs to the Scope Ch1, Ch3 (or Ch2, Ch4).

Note: In this example, the length of the Calibration Channel combination is approximately 27 dB +/- 0.25 dB, and shall be adjusted for the total channel loss to meet the frequency profile in Figure 34.

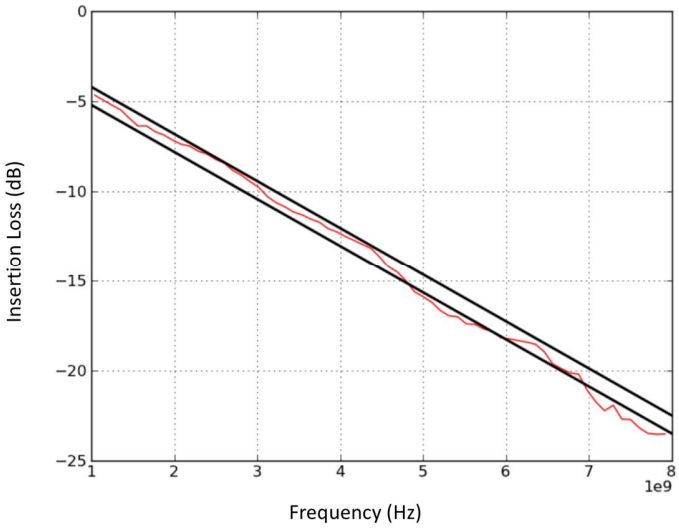

FIGURE 36. CALIBRATED IL USING GRL-BSXPCI4BSE

4.4.2 Run Calibration Steps at TP2

Repeat Section 4.3.3 to complete the selected calibration steps at TP2.

After Calibrating the Loss profile to be used by adjustment of De-Emphasis as shown in Figure 34; ISI/Insertion Loss Measurement, Optimized Preset/Final ISI, CM Sinusoidal Interference, DM Sinusoidal Interference, and Stressed Voltage Jitter adjustments to achieve calibrated eye height and width, the final calibrated stressed Eye diagram is calculated by Seasim and SigTest, and should look similar to the below example.

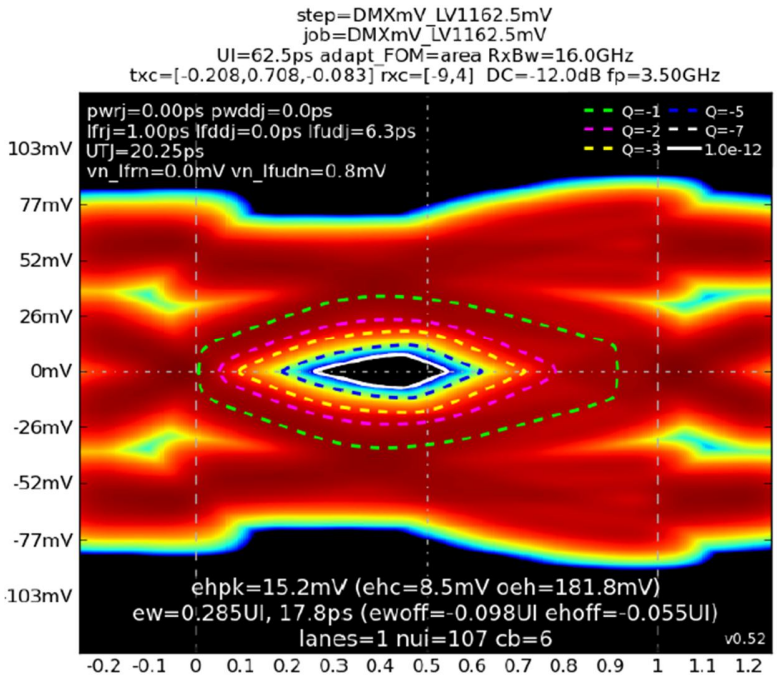

FIGURE 37. FINAL CALIBRATED STRESSED EYE DIAGRAM EXAMPLE

4.4.3 Validating the Stressed Eye Diagram Using Tektronix SDLA and DPOJET

The PCIe4 Base Specification Rev4.0, Version 1.0 has the following requirement:

- 2 million unit interval waveforms with compliance pattern are captured at each Tx EQ at the end of the channel. The Tx EQ is calibrated to the nominal values for each preset at the pattern generator output before doing the captures.
- For the preset that gives the largest eye area with the waveform post processing tool, the EH and EW @ E-12 BER must match 15 mV and 0.3 UI within +/- 15%.

Tektronix SDLA (Serial Data Link Analysis) can provide the equalization for the PCIe4 captured waveform, and DPOJET (Jitter and Eye Tools for DPO Scopes) can be used to make EH and EW measurements.

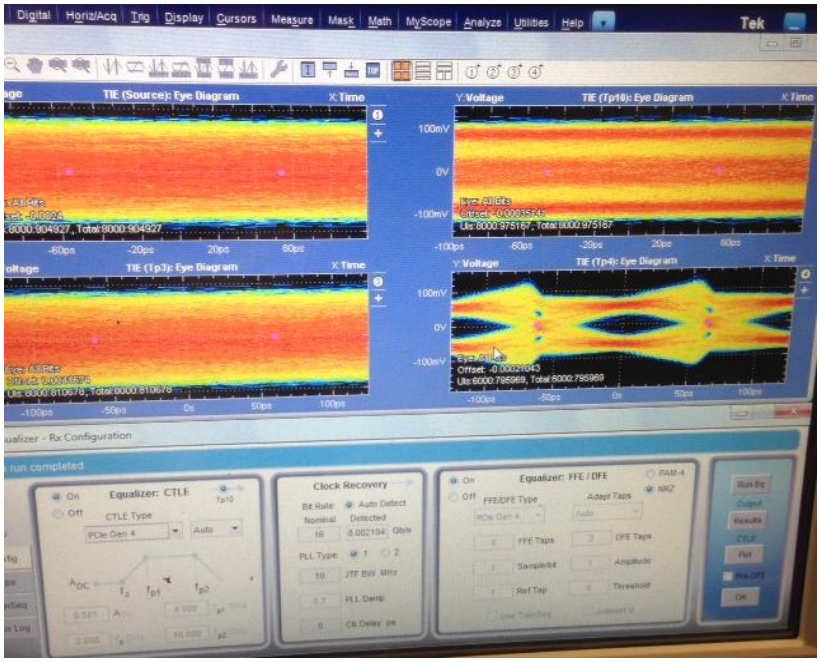

FIGURE 38. PROPOSED VALIDATION TECHNIQUE USING SDLA AND DPOJET

5 Testing Using GRL-BSXPCI4BSE Software

Once the final stressed eye has been calibrated successfully, receiver jitter tolerance and margin testing can then be performed on the device under test (DUT). The DUT should have a Replica Channel of the same Insertion Loss as the Replica Channel used for calibration. The Replica Channel is removed when performing the DUT tests.

The GRL-BSXPCI4BSE software automates the receiver compliance and jitter tolerance testing, at the spec-defined or user-defined jitter frequency steps. The GRL software also supports nested loop testing of multiple parameters to facilitate silicon PVT testing or testing across multiple test conditions. When testing is completed, the results will be logged in an aggregated test report which can be generated into a PDF format.

Receiver device compliance ensures the receiver DUT is able to correctly interpret data from a received signal with valid voltage and timing characteristics by achieving an acceptable bit error ratio (BER) of less than 1E-12. The signal used for verifying receiver tolerance must contain the maximum allowable jitter, noise, and signal loss. The stressed receiver tolerance test should include various differential mode sinusoidal interference, minimum transmitter voltage amplitude, and jitter which includes random jitter and a sinusoidal periodic jitter component that is swept across specific frequency intervals.

The receiver DUT can operate in the Common Clock (CC) Refclk and Independent Refclk (IR) clock modes. For the CC clock mode, a single Refclk source is applied for both the BERT signal generator and the DUT along with SSC and SJ mask.

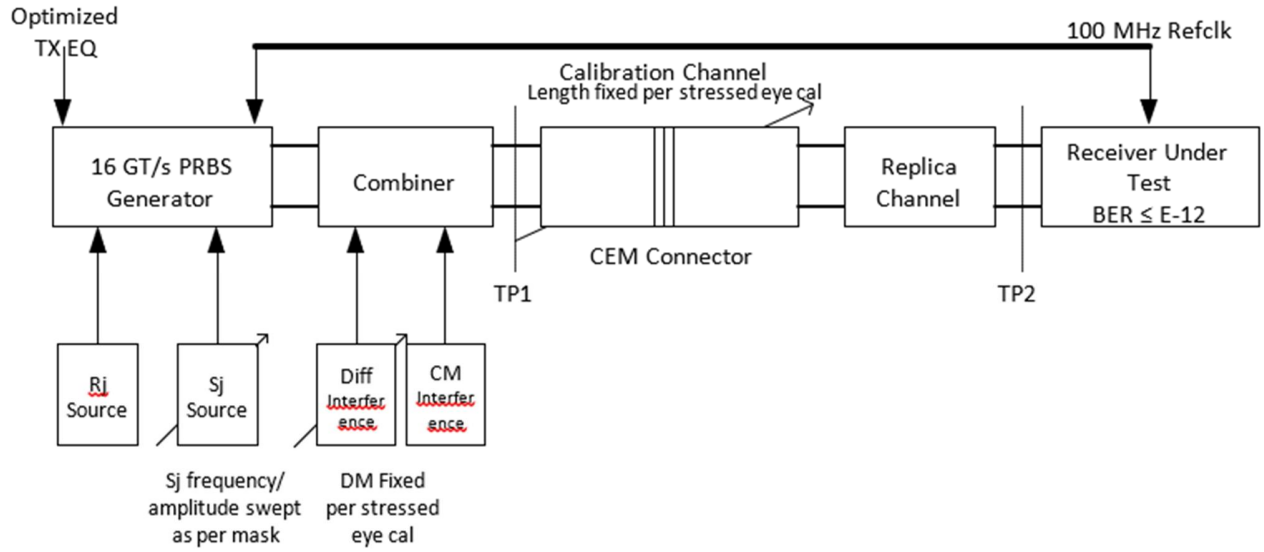

FIGURE 39. RX DUT STRESS JITTER TEST (CC MODE) BLOCK DIAGRAM FROM PCIE GEN 4 BASE SPECIFICATION

For the IR clock mode, two Refclk sources are applied for both the BERT signal generator and the DUT along with independent SSC and SJ mask.

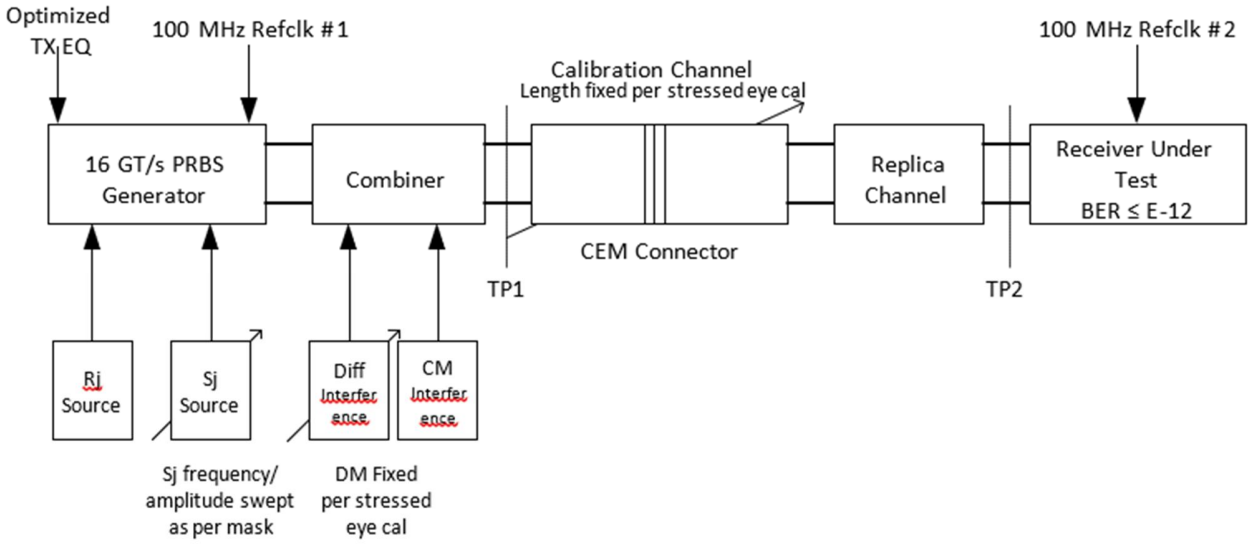

FIGURE 40. RX DUT STRESS JITTER TEST (IR MODE) BLOCK DIAGRAM FROM PCIE GEN 4 BASE SPECIFICATION

Once the stressed receiver tolerance test setup has been calibrated, the BERTScope transmits a modified compliance pattern to the receiver and monitors that the loopback pattern achieves a target BER that is less than 1E-12.

5.1 Test Setup for Testing the DUT

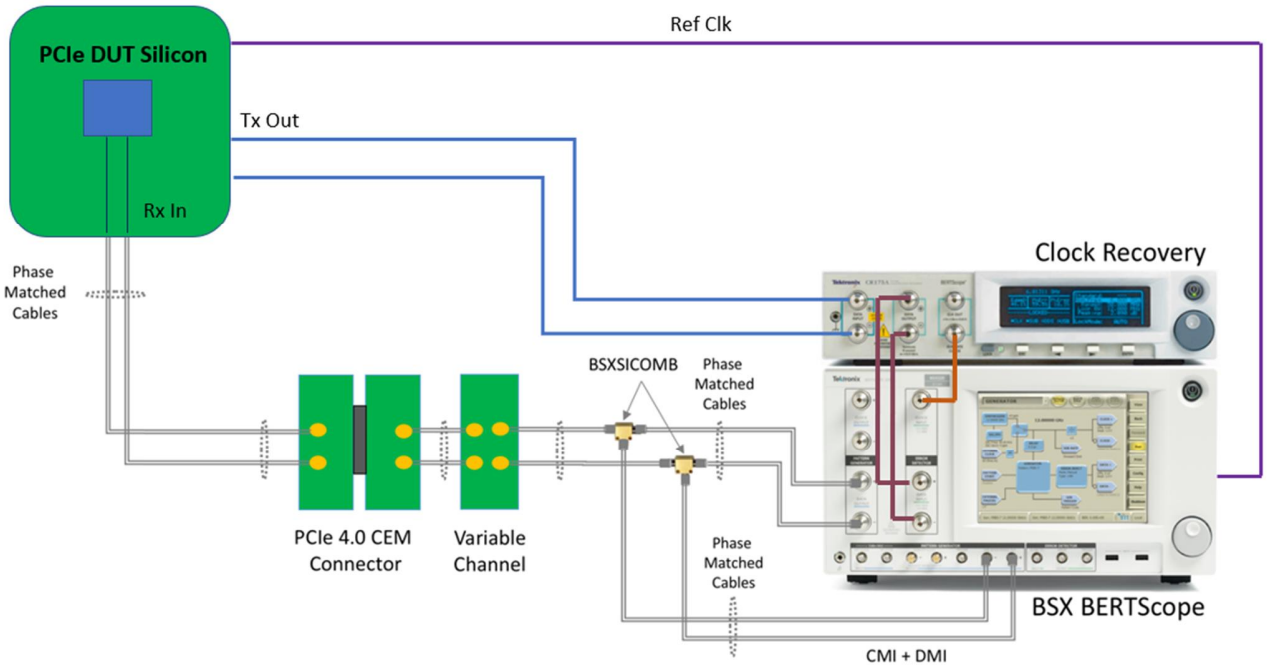

FIGURE 41. TYPICAL DUT TEST SETUP

Connection Steps:

1. Using back the same connections from the TP2 calibration setup, disconnect and remove the Scope and Replica Channel from the setup.
2. Connect the PCIe 4.0 CEM Connector Segment outputs to the DUT Rx inputs.
3. Connect the DUT Tx outputs to the Clock Recovery Unit (CRU) Data In.
4. Connect the CRU Data Out to the BERTScope Error Detector Data In.
5. Connect the CRU Subrate Clock Out to the BERTScope Error Detector Clock In.
6. Connect the BERTScope Ref Out to the DUT as Reference Clock (100 MHz).

5.1.1 Receiver Compliance Tests

Select Tests > Stress Voltage Jitter Test is selected as below if tests at the Compliance Jitter Limits are to be performed.

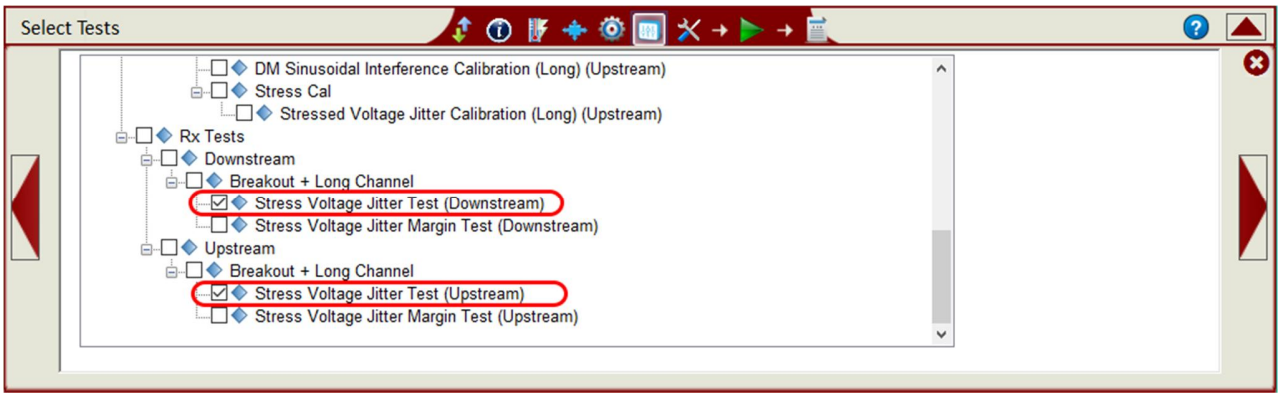

FIGURE 42. SELECTING COMPLIANCE TESTS

Once eye height and eye width have been calibrated, the Rx DUT will be connected to the far end of the calibration channel for testing. Optimization for the transmitter equalization will then be performed (equalization must also be optimized for the Rx DUT as well). SJ will be set to an initial value of 0.1 UI at 100 MHz that allows the receiver CDR to achieve lock which will then be swept over the frequency range as shown below, while maintaining fixed Tx equalization. The 100 MHz SJ initial tone will then be removed to perform testing for the appropriate swept SJ profile.

Note that an additional SJ tone at 210 MHz shall be present for all testing, while having the same amplitude as the 100 MHz SJ to achieve the target eye width minus 0.1 UI. This is not required if the SJ calibration is less than 0.1 UI.

The DUT must achieve a compliance BER of 10E-12 or lower for the entire swept SJ range. The Rx DUT is tested using an SJ mask in the 400 kHz to 1.0 MHz range and the 33 kHz single tone magnitude of 25 ns PP with 400 UI PP.

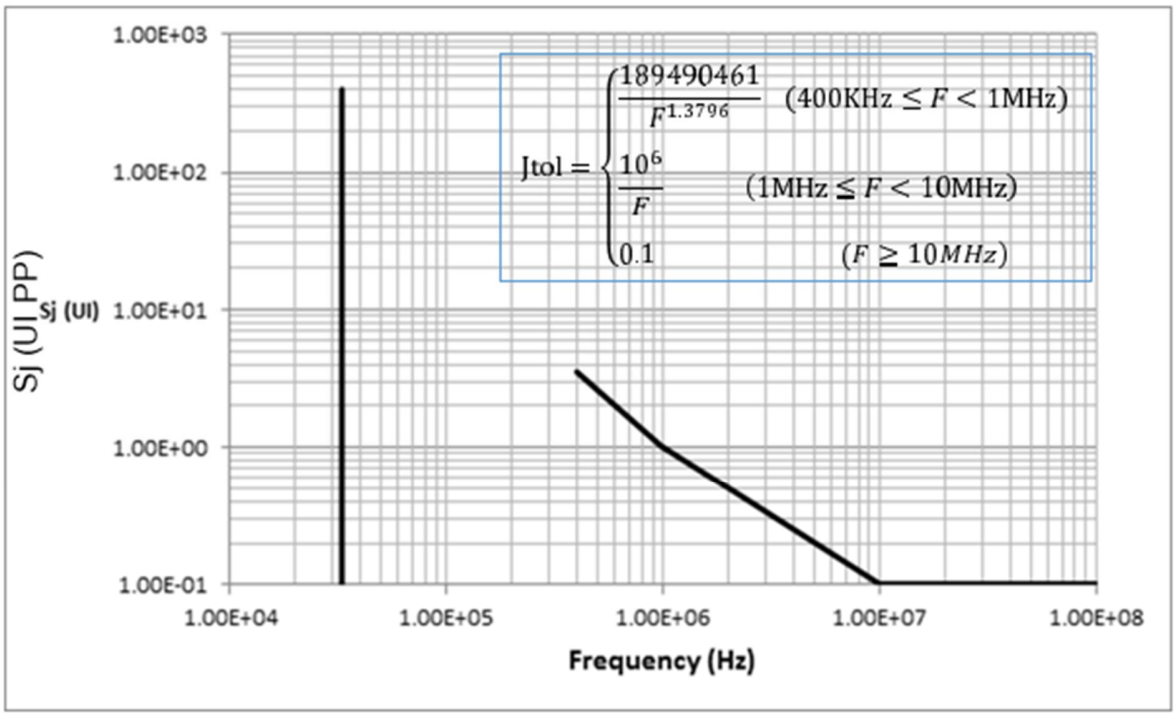

FIGURE 43. SJ MASK FUNCTION IN IR MODE FROM PCIE GEN 4 BASE SPECIFICATION

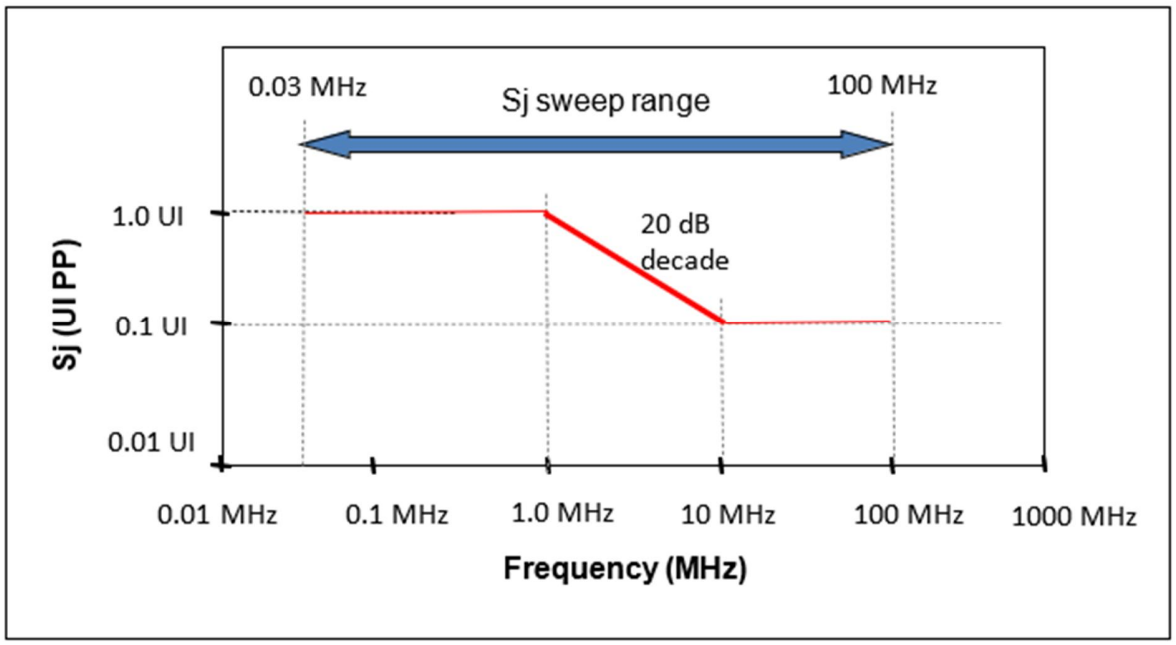

FIGURE 44. SJ MASK FUNCTION IN CC MODE FROM PCIE GEN 4 BASE SPECIFICATION

The stress jitter voltage tests are run from the same Run Tests page as shown in Figure 32.

5.1.2 Receiver Margin Tests

Select Tests > Stress Voltage Jitter Margin Test is selected as below if Jitter Margin testing is to be performed.

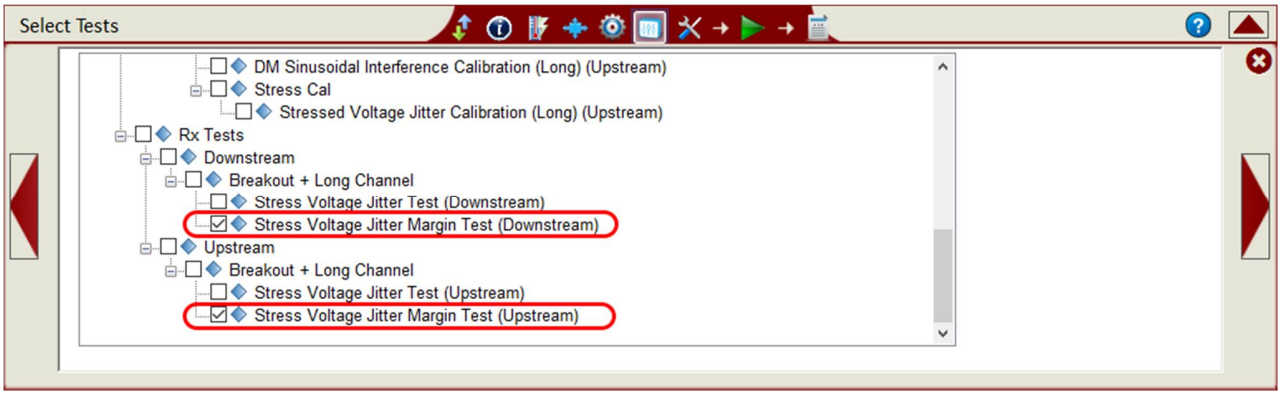

FIGURE 45. SELECTING MARGIN TESTS

Tests are run from the same Run Tests page as shown in Figure 32.

5.1.3 Receiver Sweep Tests

Select Tests > Stress Voltage Jitter Sweep Test is selected as below if Jitter Sweep testing is to be performed. The Jitter Sweep Test will only be available when the Advanced PVT features are enabled from the Configurations menu (*see Section 7 and Appendix for more details).*

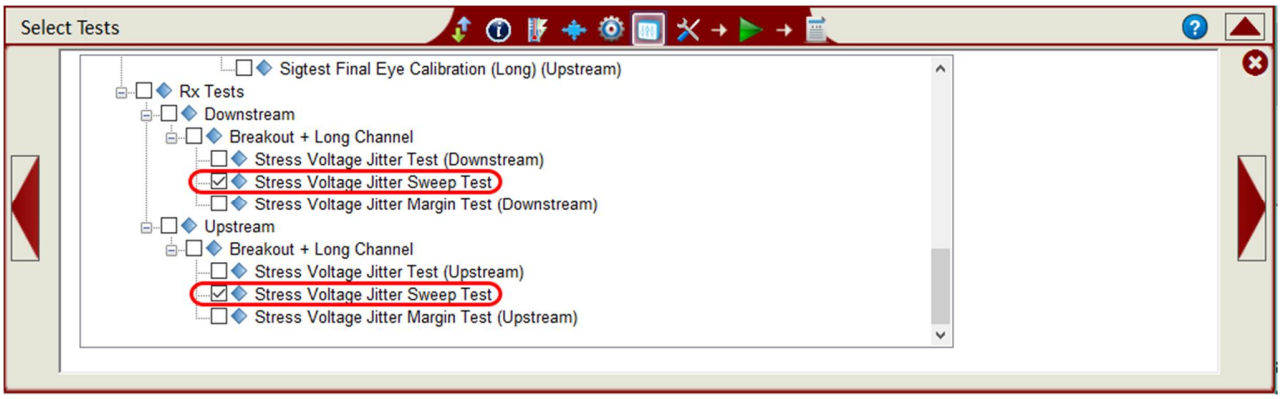

FIGURE 46. SELECTING ADVANCED SWEEP TESTS

Tests are run from the same Run Tests page as shown in Figure 32.

6 Interpreting Test Report

The **Report** page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate Report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

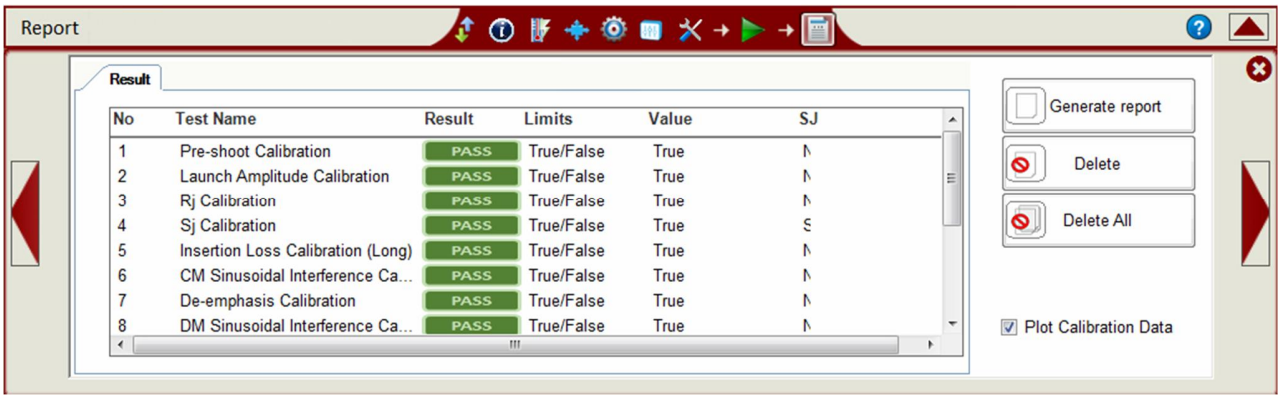

FIGURE 47. REPORT RESULTS PAGE

6.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.

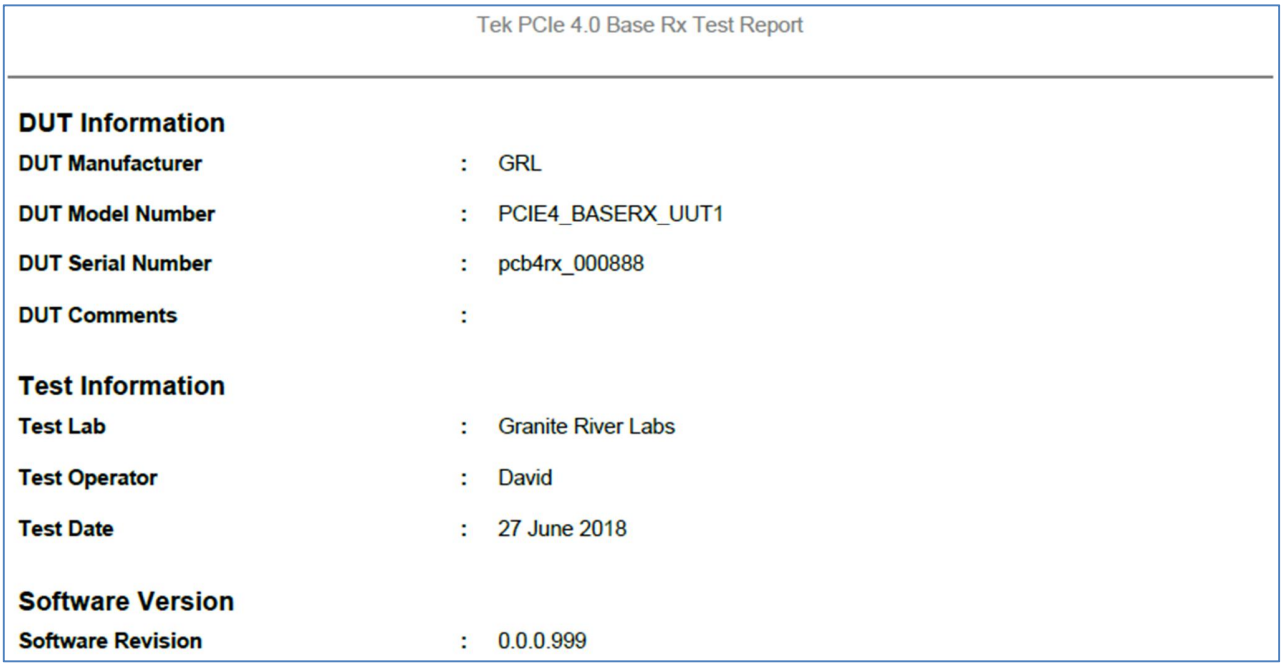

FIGURE 48. DUT INFORMATION

6.2 Summary Table

This portion is populated from the tests performed and its results. This gives an overall view of all the results and its test conditions.

No	TestName	Limits	Value	Results	SJ
1	Pre-shoot Calibration	True/False	True	Pass	
2	De-emphasis Calibration	True/False	True	Pass	
3	Launch Amplitude Calibration	True/False	True	Pass	
4	Rj Calibration	True/False	True	Pass	
5	Sj Calibration	True/False	True	Pass	SJLF_1
6	Sj Calibration	True/False	True	Pass	SJLF_2
7	Sj Calibration	True/False	True	Pass	SJLF_3
8	Sj Calibration	True/False	True	Pass	SJLF_4
9	Insertion Loss Calibration (Long) (Downstream)	True/False	True	Pass	
10	Eye Height and Eye Width Measurement (Long) (Downstream)	True/False	True	Pass	
11	CM Sinusoidal Interference Calibration (Long) (Downstream)	True/False	True	Pass	
12	DM Sinusoidal Interference Calibration (Long) (Downstream)	True/False	True	Pass	
13	Stressed Jitter Voltage Calibration (Long) (Downstream)	True/False	True	Pass	
14	Insertion Loss Calibration (Long) (Upstream)	True/False	True	Pass	
15	Eye Height And Eye Width Measurement (Long) (Upstream)	True/False	True	Pass	
16	CM Sinusoidal Interference Calibration (Long) (Upstream)	True/False	True	Pass	
17	DM Sinusoidal Interference Calibration (Long) (Upstream)	True/False	True	Pass	
18	Stress Jitter Voltage Calibration (Long) (Upstream)	True/False	True	Pass	
19	Stress Jitter Voltage Test (Long) (Downstream)	True/False	True	Pass	SJLF_1
20	Stress Jitter Voltage Test (Long) (Downstream)	True/False	True	Pass	SJLF_3
21	Stress Jitter Voltage Test (Long) (Downstream)	True/False	True	Pass	SJLF_4
22	Stress Jitter Voltage Test (Long) (Downstream) (Downstream)	True/False	False	Fail	SJLF_2

FIGURE 49. SUMMARY TABLE

6.3 Calibration Data Results

If Plot Calibration Data checkbox is checked, then the plots are shown in this part of the report.

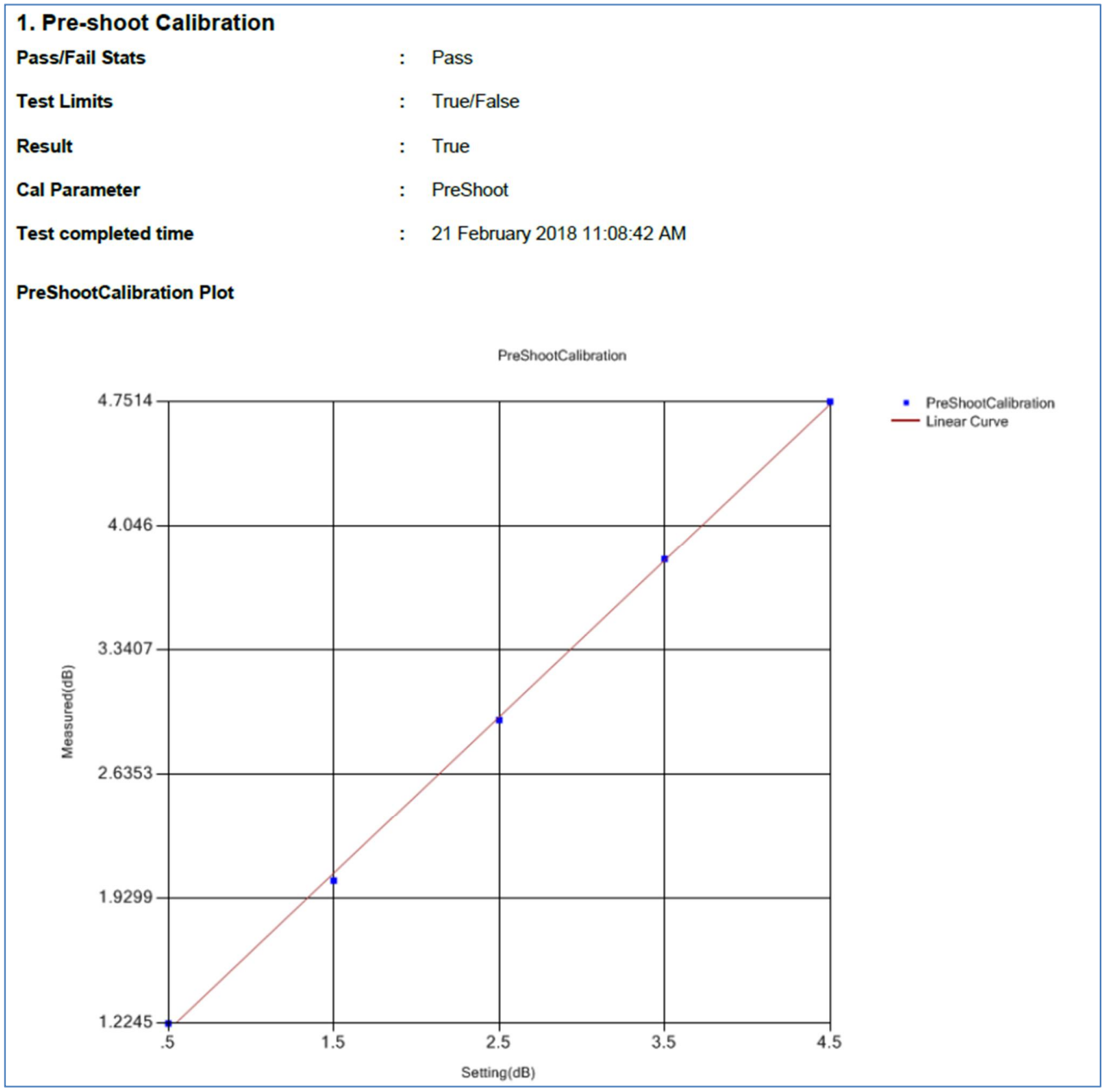

FIGURE 50. CALIBRATION RESULTS EXAMPLE

6.4 Compliance Test Results

27. Stress Jitter Voltage Test (Long) (Upstream) [SJLF_4]		
Pass/Fail Stats	:	Pass
Test Limits	:	True/False
Result	:	True
Test Frequency	:	100 MHz
ISI Generator	:	Artek
Preshoot (dB)	:	0 (0)
DeEmphasis (dB)	:	-6 (-6.35)
RJ (ps RMS)	:	1 (0.24)
SJ (ps)	:	12.5 (0.17)
Amplitude (mV)	:	500 (330)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	11.06383039056 (26.2475834324656)
CM Freq (MHz)	:	120
CMSI (mV)	:	150 (169228.754408806)
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	12.5 (0.17229946287562)
Max Error Allowed	:	0
Error Counts	:	0
Test completed time	:	20 February 2018 22:47:36 PM

FIGURE 51. COMPLIANCE TEST RESULTS EXAMPLE

6.5 Margin Tests Results

29. Stress Jitter Voltage Margin Test (Long) (Downstream) [SJLF_2]		
Pass/Fail Stats	:	Fail
Test Limits	:	True/False
Result	:	False
ISI Generator	:	Artek
Preshoot (dB)	:	0 (0)
DeEmphasis (dB)	:	-6 (-6.35)
RJ (ps RMS)	:	1 (0.24)
Amplitude (mV)	:	350 (230)
DMSI Freq (GHz)	:	2.1
DMSI (mV)	:	16.3780929451514 (42.6636011745818)
CM Freq (MHz)	:	120
CMSI (mV)	:	150 (168440.228264395)
SJ Tone Freq (MHz)	:	210
SJ Tone (ps)	:	12.5 (0.17229946287562)
Sj Specs	:	125 UI
Max Error Allowed	:	0
Last Passing Sj	:	-900000000000000000000000000.0000 GUI
Test completed time	:	20 February 2018 22:06:29 PM

FIGURE 52. MARGIN TEST RESULTS EXAMPLE

7 Additional Parameters Configuration

Select  from the main menu to access the Configurations page.

Set any of the available parameters required for measurement as described below. To return all parameters to their default values, select the 'Set Default' button.

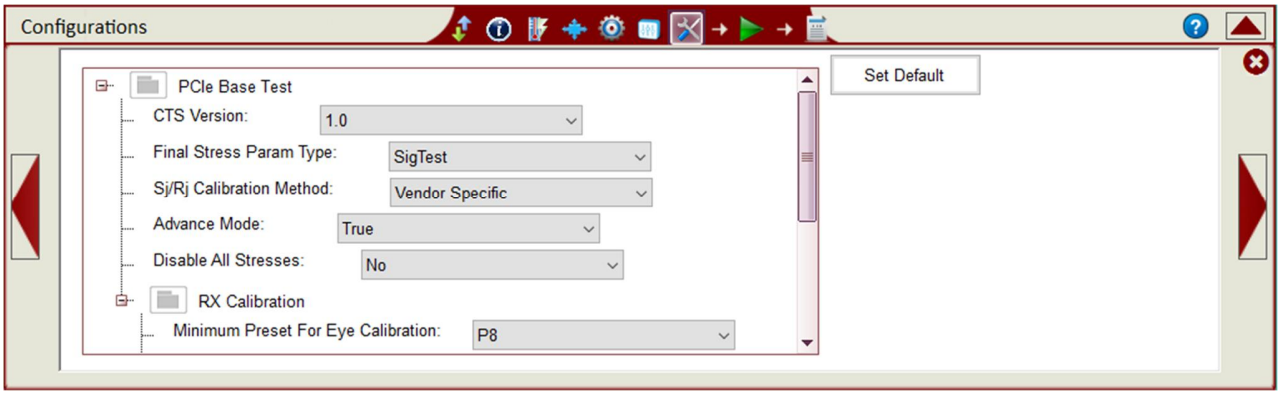

FIGURE 53. ADDITIONAL PARAMETERS CONFIGURATION PAGE

TABLE 3. PARAMETERS DESCRIPTION

Parameter	Description
CTS Version	Select the Version of the CTS that is used as the reference specs to perform calibration and tests. (*Note: This selection causes the Select Tests page to display different test lists for the specific CTS version.)*
Final Stress Parameter Type	Select either the SigTest or Seasim application to be used for post processing signal quality testing. Make sure that the SigTest or Seasim application is already installed in the test controller system.
SJ/RJ Calibration Method	Select either the SigTest or a vendor specific based methodology to be applied during calibration of SJ or RJ.
Advanced Mode	Select 'True' to enable Advanced PVT Automation control to support repeated testing within sequences of parameter values, which are applied to the DUT during testing.
Disable All Stresses	Select the option to turn off all stresses applied during testing.
Minimum & Maximum Preset for Eye Calibration	Select the range of presets to be applied for stressed eye calibration.
Parallel SigTest Run	Select 'True' to enable running the SigTest application in parallel mode with the Long Channel TP2 calibration.
SigTest Acquisitions (N)	Enter the number of measurements to acquire when running the SigTest application over the Long Channel TP2 calibration.
SigTest Version	Enter the Version number of the SigTest application if used.
Maximum Thread Spawn	Set the maximum process threads to generate for checking the Rx device functionality during Long Channel TP2 calibration.
Custom ISI Trace	Select 'True' to enable generating custom ISI trace for ISI calibration.

Auto DUT Reset	Select the method to perform automated reset of the DUT using a 'IP Power Switch' or 'None' if not using this function.
Power Switch IP Address & Credentials	If 'IP Power Switch' is selected to perform auto reset of the DUT, enter the respective IP address and instrument ID for the switch to connect with the GRL software.

8 Saving and Loading Test Sessions

The GRL-BSXPCI4BSE software enables Calibration and Test Results to be created and maintained as a 'Live Session' in the application. This allows you to quit the application and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To save a session, with all of the PVT parameter information, the test results, and any waveforms, use the "Options" command on the menu bar, then the "Save Session" command.

To load a session back into the software, including the saved parameter settings, use the "Options" command on the menu bar, then the "Load Session" command.

To create a New session and return the application back to a default configuration, use "Options" command on the menu bar, then the "New Session" command.

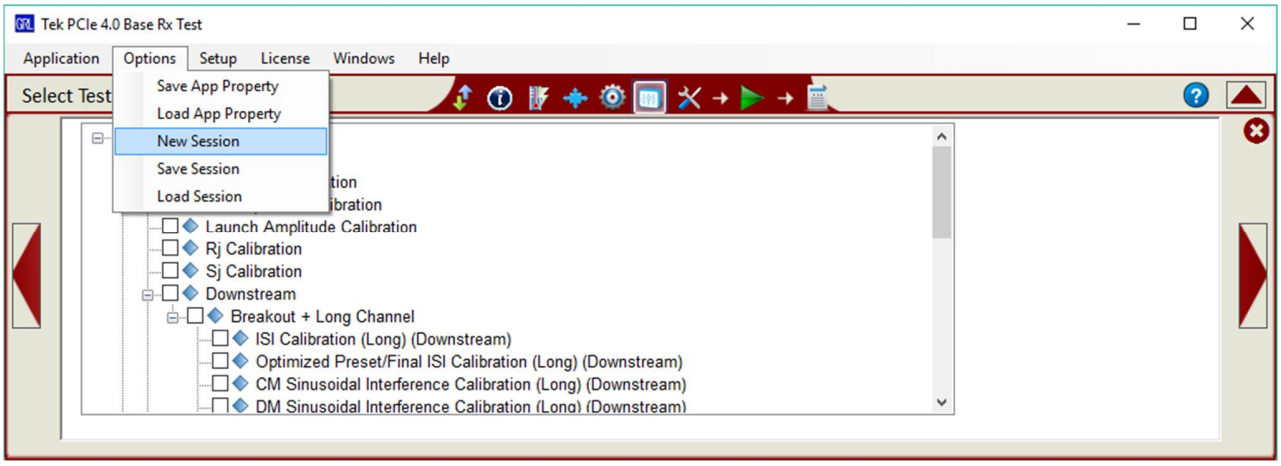

FIGURE 54. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

9 Appendix A: Implementation Method Using Automation

The GRL-BSXPCI4BSE software automates Calibration and Testing of PCIe Gen 4 Receivers. This section provides sample methodology to automate PCIe Gen 4 Base Rx calibration using GRL-BSXPCI4BSE at 16 GT/s, which should ensure Receiver Impairment adjustments on the BERTScope are accurate before running DUT compliance tests.

9.1 Perform Calibration at TP1

9.1.1 Pre-shoot Calibration

The **Caltable** method is used to calibrate pre-shoot:

1. Set 800mV (p-p) amplitude.
2. Set 0dB for de-emphasis.
3. Measure:

   1dB, then measure pre-shoot, record
   2dB, measure again, record
   3dB, measure again, record
   .....
   5dB, measure again, record.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured pre-shoot at Min 1dB and Max 4dB.

9.1.2 De-emphasis Calibration

The Caltable method is used to calibrate de-emphasis:

1. Set 800mV (p-p) amplitude.
2. Set 0dB for pre-shoot.
3. Measure:

   -8dB, then measure de-emphasis, record
   -7dB, measure again
   -6dB, measure again
   .....
   0dB.

4. Plot a Caltable graph.
5. Passing criteria is to obtain measured de-emphasis at Min -1dB and Max -6dB.

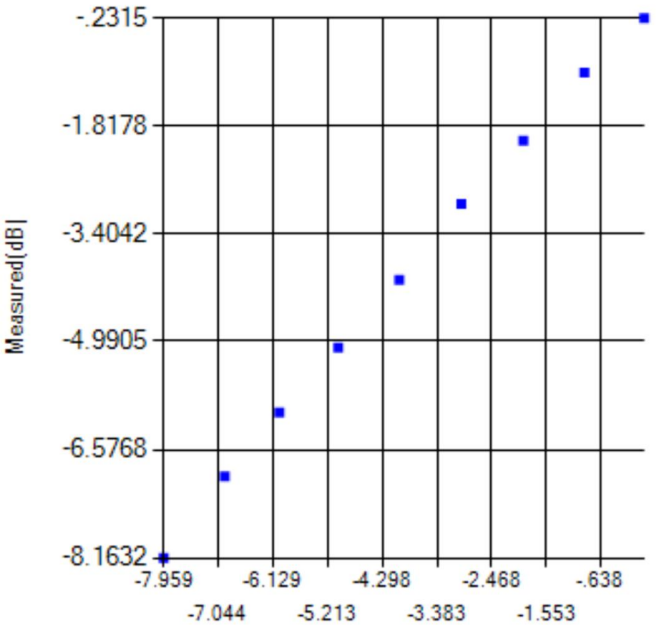

FIGURE 55: DE-EMPHASIS CALIBRATION CALTABLE GRAPH

9.1.3 Launch Amplitude Calibration

The Caltable method is used to calibrate Launch Amplitude:

1. Initialize BERTScope.
2. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
3. Set 300mV Amplitude, then measure the amplitude in scope, record it.
4. Increase 100mV on each iteration, measure the amplitude in scope, until measured amplitude meets or exceeds 1200mV.
5. Plot a Caltable graph.
6. Passing criteria is to obtain MEAN value of Launch Amplitude measurement at 720-800mV.

9.1.4 RJ Calibration

The Caltable method is used to calibrate RJ:

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
4. Set All Stresses to 0mV.
5. Set 1100 Pattern on BERTScope.
6. Set intrinsic jitter value (%UI) as base value in RJ.
7. Measure RJ (in ps(RMS)) from scope using DPOJET, record.
8. Increase 5%UI on each iteration, measure RJ from scope, until measured RJ meets or exceeds 1.0ps(RMS).
9. Plot a Caltable graph.
10. Passing criteria is to obtain measured RJ at 1.0ps(RMS).

9.1.5 SJ Calibration

The Caltable method is used to calibrate SJ:

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
4. Set All Stresses to 0mV.
5. Set 1100 Pattern on BERTScope.
6. Set the SJ Frequency of the first Permutation (30kHz, 1MHz, 10MHz, 100MHz).
7. Set 0 (%UI) as base value in SJ, measure SJ (in ps) from scope using DPOJET, record.
8. Increase 10%UI on each iteration for SJ Frequency 1MHz, 10MHz, 100MHz; Increase 20%UI on each iteration for SJ Frequency 30KHz.
9. Measure SJ from scope until measured SJ meets or exceeds 62.5ps for 30KHz SJ Frequency or 20.0ps for SJ Frequency 1MHz, 10MHz, 100MHz.
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 6ps (p-p) and Max 62.5ps (p-p) for 30KHz, 20.0ps (p-p) for 1MHz, 10MHz, 100MHz.
12. Proceed to next permutation.

9.1.6 SJ Tone (33KHz SSC) Calibration

The Caltable method is used to calibrate SJ Tone:

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stresses to 0mV.
5. Set 1100 Pattern on BERTScope.
6. Set SJ2 Frequency (210MHz).
7. Set 0 (%UI (p-p)) as base value in SJ2, measure SJ (in ps (p-p)) from scope using DPOJET, record.
8. Increase 0.1UI (p-p) on each iteration.
9. Measure SJ from scope until measured SJ meets or exceeds 10ps (p-p).
10. Plot a Caltable graph.
11. Passing criteria is to obtain measured SJ at Min 5ps (p-p) and Max 10ps (p-p).

9.2 Perform Calibration at TP2

Calibrations at TP2 can be performed for Downstream (for Host) or Upstream (for Device).

9.2.1 Insertion Loss Calibration *(Applicable only if CTS version '0.7' is being used as the measurement reference method)*

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
4. Set All Stresses to 0mV.
5. Set clk/256 Pattern on BERTScope.
6. Use 31"+5" trace on Fixed ISI board.
7. Trigger the waveform on scope to display waveform.
8. Save the waveform as .dat file (Y only).
9. Convert the saved waveform to Seasim-compatible waveform (step response) with X component (start from 0), and save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain the .log file and .csv file from Seasim.
13. Read the insertion plot from .csv. Check against upper and lower limit of specs.
14. Use GRL script to plot the output of insertion loss curve with specs.
15. If the calibration fails, increase the trace length by a small amount and repeat the calibration process.
16. Passing criteria is to ensure that 60% of the curve is within the upper and lower limit.

9.2.2 ISI Calibration (CEM Connector Channel + Replica Channel) *[Applicable only if CTS version '1.0' is being used as the measurement reference method AND supported ISI Generator of either PCIe ISI Board or Artek is used.]*

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stresses to 0mV.
5. Set Clk/256 Pattern on BERTScope.
6. Start with PCIe CEM Variable ISI board Lane 3.
7. Trigger waveform on scope to display waveform.
8. Save waveform as .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (start from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for IL calculation.
11. Run Seasim with config file and step response.
12. Obtain .log file and .csv file from Seasim.
13. Record insertion loss at 8GHz in dB from .csv file. Check against upper and lower specification limits.
14. If insertion loss at 8GHz is above 27dB, decrease Lane number and repeat steps 7 to 13.
15. If insertion loss at 8GHz is below 30dB, increase Lane number and repeat steps 7 to 13.
16. Insertion loss (IL) profile curve will be generated to determine Lane number that corresponds to 27dB, 27.5dB, 28dB, 28.5dB, 29.5dB and 30dB losses for use in next step of calibration.

9.2.3 Common Mode (CM) Sinusoidal Interference Calibration

The Caltable method is used to calibrate CM-SI:

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
4. Set All Stresses to 0mV.
5. Set All Zero Pattern on BERTScope.
6. Set the ISI % value based on above calibrated data.
7. Set Sine Wave to 120MHz.
8. Set 0.5V as base value.
9. Measure Amplitude (in mV) from scope, record.
10. Increase 0.5V on each iteration, measure Amplitude from scope until measured value meets or exceeds 150mV.
11. Plot a Caltable graph.
12. Passing criteria is to obtain measured CM-SI at Min 100mV and Max 150mV.

9.2.4 Differential Mode (DM) Sinusoidal Interference Calibration

This calibration is to ensure that the waveform achieves the calibrated eye height.

The Caltable method is used to calibrate DM-SI:

1. Initialize BERTScope.
2. Set 800mV (p-p) amplitude (based on calibrated value).
3. Set to 0dB Pre-shoot and De-emphasis obtained from Caltable, as measured above.
4. Set All Stresses to 0mV.
5. Set All Zero Pattern on BERTScope.
6. Set the ISI % value based on above calibrated data.
7. Set Common Mode Output to OFF.
8. Set BERTScope SI-Out to External.
9. Set the Frequency to 2.1GHz.
10. Set 0.89dBm as base value in SI-OUT amplitude of BERTScope.
11. Measure Amplitude (in mV) from scope, record.
12. Increase 0.174dBm/10mV on each iteration, measure Amplitude from scope until measured value meets or exceeds 30mV.
13. Plot a Caltable graph.
14. Passing criteria is to obtain measured DM-SI at Min 15mV and Max 40mV.

9.2.5 Optimized Preset/Final ISI Calibration

This calibration is to determine the optimum Preset, Equalization (EQ) gain, and final ISI trace to be used for final eye calibration in the next step.

1. Initialize BERTScope.
2. Set 500mV (p-p) amplitude (based on calibrated value).
3. Set 0dB Pre-shoot and De-emphasis obtained from Caltable as measured above.
4. Set All Stresses to 0mV.
5. Set Clk/256 Pattern on BERTScope.
6. Change to ISI trace at 27dB loss.
7. Set Preset to P5.
8. Trigger waveform on scope to display waveform.
9. Save waveform to .dat file (Y only).
10. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
11. Create Seasim config file with predefined values for Eye Opening calculation, starting with CTLE at 8.00dB gain.
12. Run Seasim with config file and step response.
13. Obtain .log file from Seasim.
14. Record eye height (EH) and eye width (EW) from .log file.
15. Calculate Area = EH x EW.
16. Repeat step 11 with CTLE DC gain of 0.25dB incremental up to 9.5dB. Record the DC gain for the maximum Area and EH and EW obtained.
17. Change Preset to P6. Repeat steps 8 to 16.
18. Determine optimized EH and EW with maximum Area from either P5 or P6 Preset.

19. If optimized EH is above 15mV and EW above 0.3UI, repeat step 6 by adding on 0.5dB ISI up to 30dB.
20. If optimized EH or EW falls below specification (15mV or 0.3UI), the last ISI trace and its associated optimized Preset and EQ shall be applied in the next step of calibration.
21. Once EH and EW at 0, 5, 10, 15mV are obtained, plot Caltable graph.

9.2.6 Stress Jitter Voltage Eye Calibration

This calibration is to ensure that the waveform achieves the calibrated eye width and eye height.

1. Initialize BERTScope.
2. Set 500mV (p-p) amplitude (based on calibrated value).
3. Set to optimized Preset obtained from previous calibration step.
4. Set All Stresses to 0mV.
5. Set Clk/256 Pattern on BERTScope.
6. Change to ISI trace obtained from previous calibration step.
7. Trigger waveform on scope to display waveform.
8. Save waveform to .dat file (Y only).
9. Convert saved waveform to Seasim-compatible waveform (step response) with X component (starting from 0). Save to xxx_vict.rfstep1. The _vict.rfstep1 format consists of time[SPACE]Voltage_level[New Line].
10. Create Seasim config file with predefined values for Eye Opening calculation, starting with 0mV DM-SI.
11. Run Seasim with config file and step response.
12. Obtain .log file from Seasim.
13. Read eye height (EH) and eye width (EW).
14. Record EH vs. DM, and EW vs. DM for 500mV.
15. Increase DM-SI (in Seasim config) to 5mV, run Seasim again, obtain EH and EW.
16. Once EH and EW at 0, 5, 10, 15mV are obtained, plot Caltable graph.
17. If EH and EW do not fall within 0.3UI and 15mV, increase SJ by 0.1UI. Repeat method to obtain EH and EW by adjusting DM.
18. If EH and EW do not fall within 0.3UI and 15mV after SJ variation, adjust Amplitude and repeat method to obtain EH and EW.
19. Repeat until EH and EW fall within specifications.
20. Record measured Amplitude, SJ, and DM.

9.2.7 DM Optimization and Final Eye Calibration Using SigTest

This calibration applies the SigTest post processing method to determine the final eye height and eye width. *(Note: SigTest Final Eye Calibration is applicable only for CTS version '1.0'.)*

1. Initialize BERTScope.
2. Set to final amplitude obtained from previous calibration step.
3. Set to optimized Preset obtained from calibration step of 9.2.5 Optimized Preset/Final ISI Calibration.
4. Set DM and SJ to calibrated values obtained from previous calibration step.
5. Set RJ to calibrated value from 9.1.4 RJ Calibration step.
6. Change Pattern on BERTScope to PCIe Compliance Pattern.

7. Change to ISI trace obtained from calibration step of 9.2.5 Optimized Preset/Final ISI Calibration.
8. Trigger waveform on scope and capture waveform.
9. Run SigTest (current version 4.0.38) using *'PCIE_4_0_RX_CAL\PCIe_4_16G_Rx_CAL_CTLE_XdB'* template, where XdB is the DC gain obtained from calibration step of 9.2.5 Optimized Preset/Final ISI Calibration.
10. Record eye height (EH) and eye width (EW).
11. If EH and EW are not within specifications, adjust amplitude and SJ until EH and EW achieve target specs.

10 Appendix B: PVT Automation Features

The GRL-BSXPCI4BSE software provides support for repeated testing within sequences of parameter values, which are applied to the DUT during the tests. These features are enabled by the “Advanced Mode” setting in the software Configurations menu. Advanced sequencing can be used to manage repetitive test loops needed when performing PVT (Process, Voltage, Temperature) characterization on the PCIe Gen 4 transceiver silicon.

10.1 Available Parameters

The following table lists the parameters that can be controlled through PVT Automation. Up to eight values may be specified for each parameter.

TABLE 4. AVAILABLE PARAMETERS

Symbol	Parameter	Units
RJ	Random Jitter	Picoseconds
ISI	Inter Symbol Interference	Percent of UI
SJ	Sinusoidal Jitter	UI
Amplitude	Launch Voltage	Millivolts
CM	Common Mode (noise source)	Millivolts
DM	Differential Mode (noise source)	Millivolts

10.2 Applicable Test

The GRL-BSXPCI4BSE software provides PVT Automation control for running the Stressed Voltage Jitter Sweep test for the Long Channel. PVT parameters have no effect on other tests in the list.

10.3 Setting Up PVT Automation

1. To enable advanced PVT features in GRL-BSXPCI4BSE, in the Configurations menu, set Advance Mode to “True”.

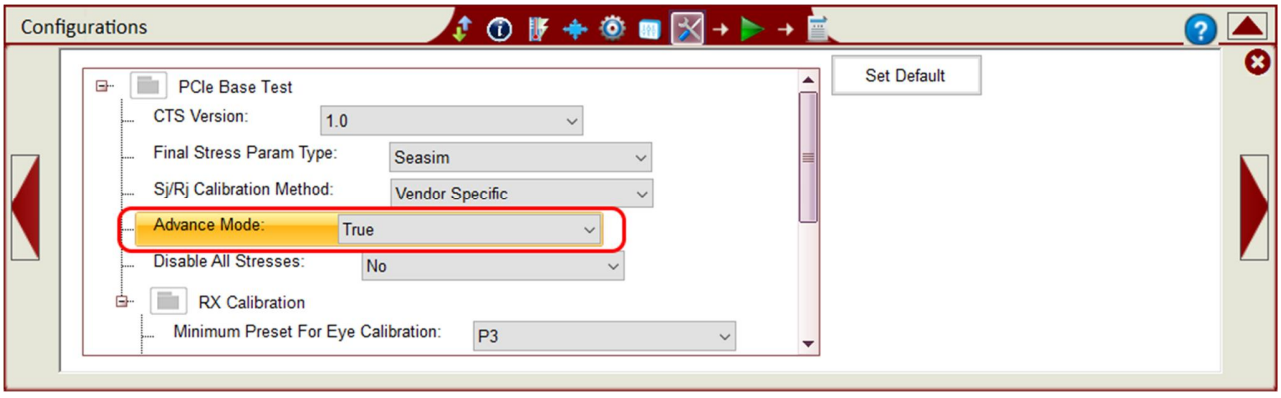

FIGURE 56. ENABLE PVT FUNCTION

2. The PVT Configuration icon  will appear on the toolbar menu.
3. Select the PVT Configuration icon to access the PVT Configuration page.

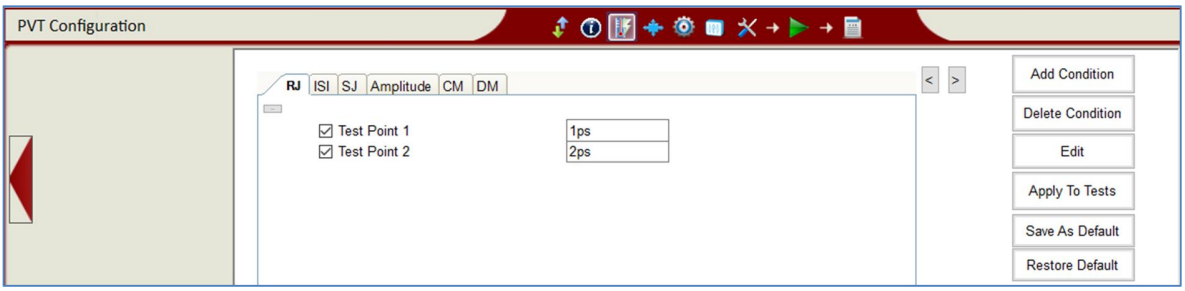

FIGURE 57. PVT CONFIGURATION PAGE

4. Add a parameter to the selected test by selecting "Add Condition" as shown below, which selects 'SJ_1' as the new condition group. No drop-down menu of allowed parameter names is provided (see Table 4). A short description may be provided. This description, and the names of the individual step 'Variables' are all included in the Test Report.

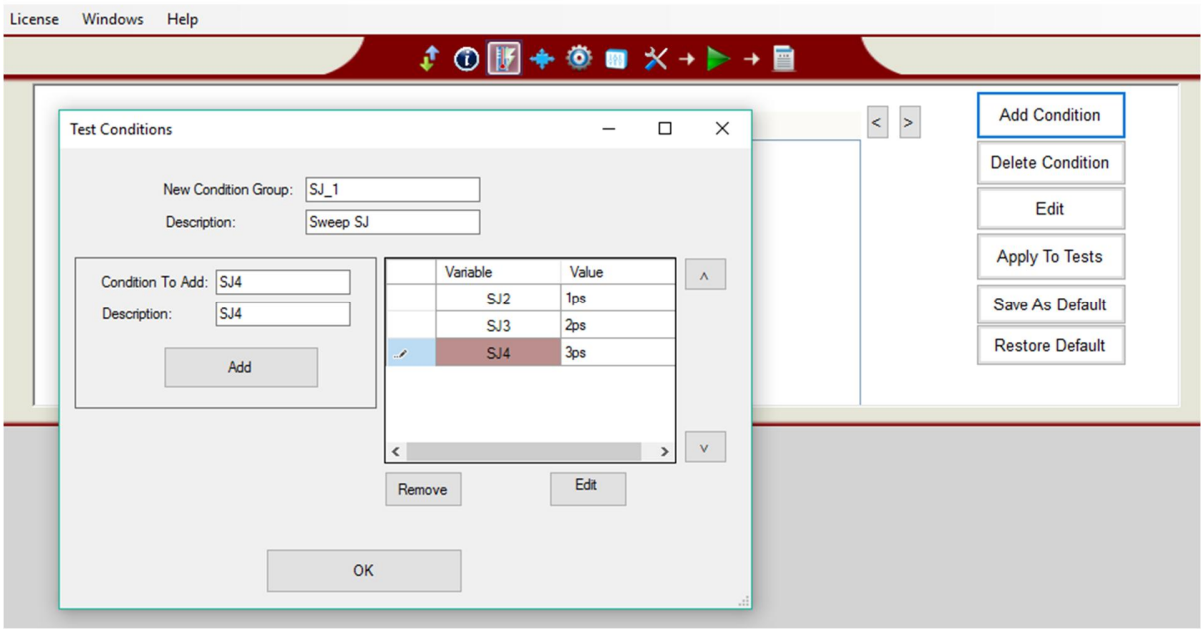

FIGURE 58. ADD FIRST PVT AUTOMATION PARAMETER

5. Enter one or more parameter values for the steps of the test condition sequence. Make sure to include the suffix for the units, and to assign values which are appropriate for that parameter according to the PCIe Gen 4 specification. The following example shows four steps for parameter 'SJ', named 'SJ1', 'SJ2', 'SJ3' and 'SJ4', and assigned values 1ps, 1.2ps, 1.8ps and 3ps, respectively. When finished editing the Test Conditions, select "OK". Note that individual steps may be selected, then edited or removed from the list.

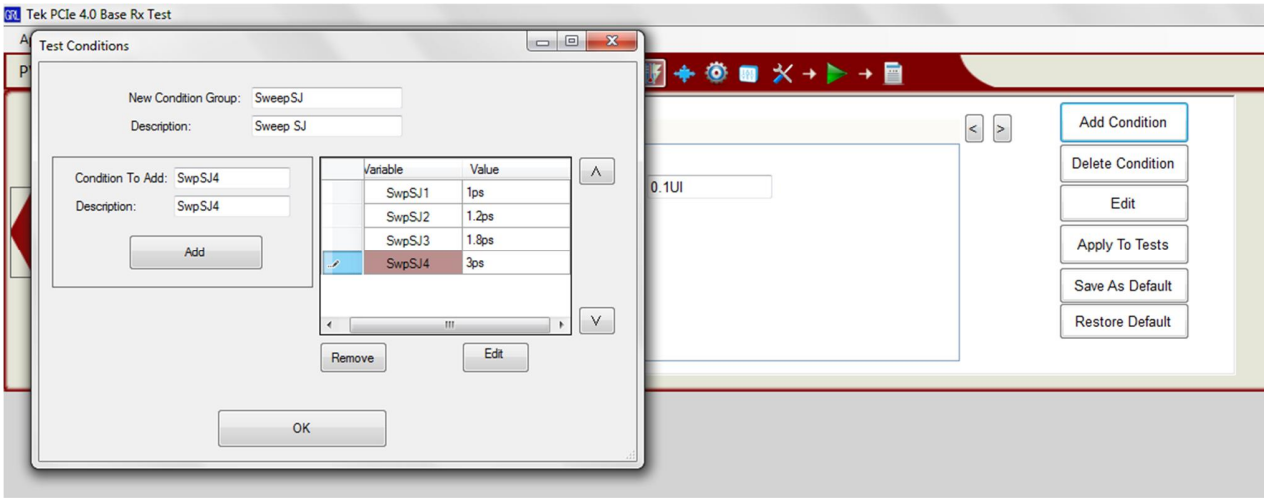

FIGURE 59. SET EACH PVT PARAMETER VALUE IN SEQUENCE

6. Add a second parameter as shown below, which adds 'SweepISI', with three values, each expressed as a percentage.

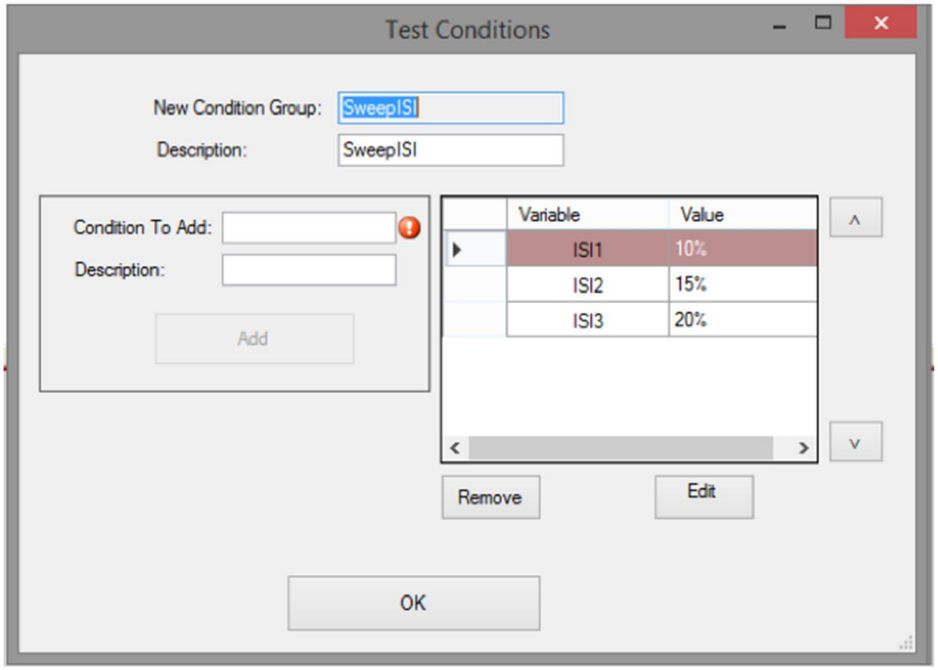

FIGURE 60. ADD SECOND PVT PARAMETER

7. Repeat setting values to each of the allowed parameters. Those parameters which are not set up with explicit values will use the default value.

8. From the menu, apply the sequences of parameters to the selected tests (see figures below), which builds a “Stress Test Plan”.

FIGURE 61. APPLY TO TESTS

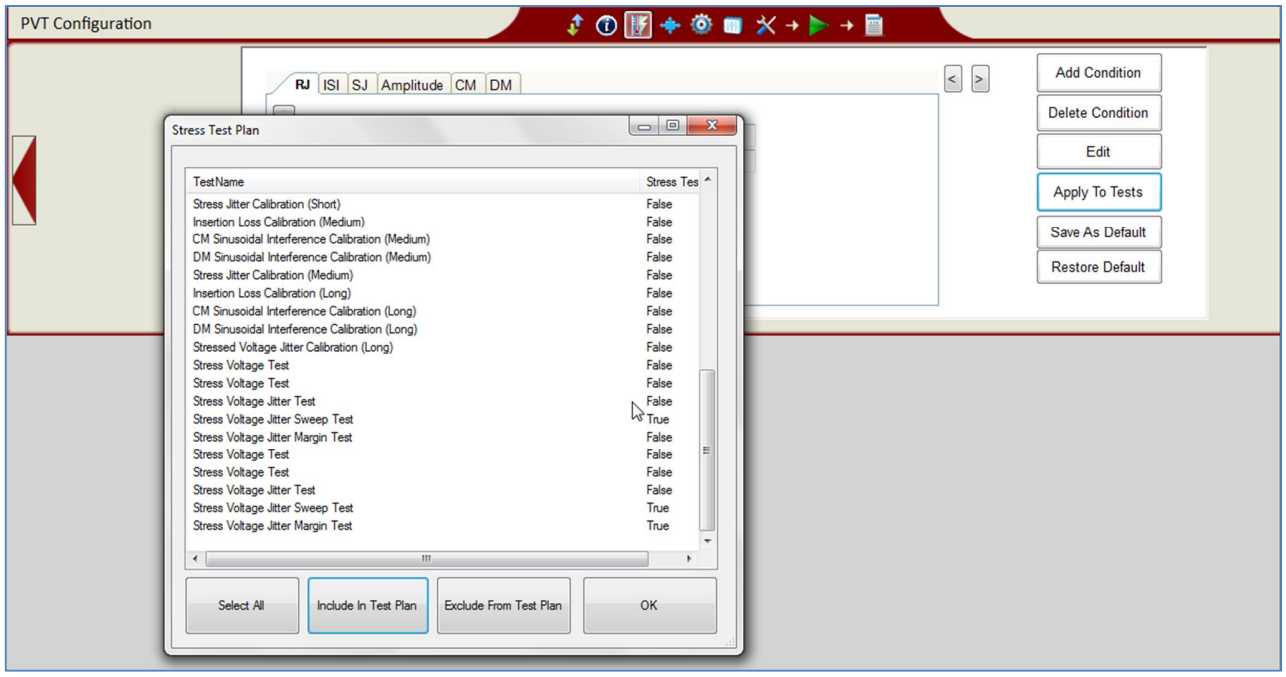

FIGURE 62. SELECT APPLICABLE TESTS

9. Select the PVT tests to run as shown below.

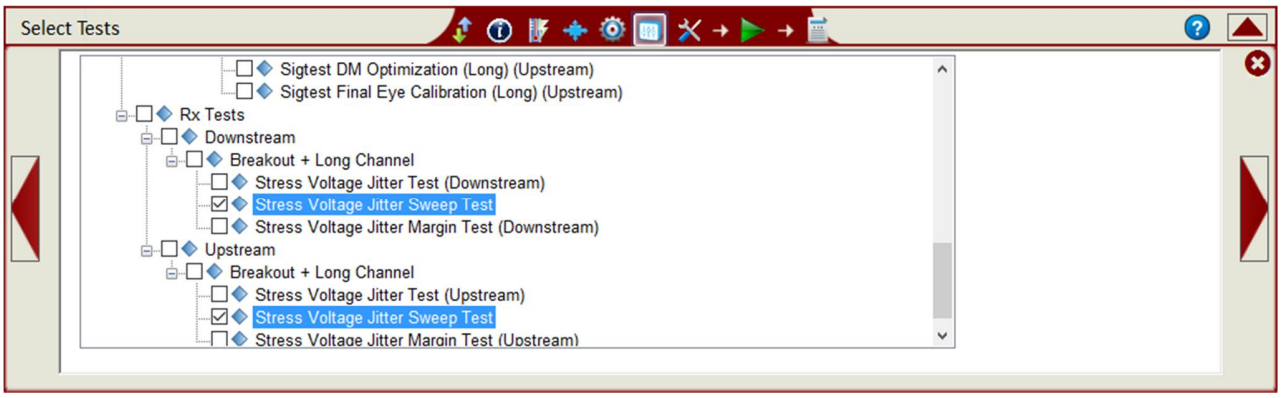

FIGURE 63. SELECT PVT TESTS TO RUN

10. Run the tests using the “Run Tests with PVT” button as shown below.

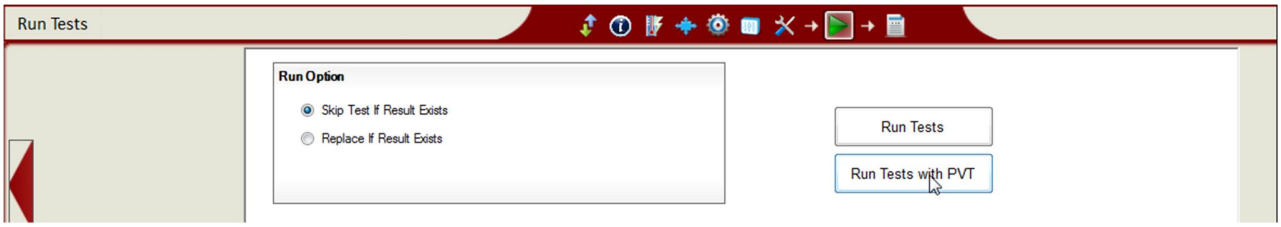

FIGURE 64. RUN TESTS WITH PVT

After selecting the parameters and their ranges, user may also select from a list of search algorithms to find the bounds of jitter margin.

10.4 Test Results

Results from the selected PVT tests, each using one or more defined PVT parameters, are collected in the Test Report.

The selected tests are all run, one after the other, for each permutation of the parameters. The parameter defined first is varied most slowly; the last-defined parameter is defined most quickly.

For example, considering the parameters and tests defined and selected in Figure 58 to Figure 63 will iterate as shown in Table 5. (Individual parameter step names are not shown.)

TABLE 5. PVT AUTOMATION – ITERATION SEQUENCE EXAMPLE

Seq.	SJ	ISI	Tests
1	1.0ps	10%	All 4 Parameter Sweeping Tests
2	1.2ps	15%	All 4 Parameter Sweeping Tests
3	1.8ps	20%	All 4 Parameter Sweeping Tests
4	3.0ps	10%	All 4 Parameter Sweeping Tests
5	1.0ps	15%	All 4 Parameter Sweeping Tests
6	1.2ps	20%	All 4 Parameter Sweeping Tests
7	1.8ps	10%	All 4 Parameter Sweeping Tests
8	3.0ps	15%	All 4 Parameter Sweeping Tests
9	1.0ps	20%	All 4 Parameter Sweeping Tests
10	1.2ps	10%	All 4 Parameter Sweeping Tests
11	1.8ps	15%	All 4 Parameter Sweeping Tests
12	3.0ps	20%	All 4 Parameter Sweeping Tests

11 Appendix C: ARTEK CLE Model Series Installation

11.1 ISI Generator Driver Installation

If using a Artek CLE Model for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the Artek unit to the PC being used as the controller using a USB 2.0 cable.
2. Turn on the front panel power switch on the Artek unit.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for Artek has been installed, you will see a 'bang' in the Device Manager.

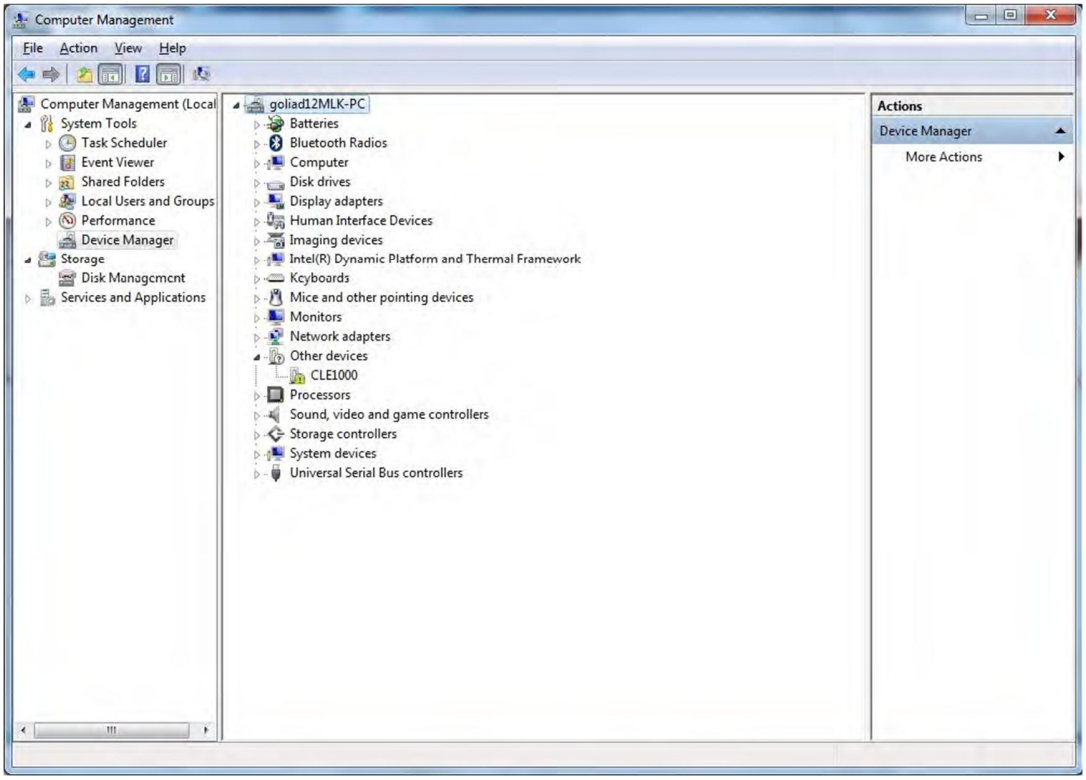

FIGURE 65. DEVICE MANAGER WINDOW

4. To install the Artek driver, go to http://www.aceunitech.com/support.html and download the Control Software package for the CLE Series.
5. Unpack the CLE Series Software .zip file.
6. Install the CLE Series Driver:
   a) In Device Manager, right-click on **CLExxxx** > **Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 66.
   c) Browse to the root directory of the unzipped CLE Series Software folder.
   d) Click **Next**. You will be asked to confirm your request to install a driver. See Figure 67.
   e) Click **Install**. The driver software will complete the installation.
7. Once installation has completed, the Device Manager should look like Figure 68.

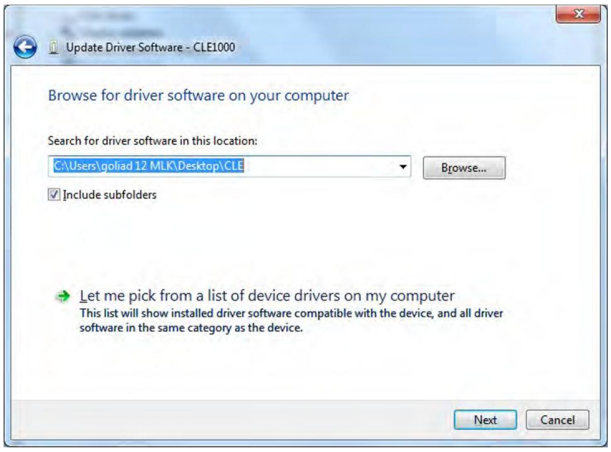

FIGURE 66. UPDATE DRIVER WINDOW

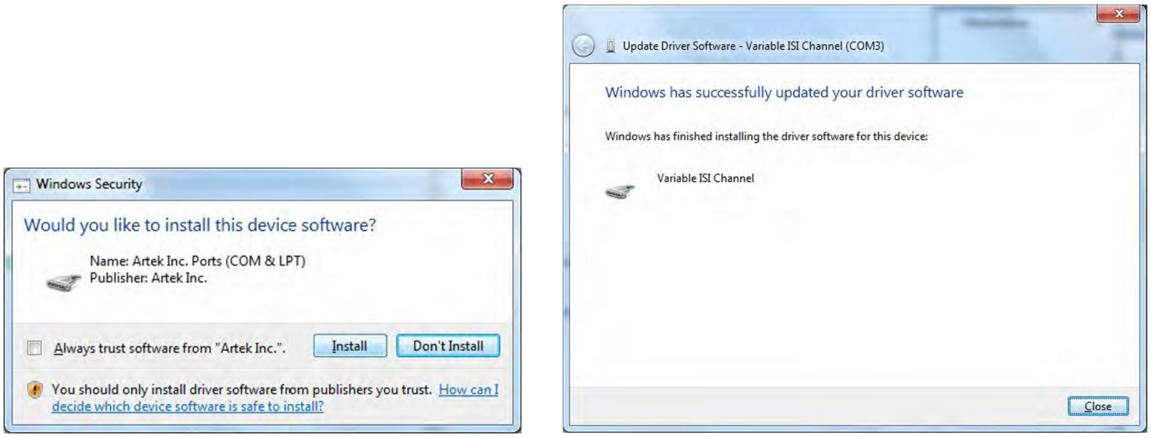

FIGURE 67. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

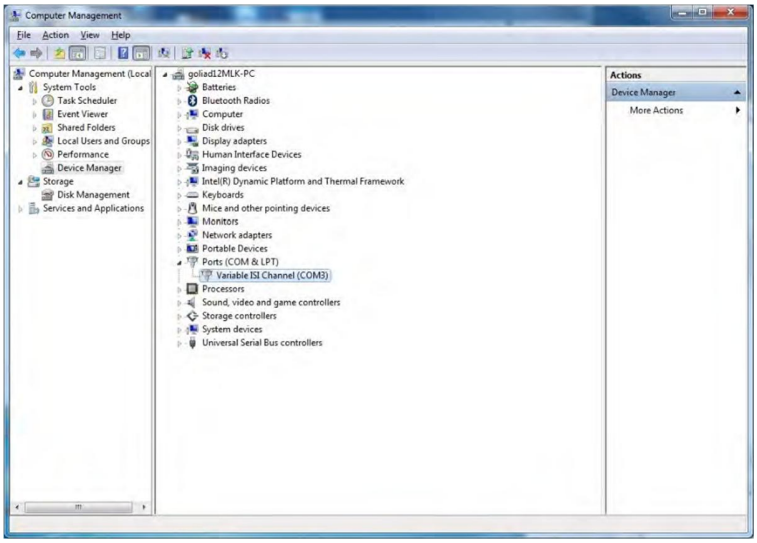

FIGURE 68. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE Series software driver is now installed and the Artek unit can now be selected for use remotely using the GRL software.

11.2 CLE Series GUI Installation

It may also be useful to install the CLE Series GUI, so that the ISI channel can also be controlled manually from the PC. To install the software, do the following:

1. In the CLE Series Software folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you do not want to have manual control.

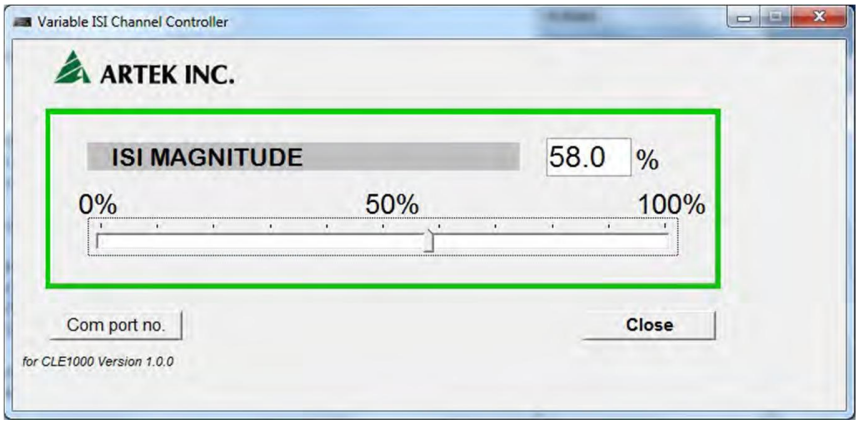

FIGURE 69. CLE SERIES GUI

12 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a PC to control the Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope with the PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

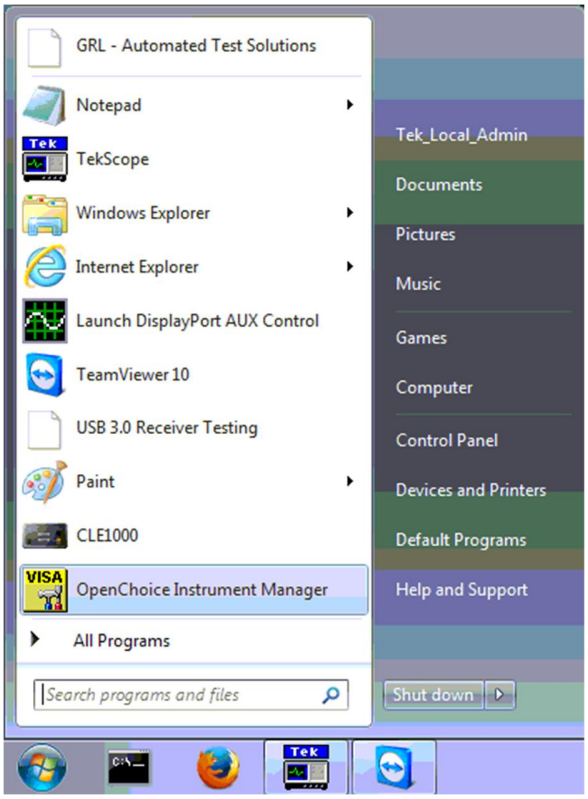

FIGURE 70. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

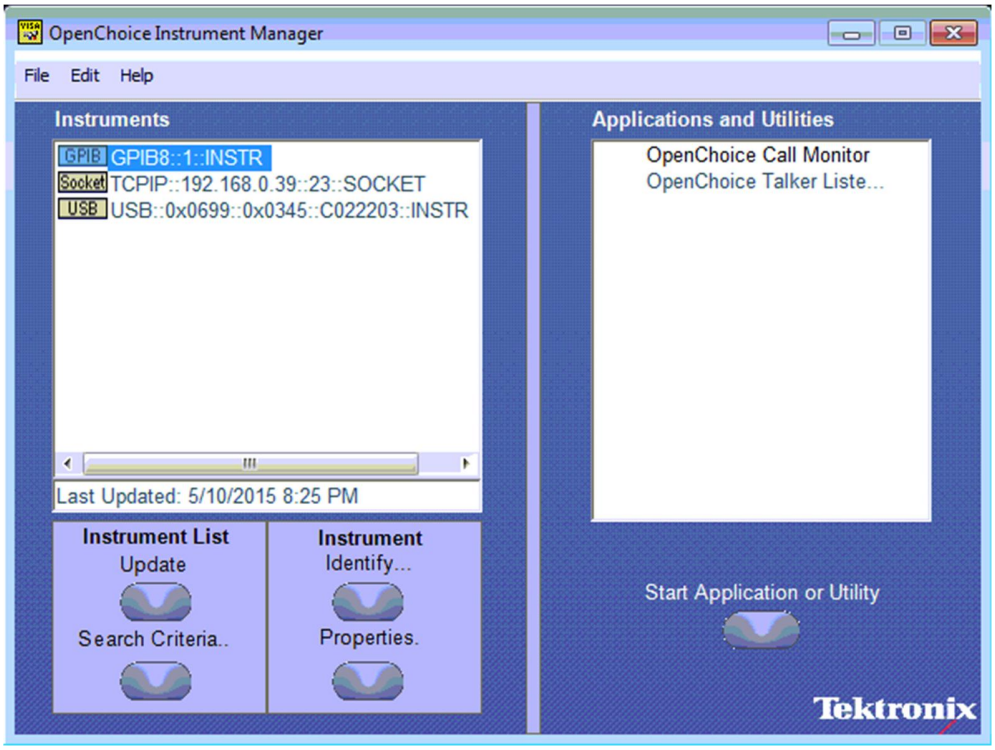

FIGURE 71. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe 4.0 Base Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe 4.0 Base Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

END_OF_DOCUMENT