Granite River Labs

PCI Express® 3.0 and 4.0 Base Specification (8 GT/s)

Receiver Test User Manual and Method of Implementation (MOI)

for Tektronix 8Gbps Physical Layer Test Suite

Using Tektronix BSA/BSX Series BERTScope and Real Time Oscilloscope,

with BSXPCIE4BSE or GRL-PCIE3-BASE-RX Receiver Calibration and Test Automation Software

Contact the GRL office to obtain the latest revision of this document

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Revision Record

Version	Date	Description of Changes	Author(s)
1.0	5/2016	GRL-PCIE3-MOI Add Software Guide. Add Advanced Features.	Bill Altmann (GRL) baltmann@graniteriverlabs.co m
1.01	11/2016	Update based on GRL app Rev1.00.00.44	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.02	1/2017	Add Return Loss Limitations of CLE-1000	Mike Engbretson (GRL) mikeen@graniteriverlabs.com
1.1	01/2018	Add Tektronix BSX BERTScope implementation. Update based on GRL app Rev1.00.051.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.11	04/2018	Update doc nomenclature to reflect support of PCIe3-BASE & PCIe4-BASE (8 GT/s) Rx for BSA and BSX Model BERTScopes.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.12, 1.13	07/2018, 08/2018	General updates	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.14	08/2018	Update based on GRL app Rev1.00.051.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.15	10/2018	Update step to connect Tektronix Scope via GPIB if GRL software is installed on Scope.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com
1.2	05/2019	Add Link Training requirements based on GRL app Rev1.00.24.	Ong Gaik Pheng (GRL) gpong@graniteriverlabs.com

Reference Documents

[1] PCI Express® Base Specification Rev. 3.1a December 7, 2015

[2] Tektronix PCIe Gen3 Base MOI (55w-2428589-0)

[3] PCI Express Base Specification, Rev. 4.0, Version 1.0, September 27, 2017

Note: The most current versions of above documents and ECNs are available to PCI-SIG Working Group members at: http://www.pcisig.com/specifications/pciexpress/

1 Introduction

Receiver device compliance ensures correct data detection by the receiver for an acceptable bit error ratio (BER). PCIe Base Gen-3 devices shall support a BER that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits) when a signal with valid voltage and timing characteristics are delivered to the receiver compliance point [1]. The corresponding signal properties for verifying receiver tolerance should include the maximum allowable jitter, noise and signal loss.

This document describes how to set up the GRL-PCIE3-BASE-RX or GRL-BSXPCI4BSE test software for automation control of PCIe3-BASE or PCIe4-BASE (8 GT/s) receiver calibration and testing, as well as the manual methodology to perform receiver calibration and stress tolerance tests as specified by the PCIe Base Standard using the Tektronix BSX or BSA Model BERTScope. The BERTScope and appropriate accessories provide the necessary test patterns with jitter, ISI, and crosstalk. Additionally, the DPP125C Digital Pre-Emphasis Processor adds the required transmitter equalization. The receiver tolerance test includes various Differential Mode Sinusoidal Interference, minimum transmitter voltage amplitude, and jitter which includes random jitter including a sinusoidal periodic jitter component that is swept across specific frequency intervals.

Once the stressed receiver tolerance test setup has been calibrated, the BERTScope transmits a Modified Compliance pattern to the receiver and monitors the loopback pattern has a BER that is less than 10^{-12} with a confidence level of 95%.

1.1 Glossary

SJ	Sinusoidal Jitter
ISI	Inter Symbol Interference
RJ	Random Jitter
CTLE	Continuous Time Linear Equalization
DFE	Decision Feedback Equalization
CDR	Clock / Data Recovery
BER	Bit Error Rate
BERT	Bit Error Rate Tester
EH	Eye Height
EW	Eye Width
DPP	Digital Pre-emphasis Processor
Downstream	Reference to Device Test Setup (Calibrated with Host Channel)
PVT	Process, Voltage, Temperature

2 Resource Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description	Key Specification
Tektronix BSA Series or BSX Series [a]	1	BERTScope BSA125/DPP125/CR125, or BSX125/CR125A (minimum)	≥ 12.5 Gb/s Requires option STR for stress generation
Tektronix DPO/MSO70000DX	1	Real-Time Oscilloscope with Tektronix DPOJET (Jitter and Eye Analysis) Software	≥ 16 GHz bandwidth with Windows 7+ OS
Tektronix CR125A or higher	1	12.5 Gb/s Clock Recovery Unit Used for DUT-sourced reference clock applications. Not required for BERT-sourced reference.	
ISI Generator	1	PCIe-3 Base Spec compliant Fixed or Variable ISI Channel [b]	
Tektronix DPP125B/C [c]	1	Digital Pre-Emphasis Processor	
Tektronix AFG3000 [c]	1	Arbitrary Function Generator	120MHz Sine Wave Generator
Tektronix BSXSICOMB or SI Combiner	1	Used for combining Differential Mode (DM) SI and AC Common Mode (CM) SI with stressed Rx test pattern. BSXSICOMB — Interference 40 GHz RF combiner kit for BSX version BERTScope. SI Combiner — Interference combiner kit for BSA version BERTScope.	
GRL-PCIE3-BASE-RX [d]	1	Granite River Labs PCIe® 3.0 (8 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com *(For BSA version BERTScope only)* Included with Node Locked License to single oscilloscope or PC OS	
GRL-BSXPCI4BSE [e]	1	Granite River Labs PCIe® 4.0 (16 GT/s and 8 GT/s) Base Specification Receiver Calibration and Test Automation Software – www.graniteriverlabs.com *(For BSX version BERTScope only)* Included with Node Locked License to single oscilloscope or PC OS	
Seasim	1	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software at TP2P) – www.pcisig.com	
SigTest	1	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html SigTest used with Seasim for final eye calibration	
VISA (Virtual Instrument Software Architecture) API Software		VISA Software is required to be installed on the controller PC running GRL PCIe Gen 3 Base Rx software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*	

System	Qty.	Description	Key Specification
GRL-TEK-CUST	1	User Definable GRL Automation Framework and/or GRL Custom Support Included with Node Locked License to single oscilloscope or PC OS	
Computer (laptop or desktop)	1	For automation control (Windows 7+ OS)	

[a] *Tektronix BSX BERTScope is the preferred option.*

[b] *The Artek CLE Model Series is supported for variable ISI generation. Refer to Appendix of this document for the Artek CLE Series driver installation procedure.*

[c] *Required if used with the Tektronix BSA BERTScope only.*

[d] *The Tektronix SI Combiner is included if the GRL software is ordered with the Tektronix BSA BERTScope.*

[e] *PCIe3-BASE and PCIe4-BASE will need to be installed on the BSX BERTScope to test at both 16 GT/s and 8 GT/s data rates.*

Note: Cable connector type and length requirements may vary according to the lab/equipment setup and the dimensions of the DUT board. Table 2 below is a recommended list. Please also refer to Tektronix's website for detailed cabling recommendations related to PCI Express.

TABLE 2. EQUIPMENT RECOMMENDATION – CABLES

Cable	Qty.	Tektronix P.N.
T+M SF104PE/11PC35/11PCC35/500mm 1.5ps Phase Matched	8	174-6663-00
T+M SF104PE/11PC35/11PCC35/1000mm 1.5ps Phase Matched	2	PMCABLE1M
T+M MF141/16SMA/16SMA/200mm SMA-to-SMA, Right Angle	4	174-6664-00
T+M MF141/16SMA/16SMA/300mm SMA-to-SMA, Right Angle	1	174-6665-00
T+M MF141/16SMA/16SMA/500mm SMA-to-SMA, Right Angle	1	174-6666-00
T+M MF141/11SMA/16SMA/1.829M SMA-to-SMA, Right Angle	2	174-6667-00
High-performance BNC	1	N/A

3 GRL PCIe3-BASE & PCIe4-BASE (8 GT/s) Rx Software Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL PCIe 3.0 or 4.0 Base (8 GT/s) Rx test solution. It also helps you familiarize yourself with the basic operation of the application.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

3.1 Launch and Set Up Software

3.1.1 On the BERTScope

1. Select View > System > Tools Tab.
2. Under Utilities Column, select the Remote button.
3. In Remote Window, select TCP/IP.
4. Change Terminator to "LF". Select the Connect Button. See Figure 1.

    a) If you see an error pops up when selecting the Connect button, try a different Port. For example, change Port 23 to 21.

5. Note the IP Address and Port # on Remote Client. They will be needed to connect the BERTScope to the GRL automation software.
6. Minimize, but do not close, the *Remote Client* Window.

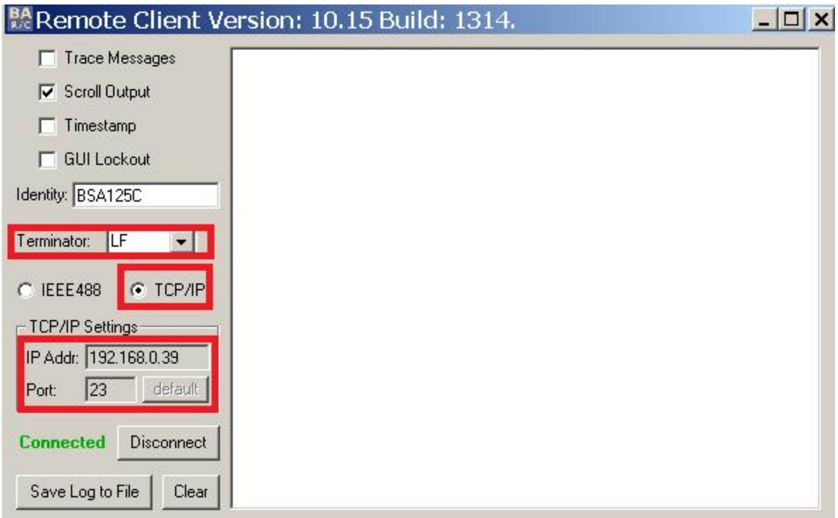


FIGURE 1. REMOTE CLIENT WINDOW

3.1.2 On the PC Used for GRL Framework Installation

Download and install the software as follows:

1. If the GRL PCIe3-BASE & PCIe4-BASE (8GT/s) Rx software is to be installed on a PC (where it is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIe3_0_BasePatternFilesInstallationxxxxxxxxxSetup.exe** – Run this on the BERTScope to install the test pattern setup files.
   - **PCIe3_0_BaseRxTestApplicationxxxxxxxxxSetup.exe** – Run this on the controller PC or oscilloscope to install the GRL PCIe3-BASE & PCIe4-BASE (8GT/s) Rx application.
   - **PCIe3_0_BaseRxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.
4. Once the software is installed, open the GRL folder from the Windows Start menu and select the GRL Framework. The GRL Framework will launch.

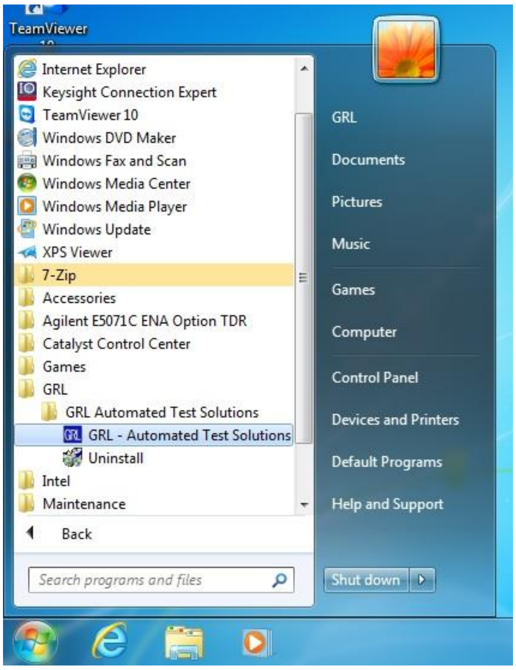


FIGURE 2. SELECT AND LAUNCH GRL FRAMEWORK

5. From the Application→Rx Test Solution drop-down menu, select 'PCIe 3.0 Base Rx Test' to start the PCIe 3.0 Base Rx Test Application. If the selection is grayed out, it means that your license has expired.

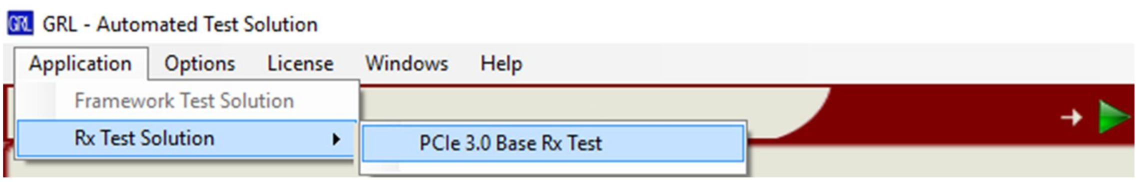


FIGURE 3. START PCIE 3.0 BASE RX TEST APPLICATION

6. To enable license, go to License→License Details.

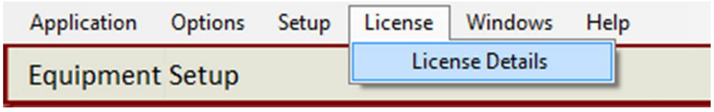


FIGURE 4. SEE LICENSE DETAILS

a) Check the license status for the installed application.

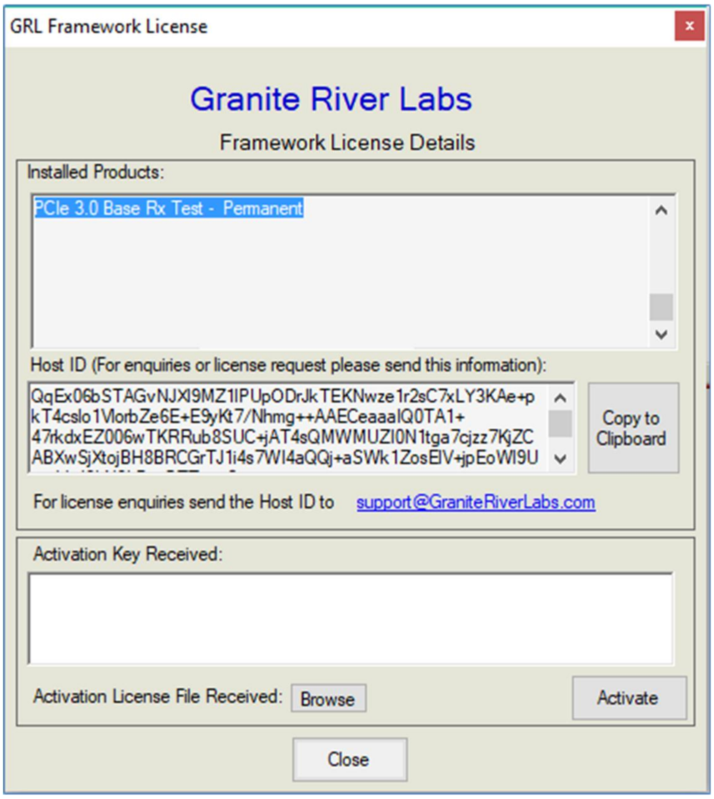


FIGURE 5. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select "Activate".
- If you do not have an Activation Key, select "Close" to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

7. Click on Equipment Setup icon  on the PCIe 3.0 Base Rx Test Application menu.
8. Enter the BERTScope IP address and Port number to match what is in the BERTScope *Remote Client* window shown in Step 4-5.
9. Attach the Tektronix AFG via USB or LAN to the Tektronix Oscilloscope.

10. On the Tektronix Scope, open the **OpenChoice Instrument Manager** application.

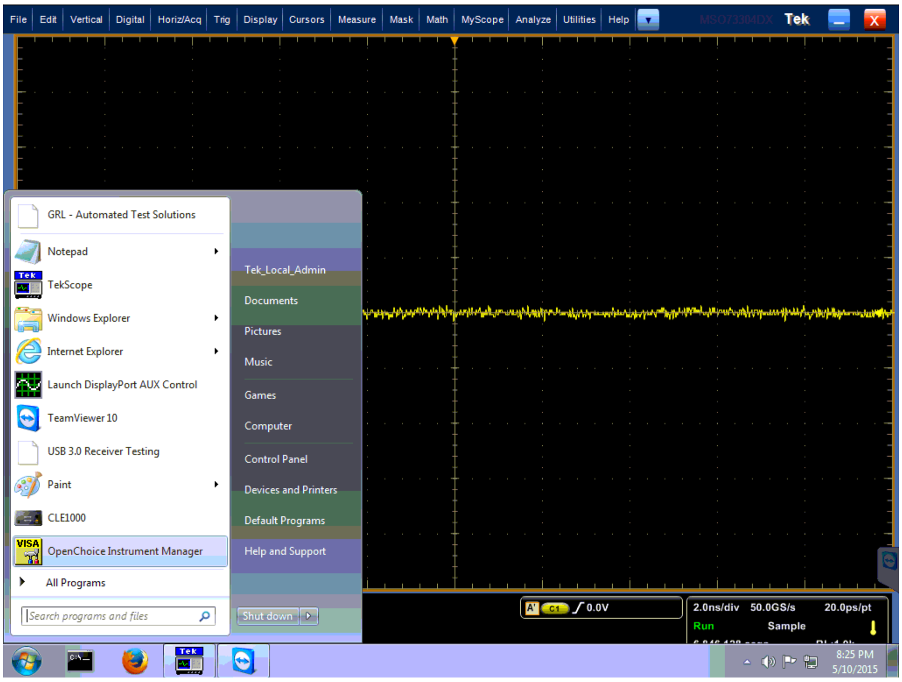


FIGURE 6. OPENCHOICE INSTRUMENT MANAGER IN START MENU

11. The Instrument Manager will display all the connected instruments on its list, for example:

a) GPIB8::1::INST (Tektronix Scope)
b) TCPIP::192.168.0.39::23::SOCKET (BERTScope)
c) USB::0x0699::0x0345::C022203::INSTR (AFG)

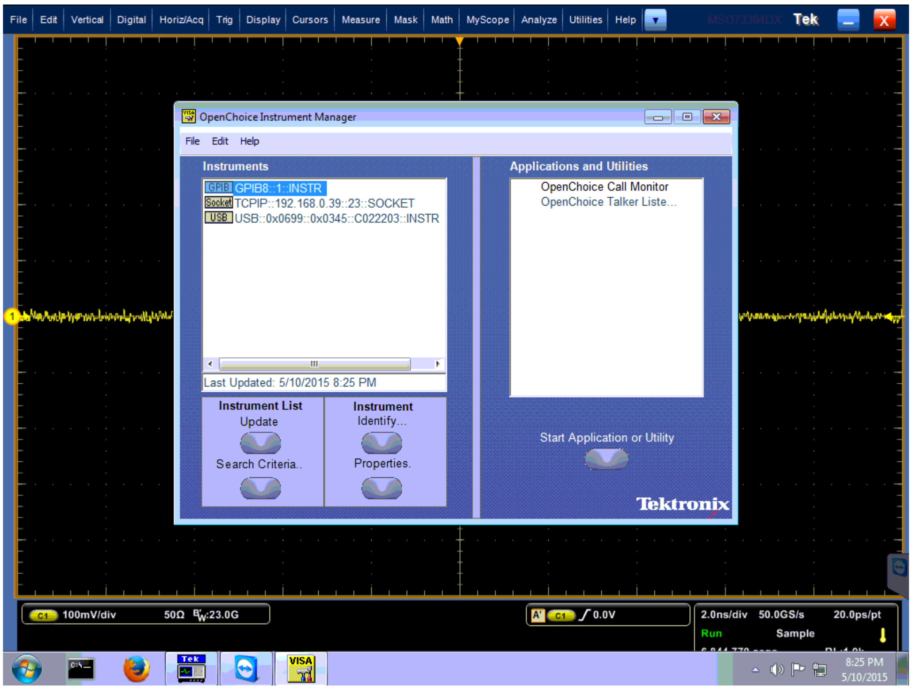


FIGURE 7. INSTRUMENT LIST IN INSTRUMENT MANAGER

12. On the Equipment Setup page of the GRL PCIe 3.0 Base Rx Test Application, type in the address of each connected instrument into the 'Address' field, for example:

    a) Scope GPIB Address
    b) BERTScope IP Address
    c) AFG USB/IP Address
    d) COM Address of the ISI Generator to be used

    Note: If the GRL software is installed on the Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR" or if installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to omit the Port number from the address.

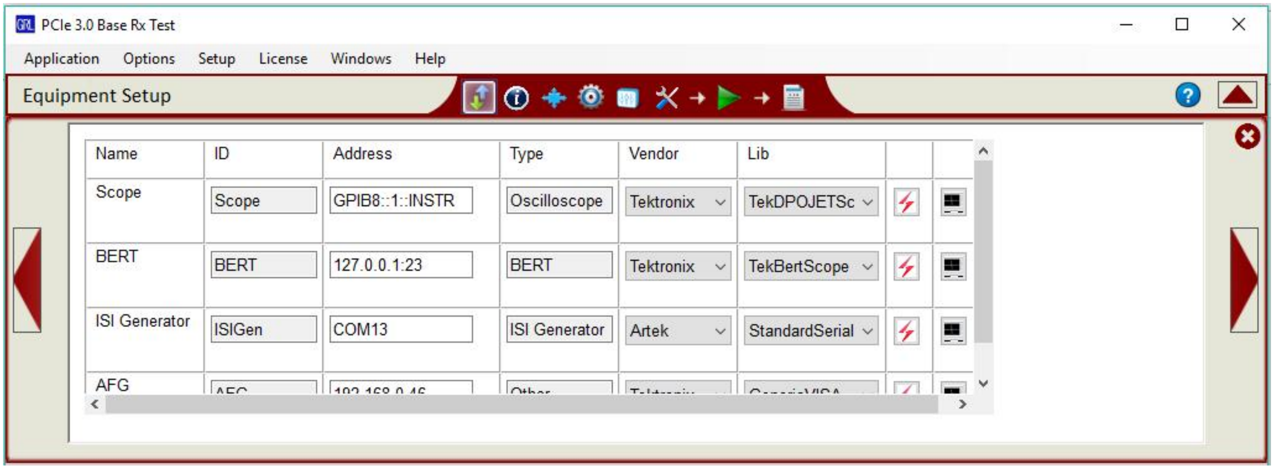


FIGURE 8. EQUIPMENT SETUP WINDOW

13. Verify the connection by selecting the "lightning" button ( ) for each connected instrument.

    The "lightning" button should turn green ( ) once the software has successfully established connection with each instrument.

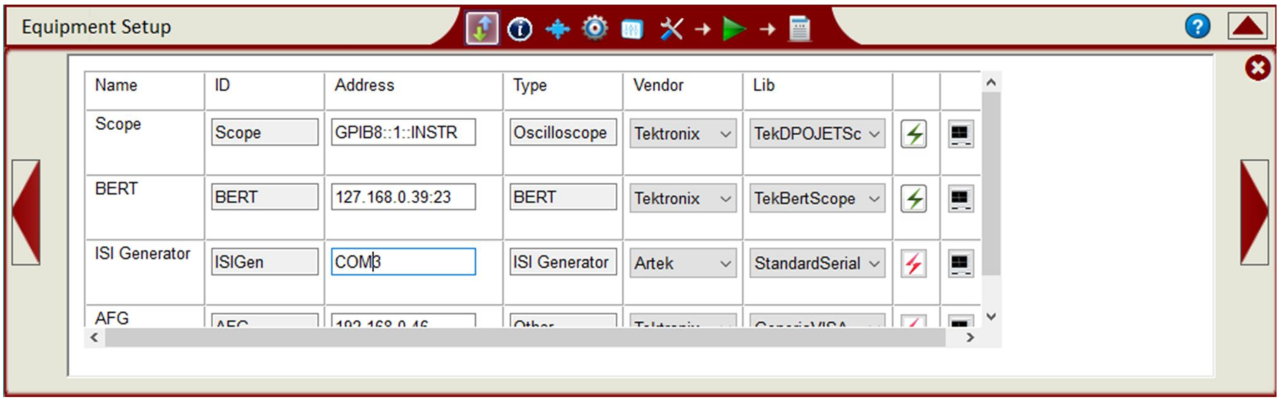


FIGURE 9. CONNECT INSTRUMENTS WITH GRL SOFTWARE

(Note: Additional information for connecting the Tektronix oscilloscope to the PC and installing the Artek CLE Series ISI Generator are provided in the Appendix of this User Guide & MOI.)

3.2 Software Configuration Before Calibration and Testing

3.2.1 Enter Test Session Information

Select from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

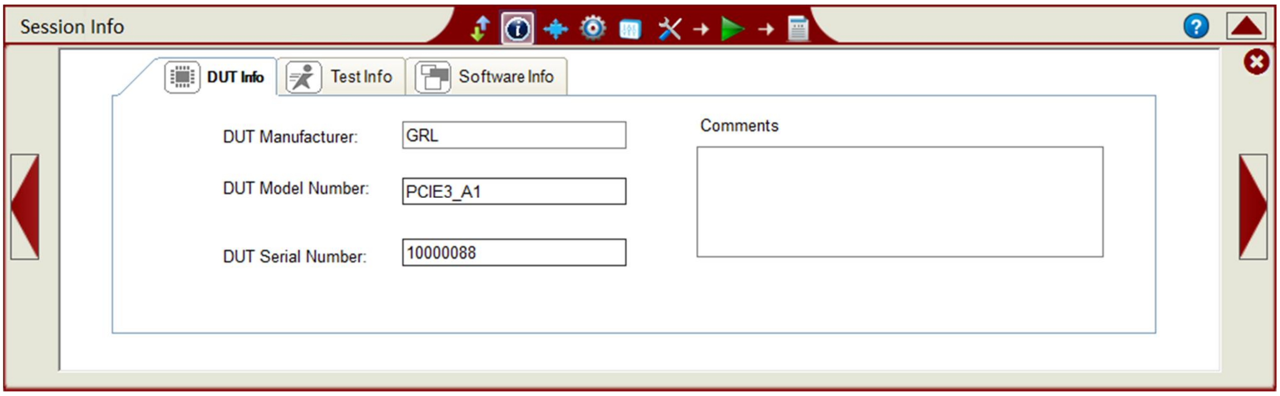


FIGURE 10. SESSION INFO PAGE

3.2.2 Set Conditions for Calibration and Testing

Select from the menu to access the **Conditions** page to set the conditions for calibration and testing.

Recommended procedure:

- *Step 1*: When calibrating, select all required conditions and perform the calibration.
- *Step 2*: Once calibration is completed and ready for testing, re-select the conditions that will be used for specific tests.

SJ tab: Select SJ Frequencies as defined by the Specification or the user for calibration or testing.

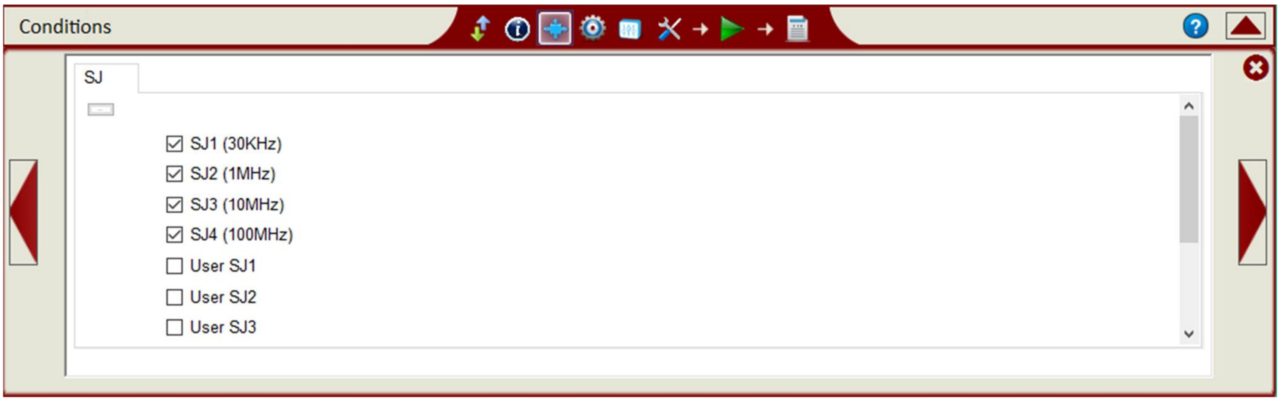


FIGURE 11. SELECT SJ FREQUENCIES

3.2.3 Set Up Calibration and Test Requirements

Use the Setup Configuration page to configure the necessary measurement-related settings prior to running calibration and tests.

3.2.3.1 ISI Generator Tab

Select the type of supported ISI generators to be used:

- "None": This is the recommended method which is used to provide -18 dB physical channel Insertion Loss for calibration and testing. A PCIe 3.0 CEM Fixture can be used in the setup for this method.
- "Artek": This is provided as an Option. The Artek CLE Series ISI Generator and an additional ISI board can be used in the setup for ISI automation. *(Also see Appendix for more information on installing the Artek CLE Series.)*
- "BSAITS": This is provided as an Option. The Tektronix BSAITS variable ISI source can be used in the setup for ISI automation. *(Only applicable for the BSA Model BERTScope.)*

The selected ISI Generator will be used for both calibration and testing.

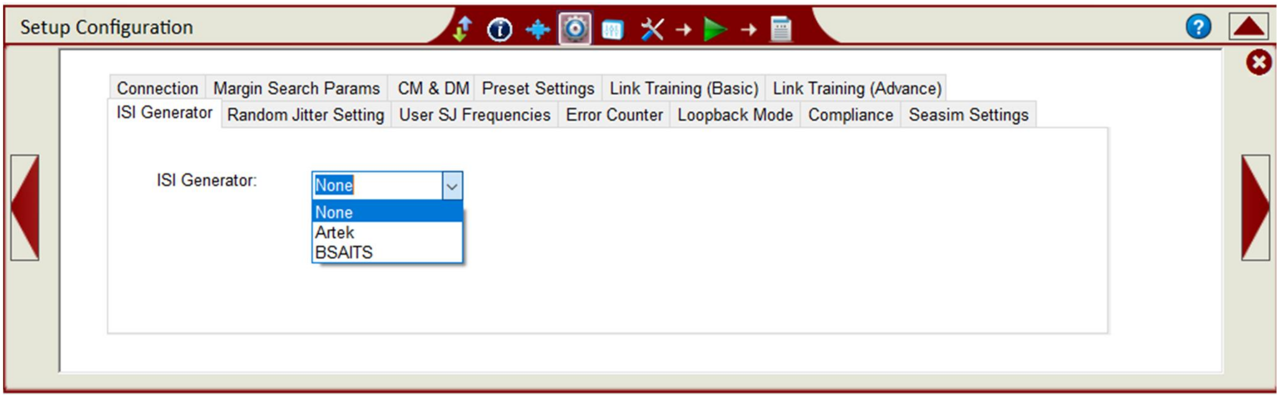


FIGURE 12. SELECT ISI GENERATOR

Notes:

For more information on how to generate desired insertion loss using the BERTScope ISI Trace board, refer to Appendix C: BERTScope ISI Trace Board.

If the Artek CLE1000-A2 is being used, take note that the insertion loss specification of the CLE1000-A2 does not meet the PCI Express 3.0 Base Specification Requirement of -18 dB from 500 MHz to 5 GHz. Refer to Appendix B, Return Loss Limitations of the Artek CLE1000-A2 for more information.

3.2.3.2 Random Jitter Setting Tab

Set the RJ intrinsic value in % unit interval for the BERTScope.

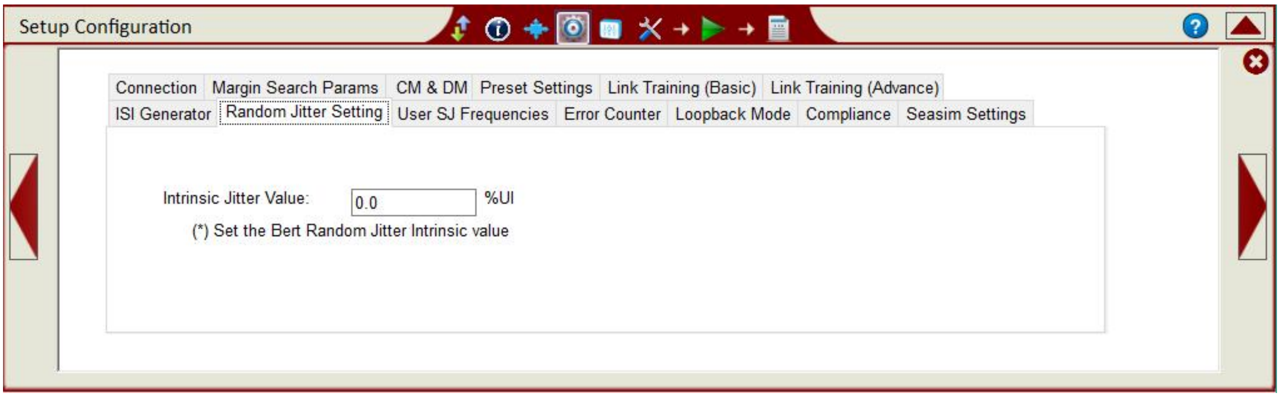


FIGURE 13. SET RANDOM JITTER

3.2.3.3 User SJ Frequencies Tab

Set the values for the User SJ frequencies that have been selected from the Conditions page.

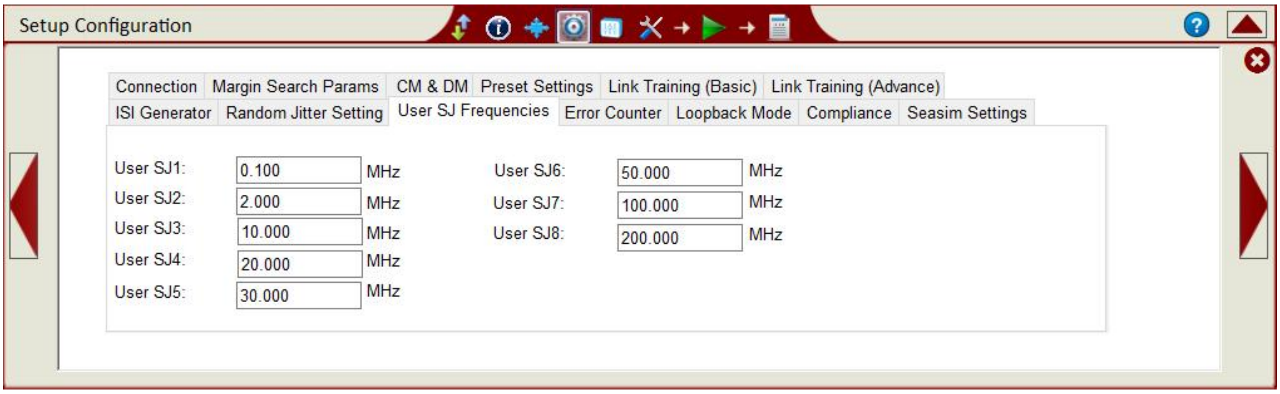


FIGURE 14. SET USER SJ FREQUENCIES

3.2.3.4 Error Counter Tab

Select the DUT receiver base loopback capability for error detection. If the DUT can be configured for the loopback test mode, select 'LoopBack', or otherwise select 'Manual'.

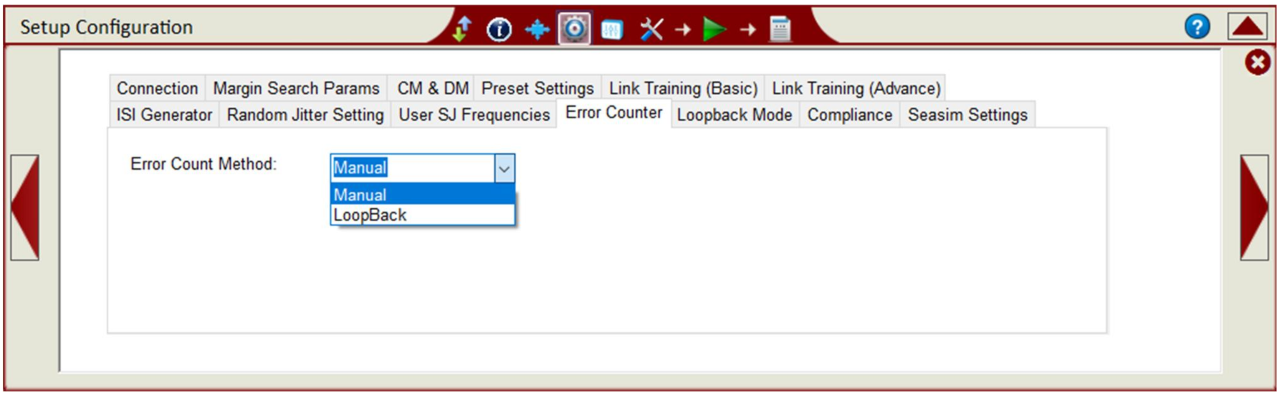


FIGURE 15. SET ERROR COUNT METHOD

3.2.3.5 Loopback Mode Tab

If the 'LoopBack' mode has been selected from the Error Counter tab, then user needs to select 'Clock Recovery' in the Clock Recovery Method drop-down and set the clock recovery loop bandwidth. *Other options on the Clock Recovery Method drop-down are not yet supported.*

To perform clock synchronization which extracts the clock signal from the data to produce a synchronous clock signal, select the 'Grab and Go Sync' checkbox.

Optionally, user can choose to use a custom test pattern for error detection by selecting the checkbox. Then, enter the pattern file name in the ED Pattern field. If the checkbox is not selected, the default test pattern will be used.

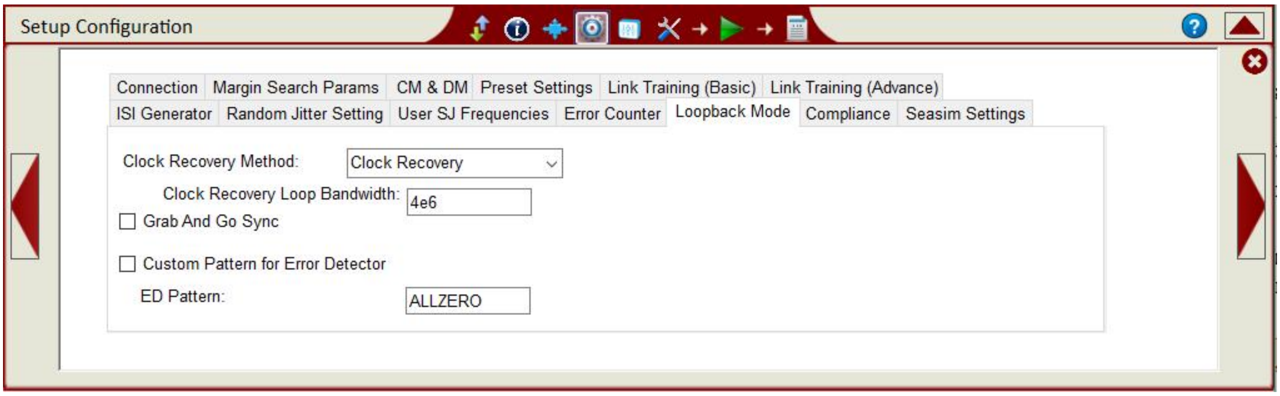


FIGURE 16. SET UP LOOPBACK MODE

3.2.3.6 Compliance Tab

Set the target BER and Maximum Error allowed for compliance during testing. By default, the limit values in these fields are set according to Specifications. Other values can also be defined by the user, as required.

Note: The syntax '1e-12' indicates $1x10^{-12}$, and is the only syntax supported in this field.

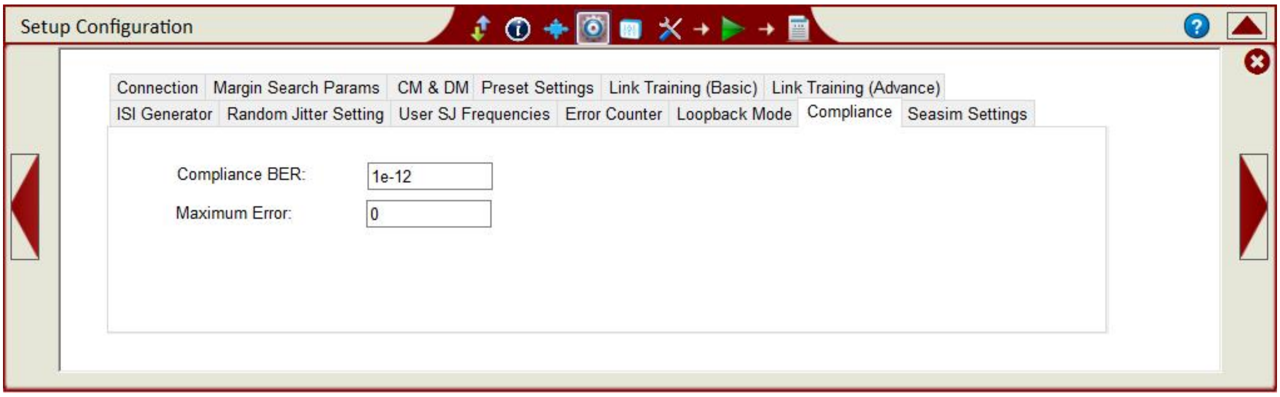


FIGURE 17. SET UP COMPLIANCE BER AND MAXIMUM ERROR

3.2.3.7 Seasim Settings Tab

Set up the Seasim parameters if using the Rx Behavioral package during Eye Height and Eye Width Calibration. Also set the intrinsic jitter (if required) to be used in the Seasim calculation.

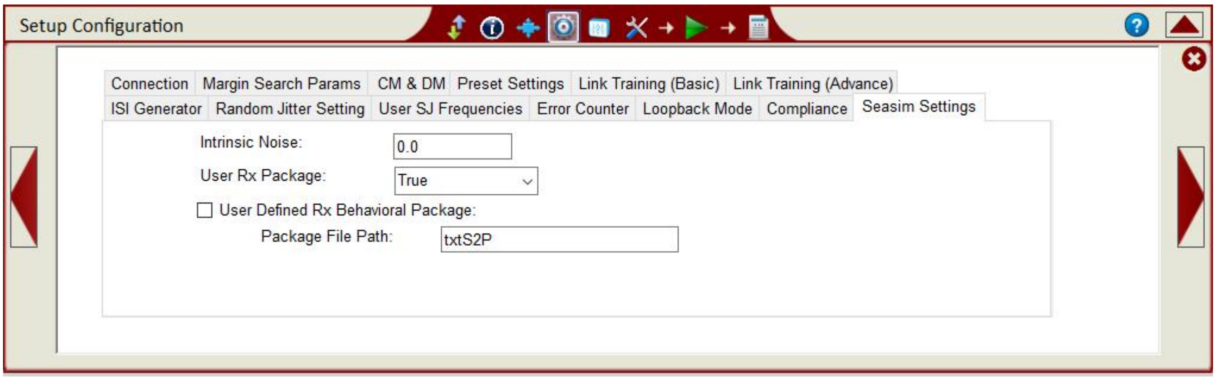


FIGURE 18. SET UP SEASIM

3.2.3.8 Connection Tab

Set up the connected Data+ and Data- channels on the Oscilloscope. Scope channels shall be assigned according to how the scope cables are attached to the test setup.

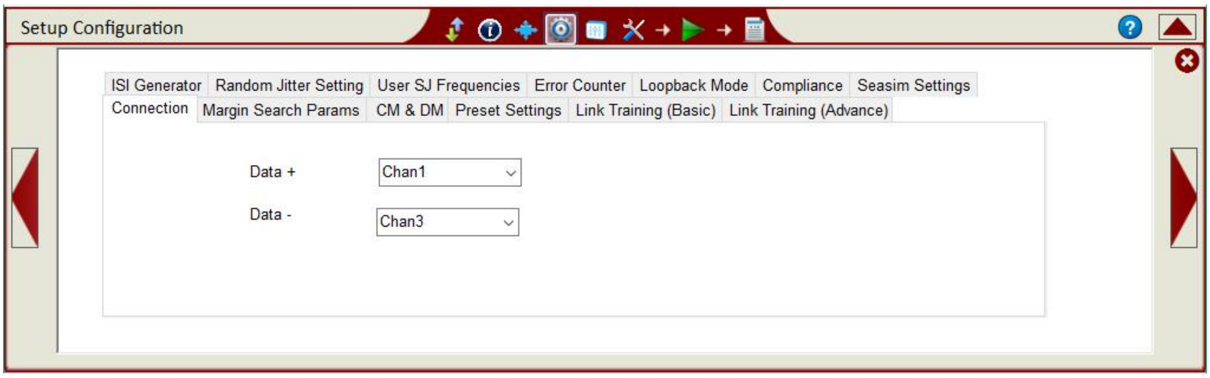


FIGURE 19. SET UP SCOPE CHANNEL CONNECTION

3.2.3.9 Margin Search Parameters Tab

Set the compliance BER, margin step size, maximum error and steps to be used when running margin search tests.

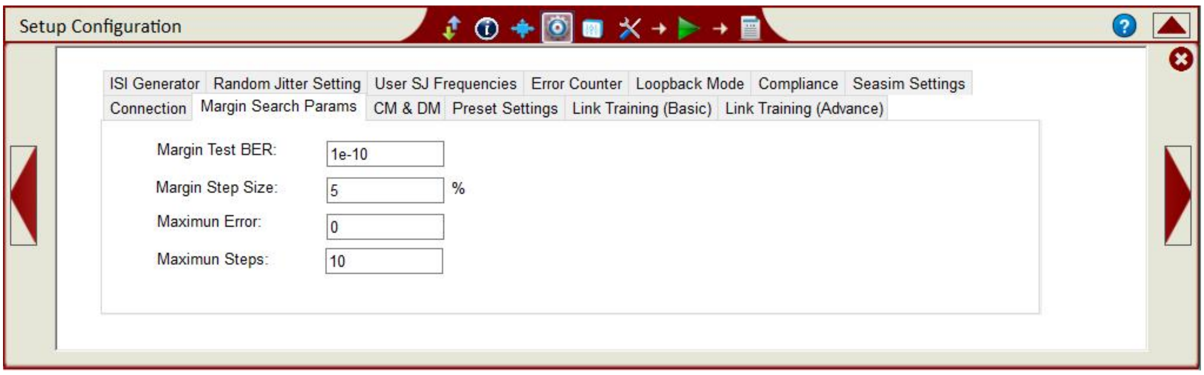


FIGURE 20. SET UP MARGIN SEARCH PARAMETERS

3.2.3.9 CM & DM Tab

Note: These settings are only applicable if using the Tektronix BSX320 BERTScope.

Select the BSX320 BERTScope channels to be used for the Common Mode and Differential Mode Sinusoidal Interference (SI) connections.

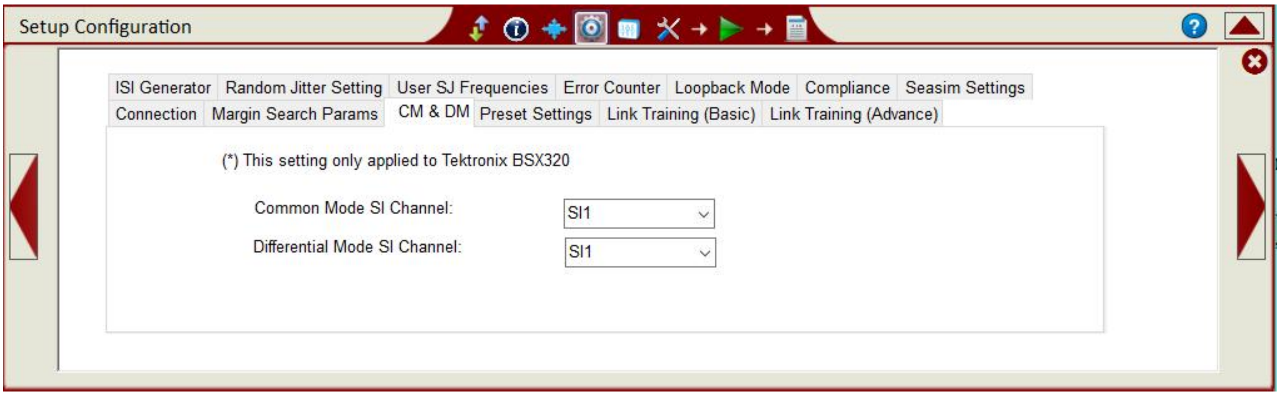


FIGURE 21. SELECT CM AND DM SI CHANNELS

3.2.3.10 Preset Settings Tab

Select to use a pre-defined preset and preset hint for each Rx lane, or select the checkbox to use a custom preset. If using a custom preset, enter the Preshoot and Deemphasis values for the preset.

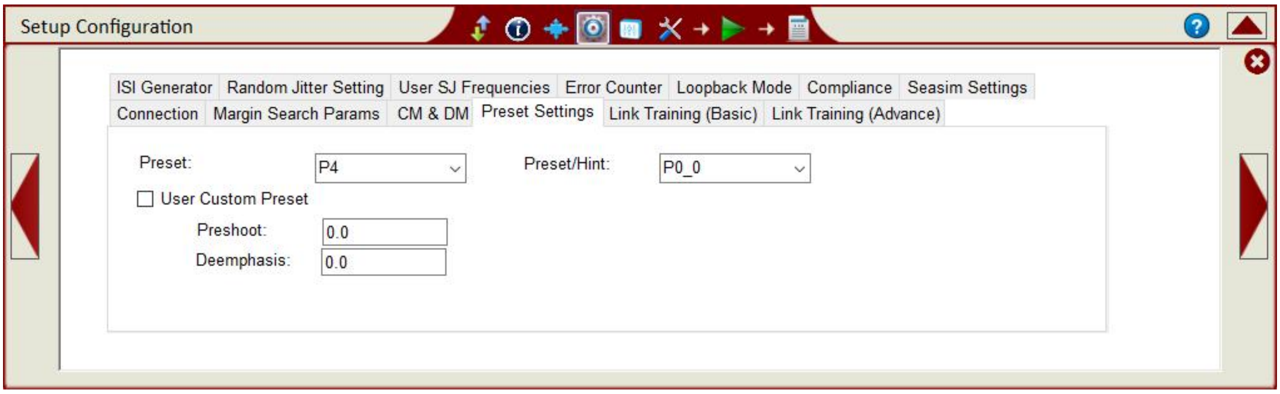


FIGURE 22. CONFIGURE PRESET

3.2.3.11 Link Training (Basic) Tab

To perform link equalization, select the 'Use Link EQ' checkbox. Select the Lane and Link numbers along with the Fast Training Sequence (FTS) value required by the receiver from 0 to 255. FTS is used within an Ordered Set when transitioning from L0s to L0.

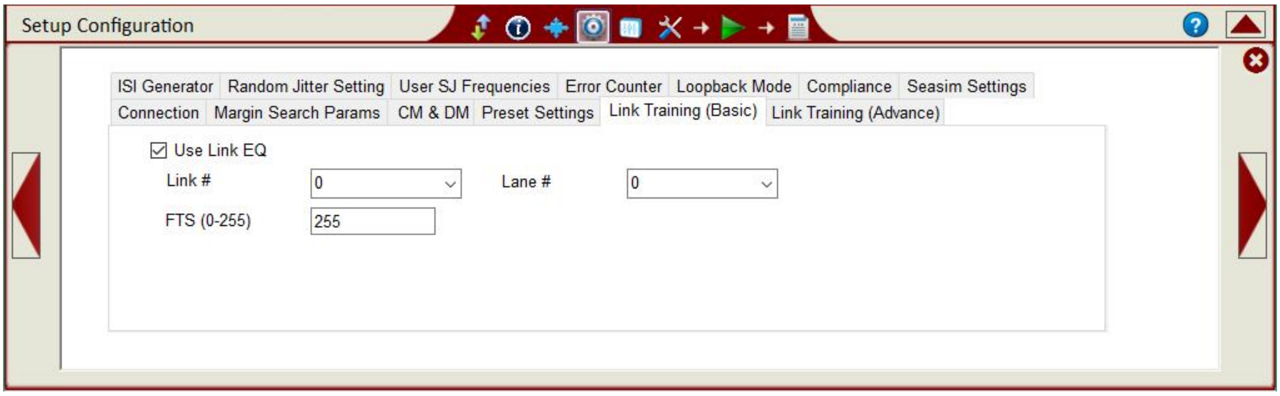


FIGURE 23. SET UP BASIC LINK TRAINING

3.2.3.12 Link Training (Advance) Tab

Set up advanced parameters for link training by entering the limit of extended synchronization bit, full swing (FS) and low frequency (LF) values as well as Electrical Idle length.

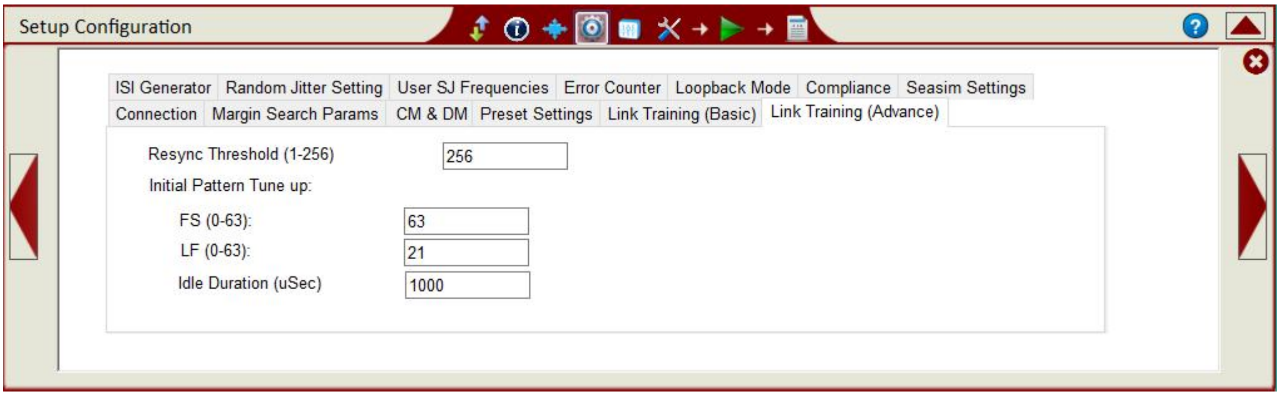


FIGURE 24. SET UP ADVANCE LINK TRAINING

3.2.4 Select Calibration

The **Select Tests** page is the place where the different types of calibration that need to be performed are selected. Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Rx Tests will show an error message.

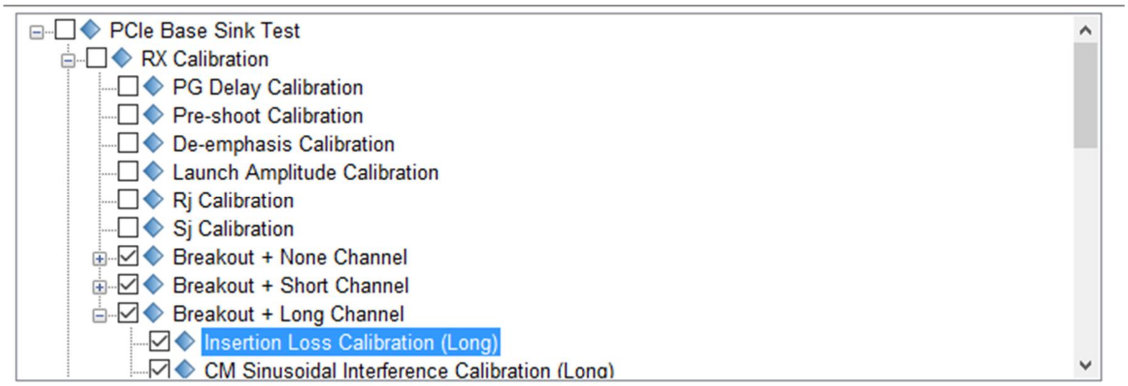


FIGURE 25. SELECT CALIBRATION

3.2.5 Run Automation Calibration

Once calibration have been selected and set up from the previous sections, the calibration are ready to be run.

Select from the menu to access the Run Tests page. The GRL software automatically runs the selected calibration when initiated.

Before running the calibration, select the option to:

- **Skip Test if Result Exists –** If results from previous calibration exist, the software will *skip* those calibration.
- **Replace if Result Exists –** If results from previous calibration exist, the software will *replace* those calibration with new results.

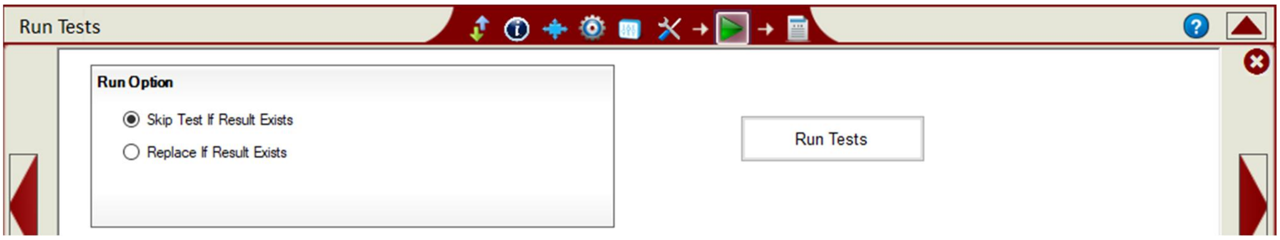


FIGURE 26. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration. The connection diagram for the calibration being run will initially appear to allow the user to make sure that the calibration environment has been properly set up before calibration can proceed.

4 Software Calibration and Testing

PCIe3/4 Base (8 GT/s) Rx calibration will be performed for PG Delay (if using the Tektronix BSA BERTScope) as well as 3 test points: TP1, TP2, and TP2P. TP1 is a physical test point for calibration without the effect of breakout channel length. TP2 is a test point that will affect the eye opening due to trace length. TP2P is a test point calculated by the ***Seasim*** software tool to simulate the eye opening after applying Rx Behavioral package, Rx CTLE, and DFE (if required).

PCIe3/4 Base (8 GT/s) Rx testing will be generally performed for both DUT receiver compliance and margin tolerance. Receiver compliance is tested for stress tolerance with and without the effect of breakout channel length. Receiver margin tolerance is an optional test which measures the stress margins with and without applying trace length.

4.1 Calibration Connection Setups

4.1.1 Calibration for PG Delay (if using the BSA BERTScope)

This will calibrate the delay of the pattern generator and the BSA BERTScope to ensure that the data output of the pattern generator matches the pattern specified in the BERTScope.

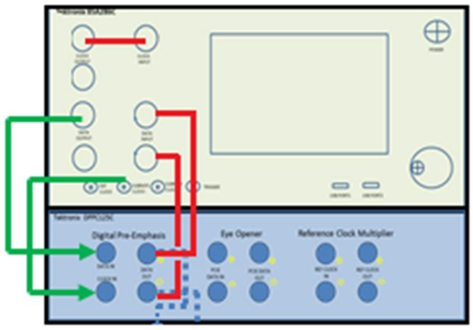


FIGURE 27. TYPICAL SETUP FOR PG DELAY CALIBRATION

Connection Steps:

1. Using ~0.3 m (12″) long cable, connect BERTScope Data(+) Out to DPP Data In.
2. Using ~1.8 m (72″) long cable, connect BERTScope Subrate Clock Out to DPP Clock In.
3. Loop back DPP Outputs to BERTScope Analyzer Error Detector Inputs (cable length is not mandatory).
4. Connect BERTScope Clock Out to BERTScope Analyzer Error Detector Clock In.

4.1.2 Calibration for TP1

4.1.2.1 Using Tektronix BSA BERTScope

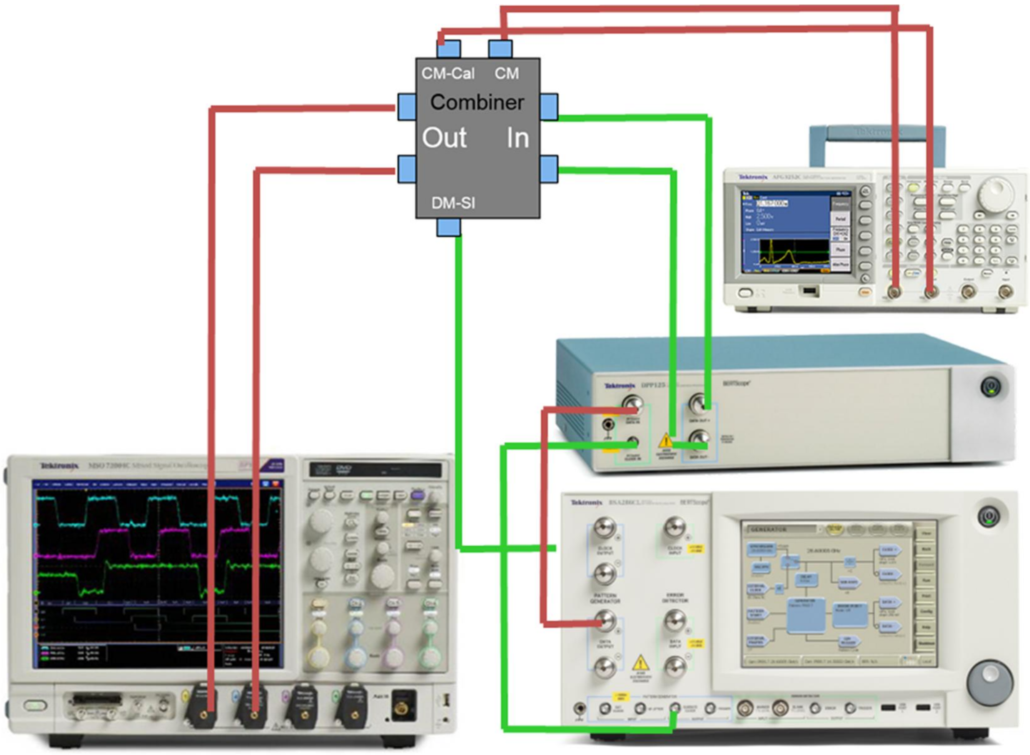


FIGURE 28. TYPICAL SETUP FOR TP1 CALIBRATION (USING TEKTRONIX BSA BERTSCOPE)

Connection Steps:

1. Connect BERTScope Data(+) Out to DPP.
2. Connect BERTScope Clock Out to DPP.
3. Connect DPP Data(+) Out to Combiner In.
4. Connect DPP Data(-) Out to Combiner In.
5. Connect AFG Output1 to Combiner CM-In.
6. Connect AFG Output2 to Combiner CM-Cal.
7. Connect BERTScope (real panel) SI-Out to Combiner DM-In.
8. Connect Combiner Data Outputs to Oscilloscope Chan1 and Chan2.

4.1.2.2 Using Tektronix BSX BERTScope *(Recommended option)*

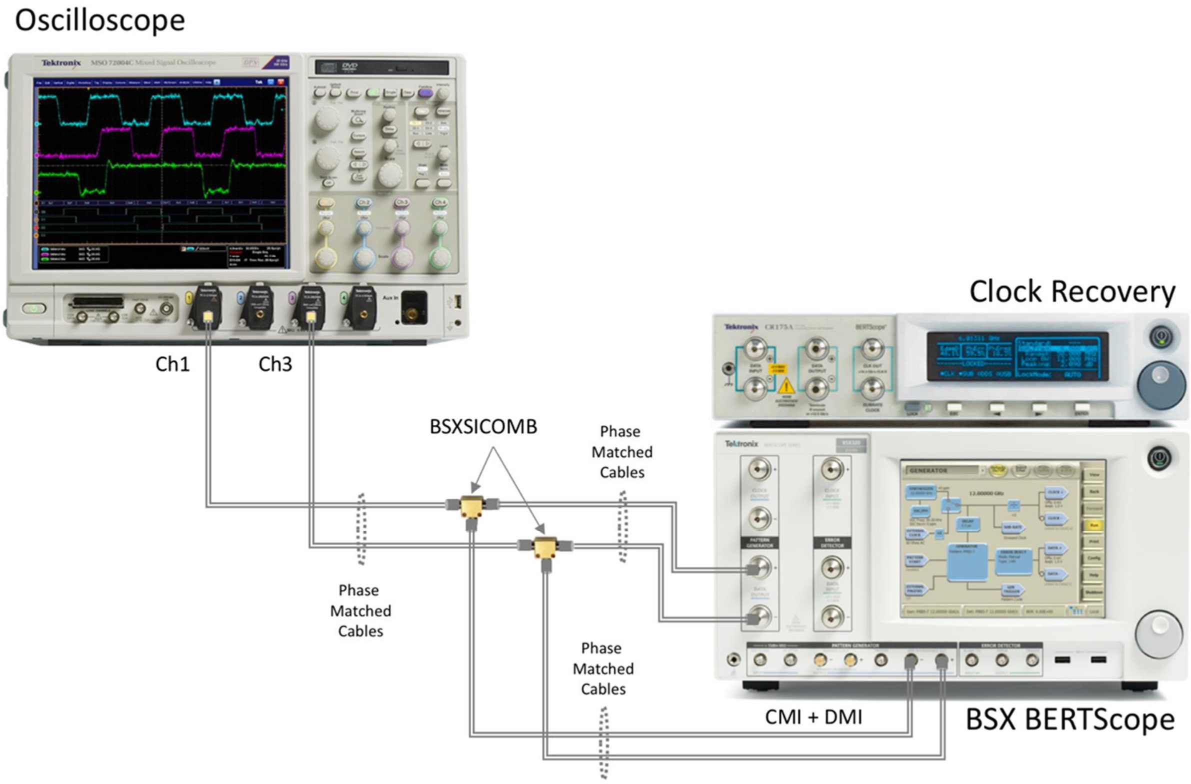


FIGURE 29. TYPICAL SETUP FOR TP1 CALIBRATION (USING TEKTRONIX BSX BERTSCOPE)

Connection Steps:

1. Connect BERTScope Data (+/-) Out to BSXSICOMB In.
2. Connect BERTScope SI1-Out to BSXSICOMB CMI/DMI-In.
3. Connect BERTScope SI2-Out to BSXSICOMB CMI/DMI-In.
4. Connect BSXSICOMB Out to Scope Ch1, Ch3 (or Ch2, Ch4).

4.1.3 Calibration for TP2

4.1.3.1 Using Tektronix BSA BERTScope

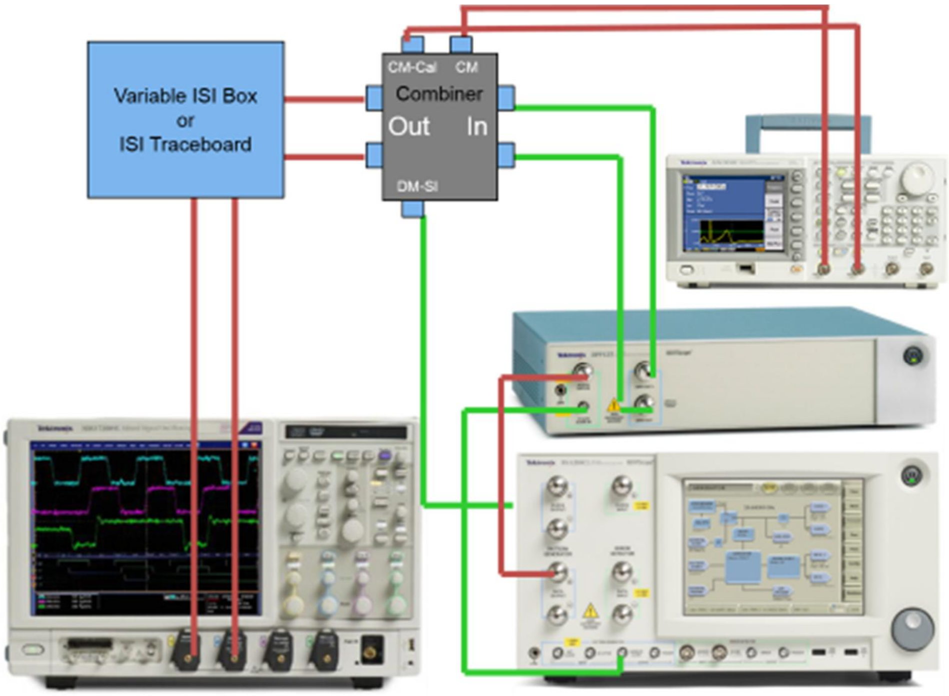


FIGURE 30. TYPICAL SETUP FOR TP2 CALIBRATION (USING TEKTRONIX BSA BERTSCOPE)

Connection Steps:

1. Connect BERTScope Data(+) Out to DPP.
2. Connect BERTScope Clock Out to DPP.
3. Connect DPP Data(+) Out to Combiner In.
4. Connect DPP Data(-) Out to Combiner In.
5. Connect AFG Output1 to Combiner CM-In.
6. Connect AFG Output2 to Combiner CM-Cal.
7. Connect BERTScope (real panel) SI-Out to Combiner DM-In.
8. Connect Combiner Data Outputs to ISI Generator Inputs.
9. Connect ISI Generator Outputs to Oscilloscope Chan1 and Chan2.

Note: The above diagram shows either a variable ISI generator or a fixed ISI channel being used for ISI generation, that is selected from the 'ISI Generator' tab on the Setup Configuration page. See Appendix A and B in this document for more information on the use of variable and fixed ISI generation.

4.1.3.2 Using Tektronix BSX BERTScope *(Recommended option)*

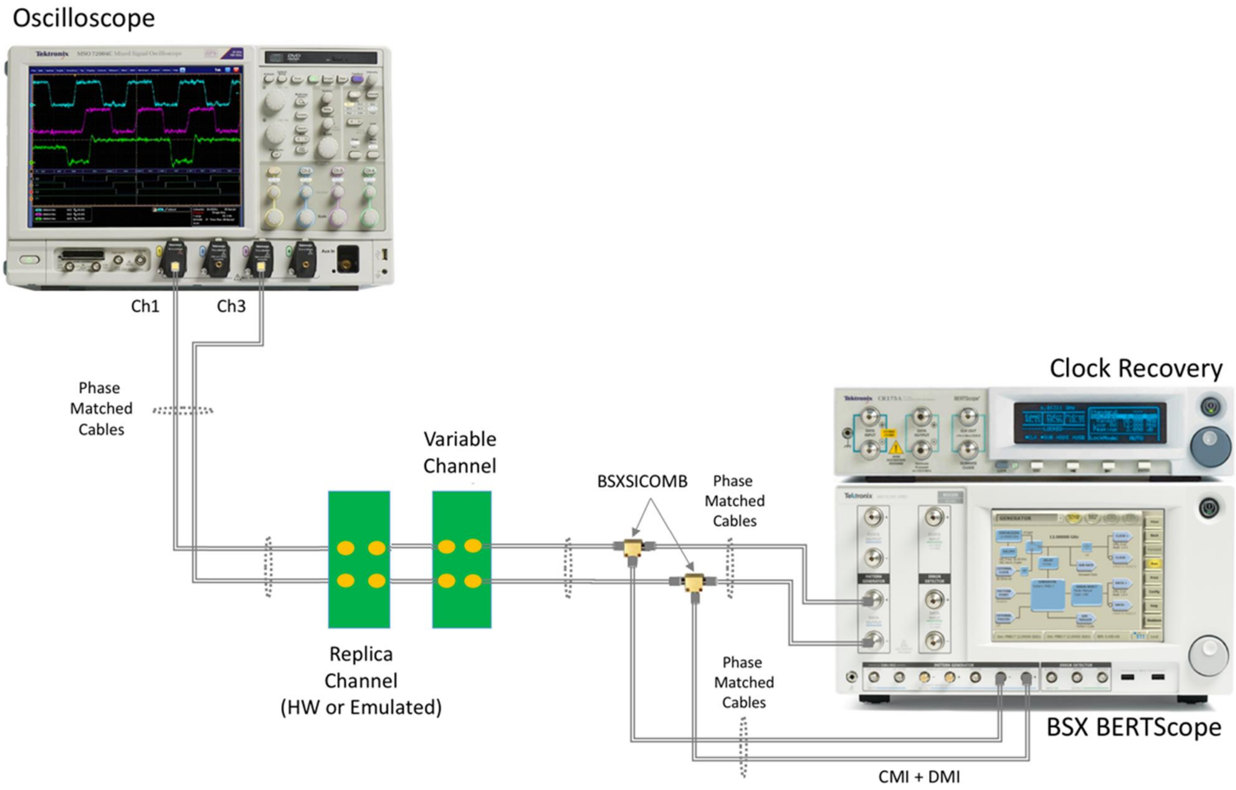


FIGURE 31. TYPICAL SETUP FOR TP2 CALIBRATION (USING TEKTRONIX BSX BERTSCOPE)

Connection Steps:

1. Using back the same connections from the TP1 calibration setup, disconnect the BSXSICOMB Out from the Scope channels.
2. Connect the BSXSICOMB Out to a Variable ISI Channel inputs.
3. Connect the Variable ISI Channel outputs to a Replica Channel inputs.
4. Connect the Replica Channel outputs to the Scope Ch1, Ch3 (or Ch2, Ch4).

Note: The above diagram shows a variable ISI generator being used for ISI generation, that is selected from the 'ISI Generator' tab on the Setup Configuration page. See Appendix A and B in this document for more information on the use of variable and fixed ISI generation.

4.2 Test Selection

The **Select Tests** page is the place where the Rx compliance, margin tolerance, and advanced sweep tests that need to be performed are selected.

Note: The advanced parameter sweep tests will only appear for selection if the Advanced PVT Features are enabled. *Refer to Section 4.3 for how to enable Advanced PVT as well as Section 11 for details on using the Advanced PVT features.*

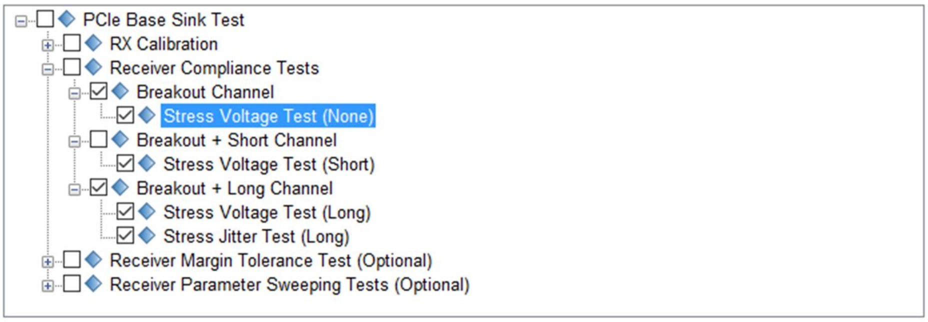


FIGURE 32. SELECT DUT RX TESTS

Tests are run from the same page similar to calibration as shown in Section 3.2.5.

4.2.1 Connection Setup for No Breakout Channel Length Effect

4.2.1.1 Using Tektronix BSA BERTScope

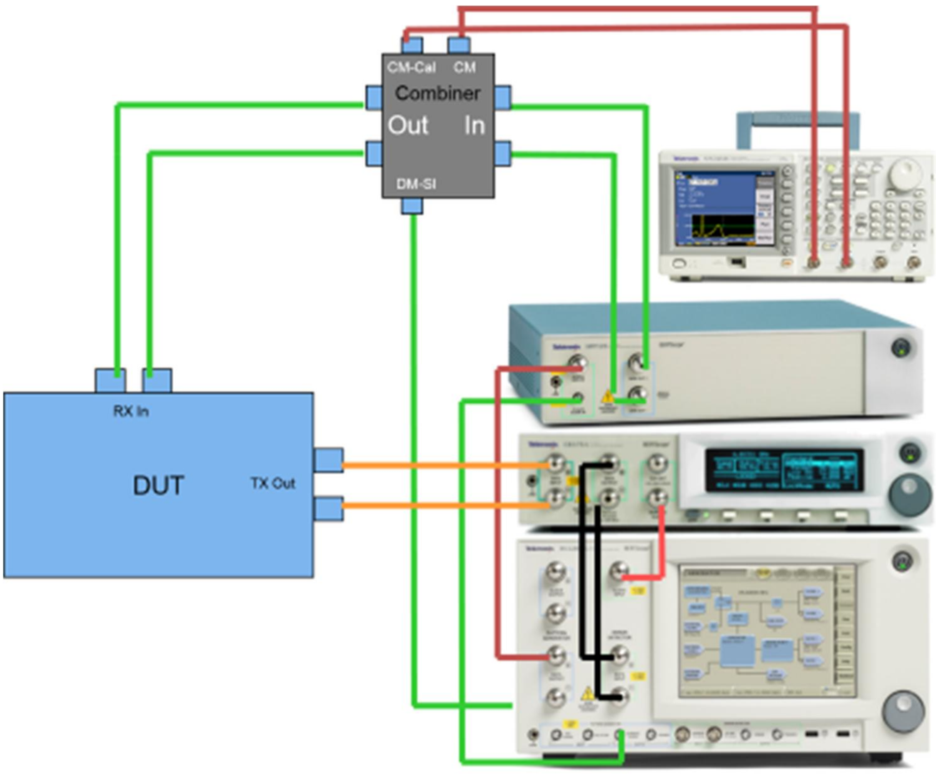


FIGURE 33. TYPICAL SETUP FOR RX COMPLIANCE TEST (NO BREAKOUT CHANNEL LENGTH) (USING TEKTRONIX BSA BERTSCOPE)

Connection Steps:

1. Connect BERTScope Data(+) Out to DPP.
2. Connect BERTScope Clock Out to DPP.
3. Connect DPP Data(+) Out to Combiner In.
4. Connect DPP Data(-) Out to Combiner In.
5. Connect AFG Output1 to Combiner CM-In.
6. Connect AFG Output2 to Combiner CM-Cal.
7. Connect BERTScope (real panel) SI-Out to Combiner DM In.
8. Connect Combiner Data Outputs to DUT Rx Inputs.
9. Connect DUT Tx Outputs to Clock Recovery Unit Data Inputs.
10. Connect Clock Recovery Unit Data Outputs to BERTScope Error Detector Data Inputs.
11. Connect Clock Recovery Unit Subrate Clock Out to BERTScope Error Detector Clock In.
12. Connect BERTScope External Clock to DUT as Reference Clock (100MHz).

4.2.1.2 Using Tektronix BSX BERTScope *(Recommended option)*

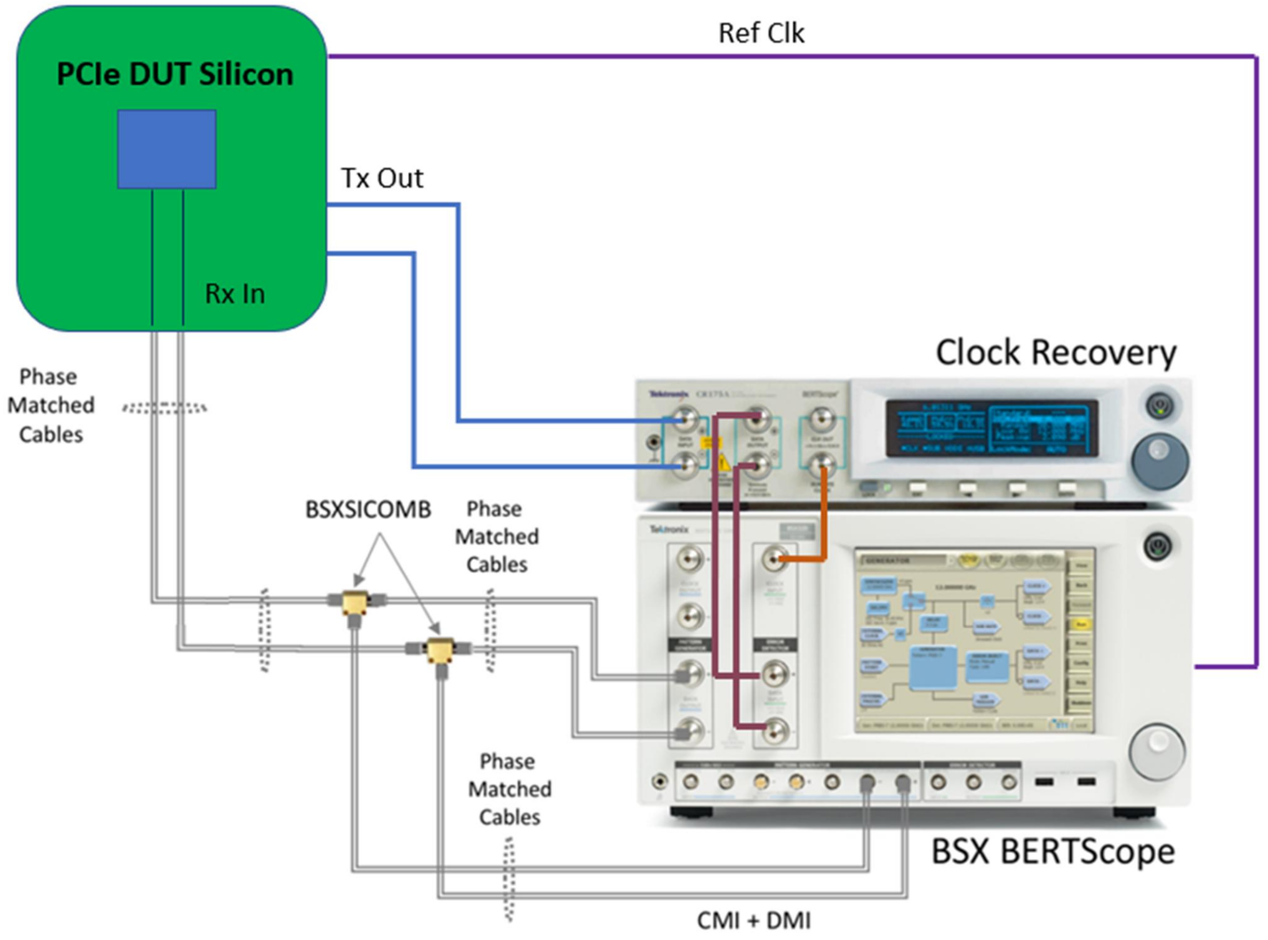


FIGURE 34. TYPICAL SETUP FOR RX COMPLIANCE TEST (NO BREAKOUT CHANNEL LENGTH) (USING TEKTRONIX BSX BERTSCOPE)

Connection Steps:

1. Using back the same connections from the TP2 calibration setup, disconnect and remove the Scope and Calibration Channel from the setup.
2. Connect the BSXSICOMB Out to the DUT Rx inputs.
3. Connect the DUT Tx outputs to the Clock Recovery Unit (CRU) Data In.
4. Connect the CRU Data Out to the BERTScope Error Detector Data In.
5. Connect the CRU Subrate Clock Out to the BERTScope Error Detector Clock In.
6. Connect the BERTScope Ref Out to the DUT as Reference Clock (100 MHz).

4.2.2 Connection Setup for Short/Long Breakout Channel Length Effect

4.2.2.1 Using Tektronix BSA BERTScope

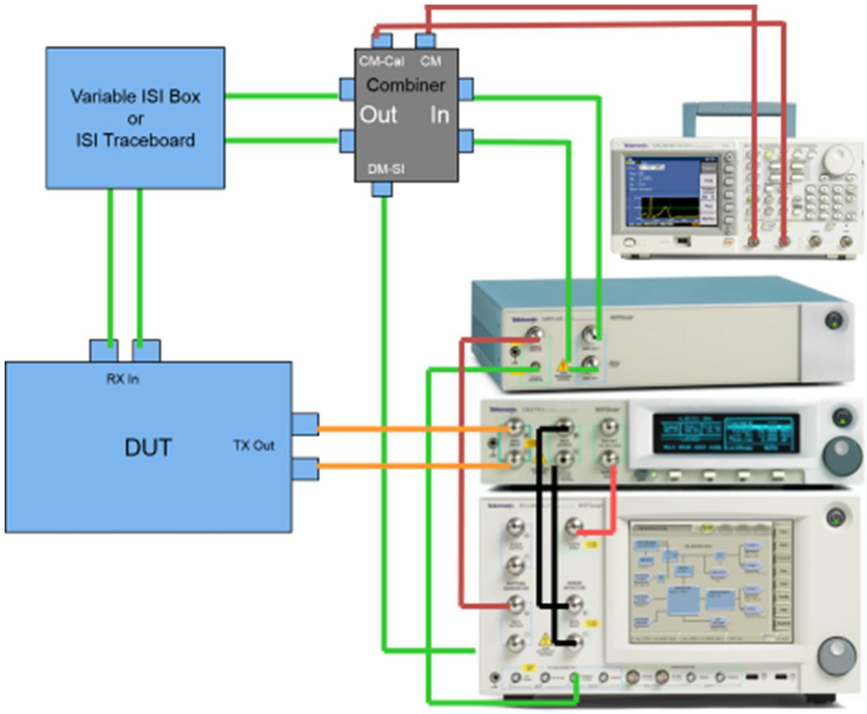


FIGURE 35. TYPICAL SETUP FOR RX COMPLIANCE TEST (WITH BREAKOUT CHANNEL LENGTH) (USING TEKTRONIX BSA BERTSCOPE)

Connection Steps:

1. Connect BERTScope Data(+) Out to DPP.
2. Connect BERTScope Clock Out to DPP.
3. Connect DPP Data(+) Out to Combiner In.
4. Connect DPP Data(-) Out to Combiner In.
5. Connect AFG Output1 to Combiner CM-In.
6. Connect AFG Output2 to Combiner CM-Cal.
7. Connect BERTScope (real panel) SI-Out to Combiner DM-In.
8. Connect Combiner Data Outputs to ISI Generator Inputs.
9. Connect ISI Generator Outputs to DUT Rx Inputs.
10. Connect DUT Tx Outputs to Clock Recovery Unit Data Inputs.
11. Connect Clock Recovery Unit Data Outputs to BERTScope Error Detector Data Inputs.

12. Connect Clock Recovery Unit Subrate Clock Out to BERTScope Error Detector Clock In.
13. Connect BERTScope External Clock to DUT as Reference Clock (100MHz).

Note: The above diagram shows either a variable ISI generator or a fixed ISI channel being used for ISI generation, that is selected from the 'ISI Generator' tab on the Setup Configuration page. See Appendix A and B in this document for more information on the use of variable and fixed ISI generation.

4.2.2.2 Using Tektronix BSX BERTScope *(Recommended option)*

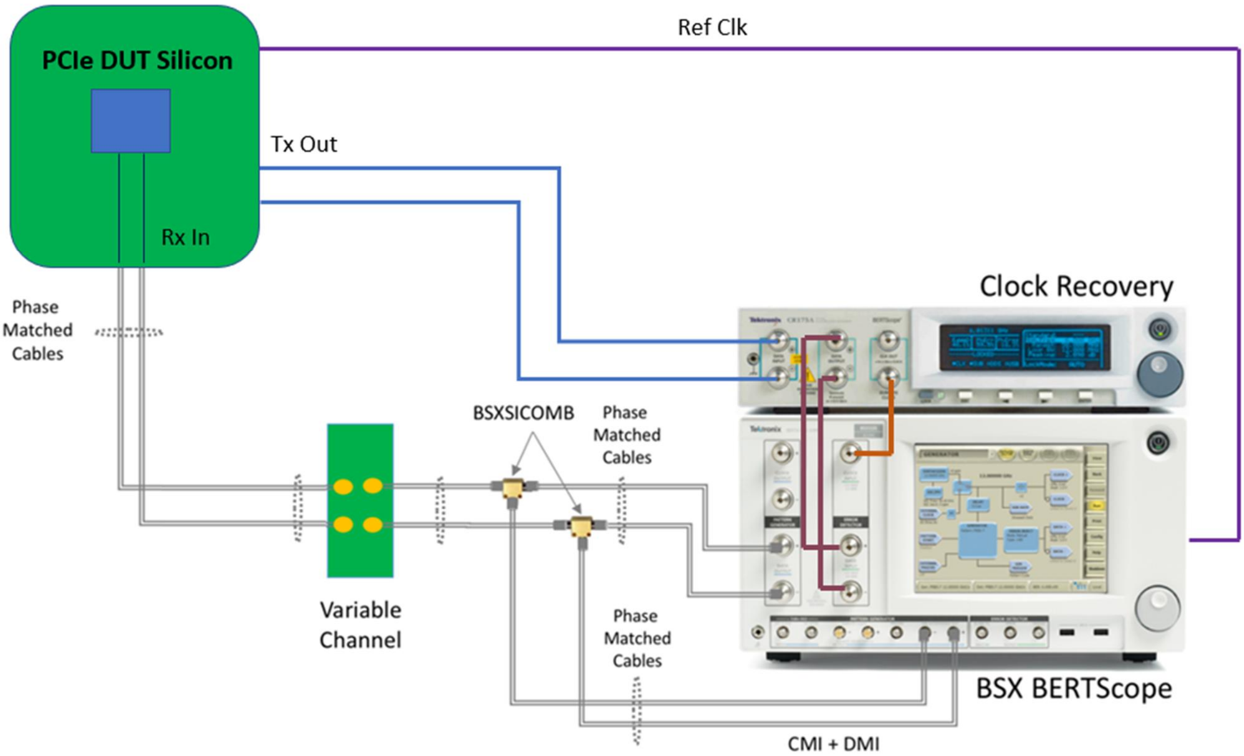


FIGURE 36. TYPICAL SETUP FOR RX COMPLIANCE TEST (WITH BREAKOUT CHANNEL LENGTH) (USING BSX BERTSCOPE)

Connection Steps:

1. Using back the same connections from the TP2 calibration setup, disconnect and remove the Scope and Replica Channel from the setup.
2. Connect the Variable ISI Channel outputs to the DUT Rx inputs.
3. Connect the DUT Tx outputs to the Clock Recovery Unit (CRU) Data In.
4. Connect the CRU Data Out to the BERTScope Error Detector Data In.
5. Connect the CRU Subrate Clock Out to the BERTScope Error Detector Clock In.
6. Connect the BERTScope Ref Out to the DUT as Reference Clock (100 MHz).

Note: The above diagram shows a variable ISI channel being used for ISI generation, that is selected from the 'ISI Generator' tab on the Setup Configuration page. See Appendix A and B in this document for more information on the use of variable and fixed ISI generation.

4.3 Test Parameters Configuration

Select  from the main menu to access the Configurations page. Set to enable Advanced PVT automation and reference clock as well as other parameters for Rx margin tolerance tests as described below.

To return all parameters to their default settings, select the 'Set Default' button.

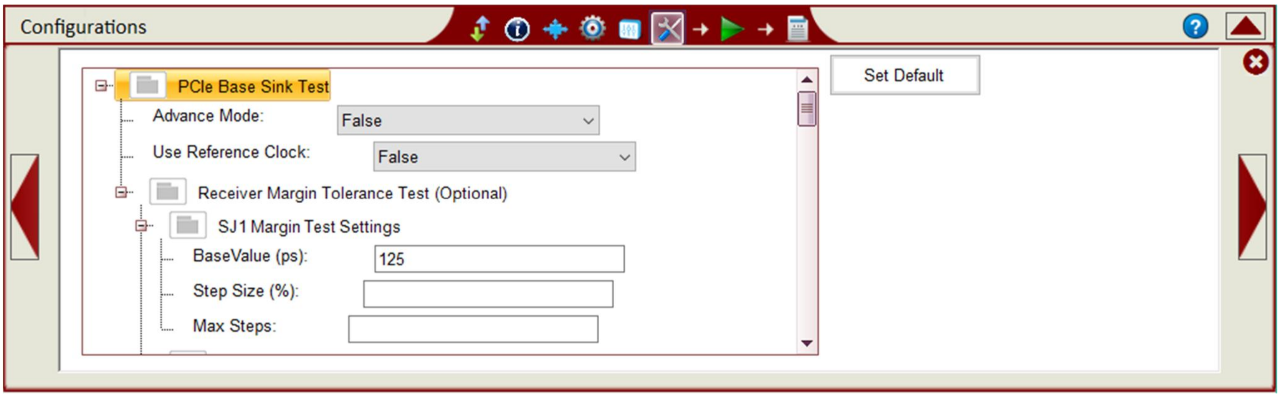


FIGURE 37. TEST PARAMETERS CONFIGURATION PAGE

TABLE 3. TEST PARAMETERS DESCRIPTION

Parameter	Description
Advance Mode	Select 'True' to enable Advanced PVT Automation control to support repeated testing within sequences of parameter values, which are applied to the DUT during testing.
Use Reference Clock	Select 'True' to enable 100 MHz reference clock output from the BERTScope to the DUT.
SJ# Margin Test Settings – Base Value	Set the duration to run margin search tests for each respective SJ margin.
SJ# Margin Test Settings – Step Size	Set the step size for stepping through SJ margins when running margin search tests.
SJ# Margin Test Settings – Max Steps	Set the maximum number of steps to step through SJ margins during margin search tests.

5 Test Results and Report Generation

The **Report** page has all the results from all the calibration and test runs displayed. If some of the results are not desired, they can be individually deleted by selecting the **Delete** button. For a PDF report, click the **Generate report** button. To have the calibration data plotted in the report, make sure the Plot Calibration Data box is checked.

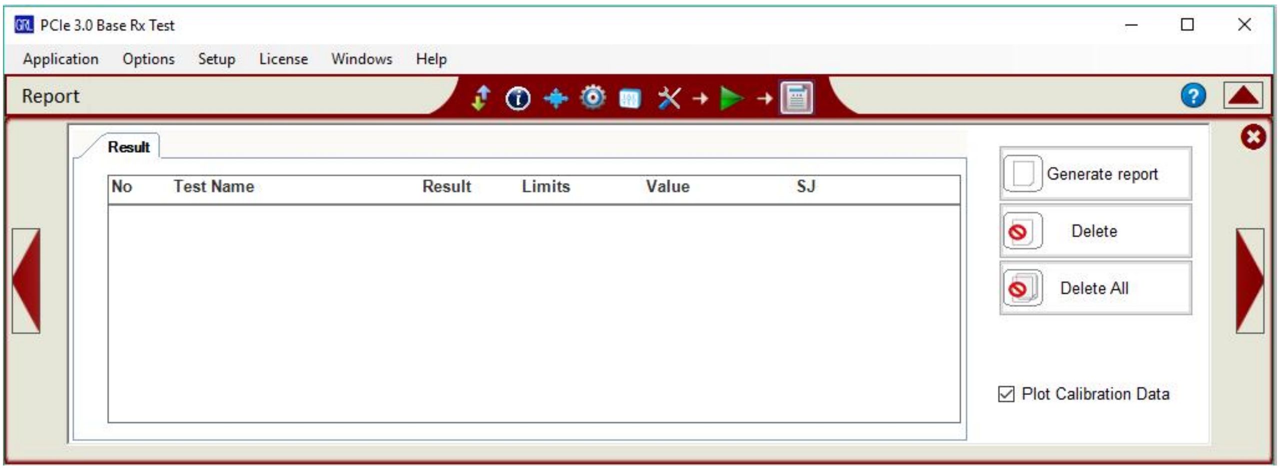
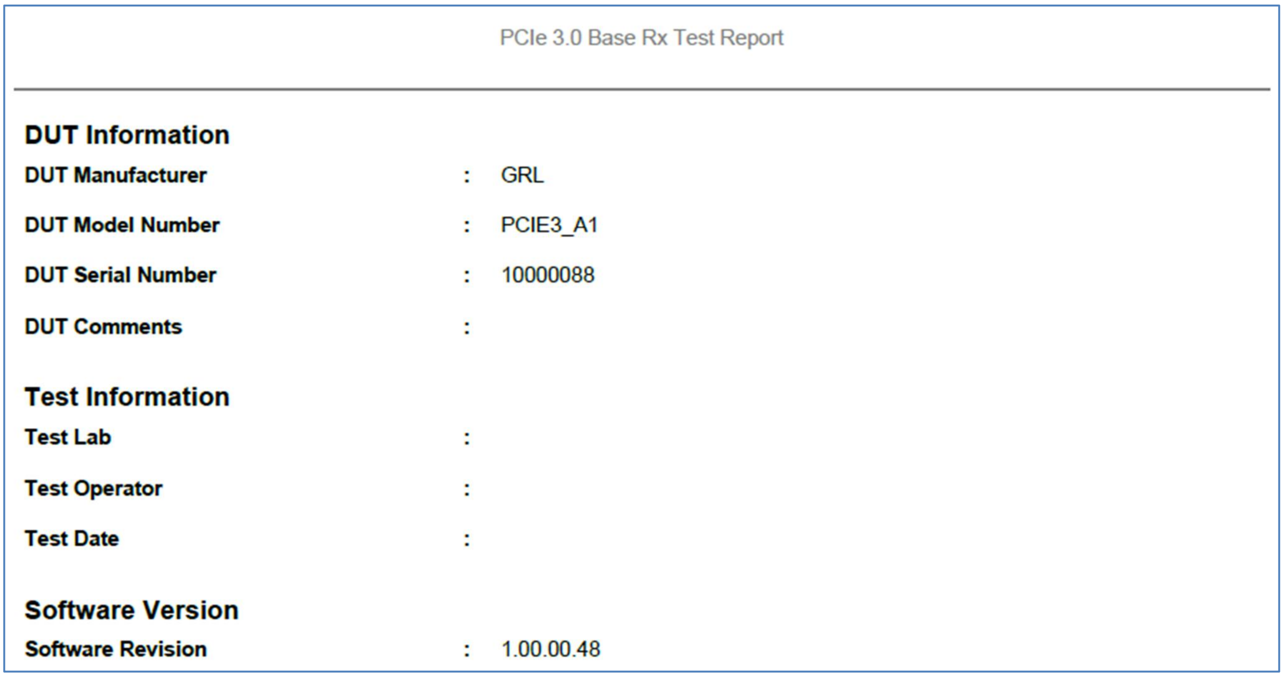


FIGURE 38. TEST RESULTS AND REPORT PAGE

5.1 Interpreting the Report

5.1.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.



PCIe 3.0 Base Rx Test Report

DUT Information

DUT Manufacturer	:	GRL
DUT Model Number	:	PCIE3_A1
DUT Serial Number	:	10000088
DUT Comments	:	

Test Information

Test Lab	:	
Test Operator	:	
Test Date	:	

Software Version

Software Revision	:	1.00.00.48

FIGURE 39. DUT INFORMATION

5.1.2 Summary Table

This portion is populated from the tests performed and its results. This gives an overall view of all the results and its test conditions.

No	TestName	Limits	Value	Results	De-Emphasis	Voltge Swing	SJ
1	Pre-shoot Calibration	True/False	True	Pass			
2	De-emphasis Calibration	True/False	True	Pass			
3	Launch Amplitude Calibration	True/False	True	Pass			
4	Rj Calibration	True/False	True	Pass			
5	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_1
6	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_2
7	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_3
8	Sj Calibration	True/False	True	Pass	N/A	N/A	SJLF_4
9	CM Sinusoidal Interference Calibration (Short)	True/False	True	Pass			
10	DM Sinusoidal Interference Calibration (Short)	True/False	True	Pass			
11	Stressed Voltage Calibration (Short)	True/False	False	Fail			
12	CM Sinusoidal Interference Calibration (Long)	True/False	True	Pass			
13	DM Sinusoidal Interference Calibration (Long)	True/False	True	Pass			
14	Stressed Voltage Calibration (Long)	True/False	False	Fail			
15	Stress Jitter Calibration (Long)	True/False	False	Fail			
16	Insertion Loss Calibration (Long)	True/False	True	Pass			
17	Insertion Loss Calibration (Short)	True/False	True	Pass			
18	Insertion Loss Calibration	True/False	False	Fail			

FIGURE 40. SUMMARY TABLE

5.1.3 Calibration Data Results

If Plot Calibration Data checkbox is checked, then the plots are shown in this part of the report.

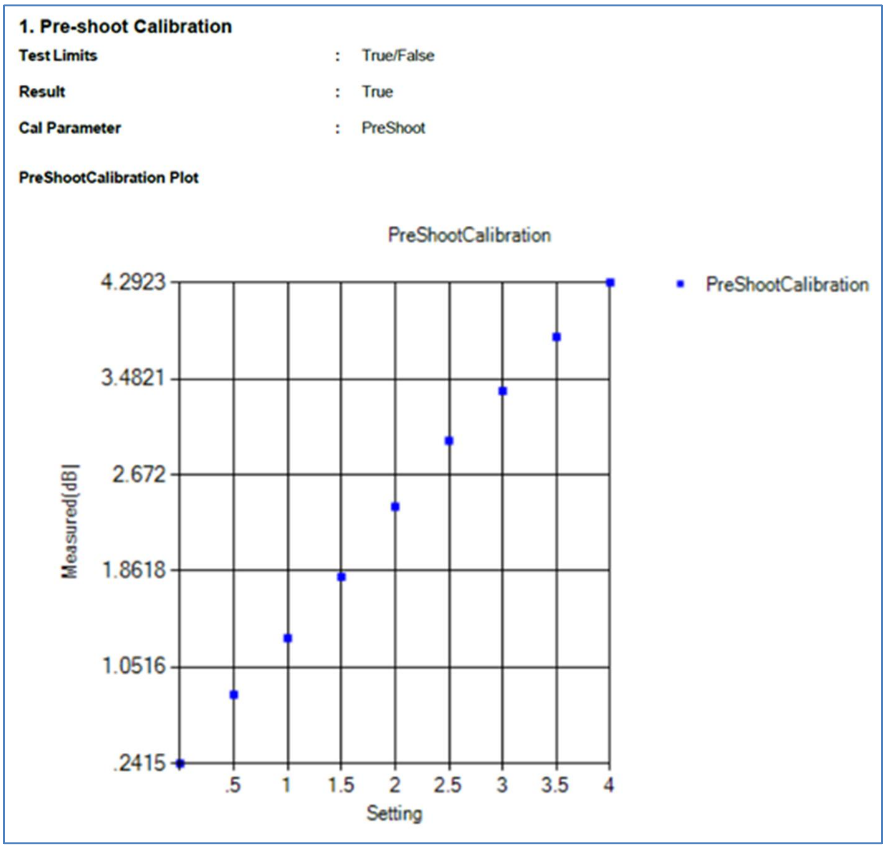


FIGURE 41. CALIBRATION RESULTS EXAMPLE

5.1.4 Compliance Test Results

Compliance Test(Main)

Sj Frequency	SJ1 - 30 KHz	SJ2 - 1 MHz	SJ3 - 10 MHz	SJ4 - 100 MHz
Result	PASS(0)	PASS(0)	PASS(0)	PASS(0)

FIGURE 42. CALIBRATION RESULTS EXAMPLE

5.1.5 Jitter Margin Results

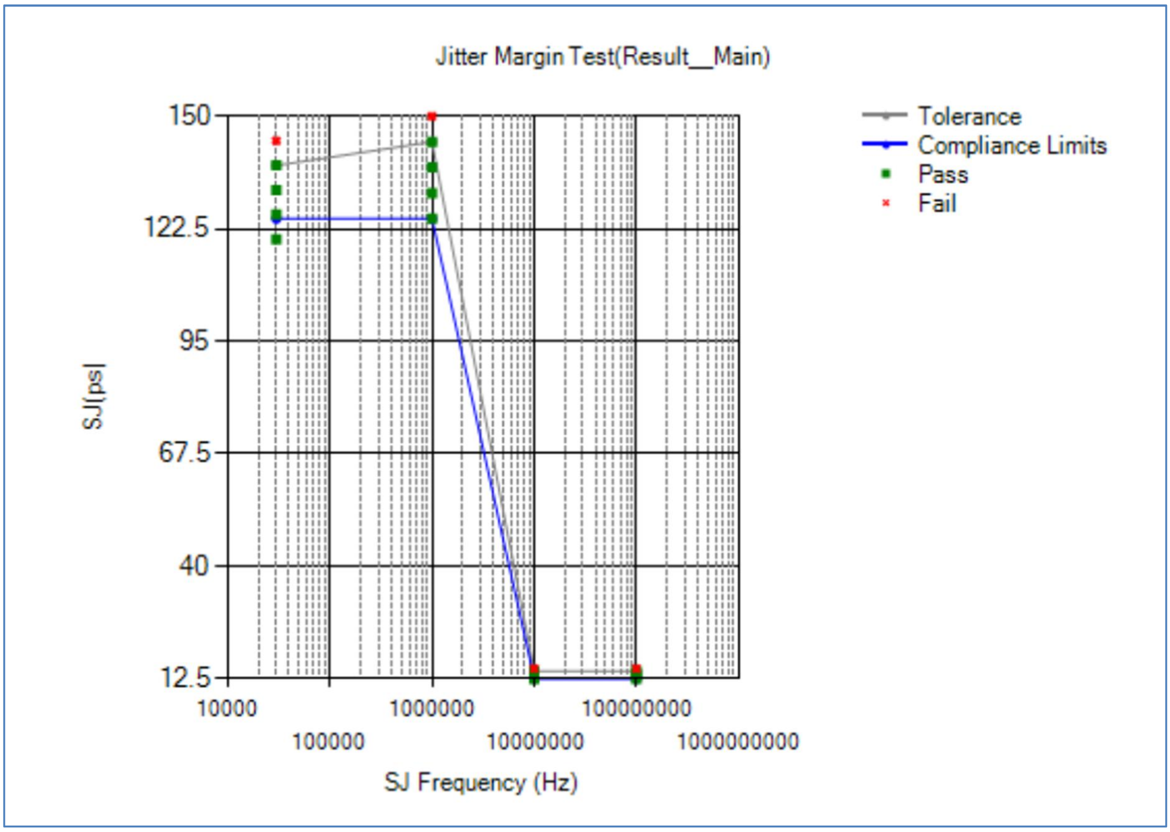


FIGURE 43. JITTER MARGIN REPORT EXAMPLE

6 Saving and Loading Test Sessions

The usage model for the GRL PCIe3-BASE & PCIe4-BASE (8GT/s) Rx software is that Calibration and Test Results are created and maintained as a 'Live Session' in the Application. This allows you to Quit the application and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To Save a session, with all of the PVT parameter information, the test results, and any waveforms, use the "Options" command on the menu bar, then the "Save Session" command.

To Load a session back into the software, including the saved parameter settings, use the "Options" command on the menu bar, then the "Load Session" command.

To create a New session and return the application back to a default configuration, use the "Options" command on the menu bar, then the "New Session" command.

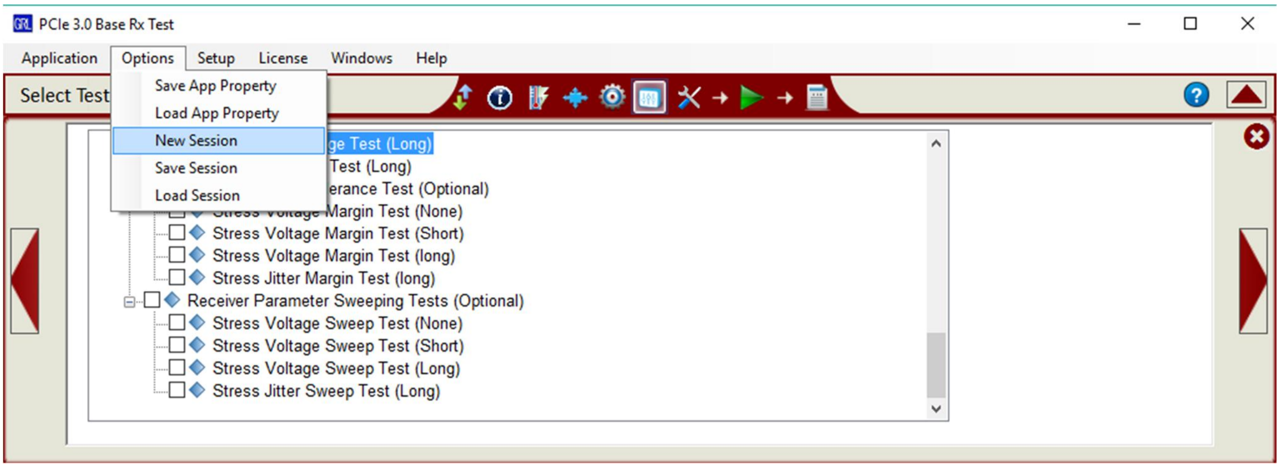


FIGURE 44. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

7 Appendix A: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

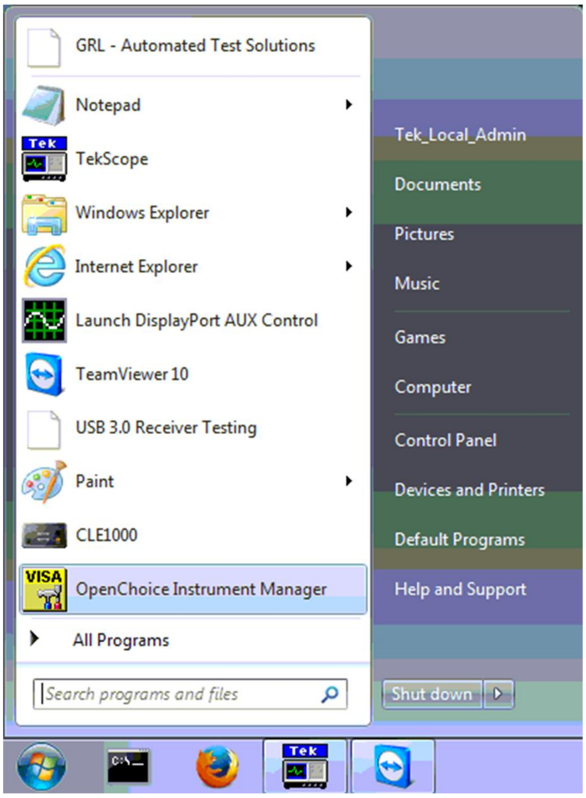


FIGURE 45. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

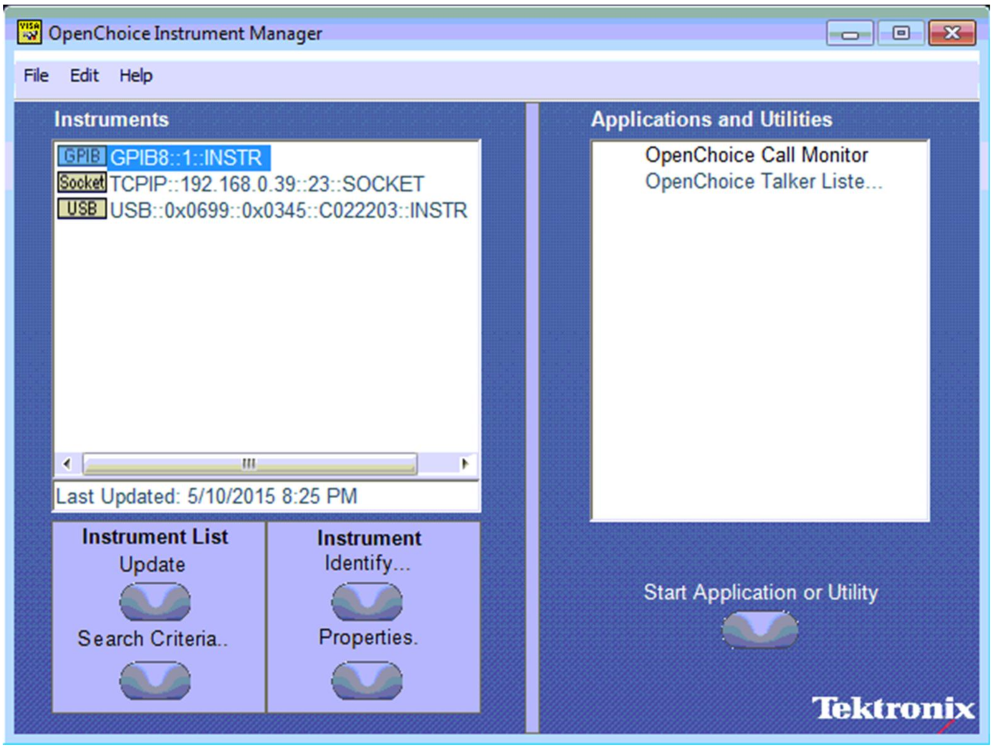


FIGURE 46. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe 3.0 Base Rx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe 3.0 Base Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

8 Appendix B: Artek CLE Model Series Installation

8.1 ISI Generator Driver Installation

If using a Artek CLE Model unit for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the Artek unit to the PC being used as the controller using a USB 2.0 cable.
2. Turn on the front panel power switch on the Artek unit.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for Artek has been installed, you will see a 'bang' in the Device Manager.

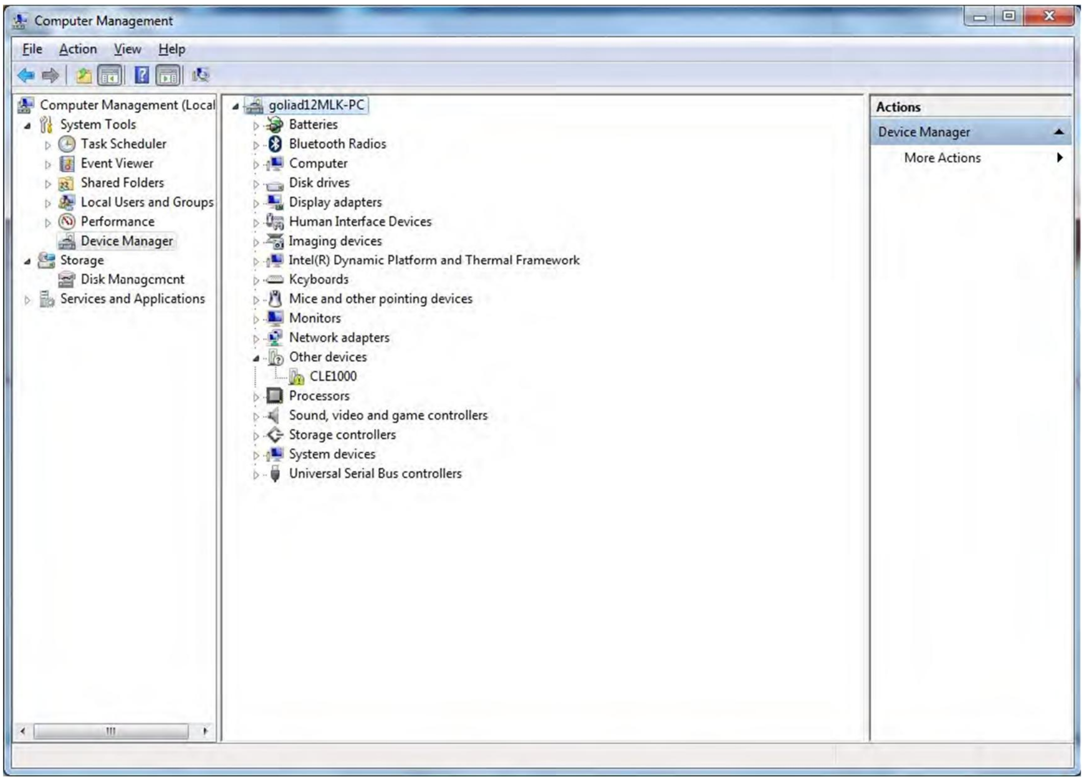


FIGURE 47. DEVICE MANAGER WINDOW

4. To install the Artek driver, go to http://www.aceunitech.com/support.html and download the Control Software package for the Artek CLE Series.
5. Unzip the CLE Series Software folder and install the driver as follows:

   a) In Device Manager, right-click on **CLExxxx** > **Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 48.
   c) Browse to the root directory of the unzipped CLE Series Software folder.
   d) Click **Next** and then click **Install** to complete installation for the driver software. See Figure 49.

   Once installation has completed, the Device Manager window should look like the example in Figure 50.

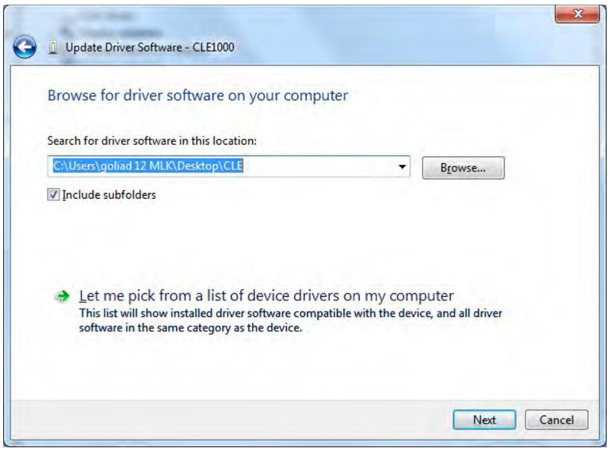


FIGURE 48. UPDATE DRIVER WINDOW

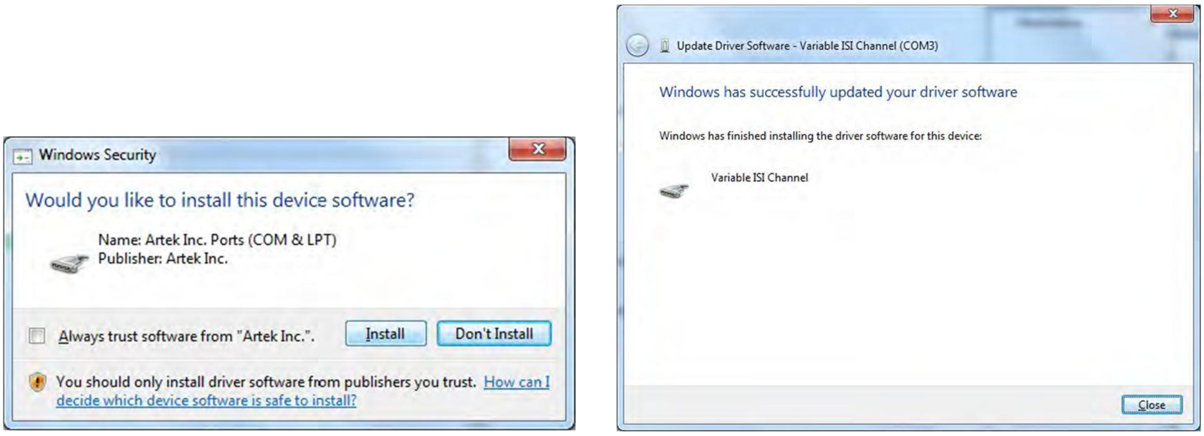


FIGURE 49. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW

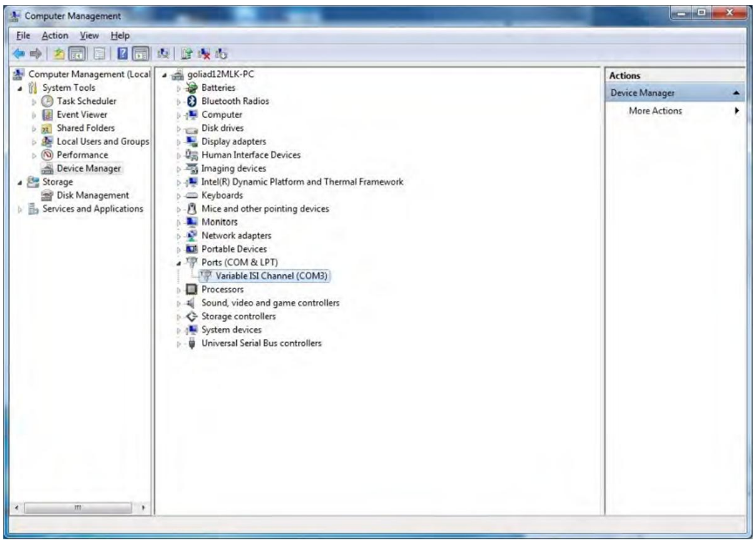


FIGURE 50. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE Series software driver is now installed and the Artek unit can now be selected for use remotely using the GRL software.

8.2 CLE Series User Interface (UI) Installation

It may also be useful to install the CLE Series UI, so that the ISI channel can also be controlled manually from the computer. To install the UI, follow these steps:

1. In the CLE Series Software folder, select and install the Setup.exe file. Upon successful installation, the following UI window will appear.
2. Close this window if manual control is not required.

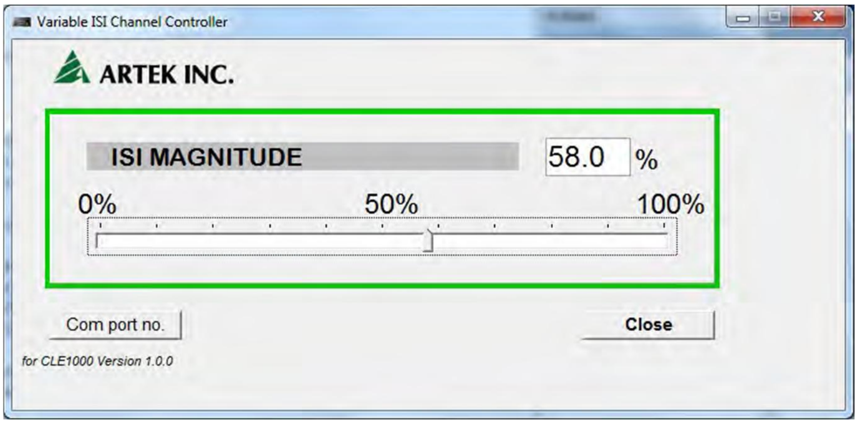


FIGURE 51. CLE SERIES UI

8.3 Return Loss Limitations of the Artek CLE1000-A2

If using the Artek CLE1000-A2 for Insertion Loss, it should be understood that the Return Loss Specifications of the CLE1000 does not meet the specific requirements of the PCI Express 3.0 Base Specification. The return loss of the CLE1000 varies with the % of ISI that is provided. The following two plots show the return loss of the CLE1000 at Channel lengths of 10% to 50%, which would be the typical range of a PCIe3 Calibrated Channel.

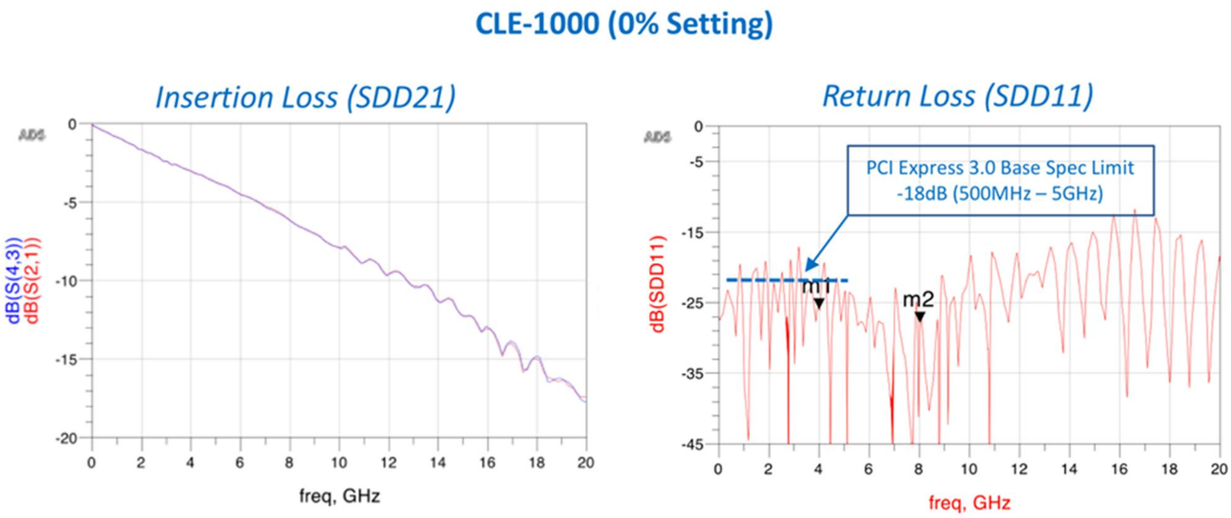


FIGURE 52. CLE1000-A2 VARIABLE ISI GENERATOR IL, RL AT 0% SETTING

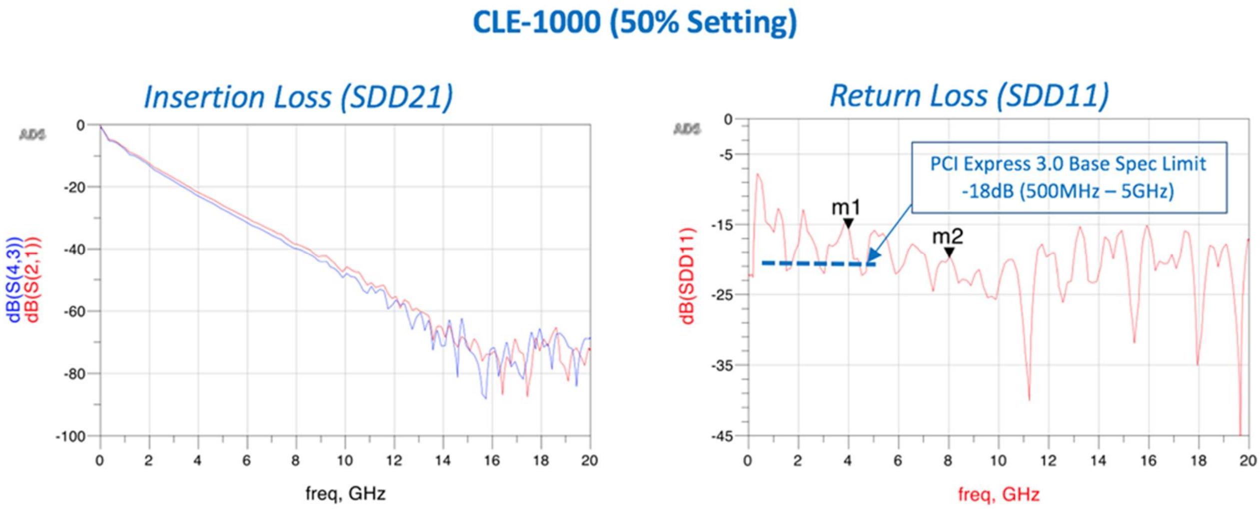


FIGURE 53. CLE1000-A2 VARIABLE ISI GENERATOR IL, RL AT 50% SETTING

9 Appendix C: BERTScope ISI Trace Board

The BERTScope ISI Trace Board is used for PCIe Base 3.0 Insertion Loss tests.

Figure 54 describes the insertion loss at 4GHz on various trace lengths on the BERTScope ISI Trace Board.

	2.42 inch	5 inch	6.75 inch	9 inch	12 inch	17 inch	24 inch	31 inch	40 inch
FREQ MHz	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB	Sdd21 dB
4000	-0.89	-1.73	-2.34	-2.99	-3.9	-5.49	-7.63	-9.7	-12.54

FIGURE 54. INSERTION LOSS PER TRACE LENGTH

For PCIe Gen3 type of trace length to be tested, follow the table in Figure 55 to connect points of the trace board to get the desired insertion loss.

	Target Insertion Loss(I.L.)	**Trace Length(Insertion Loss)**
Replica Channel	-2.5 +/- 1dB	6.75 inch (-2.34dB) Total I.L. = -2.34dB
Replica Channel + Short Channel	-12.0 +/- 2dB	6.75 inch (-2.34dB) 31 inch (-9.7 dB) Total I.L. = -12.04 dB
Replica Channel + Long Channel	-20 +/- 2dB	6.75 inch (-2.34dB) 17inch (-5.49 dB) 40 inch (-12.54 dB) Total I.L. = -20.46 dB

FIGURE 55. INSERTION LOSS CONNECTIONS TABLE

10 Appendix D: Manual Test Methods

10.1 Waveform Tests

10.1.1 Preshoot and Deemphasis

PCIe Base Gen3 uses two presets for different trace lengths of the breakout board. Both Deemphasis and Preshoot are calibrated for the target dB for each preset. See Table 4.

TABLE 4. PRESETS FOR WAVEFORM TESTS

Preset	Preshoot	Deemphasis
4	0.0dB	3.5dB
7	0.0dB	-6.0dB

10.1.1.1 BERTScope Setup

1. Set the BERTScope to defaults.
2. Set Generator to 8Gpbs (PCIe Gen3 Speed).
3. Disable all stressed jitter component (Rj, Sj etc).
4. Set the Output amplitude to 800mV.
5. Set the DPP Output 460mV.
6. Default the DPP to 0.0dB Preshoot and Deemphasis, as shown in Figure 56.
7. Load with 64 ONEs, 64 ZEROs and 128 Clk Pattern to the BERTScope.

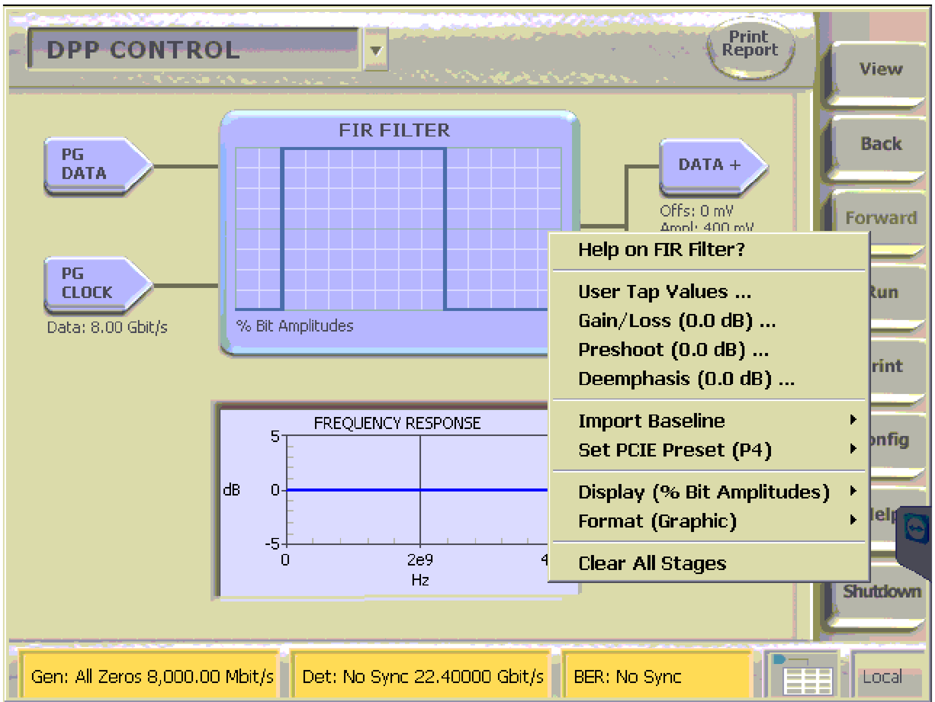


FIGURE 56. BERTSCOPE SETUP

10.1.1.2 Scope Setup and Measurement

1. Set the scope to Defaults.
2. Set the scope Sampling mode to Real Time Only.
3. Set the scope acquisition to average with 256 waveforms.
4. Set the trigger of A_Event type to timeout.
5. Set the Chan1 and Chan2 display to ON; configure the scale and offset so the waveform covers 80% of the screen.
6. Enable Math1; set Math1 to Ch1-Ch2; set the auto scale.
7. Turn off Chan1 and Chan2.
8. Acquire the waveform. An example is shown in Figure 57.

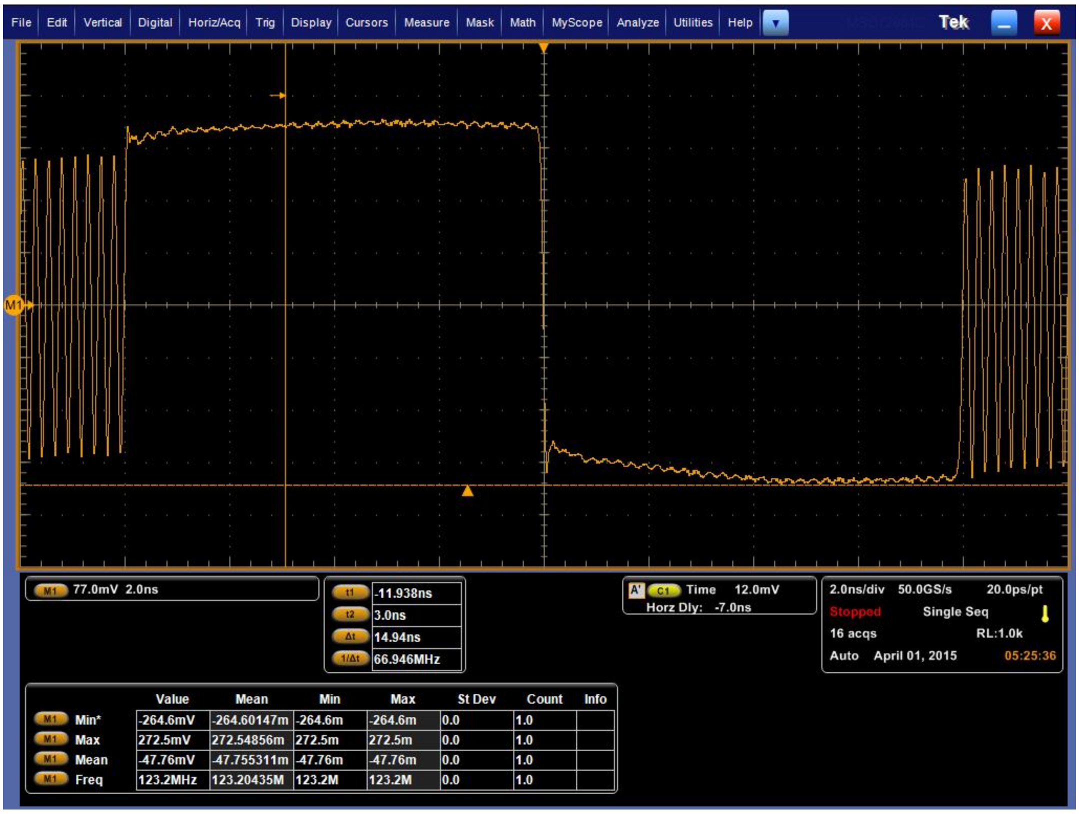


FIGURE 57. SCOPE SETUP AND MEASUREMENT

10.1.1.3 De-emphasis Measurement

Now, the actual de-emphasis and pre-shoot must be verified on the scope.

1. Using cursors, measure the peak-to-peak transition amplitude as shown Figure 58.

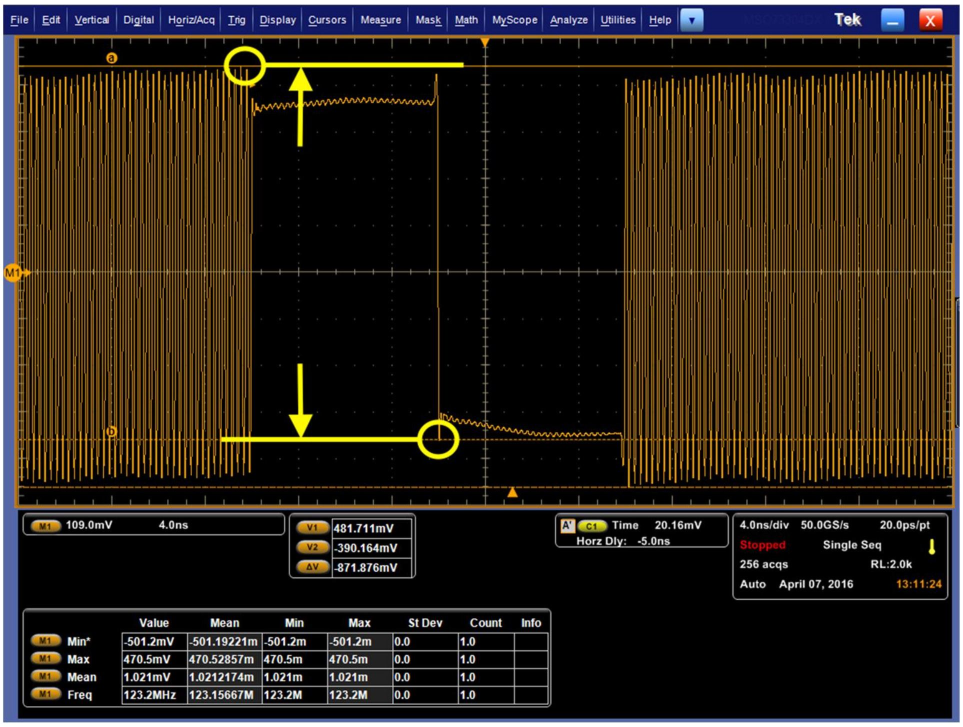


FIGURE 58. MEASURED TRANSITION AMPLITUDE (EXAMPLE 825MVPP)

2. Using cursors, measure the peak-to-peak non-transition amplitude, as shown in Figure 59.

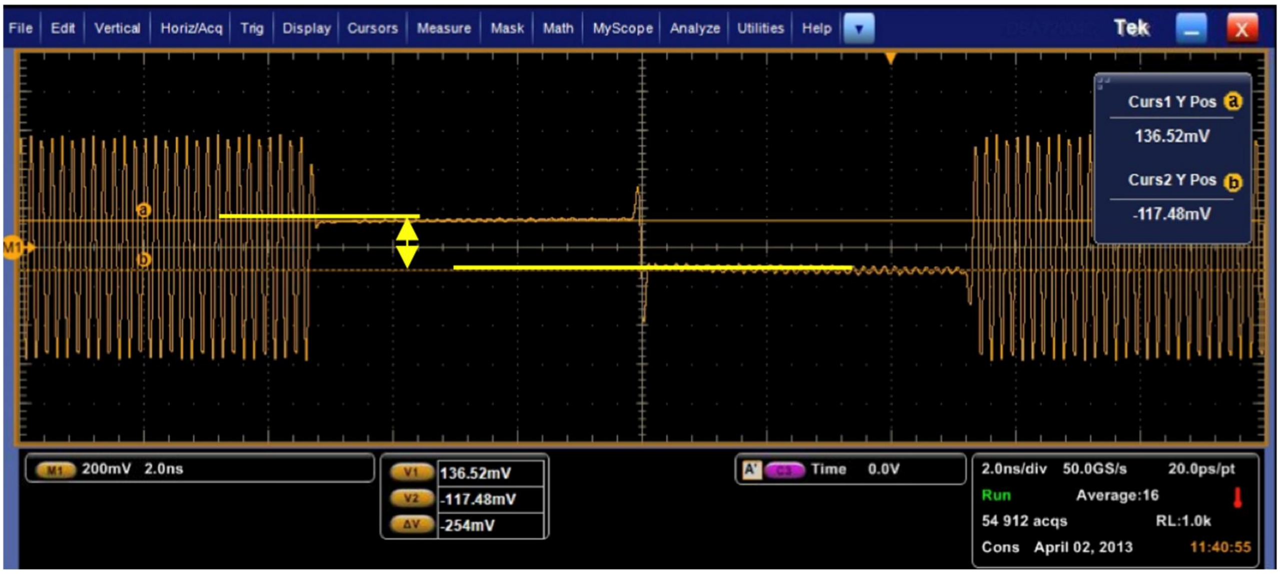


FIGURE 59. MEASURED NON-TRANSITION AMPLITUDE (EXAMPLE 254MV)

3. De-emphasis = 20log[Non-transition/Transition]

   = 20log[254mV/824mV]

   = 20log[0.31]

   = -10.2dB

10.1.1.4 Preshoot Measurement

1. Using cursors, measure pre-shoot amplitude, as shown in Figure 60.

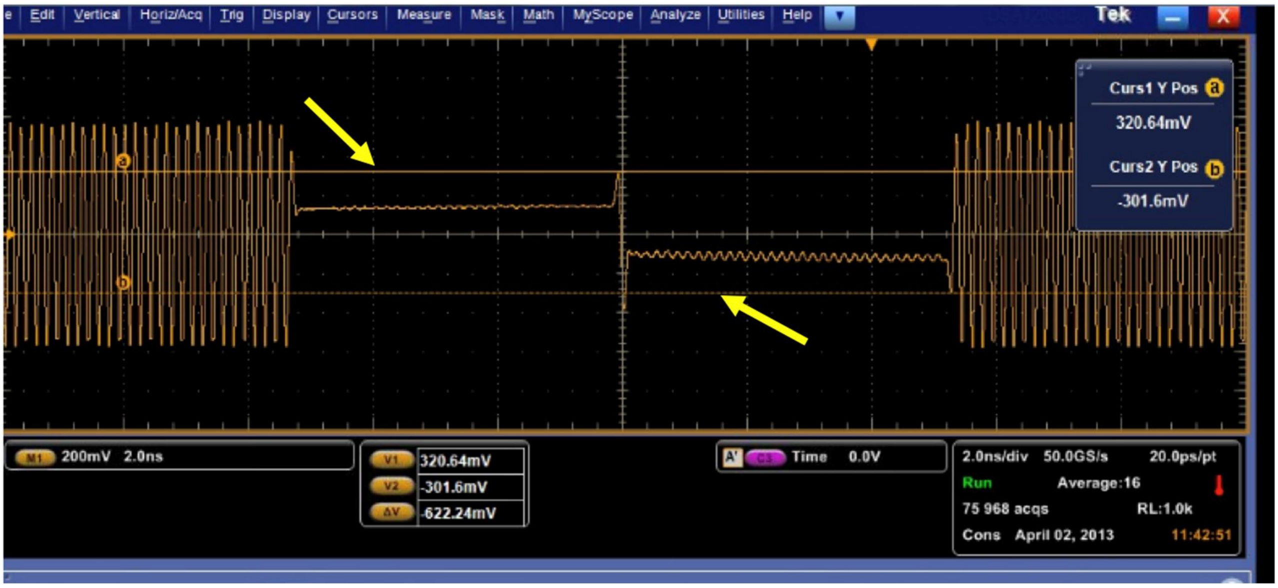


FIGURE 60. MEASURED PRE-SHOOT AMPLITUDE (EXAMPLE 622MV)

2. Measure pre-shoot amplitude.
3. Calculate the pre-shoot: 20log[Pre-shoot/Non-transition]

   = 20log[622 mV/254mV]
   = 20log[2.44]
   = 7.8dB

4. Increase the pre-shoot and de-emphasis levels to record the measured pre-shoot and de-emphasis dB for 3.5 and -6.0, measured respectively. See Figure 61 and Figure 62.
5. Record the value.

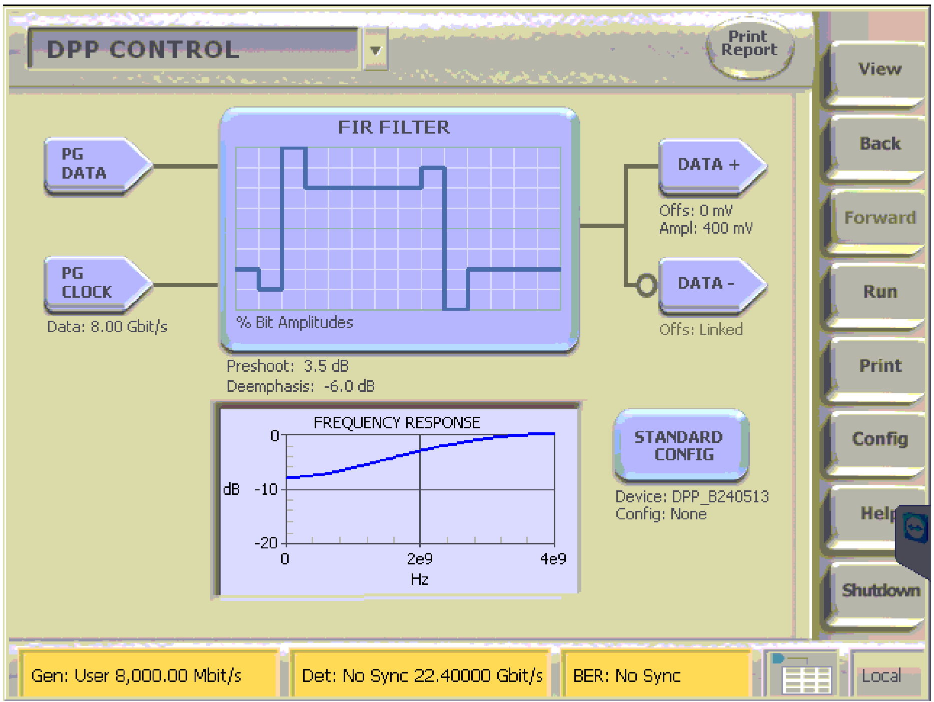


FIGURE 61. BERTSCOPE SETUP #2

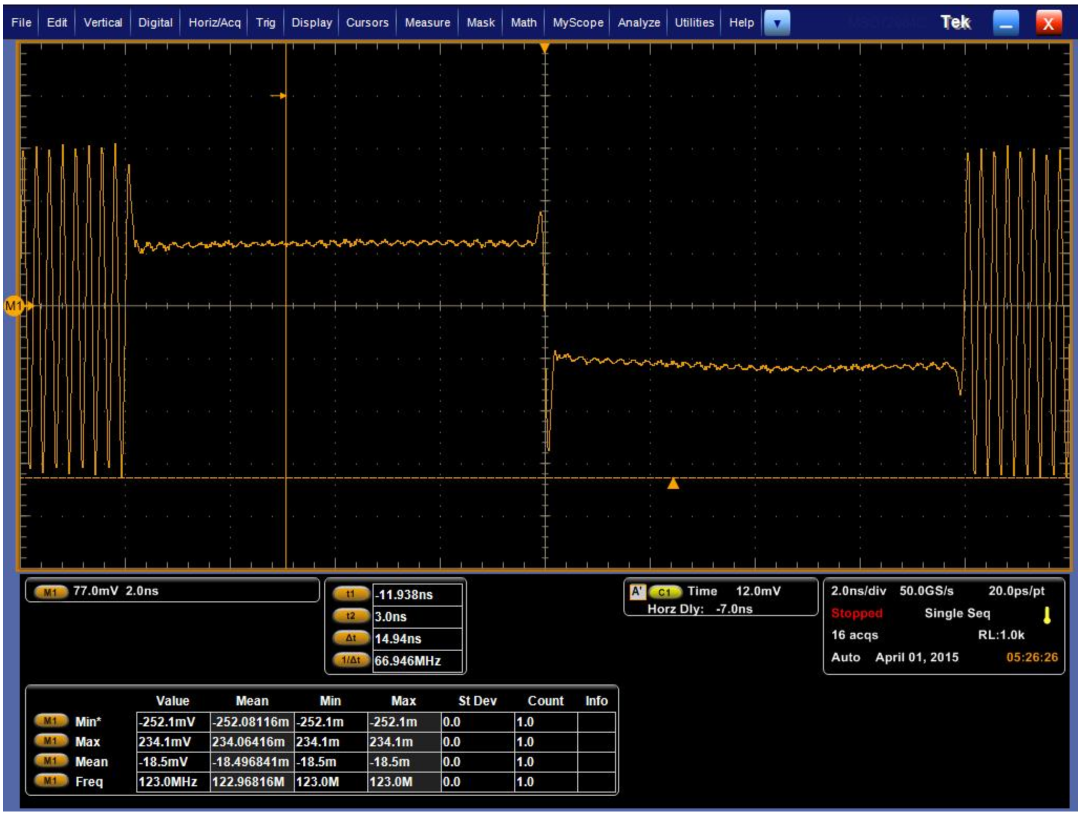


FIGURE 62. SCOPE SETUP AND MEASUREMENT #2

10.1.2 Launch Amplitude

The Launch Amplitude is calibrated for target minimum peak-to-peak amplitude of 800mVpp after combiner.

10.1.2.1 BERTScope Setup

1. Use the same TP1 Calibration Setup.
2. Set DPP to 0.0 for Pre-shoot and De-emphasis.
3. Set DPP Amplitude to 300mV.
4. Set Pattern to Clk/256.

10.1.2.2 Scope Setup and Measurement

1. Use the same Setup, scale Chan1 and Chan2 respectively.
2. Turn off Chan1 and Chan2.
3. Turn on Math1, set to ch1-ch2.
4. Set the Acquisition mode to Average of 256.
5. Set Measure Amplitude of Math1.
6. Acquire waveform.
7. Read the MEAN value of amplitude measurement.
8. Tune the DPP Output until Amplitude measured in scope is 800mV.

10.1.3 Amplitude Equalization

Perform the equalization of low frequency and high frequency amplitude at TP1. This is done by adding a small amount of De-emphasis of DPP, so that the low frequency and high frequency have the same amount of amplitude after combined.

1. Use the same setup of calibration for TP1, and same BERTScope and TekScope setting.
2. Tune the DPP Pre Cursor and Post Cursor so De-emphasis is 0.0dB.
3. Tune the DPP Post Cursor until the low frequency and high frequency component of amplitude is same level. See Figure 63.

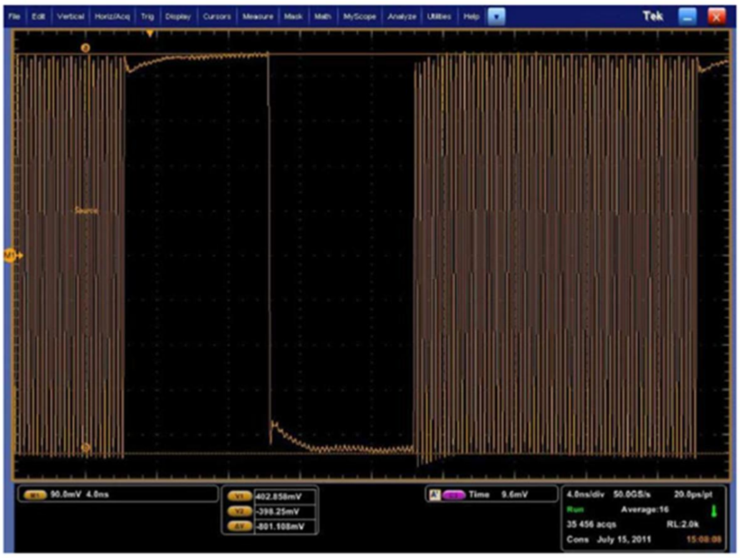


FIGURE 63. AMPLITUDE EQUALIZATION SETUP

4. Save the Post Cursor value.

10.1.4 RJ Calibration

1. Using a Clock pattern (1100), the RJ value of 0ps – 5ps will be calibrated. (Both limits are RMS values.) RJ is used to adjust the Eye Width (EW) in Stress Jitter Test.
2. RJ target is 2ps (RMS).
3. Tektronix DPOJET is used as the calibration tool.

10.1.4.1 BERTScope Setup

1. Set the Generator to 8Gpbs.
2. Set the Sub-rate clock mode is Stressed Clock.
3. Set the RJ Enable.
4. Set the SJ Enable, and set the SJ Amplitude to 0.0mV. See Figure 64.

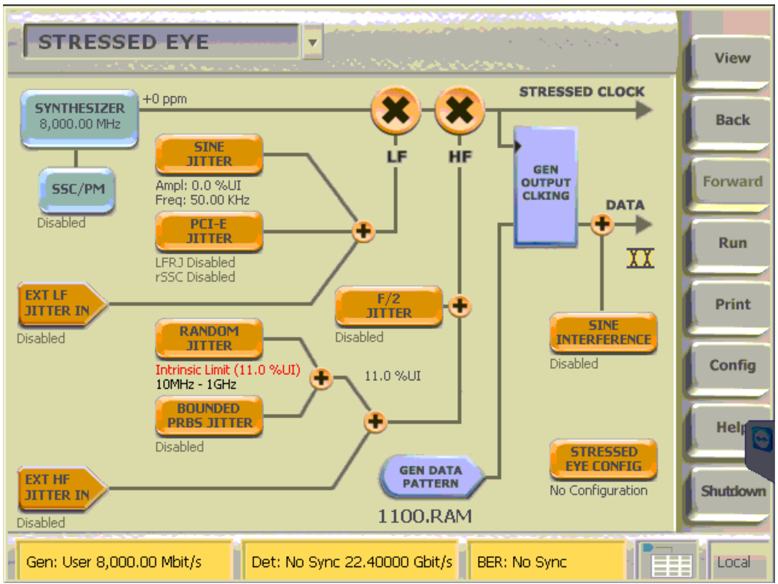


FIGURE 64. BERTSCOPE JITTER SETUP

5. Set the Pattern of generator to 1100.ram (1-1-0-0 pattern). See Figure 65.

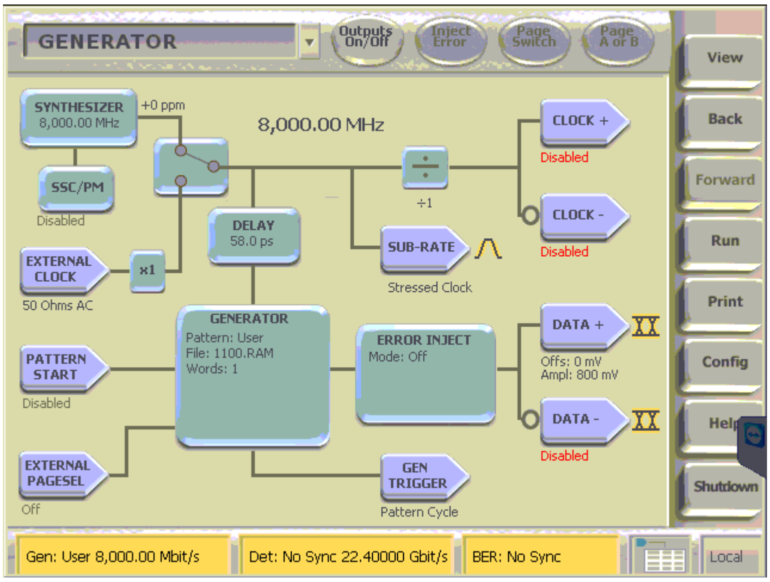


FIGURE 65. BERTSCOPE PATTERN SETUP

10.1.4.2 DPP Setup

1. Set the DPP Pre-shoot and De-emphasis using P4 preset (0.0db for both).
2. Set the post cursor and pre cursor based on equalized amplitude value recorded earlier.
3. Set the DPP output that reflects the 800mV amplitude recorded earlier.

10.1.4.3 Scope Setup

1. Set the DPOJET Configure -> Clock Recovery to Constant Clock Mean.

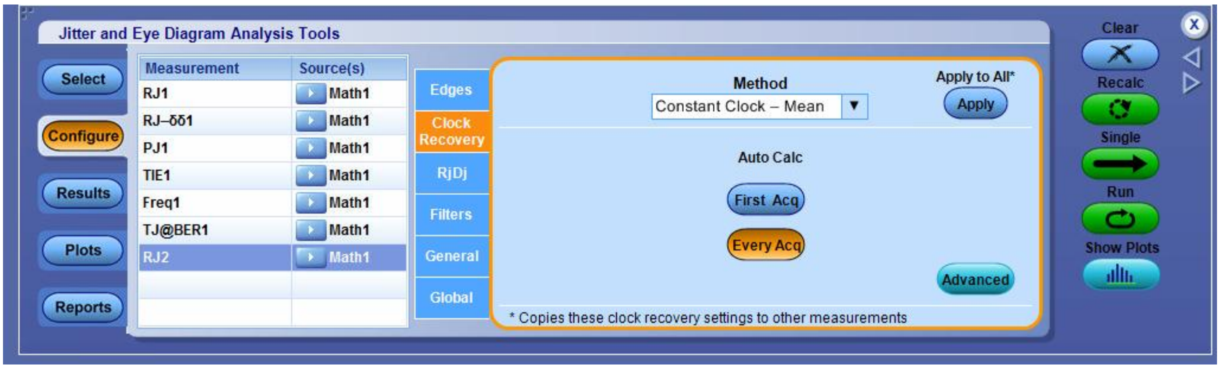


FIGURE 66. DPOJET CONFIGURE SETUP

2. Enter RJDJ settings for clock signal.

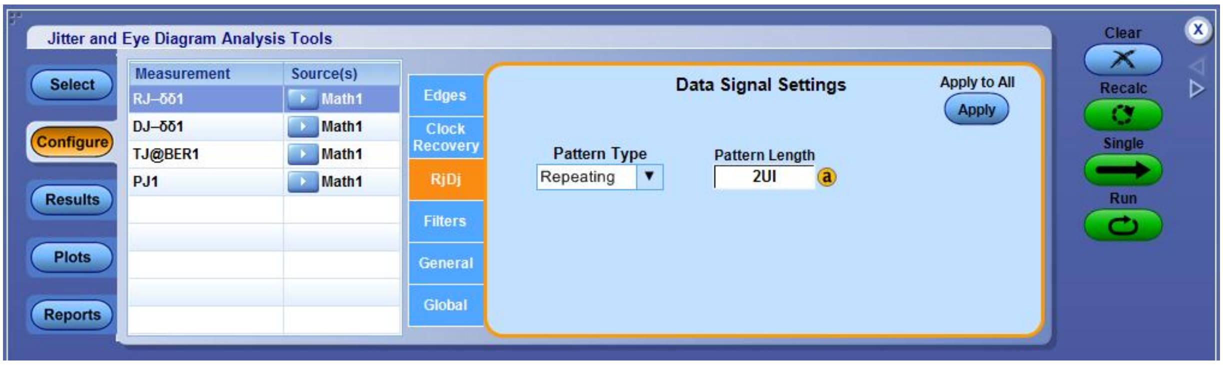


FIGURE 67. RJDJ SETUP

3. On the Advanced Setup panel, set the Nominal Data Rate to 8Gpbs.

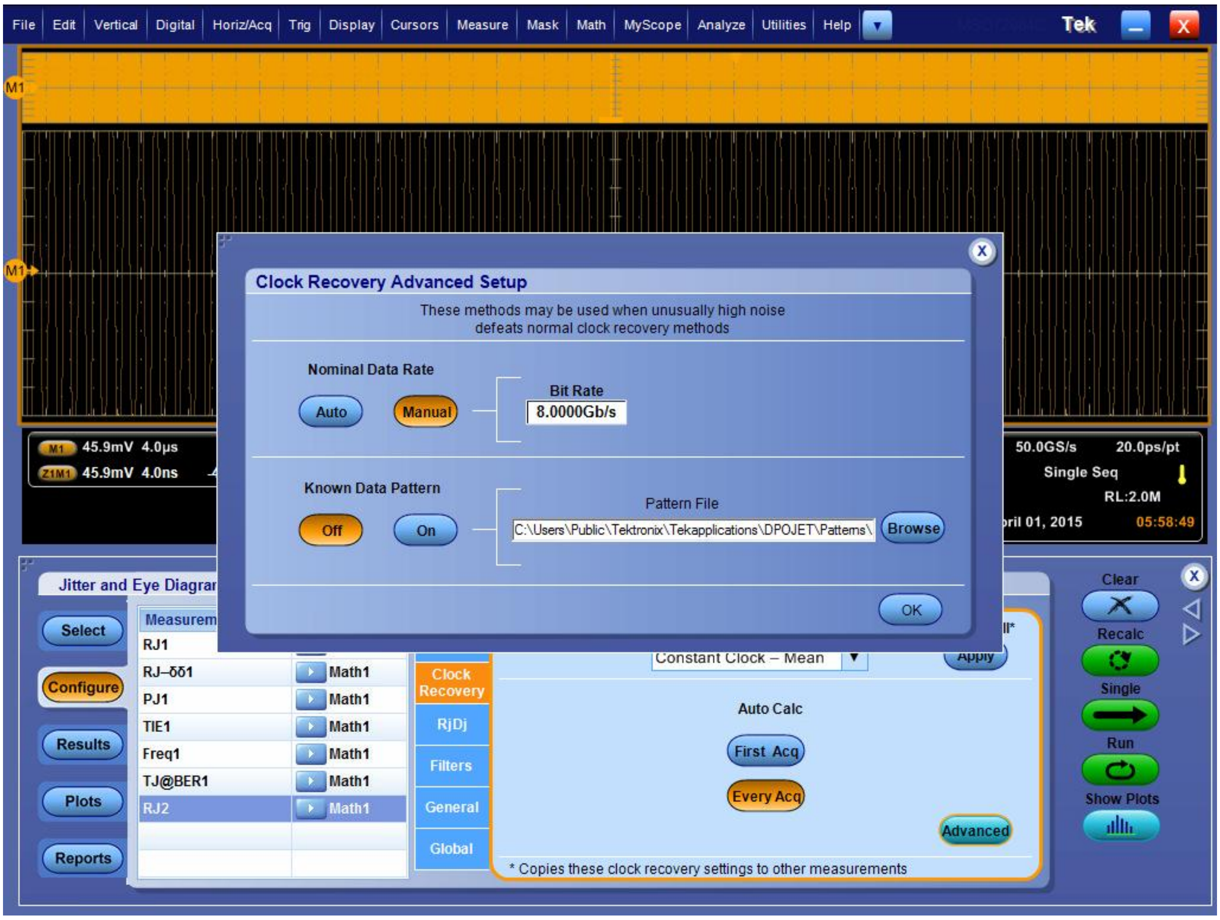


FIGURE 68. SCOPE ADVANCED SETUP

4. Set the Horizontal mode to Manual and set the record length to 2M.

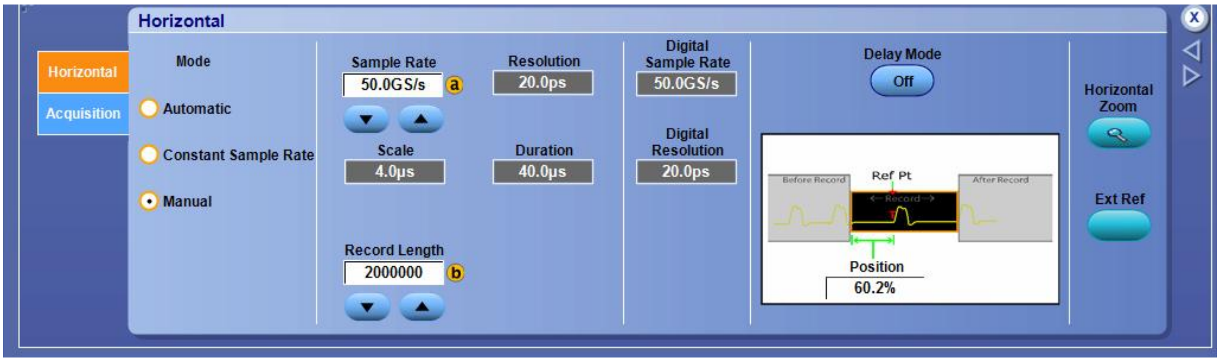


FIGURE 69. SCOPE RECORD LENGTH SETUP

5. Clear the result. Run Single.

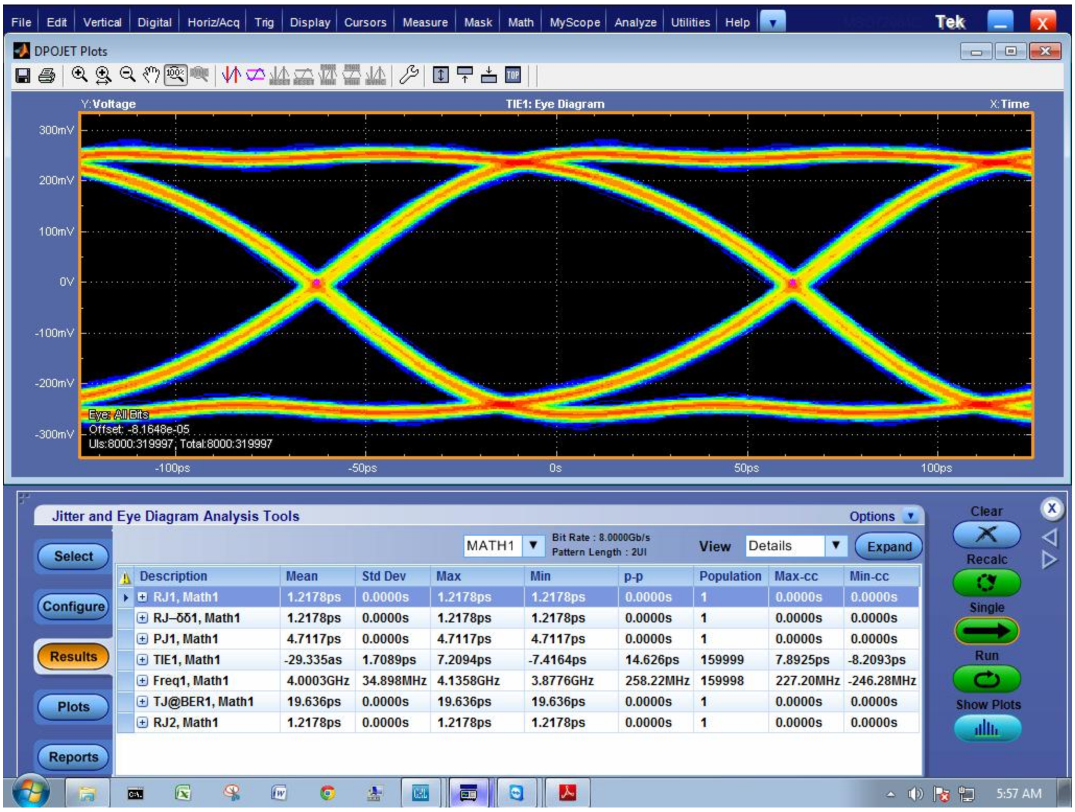


FIGURE 70. SCOPE WAVEFORM CAPTURE

6. Read the measured RJ1.
7. Tune the BERTScope RJ value.

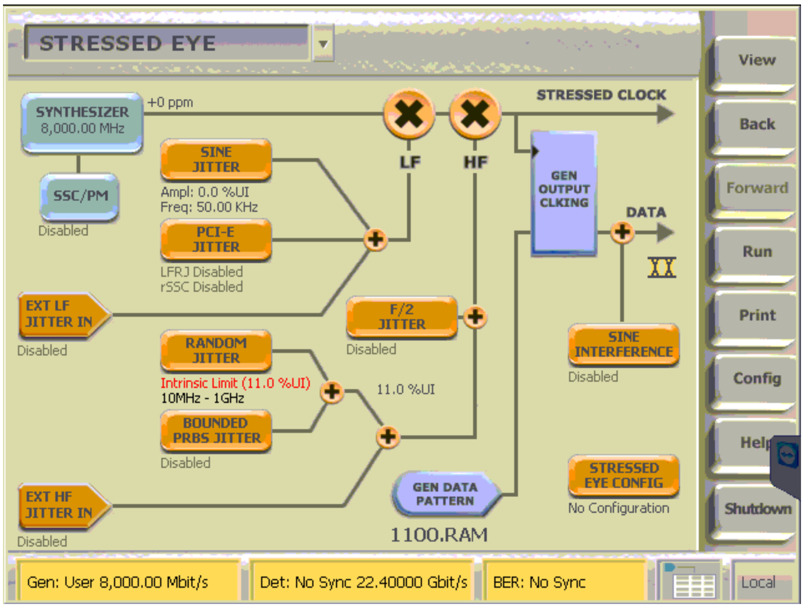


FIGURE 71. BERTSCOPE RJ CAPTURE

8. The target measured value for RJ: 2ps RMS and 3ps RMS.

10.1.5 SJ Calibration

There are four SJ (Sweep Jitter) frequencies required: 30KHz, 1MHz, 10MHz and 100MHz. SJ needs to be calibrated (with 1100 pattern) for all cases in the proper way.

TABLE 5. STRESSED JITTER TESTS

Frequency		
30KHz		
1MHz		
10MHz		
100MHz	0.1	UI PP

Stressed Voltage Test:

$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.

Stressed Jitter Test:

$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.

The Stressed Jitter test requires the test to pass each and every frequency, with its respective SJ amplitude at 30KHz, 1MHz, 10MHz and 100MHz.

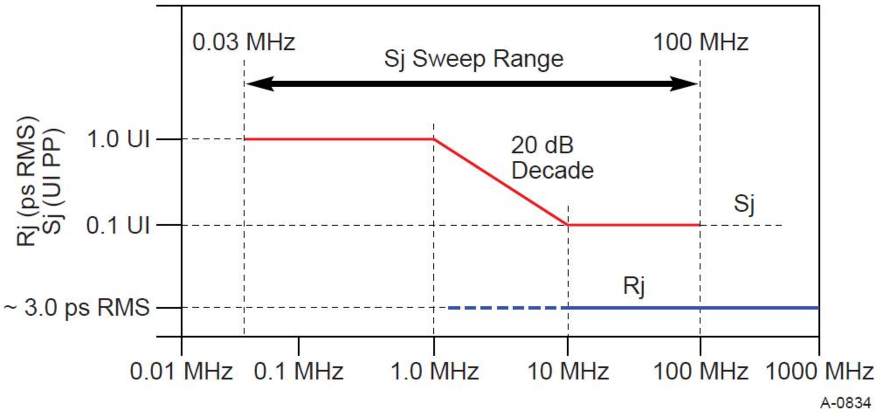


Figure 4-74: Swept Sj Mask

FIGURE 72. SWEEP JITTER RANGE AND MASK

Using this same setup at each frequency, make the measurement.

10.1.5.1 Calibrate Sweep Jitter at 30KHz.

1. On the BERTScope, enable ***Phase Modulator*** and set *PM Frequency* to 30KHz and *PM Devn* to *1UI*.

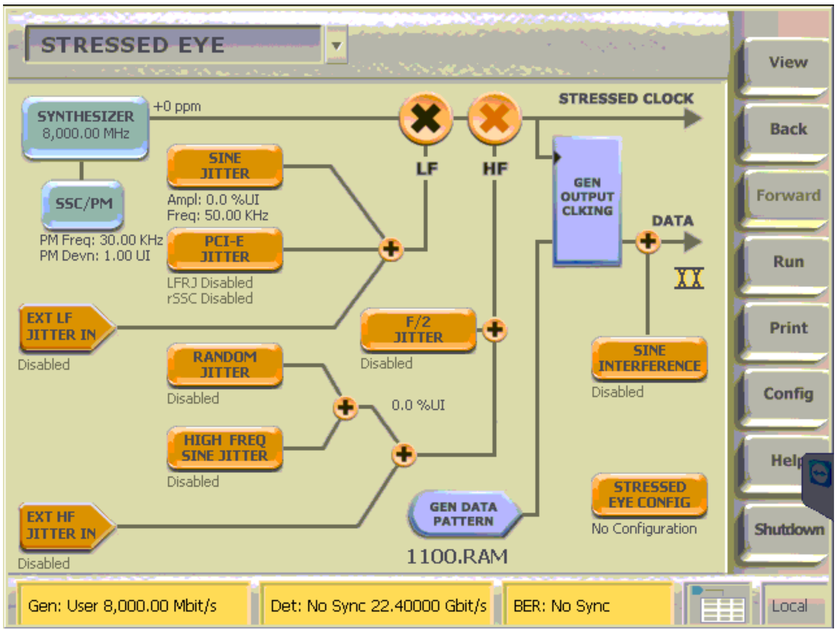


FIGURE 73. SWEEP JITTER BERTSCOPE SETUP AT 30KHZ

2. On the BERTScope, using DPOJET, measure PJ1. Note for this measurement the DPOJET Clock Recovery Method should be set to Constant Clock – Mean so as to not filter the low frequency jitter modulation that is to be verified.
3. Read the PJ1 measurement, which is in units of seconds. Convert to UI.

10.1.5.2 Calibrate Sweep Jitter at 1MHz, 10MHz, 100MHz

1. Set the Sine Jitter initially to 10% UI.

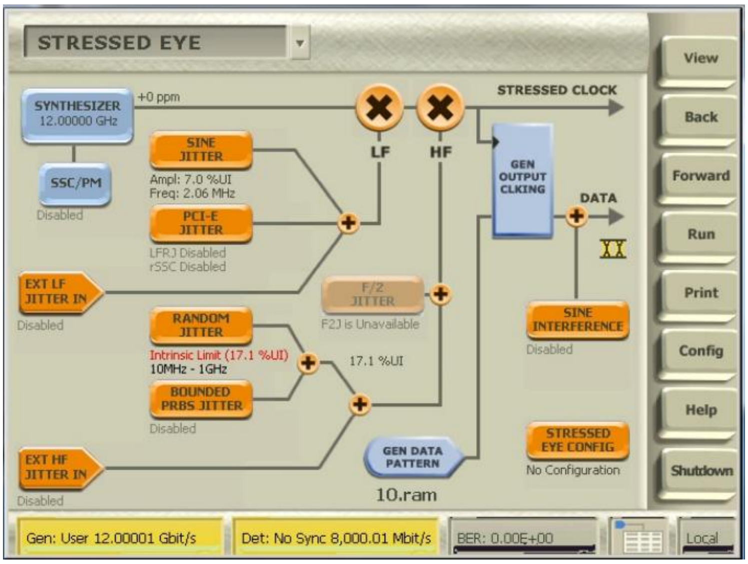


FIGURE 74. SWEEP JITTER BERTSCOPE SETUP AT 1MHZ-100MHZ

2. Measure SJ using DPOJET.

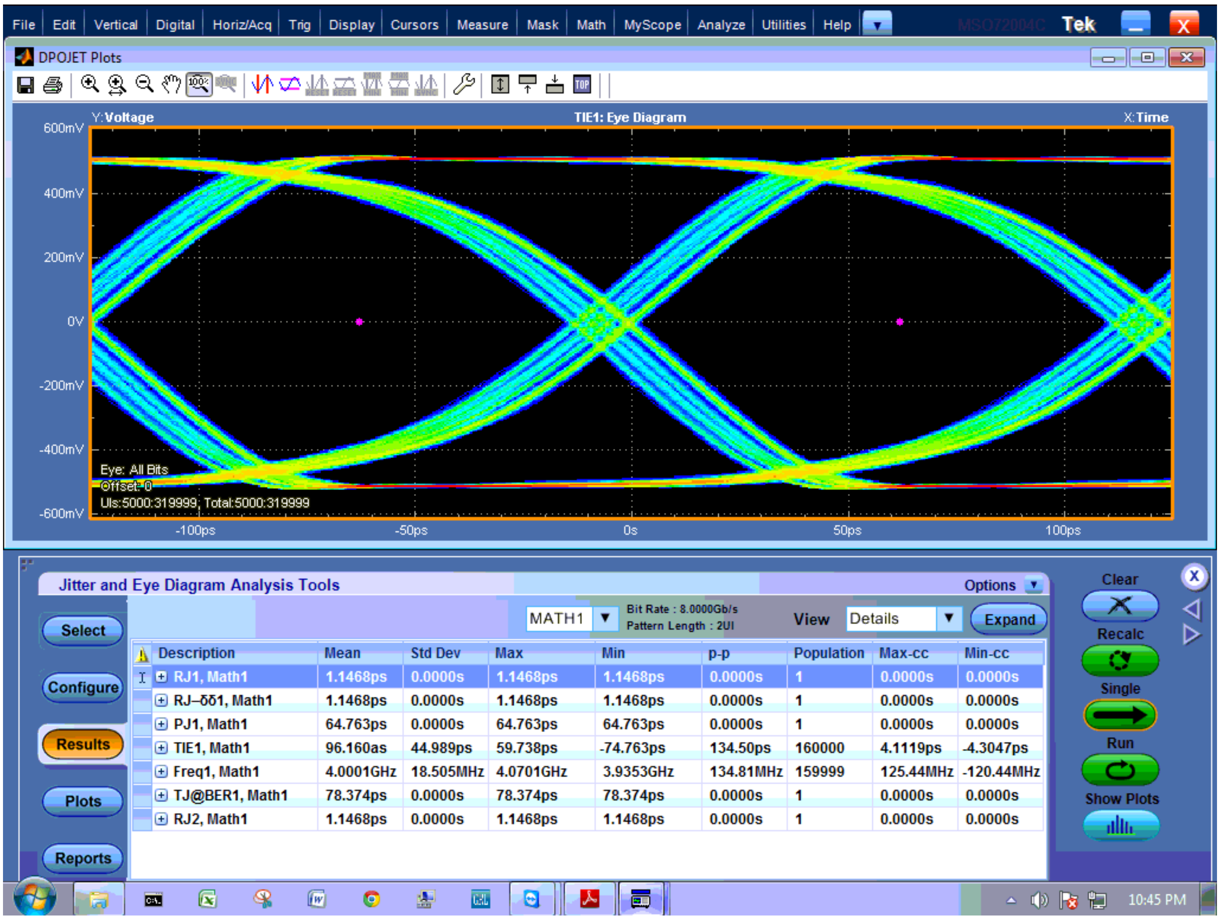


FIGURE 75. SWEEP JITTER DPOJET MEASUREMENT AT 1MHZ-100MHZ

3. Read the PJ1 value.
4. Again, note the value of SJ on the BERTScope needed to generate 10% SJ at reference point.
5. Calibration for 1MHz, 10MHz and 100MHz are needed to set the SJ Frequency and SJ Amplitude instead of PM.

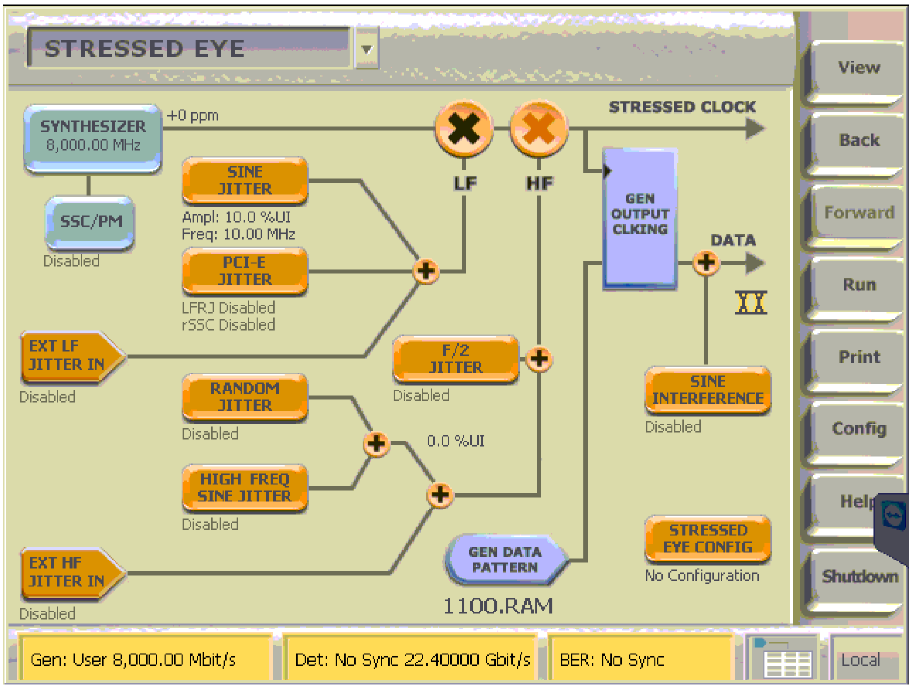


FIGURE 76. CALIBRATION AT 1MHZ-100MHZ

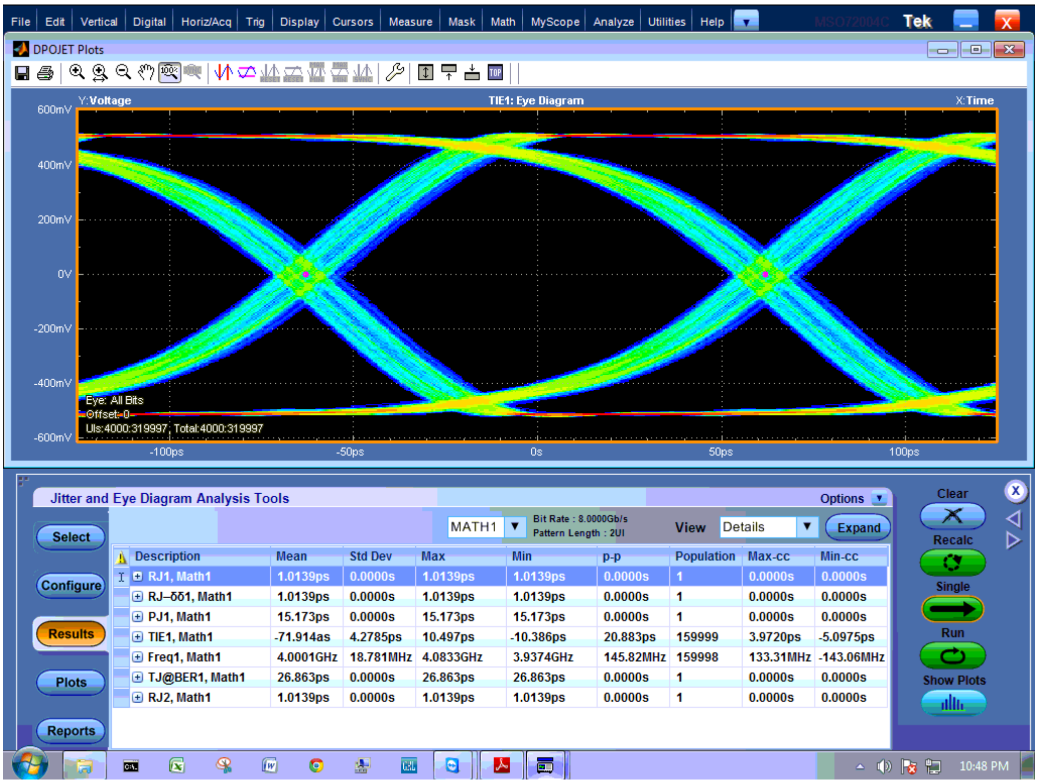


FIGURE 77. SWEEP JITTER DPOJET MEASUREMENT AT 1MHZ-100MHZ

10.2 Channel Calibration Tests (TP2)

10.2.1 Channel Calibration Insertion Loss

PCIe Gen3 defines three types of calibration channel.

- **a)** None
- **b)** Short
- **c)** Long

Defined by Figure 78, each channel insertion loss must meet the mask depending on its channel type. Variable and programmable ISI injector is needed to simulate the trace length to achieve the target loss for each channel.

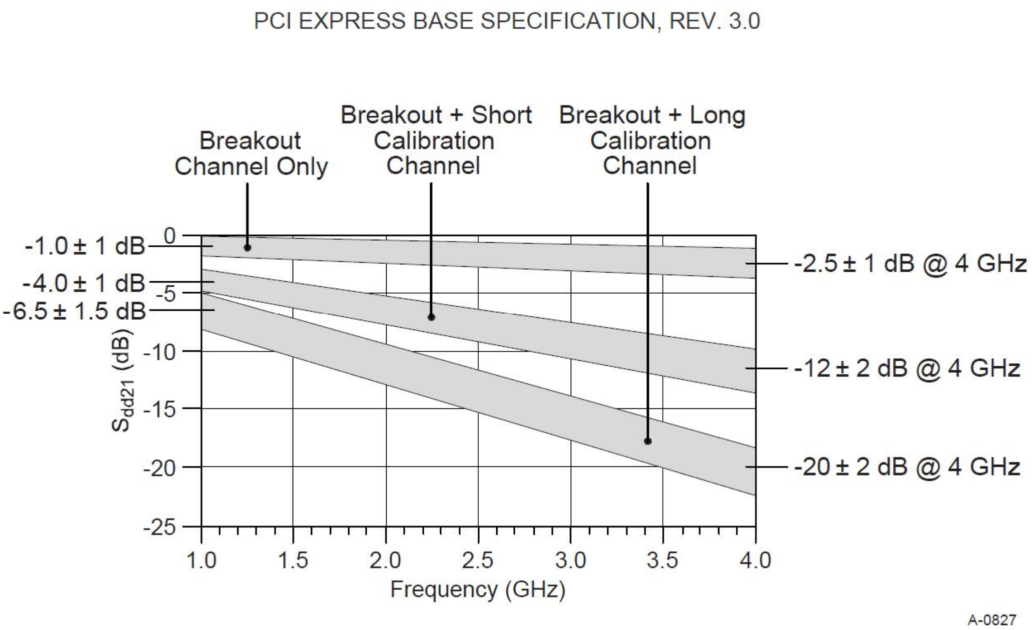


FIGURE 78. CHANNEL INSERTION LOSS MASK BY CHANNEL TYPE

Insertion loss is measured by differentiating step response, and performing the FFT of the resulting impulse response. The Seasim application provides the method to calculate the insertion loss given the step response.

10.2.1.1 BERTScope Setup

1. Set the BERTScope Set Pattern to clk/256.
2. Set the DPP Set De-emphasis and Pre-shoot to P4 with post cursor and pre cursor for equalization of amplitude recorded earlier.
3. Set the DPP output that reflects the 800mV amplitude that was recorded earlier.
4. Disable Rj.
5. Disable Sj.

10.2.1.2 ISI Setup

1. Open the Artek ISI application.
2. Set the ISI % to 0.0.

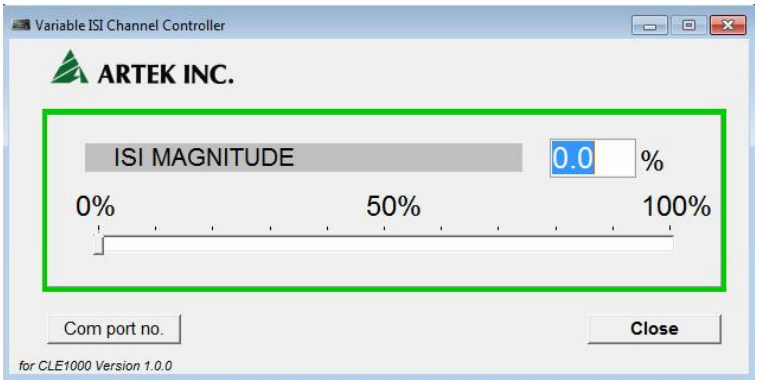


FIGURE 79. ISI SETUP

10.2.1.3 Scope Setup

1. Turn On Ch1 and Ch2, scale ch1 and ch2 correctly.
2. Turn Off ch1 and ch2.
3. Turn ON Math1, set ch1-ch2. Scale correctly.
4. Set up Trigger A Event to Edge, source to chan1.
5. Set up Trigger A-B Event with Acquisition Delay to 4ns.

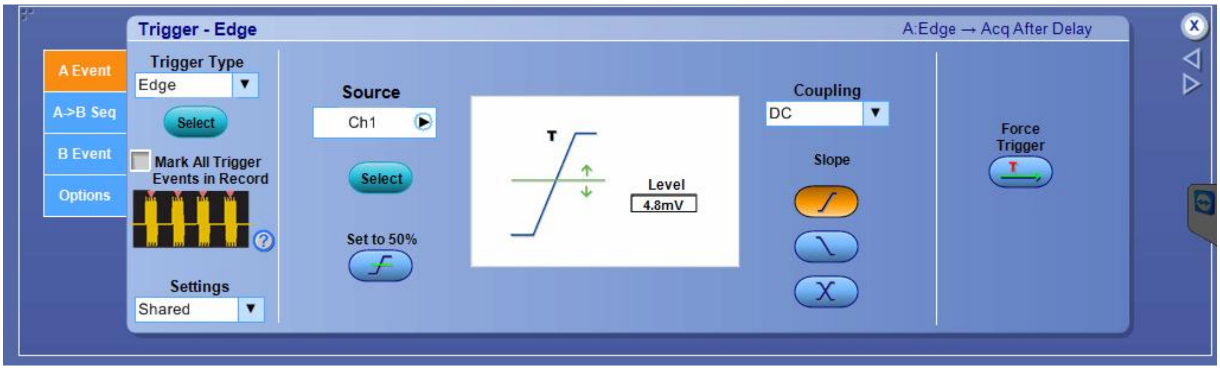


FIGURE 80. SCOPE SETUP #1

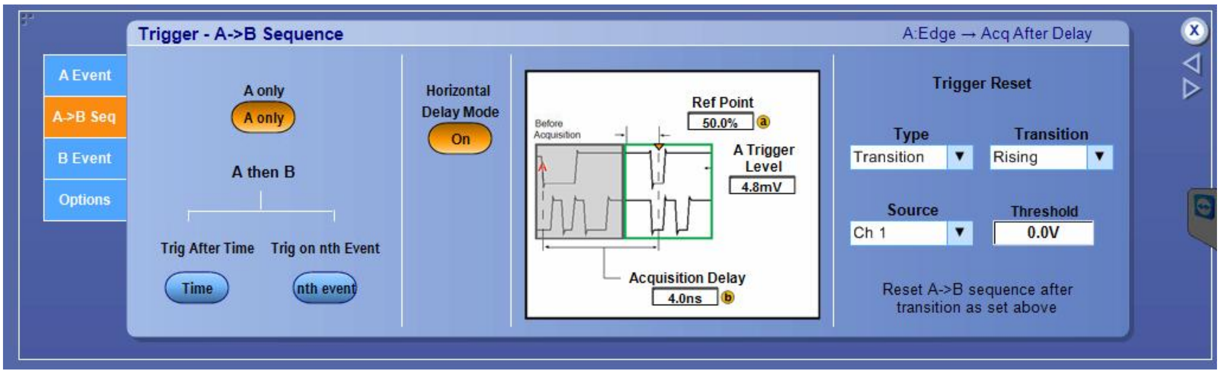


FIGURE 81. SCOPE SETUP #2

6. Set up Acquisition Mode to Average of 2048 Waveforms.

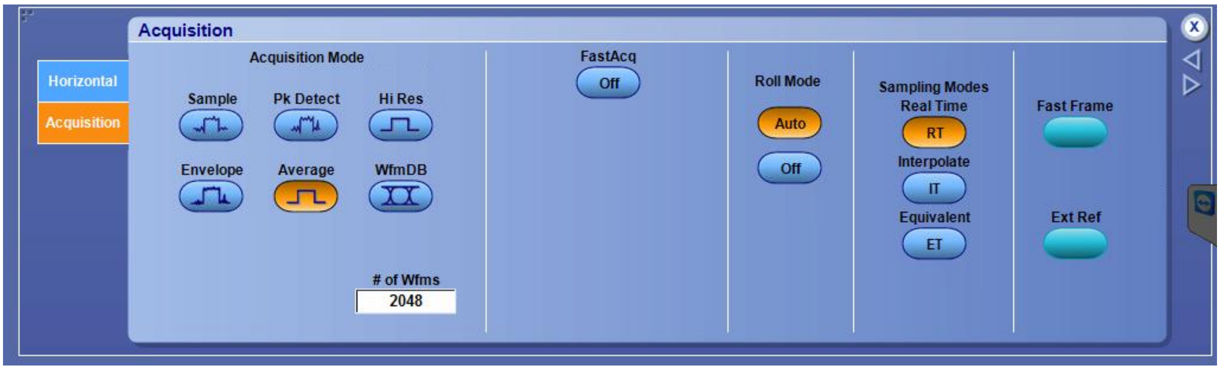


FIGURE 82. SCOPE ACQUISITION MODE SETUP

7. Run Single and capture measurement.

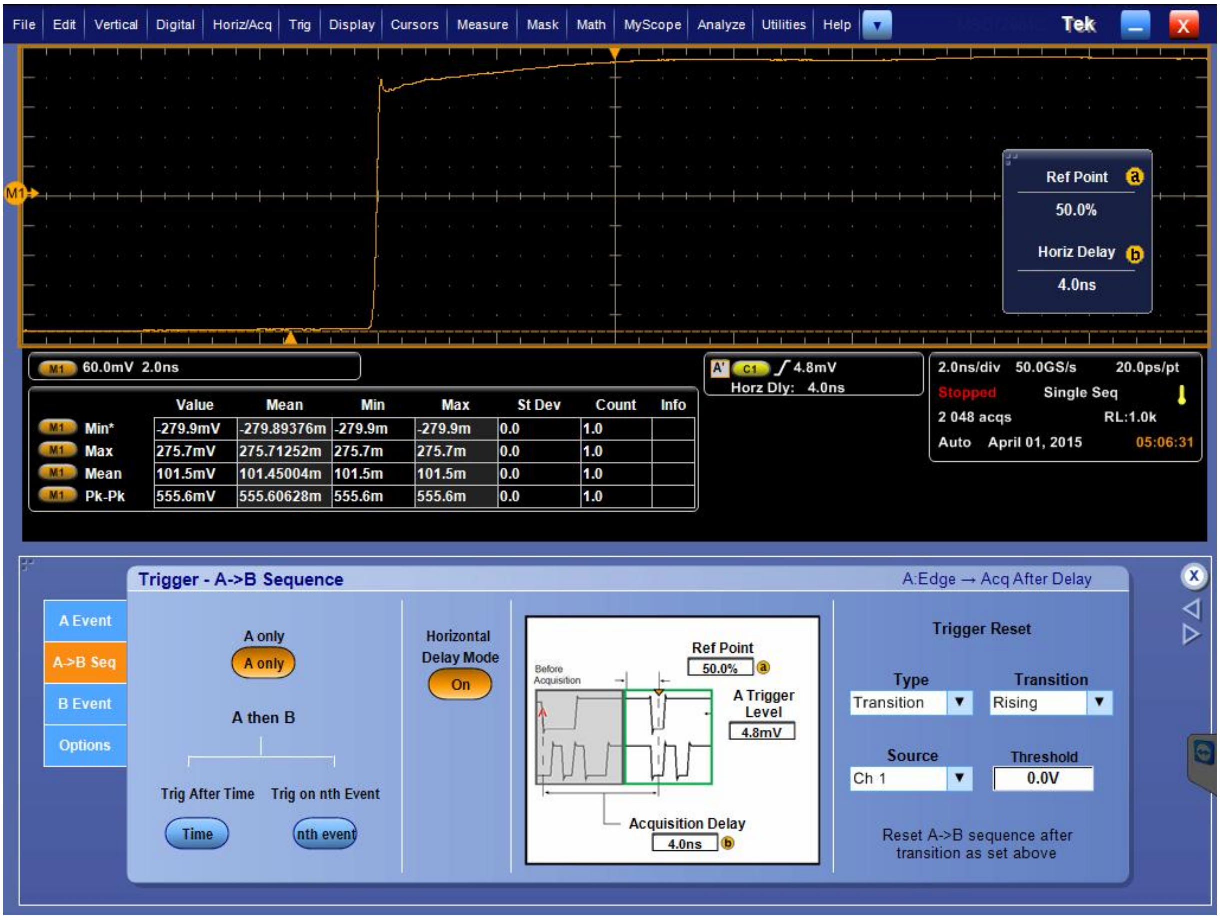


FIGURE 83. CAPTURE MEASUREMENT

8. Save the waveform to .DAT format.
9. Modify the .DAT format to the Seasim-compatible waveform with a name ending with _vict.rfstep1.
10. The _vict.rfstep1 format consists of **time**[SPACE]**Voltage_level**[New Line].
11. Copy the _vict.rfstep1 step response to the \step_response folder.

12. Launch Seasim_GUI.pyw.

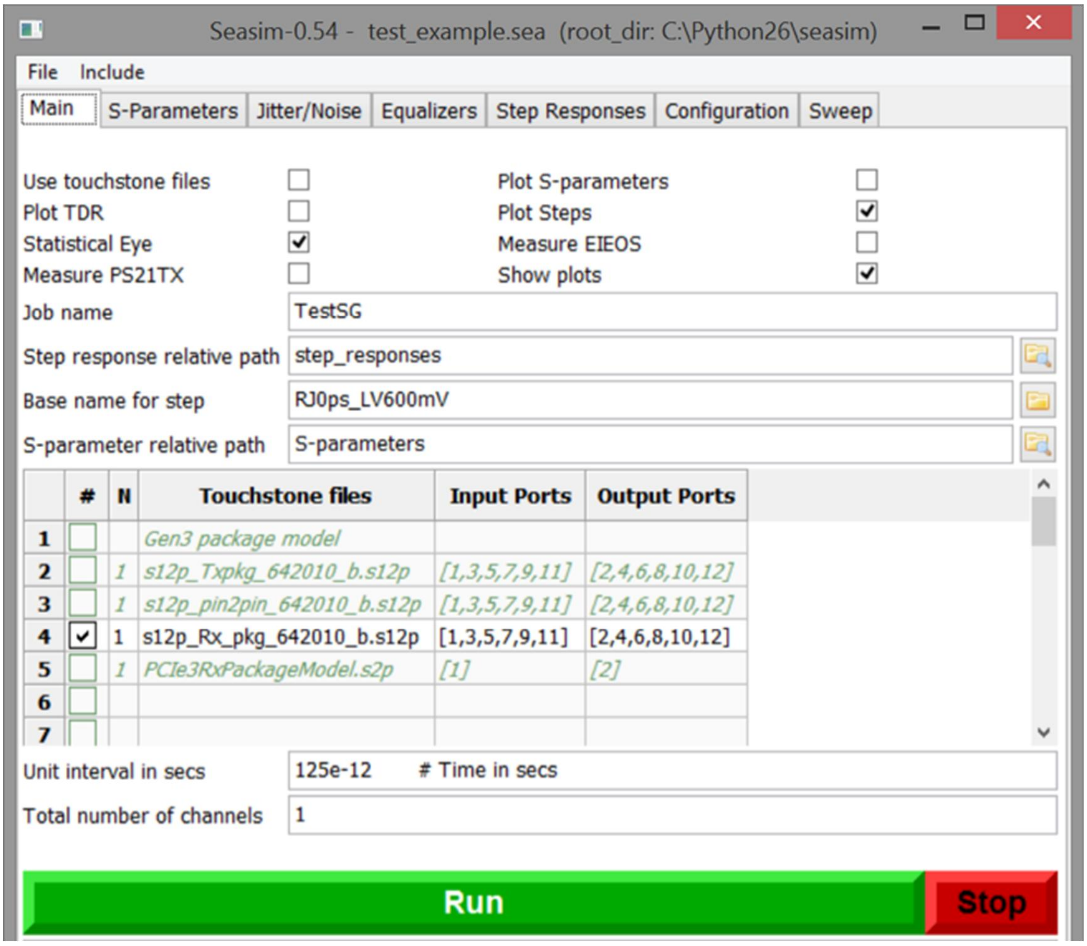


FIGURE 84. SAVE THE WAVEFORM

13. Change the file name for the 'Base name for step' to the file name saved and modified.
14. Click Run.

15. Seasim will output a graph indicating the insertion loss.

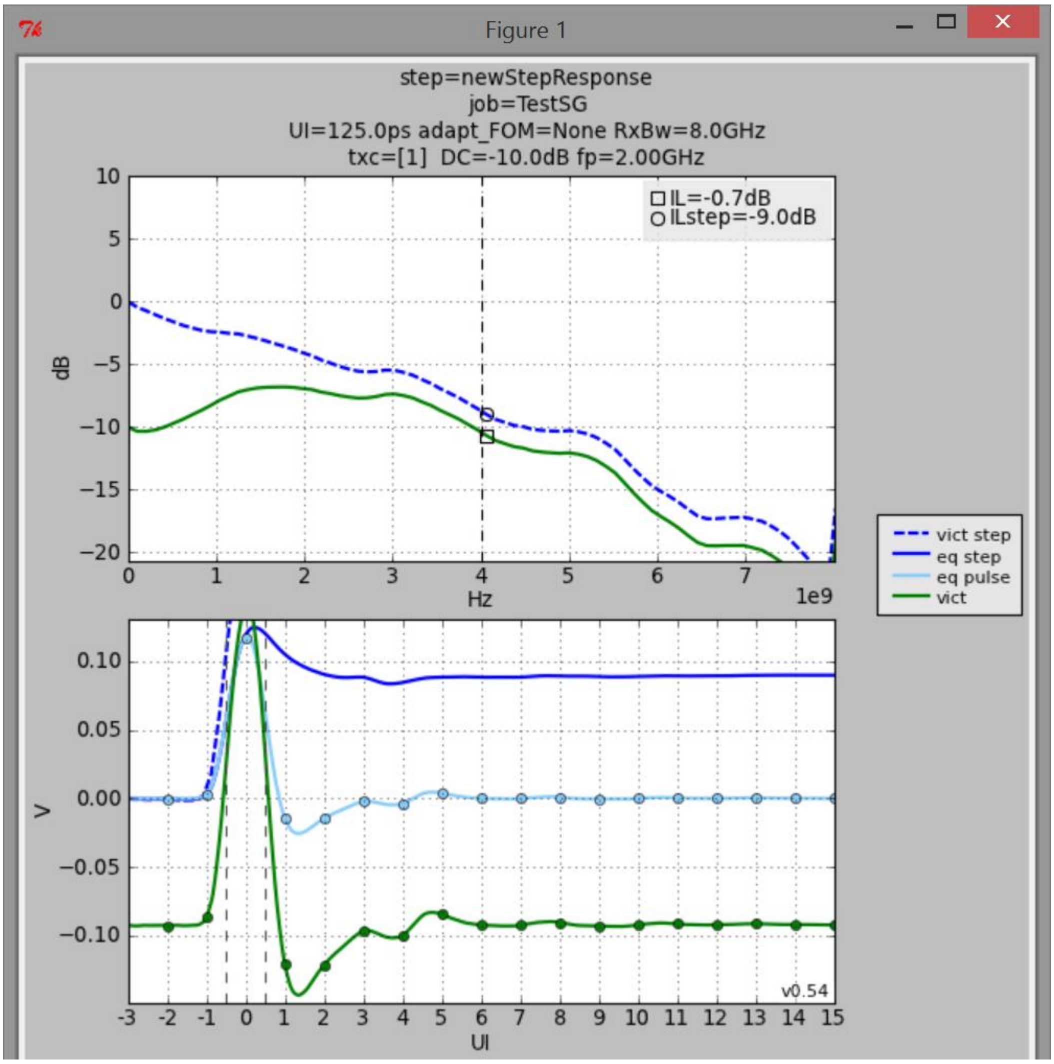


FIGURE 85. SEASIM INSERTION LOSS OUTPUT GRAPH

16. Insertion loss at 4GHz is -9dB for the sample above.
17. Increase the ISI % and then re-capture the waveform, save, modify and run Seasim.
18. Ensure the insertion loss is within the PCIe Gen3 specs range for the respective channel type.

10.2.1.4 Example Results

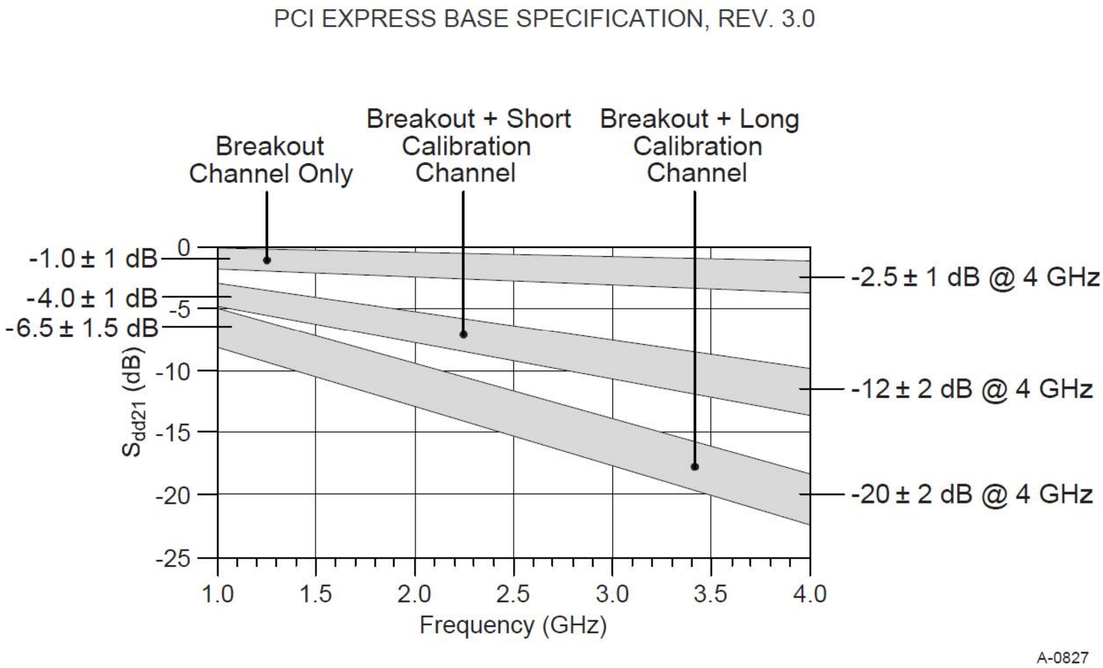


FIGURE 86. SPECIFICATION MASK

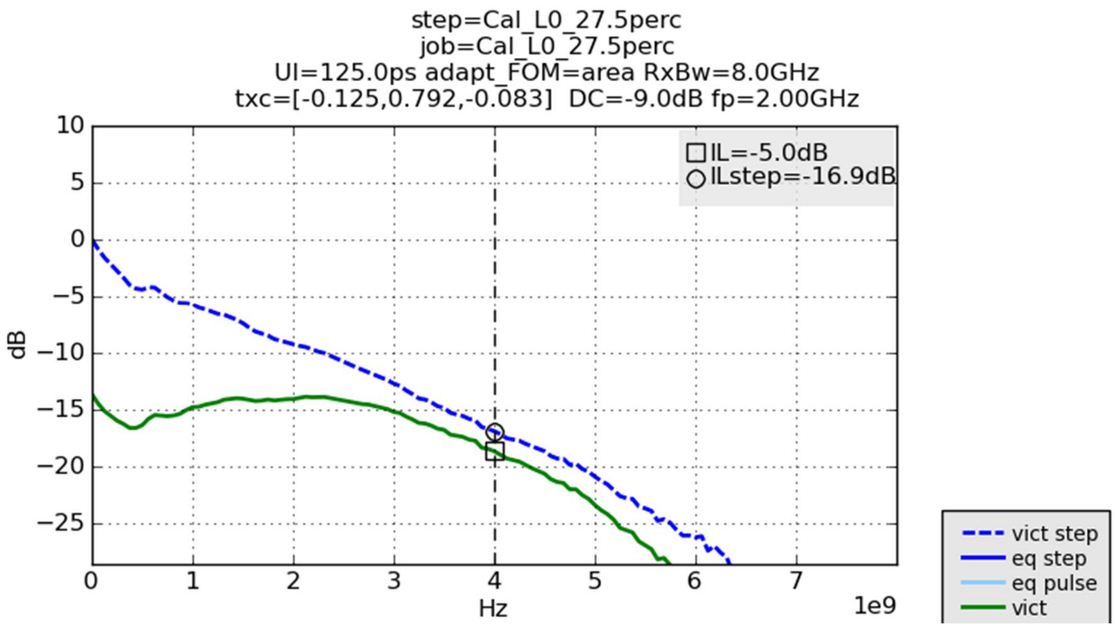


FIGURE 87. INSERTION LOSS AT 27.5% ISI (-16.9DB)

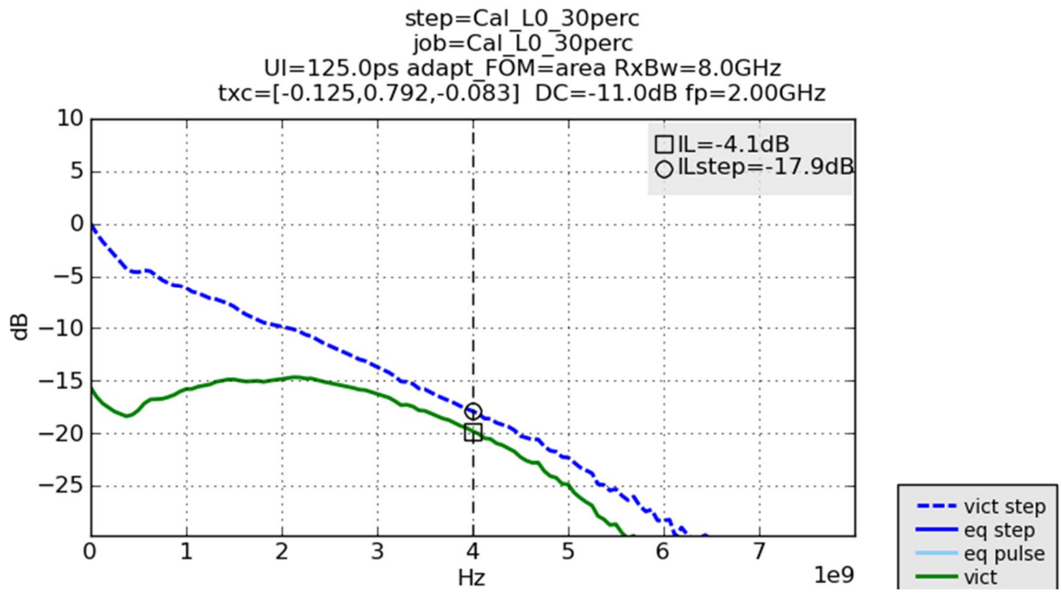


FIGURE 88. INSERTION LOSS AT 30% ISI (-17.9DB)

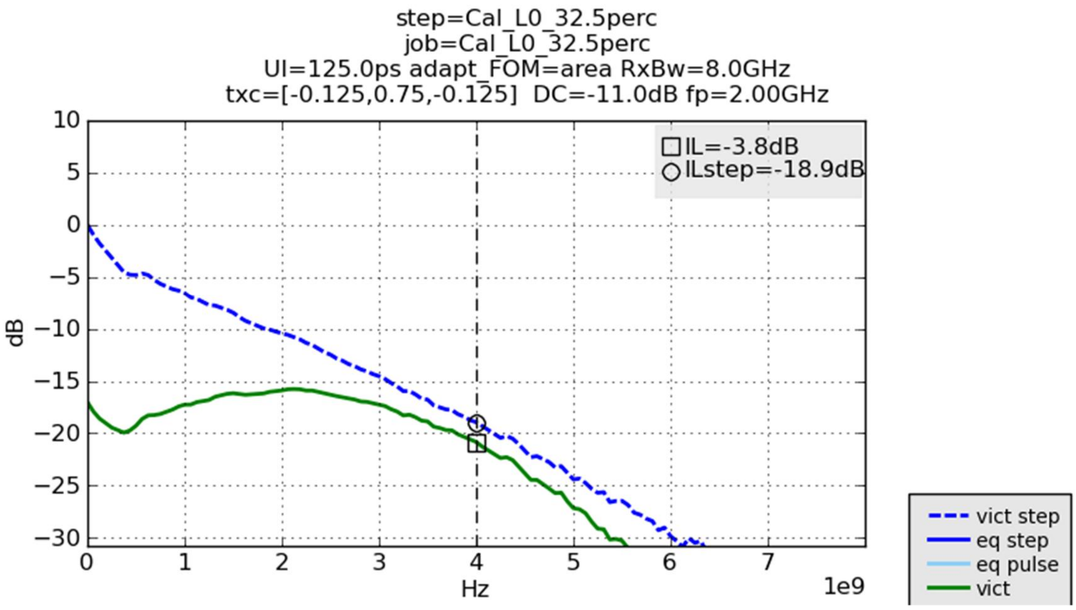


FIGURE 89. INSERTION LOSS AT 32.5% ISI (-18.9DB) WITHIN TARGET

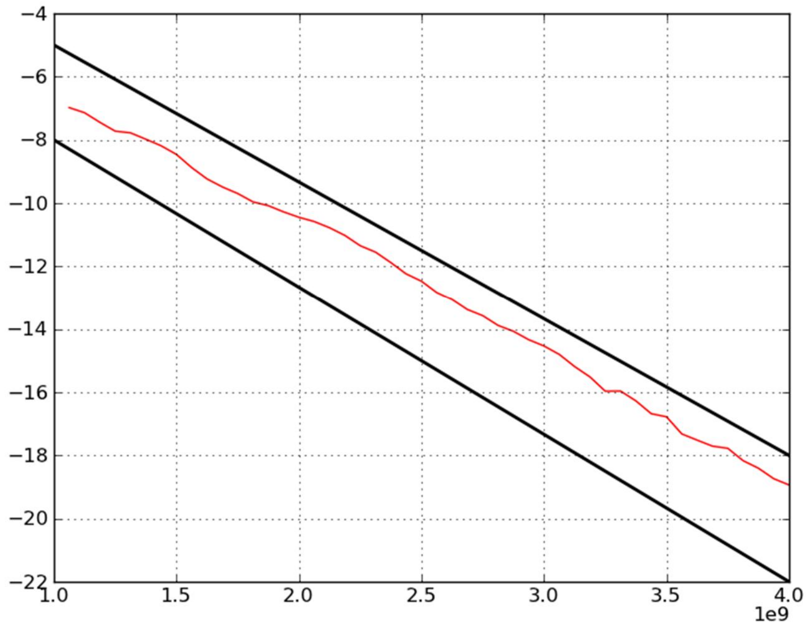


FIGURE 90. INSERTION LOSS CALIBRATION FOR LONG CHANNEL – IL FALLS BETWEEN REQUIRED MASK

10.2.2 Channel Calibration Differential Mode Sinusoidal Interference

10.2.2.1 BERTScope Setup

1. Set ALL ZERO Pattern.

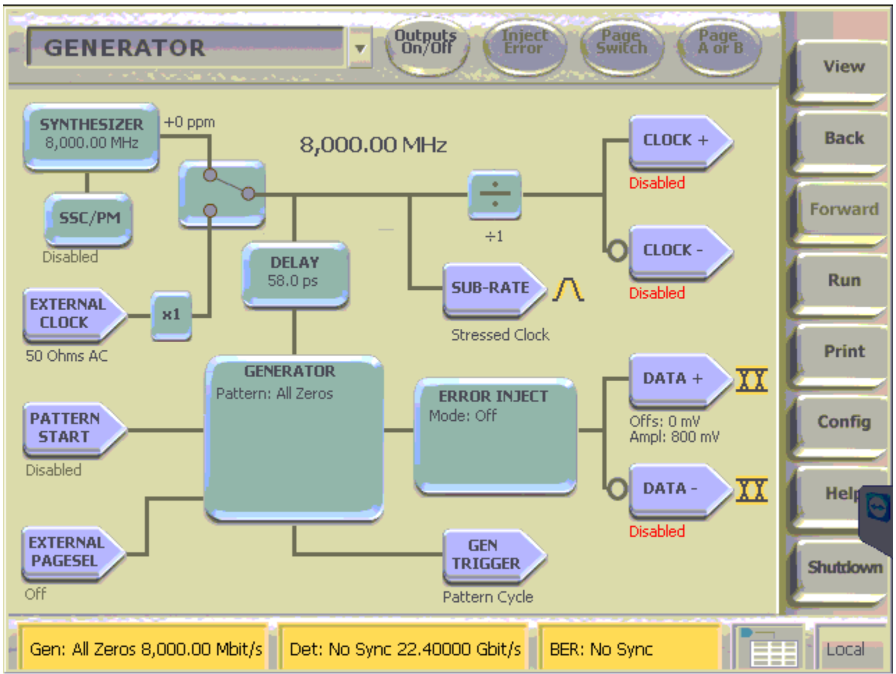


FIGURE 91. BERTSCOPE SETUP FOR ALL ZERO PATTERN

2. Set all Jitter to 0mV amplitude.
3. Enable the SINE INTERFERENCE.
4. Set the Frequency to 2.1GHz.
5. Set to External.

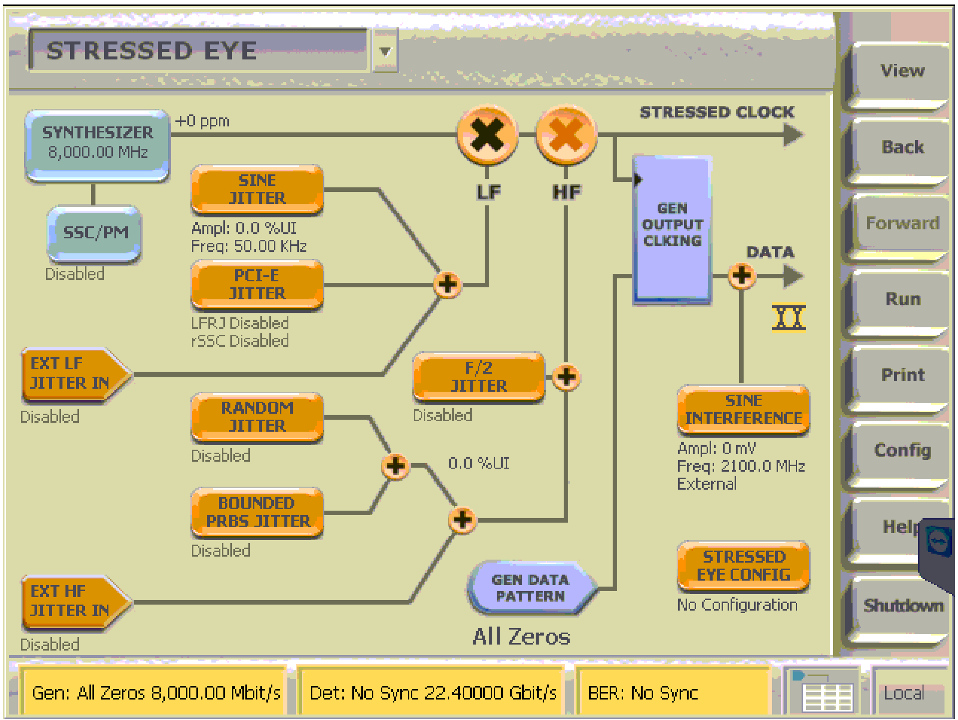


FIGURE 92. BERTSCOPE SETUP #2

6. Set the Sine Interference Amplitude to 100mV.

10.2.2.2 ISI Setup

1. Set the Artek ISI % to calibrated channel type.

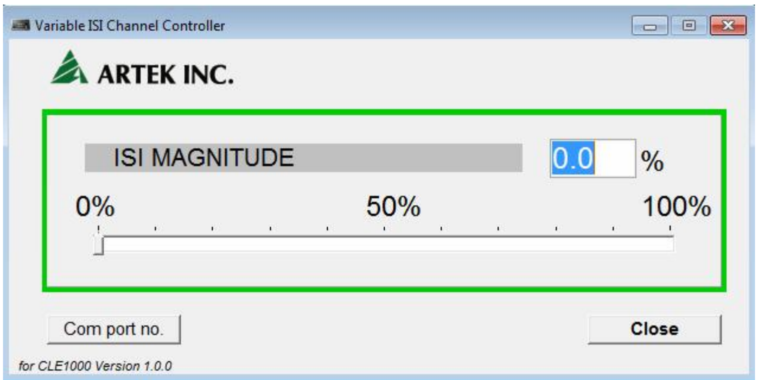


FIGURE 93 ARTEK ISI SETUP

10.2.2.3 Scope Setup

1. Set the Acquisition Average to 256.
2. Scale the Ch1 and Ch2 accordingly.
3. Turn on MATH1, ch1-ch2, and scale accordingly.
4. Measure Peak to Peak of Math1.
5. Run Single.
6. Obtain the MEAN value of Math1 Peak to Peak.
7. Tune the Sine Interference Amplitude so that the measured value is 16mV.

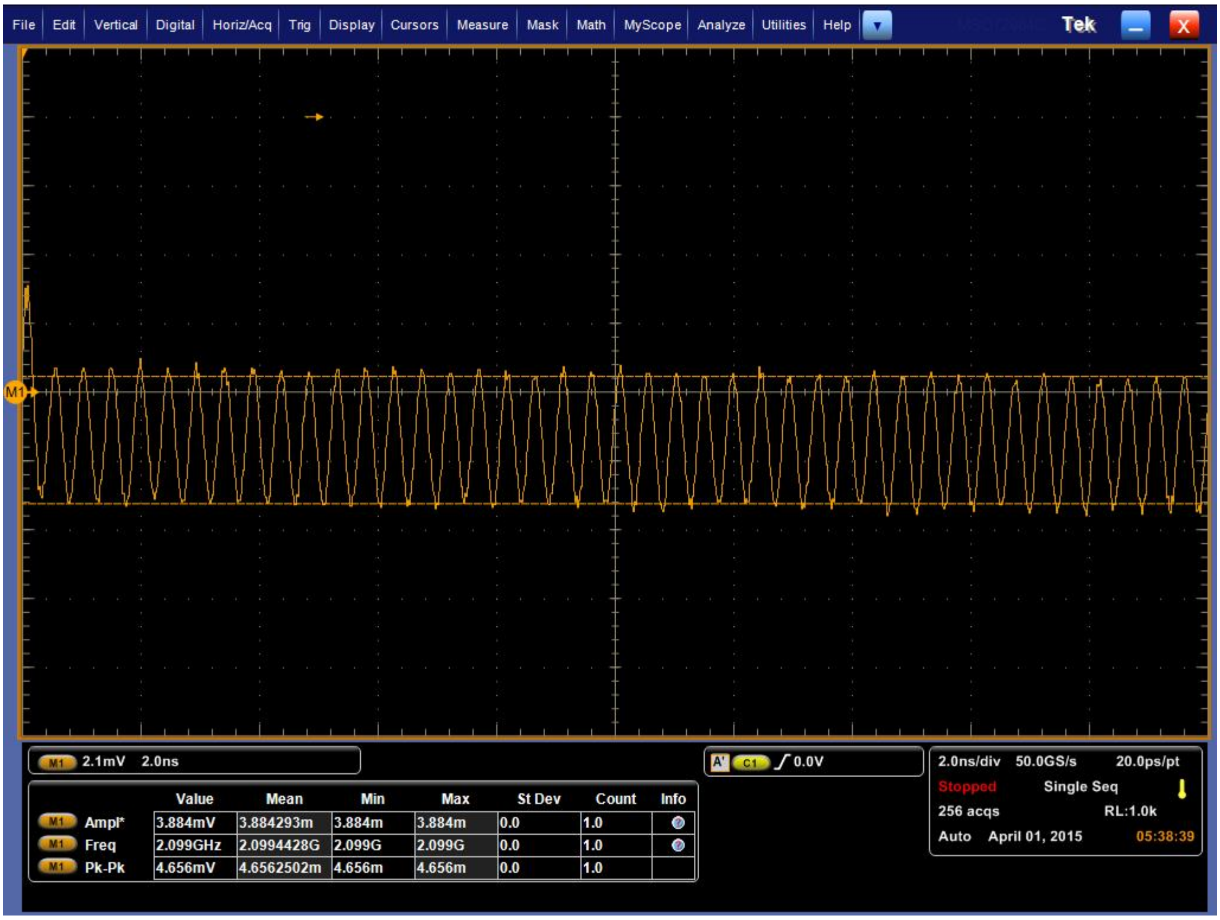


FIGURE 94. SCOPE MEASUREMENT

10.2.3 Channel Calibration AC Common Mode Sinusoidal Interference

10.2.3.1 BERTScope Setup

1. Remain ALL ZERO Pattern.
2. Set the SINE Interference amplitude to 0mV.

10.2.3.2 Setup AFG

1. Enable the AFG output 1.
2. Set the Output Mode to SINE wave.
3. Set the SINE Wave frequency to 120MHz.
4. Set the Output1 Amplitude to 1V.

10.2.3.3 Scope Setup

1. Scale Ch1 and Ch2.
2. Set MATH1 to ch1+ch2.Scale MATH1.
3. Turn OFF Ch1 and CH2.
4. Set the Acquisition to Average 256.

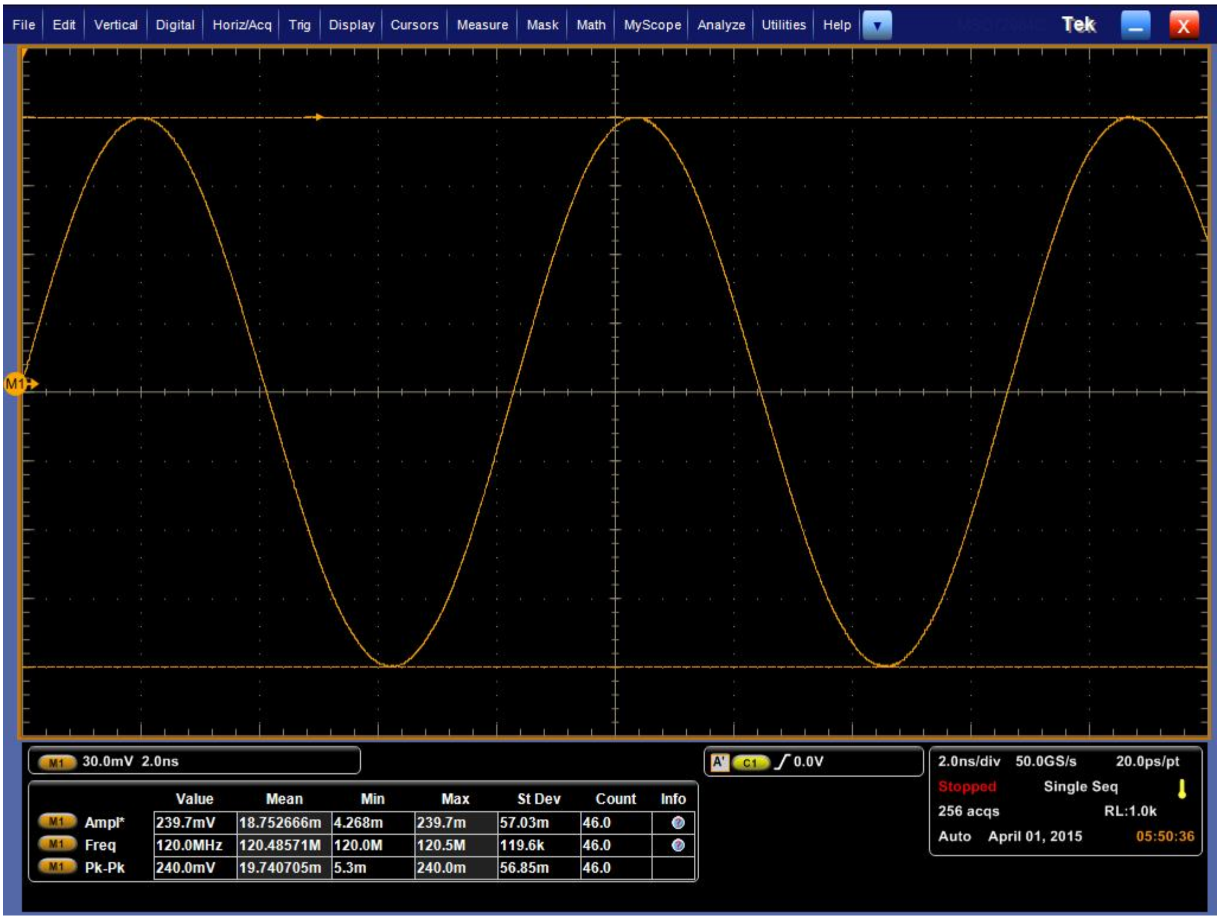


FIGURE 95. SCOPE MEASUREMENT

5. Tune the AFG Amplitude.
6. Target CM:

   150mV for Long Channel

   250mV for Short and None Channel

10.3 Calibration at TP2P

Two distinct tests are utilized to test a receiver: one for its minimum eye height (voltage), and another for its minimum eye width (jitter). The procedures for calibrating the stressed eye are similar, although the number and magnitude of signal impairment sources vary between the two tests.

10.3.1 TP2P Stressed Voltage Calibration

The configuration for calibrating a stressed voltage eye for Rx testing is shown below where the calibration procedure is performed for all three calibration/breakout channel combinations. Rj and Sj are added as defined below and common mode and differential mode noise sources are added simultaneously.

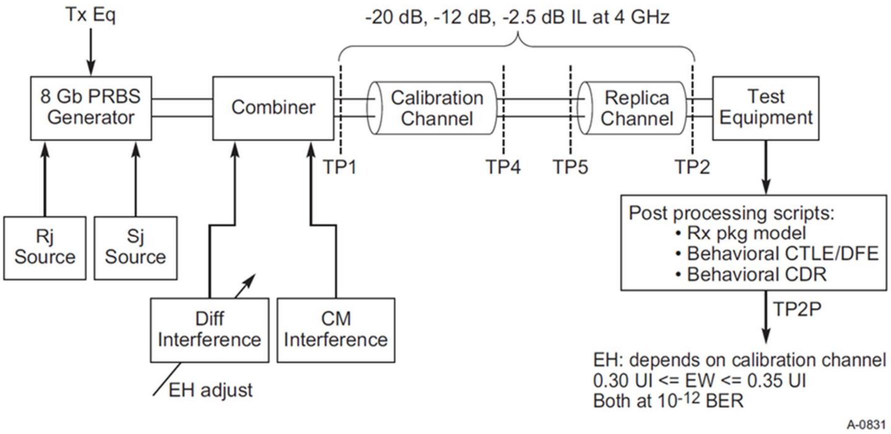


Figure 4-71: Setup for Calibrating the Stressed Voltage Eye

FIGURE 96. SETUP FOR CALCULATING THE STRESSED VOLTAGE EYE

Table 4-22: Stressed Voltage Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800	mVPP	Measured at TP1 Figure 4-65. $V_{RX-LAUNCH-8G}$ may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mVPP.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mVPP	Eye height @ BER=10^{-12}. Notes 1,2.
$T_{RX-SV-8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER=10^{-12}. Note 2
$V_{RX-SV-DIFF-8G}$	Differential mode interference	14 or greater	mVPP	Adjusted to set EH. Frequency = 2.10 GHz. Note 3.
$V_{RX-SV-CM-8G}$	Rx AC Common mode voltage at TP2P	150 (EH < 100 mVPP) 250 (EH ≥ 100 mVPP)	mVPP	Defined for a single tone at 120 MHz. Note 3.
$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Note 4.
$T_{RX-SV--RJ-8G}$	Random Jitter	2.0	ps RMS	Rj spectrally flat before filtering. Notes 4,5.
$V_{RX-MAX-SE-SW}$	Max single-ended swing	±300	mVP	Note 6.

FIGURE 97. STRESSED VOLTAGE EYE PARAMETERS

Eye width and eye height are defined after applying post processing and are defined at TP2P. The long calibration channel utilizes both CTLE and DFE, while the medium and short channels calibration channels use CTLE only.

EH is set by adjusting the amount of differential noise until the value defined by VRX-SV-8G is obtained. If it is not possible to maintain a sufficient eye width by adjusting only the differential noise, it is acceptable to inject less differential noise and adjust the generator launch voltage.

Seasim is used to post process the receiver eye at TP2P.

In this context, Rj, Sj, and DM-SI sources are input to Seasim, while CM-SI is combined with clk/256 pattern source from BERT and captured in Scope.

10.3.1.1 BERTScope Setup

1. Set the BERTScope Pattern to clk/256.
2. Turn Off Rj, Sj, DM-SI on the BERTScope.
3. Set the DPP Output to 800mV Amplitude calibrated earlier.
4. Set the DPP De-emphasis and Pre-shoot. Use “Preset 4” for the Short and None channels. Use “Preset 7” for the Long channel.

10.3.1.2 AFG Setup

1. Turn Off the AFG.

10.3.1.3 Scope Setup

1. Set up Trigger A Event to Edge, and source to chan1.
2. Set up Trigger A-B Event with Acquisition Delay to 4ns.

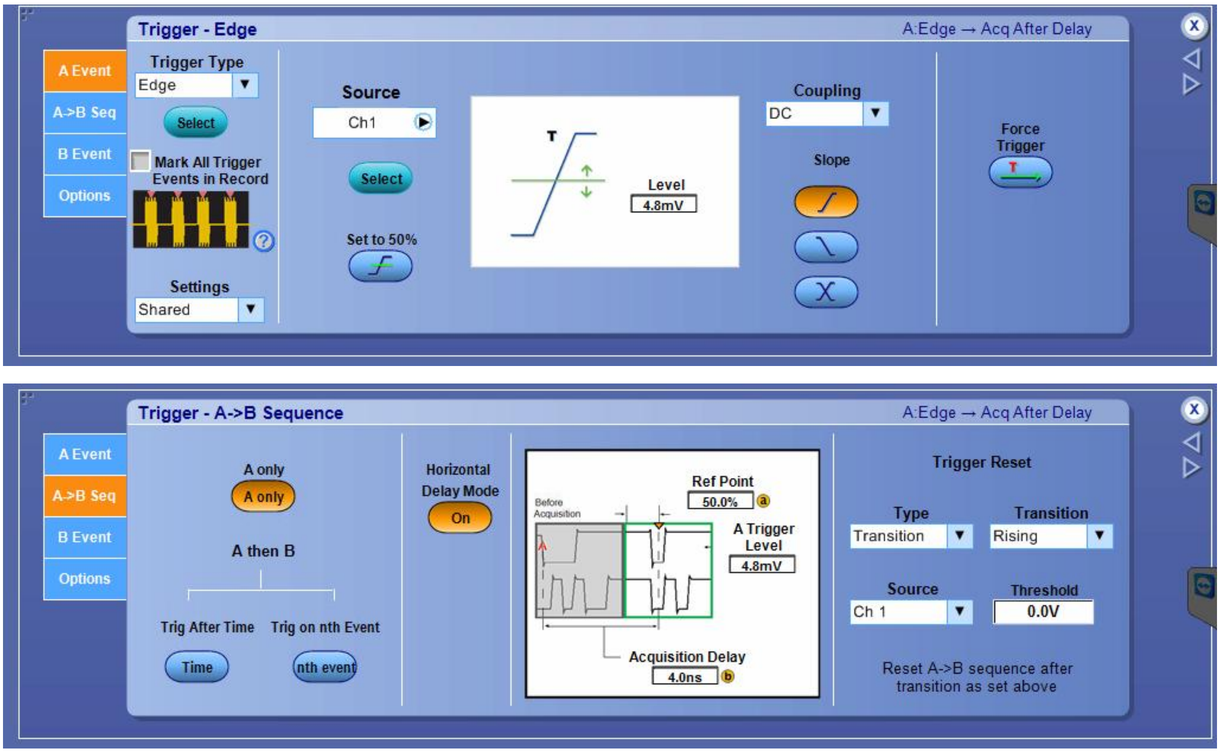


FIGURE 98. SCOPE SETUP

1. Scale Ch1 and Ch2, Math1 (ch1-ch2).
2. Set Acquisition to Average to 2048.
3. Acquire the waveform.
4. Save the waveform.

FIGURE 99. ACQUIRED WAVEFORM

5. Modify the waveform to a Seasim-compatible format.

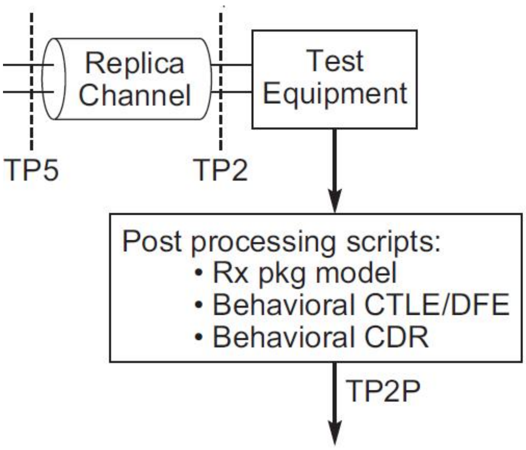


FIGURE 100. APPLY SEASIM

6. Apply the Rx Behavioral Package:
    a) Rx Behavioral Package (in S2P/S4P) file.
    b) CTLE / DFE and CDR can be simulated in Seasim.
    c) Rx Package model is convoluted externally with Step response before input to Seasim.
    d) Step response is converted to Frequency domain, then multiply the magnitude with s2p S21 magnitude and phase corresponding to its frequency range.
    e) It can be realized using python script.
    f) A comparison of original frequency response (red), and the after application of s2p (purple), showing the s2p Rx package s21 graph as a green line.

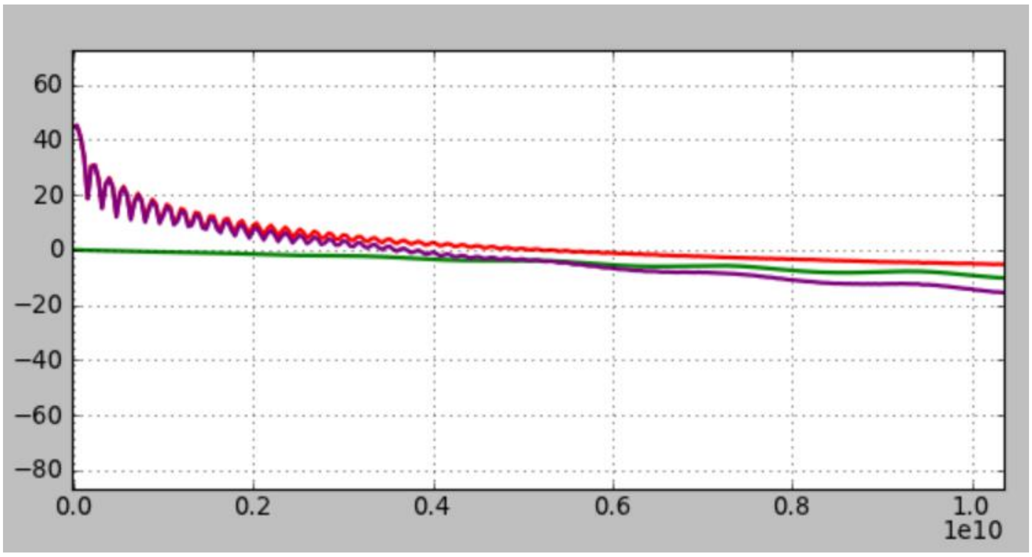


FIGURE 101. GRAPHICAL COMPARISON OF ORIGINAL AND AFTER-APPLICATION RESPONSE

    g) Step response before (red) and after (purple).

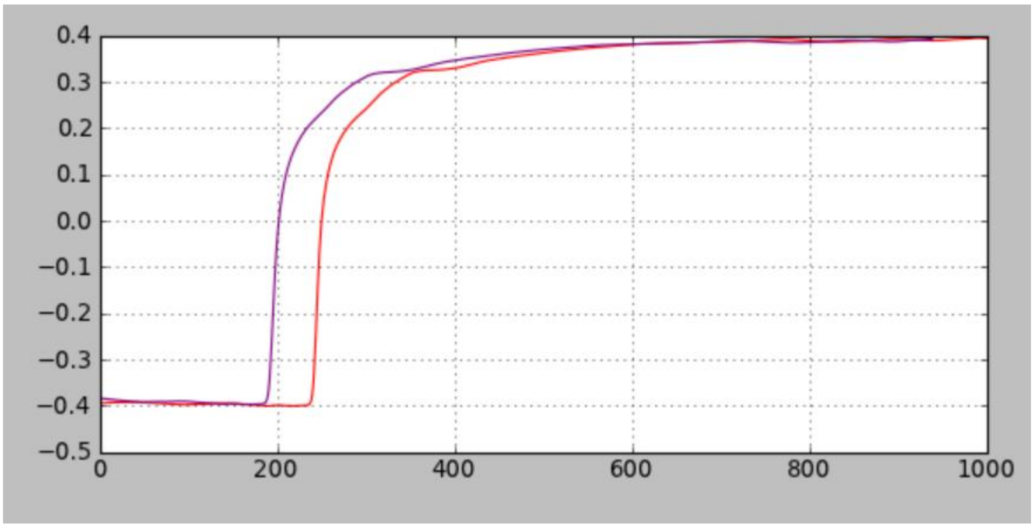


FIGURE 102. GRAPHICAL STEP RESPONSE COMPARISON

7. Run Seasim:
    a) Set the ‘Base name for step’ to the filename saved.

b) Check the options as in the picture below.

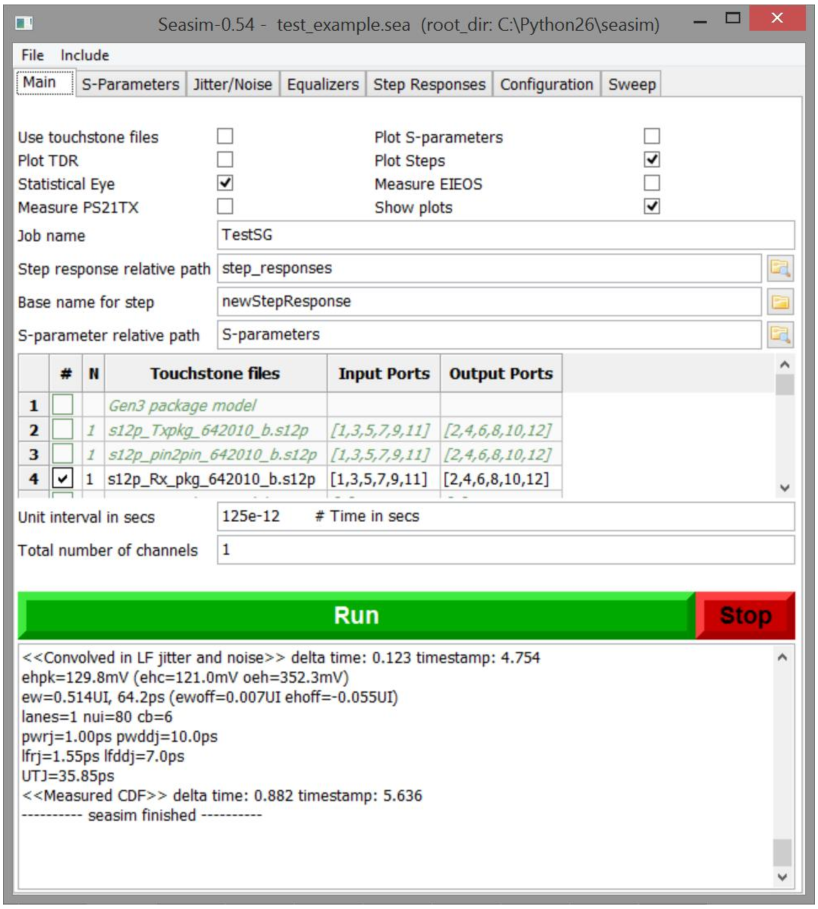


FIGURE 103. SEASIM BASE NAME SETUP

c) On the Jitter Noise tab:

i) Set the corresponding Jitter value for Rj, Sj, DM-SI.
ii) DM-SI value need to tune and vary to achieve EH.
iii) Set DM-SI to 0mV as an initial value.
iv) Set LF Random Jitter = Rj (2ps).
v) Set LR Uniformly distributed Jitter = Sj (0.1UI).

vi) Set LF Uniformly Distributed Voltage Noise = DM-SI 14mV or more.

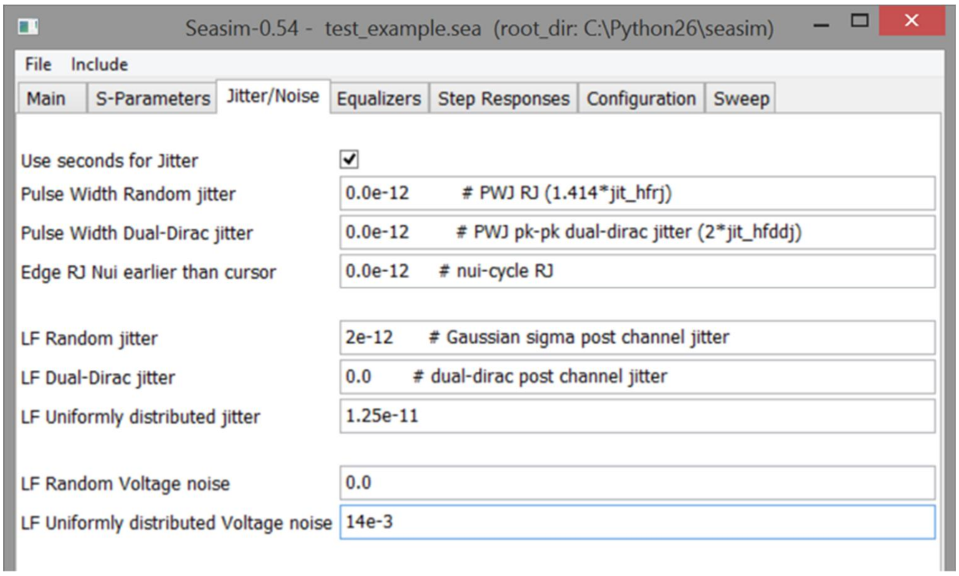


FIGURE 104. SEASIM JITTER/NOISE SETUP

d) On the Equalizer tab:

i) Set the DFE taps and max Magnitude.
ii) For the Long channel, set to [0.000] (Disable DFE).
iii) For the Short and None channels, set to [0.030], Enable with Max of 30mV.

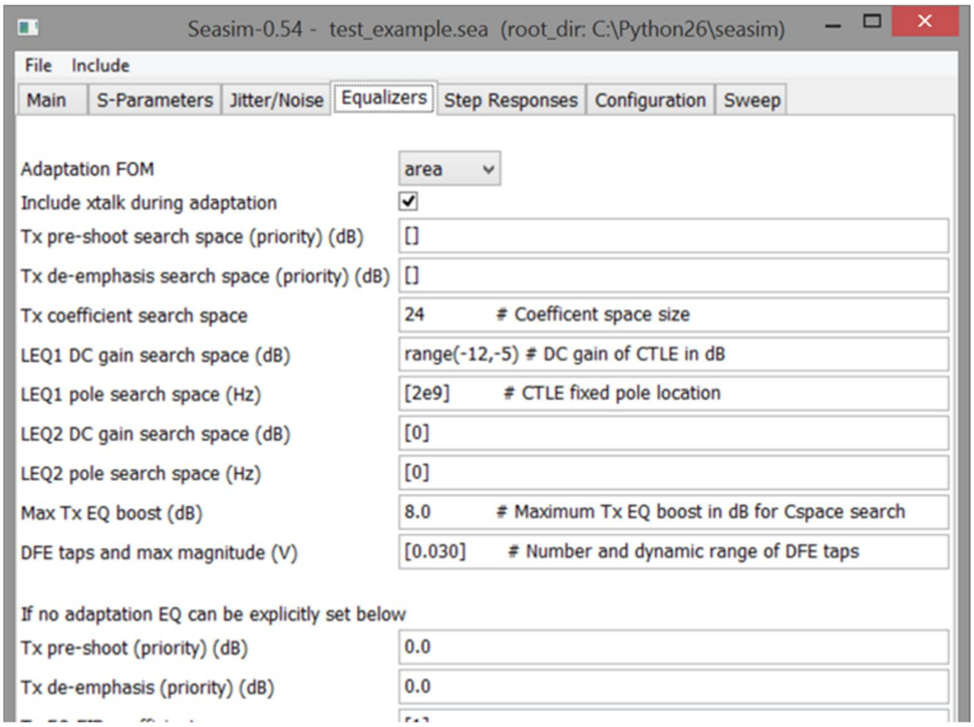


FIGURE 105. SEASIM EQUALIZER SETUP

e) Run the Simulation.

8. The simulated Eye Diagram will be created, with its calculated EH and EW at BER-12 based on the jitter input.

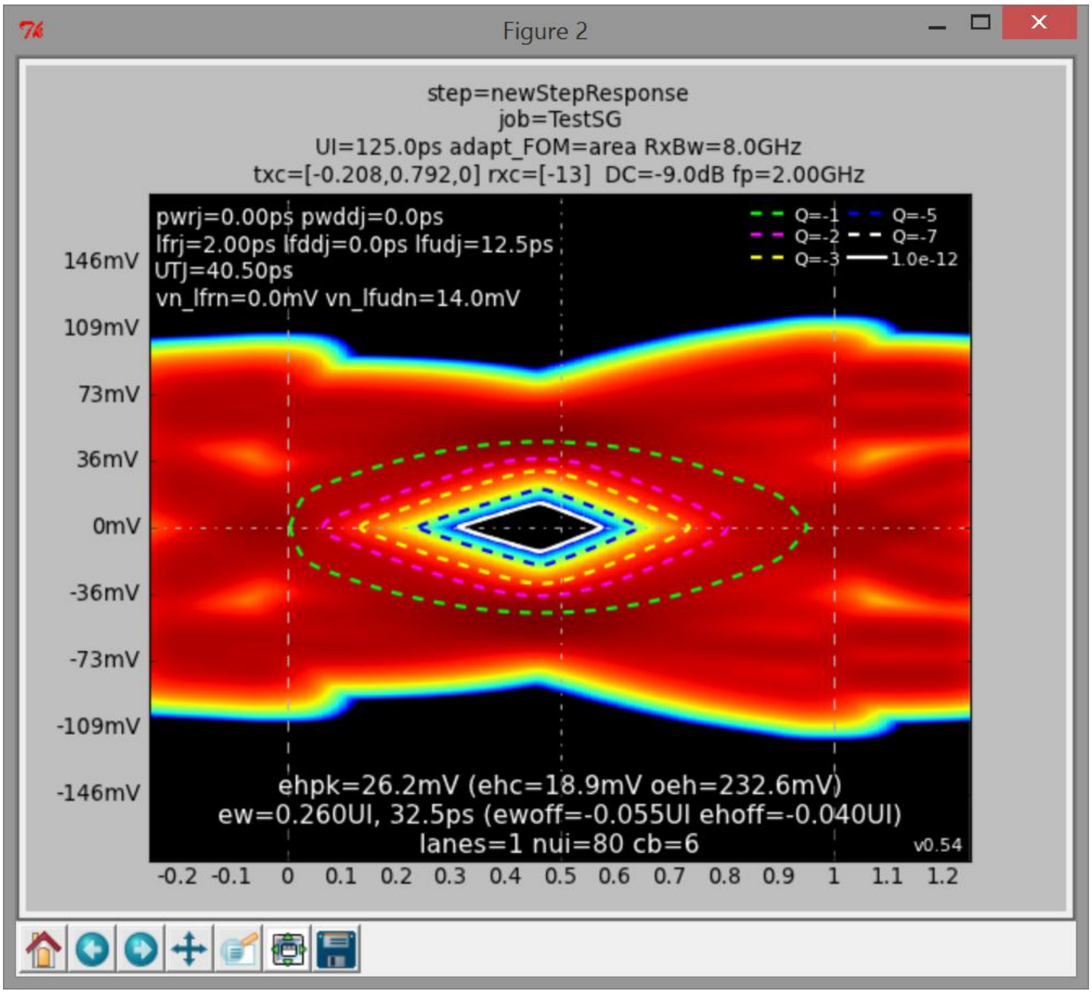


FIGURE 106. SEASIM SIMULATED EYE DIAGRAM #1

9. Observe the EH and EW.

10. Change the DM-SI value to 15mV and run the simulation again.

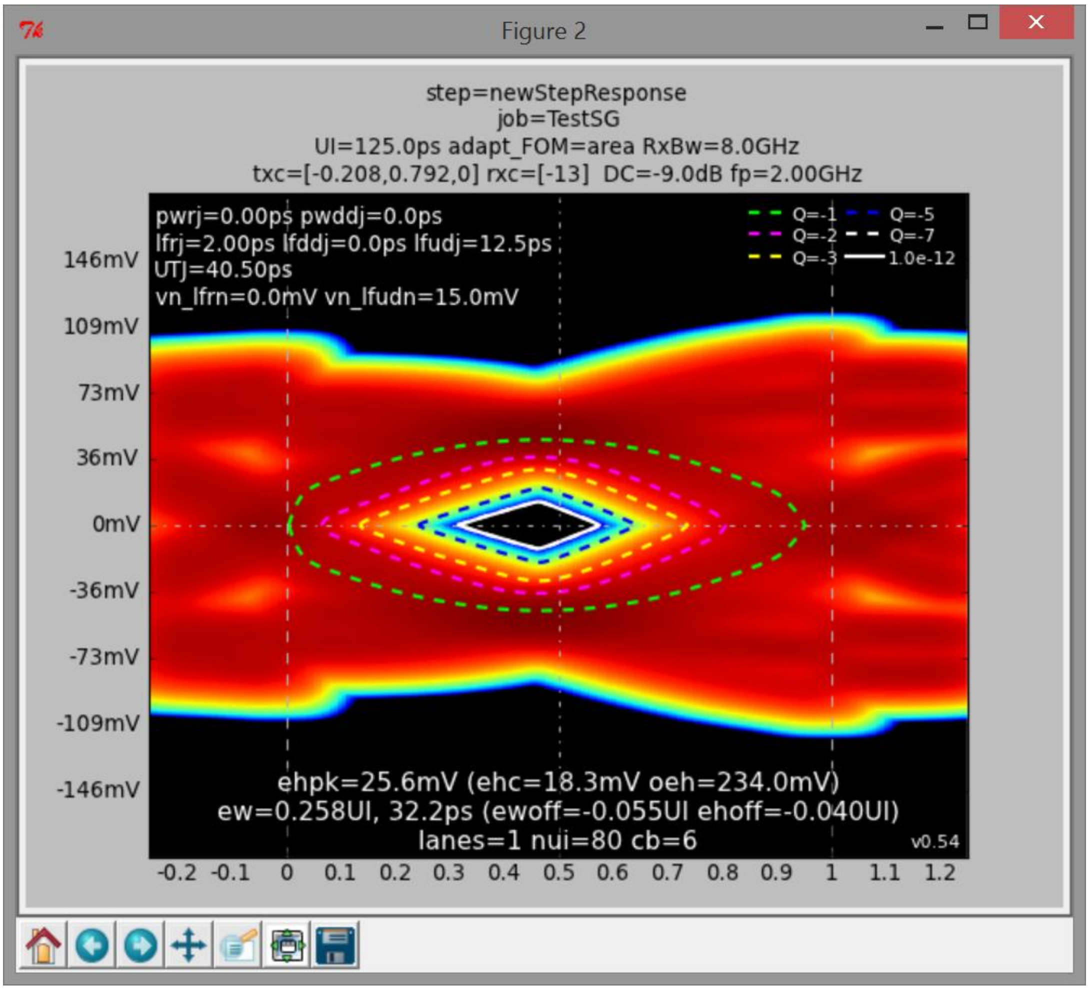


FIGURE 107. SEASIM SIMULATED EYE DIAGRAM #2

11. Change the DM-SI value to 16mV and run the simulation again.

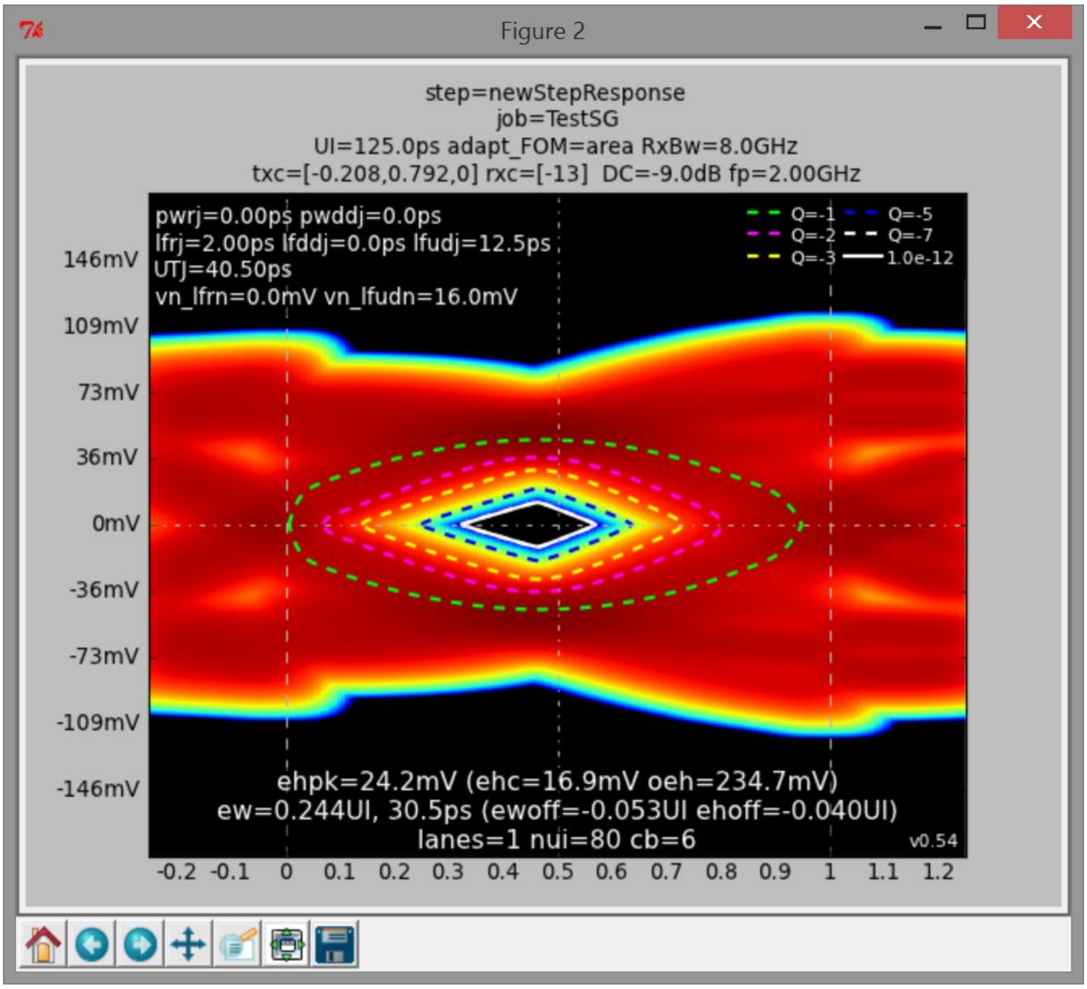


FIGURE 108. SEASIM SIMULATED EYE DIAGRAM #3

12. Calibrate until EH is obtained.

(*) If the EW range cannot be achieved, increase the Amplitude from 800mV to 900mV and perform the Stress Voltage calibration again until EH and EW are obtained.

10.3.2 Stressed Jitter Calibration (For Long Channel Only)

The stressed jitter calibration procedure is similar to that of stressed voltage. Only the long calibration channel (-20 dB) is used. Note that the same post processing scripts are applied identically as they are for the stressed voltage eye case. Eye width is fine-tuned by making adjustments to the Rj source, while EH may be adjusted by varying the launch voltage at the generator.

PCI EXPRESS BASE SPECIFICATION, REV. 3.0

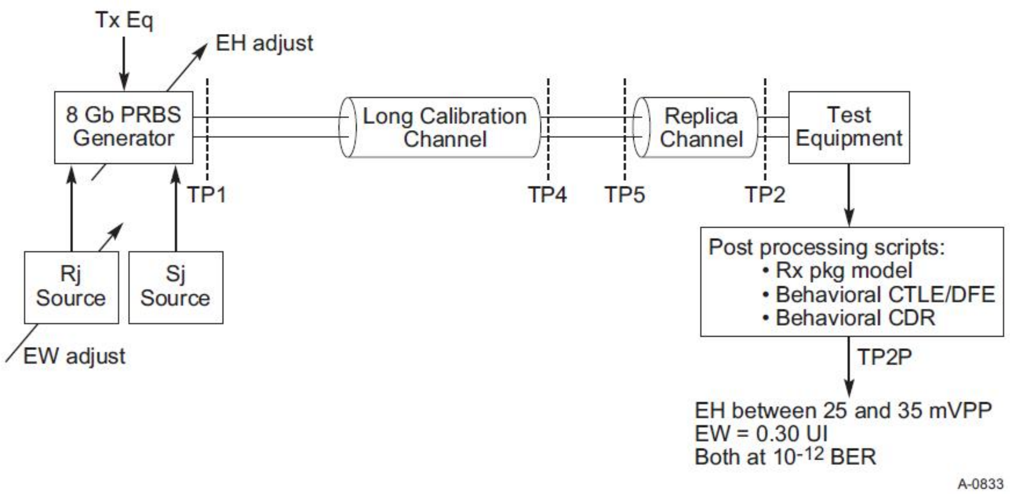


Figure 4-73: Layout for Calibrating the Stressed Jitter Eye

FIGURE 109. LAYOUT FOR LONG CHANNEL CALIBRATION

Table 4-23: Stressed Jitter Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800 (nominal)	mVPP	Measured at TP1, see Figure 4-65. See Note 1.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-ST-8G}$	Eye height at TP2P	25 (min) 35 (max)	mVPP	At BER=10^{-12}. See Note 2.
$T_{RX-ST-8G}$	Eye width at TP2P	0.30	UI	At BER=10^{-12}. See Note 2.
$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI PP	See Figure 4-74 Measured at TP1. See Note 3.
$T_{RX-ST--RJ-8G}$	Random Jitter	3.0	ps RMS	Rj spectrally flat before filtering. Measured at TP1. See Note 4.

FIGURE 110. SPECIFICATION FOR LONG CHANNEL CALIBRATION

10.3.2.1 BERTScope Setup

1. Set the BERTScope Pattern to clk/256.
2. Turn Off Rj, Sj, DM-SI on the BERTScope.
3. Set the DPP Output to the 800mV Amplitude calibrated earlier.
4. Set the DPP De-emphasis and Pre-shoot to “Preset 7” for the Short channel and “Preset 4” for other channel types.
5. Turn Off AFG.

10.3.2.2 Scope Setup

1. Set up Trigger A Event to Edge and the source to chan1.
2. Set up Trigger A-B Event with Acquisition Delay to 4ns.

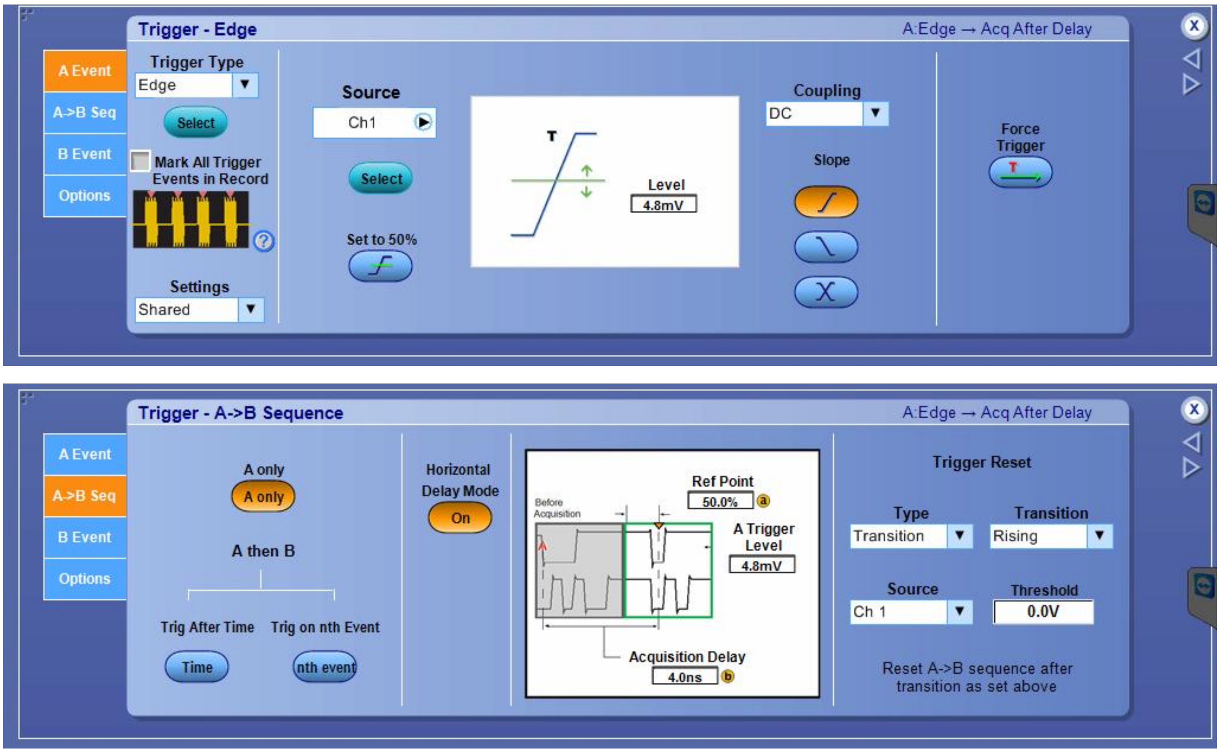


FIGURE 111. SCOPE SETUP

3. Scale Ch1 and Ch2, Math1 (ch1-ch2).
4. Set Acquisition to Average to 2048.
5. Acquire waveform.
6. Save waveform.
7. Modify waveform to Seasim-compatible format.

10.3.2.3 Apply Rx Behavioral Package

1. Run Seasim:
    a) Set the 'Base name for step' to the filename saved.
    b) Check the options as shown in Figure 112.

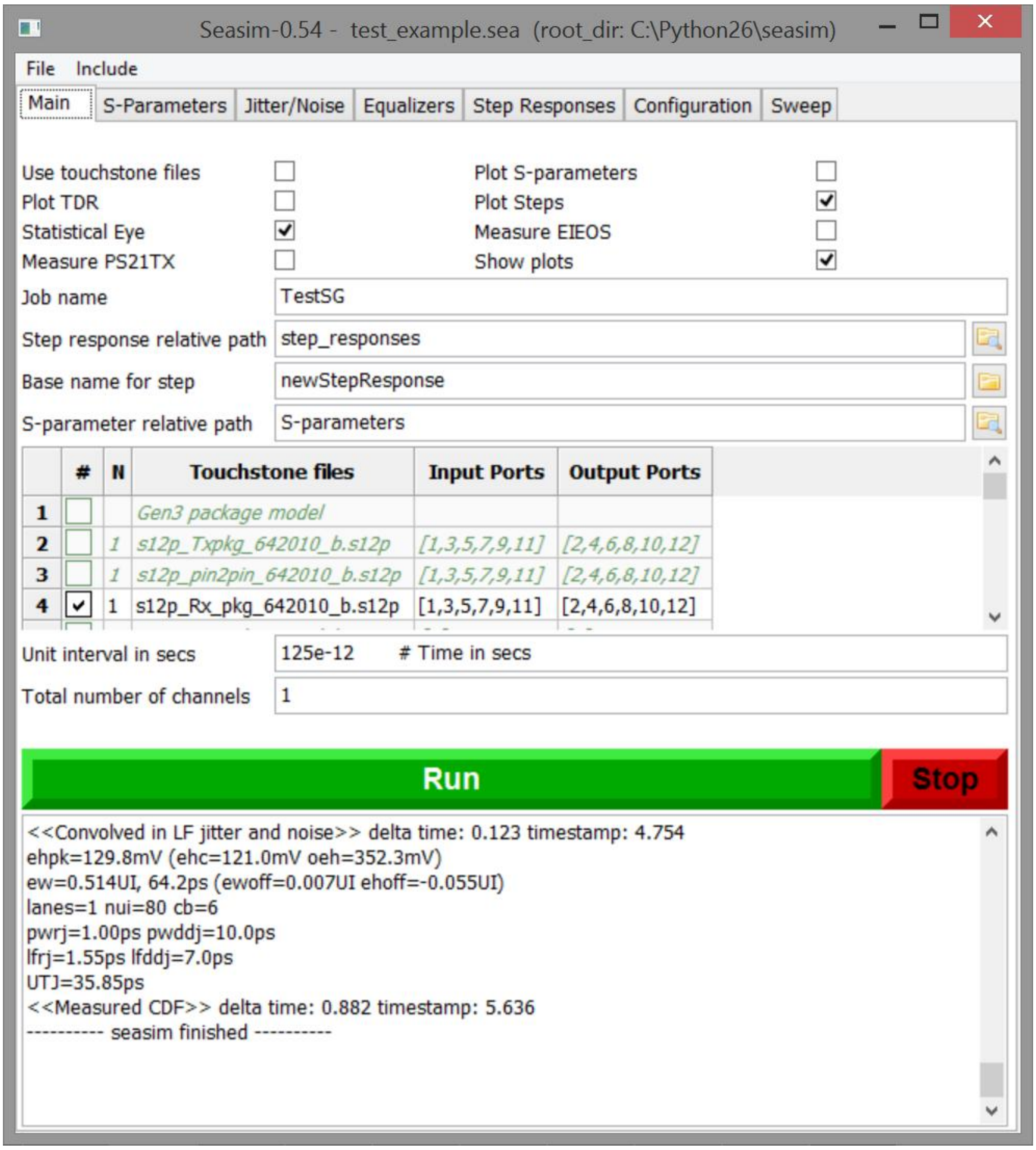


FIGURE 112. SEASIM MAIN SETUP

c) On the Jitter Noise tab:

i) Set the corresponding Jitter value for Rj, Sj.
ii) Rj value need to tune and vary to achieve EW.
iii) Set LF Random Jitter = Rj (3ps or more).
iv) Set LR Uniformly distributed Jitter = Sj (0.1UI).
v) Set LF Uniformly Distributed Voltage Noise = 0.0mV.

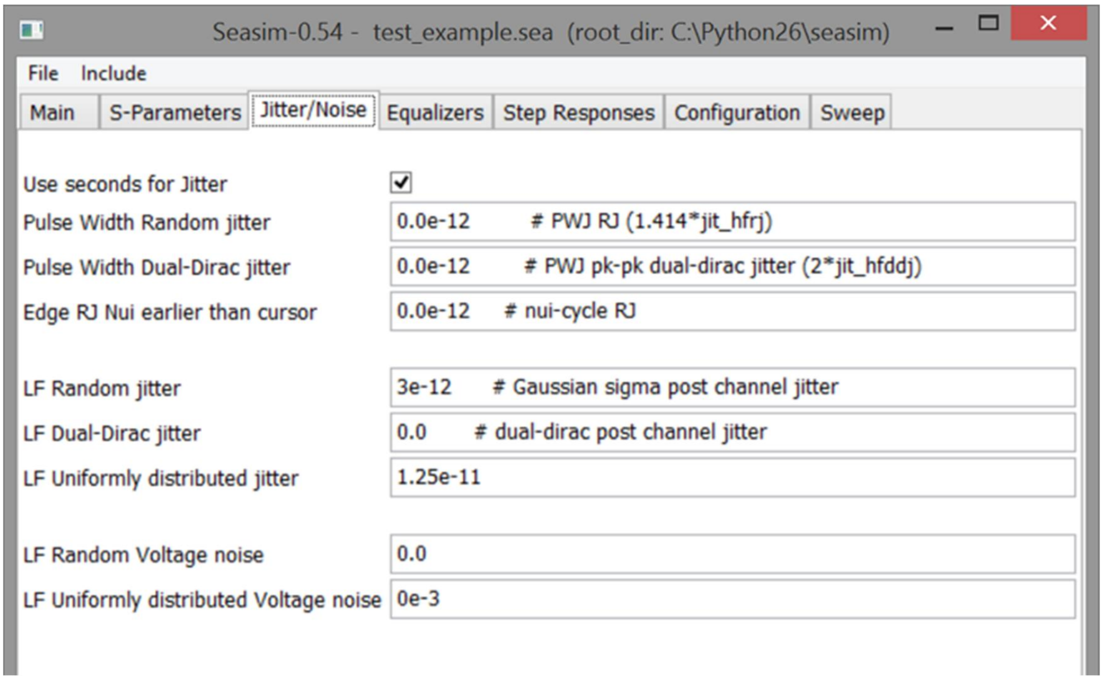


FIGURE 113. SEASIM JITTER/NOISE SETUP

d) On the Equalizer tab:

i) Set the DFE taps and max Magnitude.

ii) Set to [0.030].

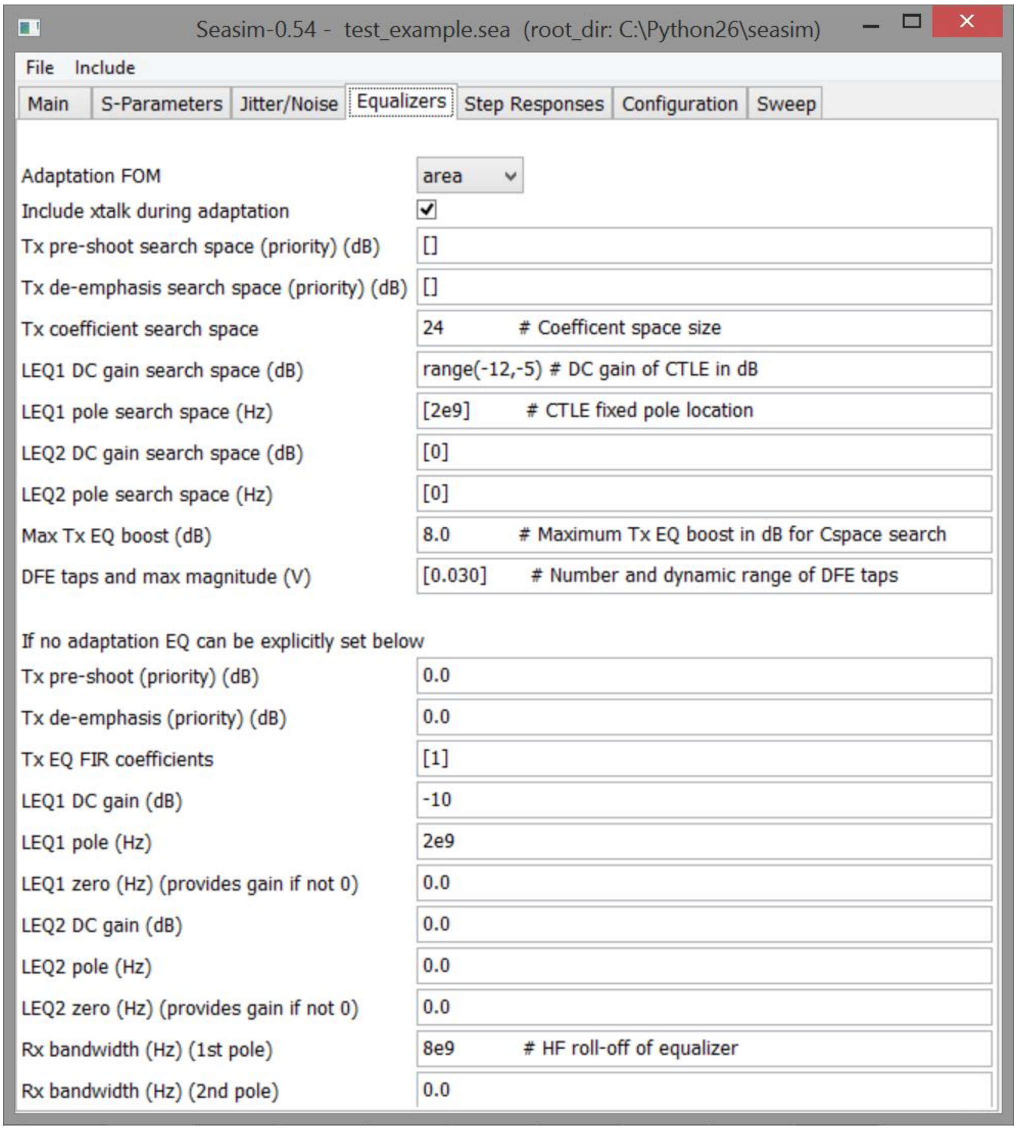


FIGURE 114 .SEASIM EQUALIZER SETUP

e) Run the Simulation.

2. The simulated Eye Diagram will be created with its calculated EH and EW at BER-12 based on the jitter input.

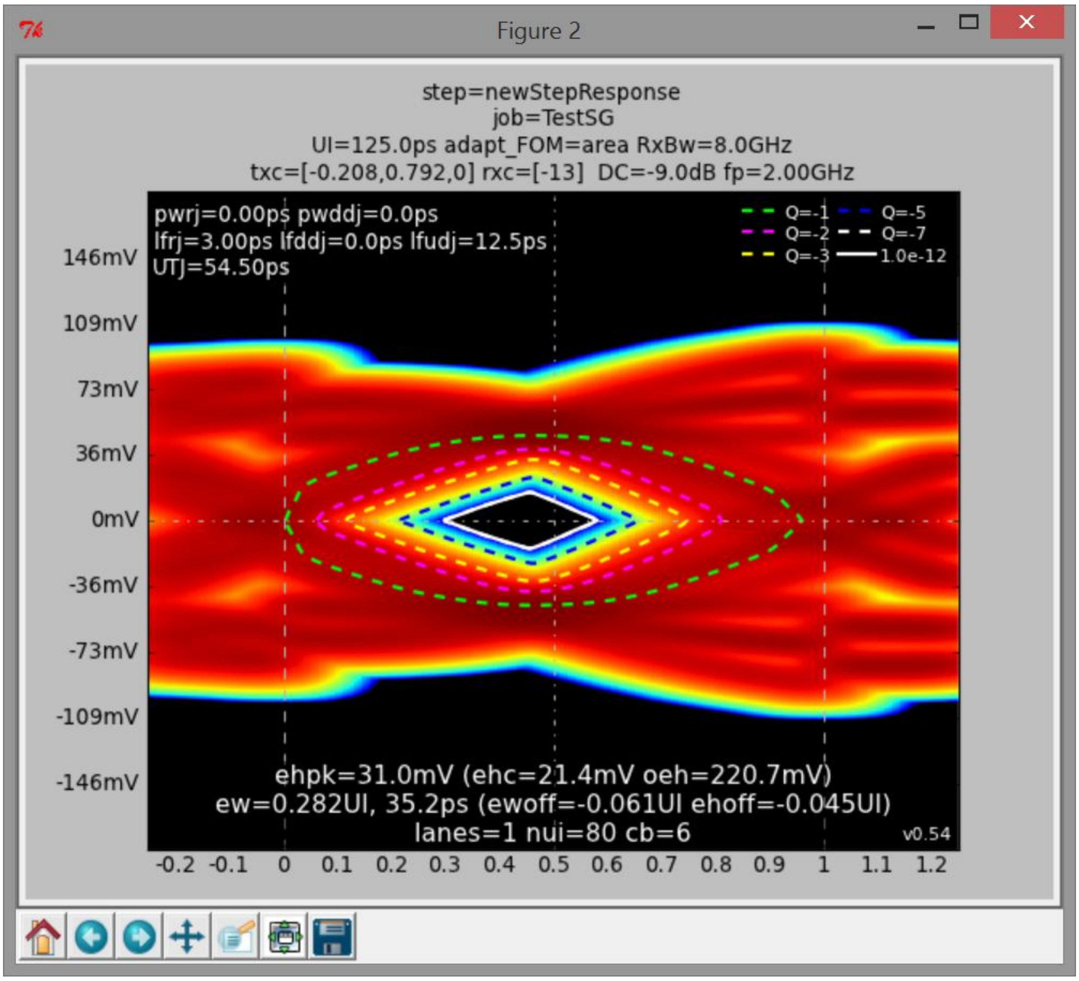


FIGURE 115. WAVEFORM #1

3. Observe the EH and EW.
4. Change the Rj value and run the simulation again.
5. Calibrate until EW is obtained.

(*) If the EH range cannot be achieved, increase the Amplitude from 800mV to 900mV and perform the Stress Jitter calibration again until EH and EW are obtained.

10.4 Receiver Test

10.4.1 Equipment Setup

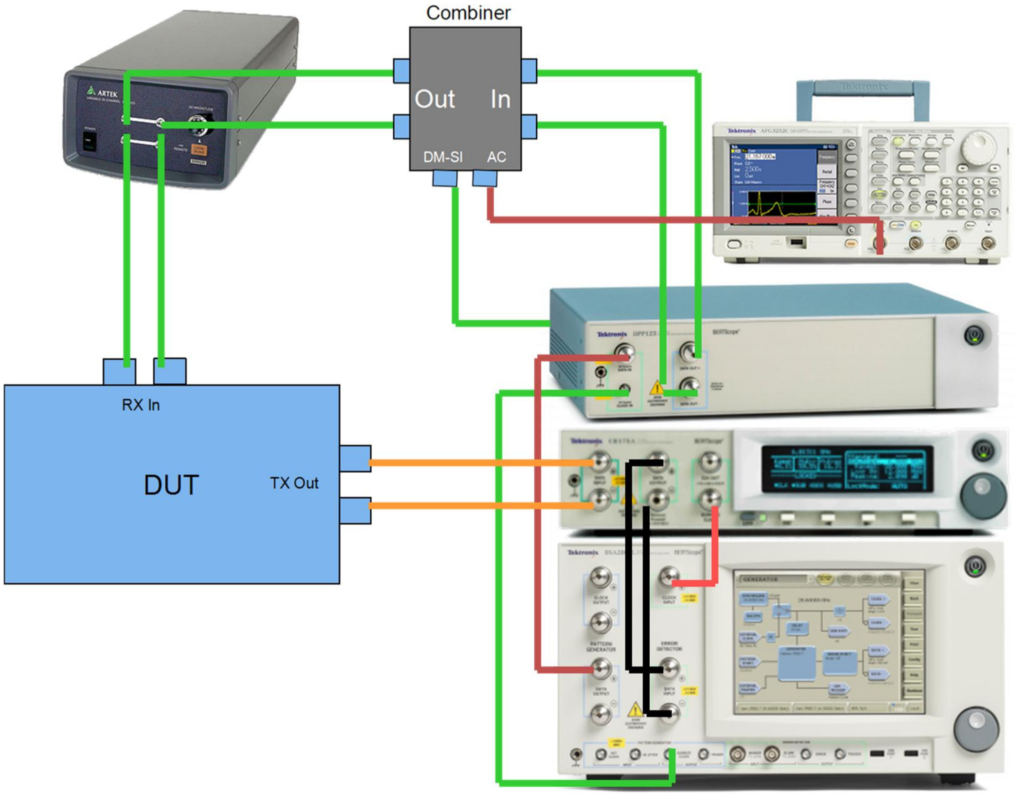


FIGURE 116. RECEIVER TEST EQUIPMENT SETUP

10.4.1.1 Connection Steps

1. Connect BERTScope Data(+) to DPP.
2. Connect BERTScope Clk Out to DPP.
3. Connect DPP Data(+) out to Combiner In.
4. Connect DPP Data(-) out to Combiner In.
5. Connect AFG Output1 to Combiner CM-IN.
6. Connect BERTScope (real panel) SI-out to Combiner DM In.
7. Connect Combiner Data Out to Artek Box.
8. Connect Artek Box Out to DUT In.
9. Connect DUT Tx Out to Clock Recovery CR125A Data In.
10. Connect CR125A Data out to BERTScope Detector Data In.
11. Connect CR125A Subrate Clock Out to BERTScope Detector Clock In.
12. Connect the External Clock from BERTScope to DUT as Ref Clk (100MHz).

10.4.2 Stressed Voltage Receiver Test

Once the calibrated EH and EW have been obtained, the cables are moved to connect the Rx DUT to the far end of calibration channel. The Tx equalization is then optimized as it was for the stressed voltage eye with the assumption that the DUT Rx will also optimize its equalization. Sj is set to an initial value that permits the receiver CDR to achieve lock.

10.4.2.1 Configure BERTScope

1. Set the Generator to 8Gpbs.
2. Set the Pattern to PCIe_8G_BruteFor.RAM.

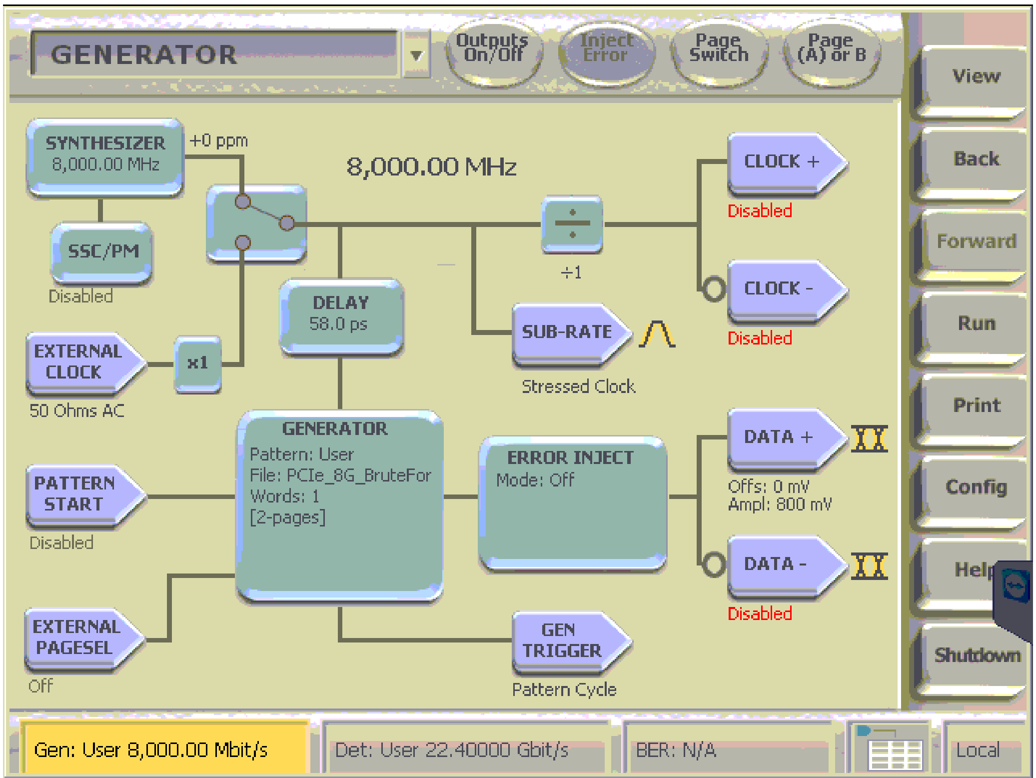


FIGURE 117. RECEIVER TEST – CONFIGURE BERTSCOPE

10.4.2.2 Configure for Stressed Jitter

1. Set the Calibrated SJ for 0.1UI at 100MHz.
2. Set the Calibrated Rj for 2ps(RMS).
3. Set the Calibrated Sine Interference Amplitude that is calibrated to achieve EH and EW (DM-SI).
4. Set the Sine Interference Frequency to 2.1GHz.
5. Set the Sine Interference mode to External.
6. Set the DPP Output to calibrated amplitude to achieve EH and EW.

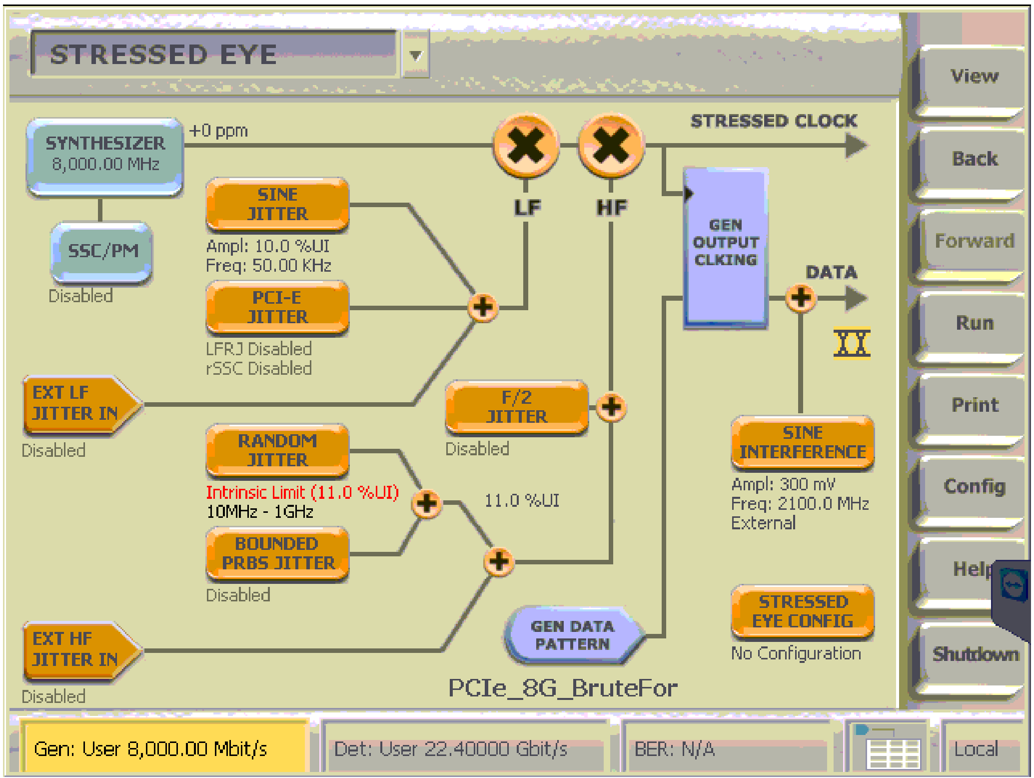


FIGURE 118. RECEIVER TEST CONFIGURE FOR STRESSED JITTER

7. Configure the ISI by setting the Artek ISI % value to the calibrated channel type.
8. Configure the AFG:
   a) Set the Output1 of AFG to ON.
   b) Set the Output1 Mode to Sine Wave.
   c) Set the Sine Wave Frequency to 120MHz.
   d) Set the Sine Wave Amplitude to the calibrated value.
9. Set up the BERTScope Detector:
   a) Click Auto Align.

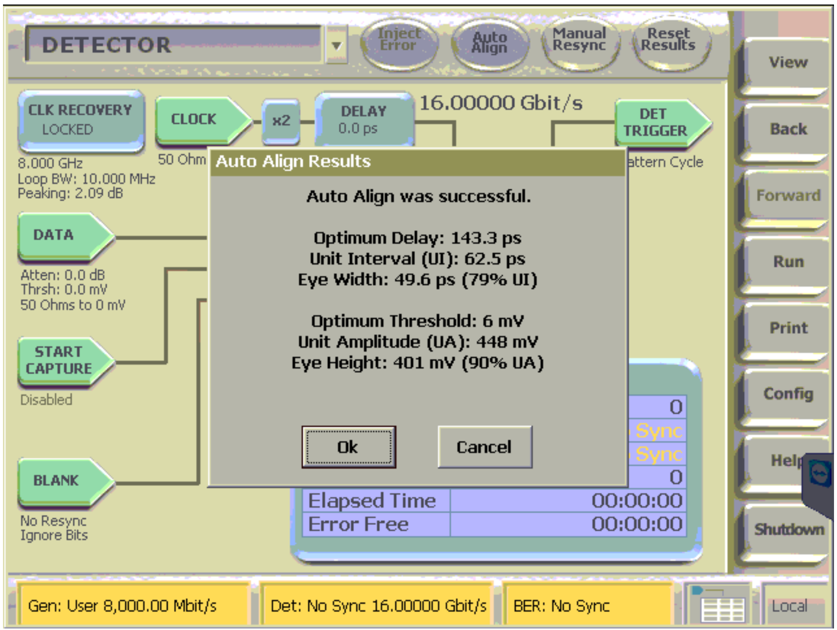


FIGURE 119. RECEIVER TEST – CONFIGURE BERTSCOPE DETECTOR

10.4.2.3 Bit Error Rate Test

1. With the DUT in loopback mode, and the BERTScope synchronized with pattern, the compliance test may begin.
2. Click Reset Result.
3. Click RUN.
4. Let the Detector runs, and stop when the bits are more than 1xE12.
5. Read the Error value.
6. If the error is zero (0), then the test passes.

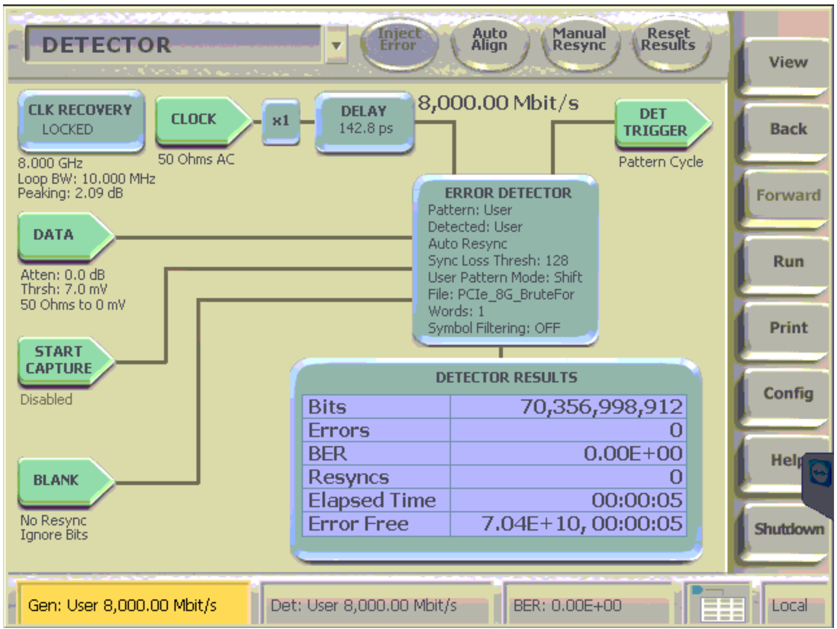


FIGURE 120. RECEIVER TEST – PERFORM BER TEST

10.4.3 Stressed Jitter Receiver Test (100MHz)

10.4.3.1 Configure BERTScope

1. Set the Generator to 8Gpbs.
2. Set the Pattern to PCIe_8G_BruteFor.RAM.

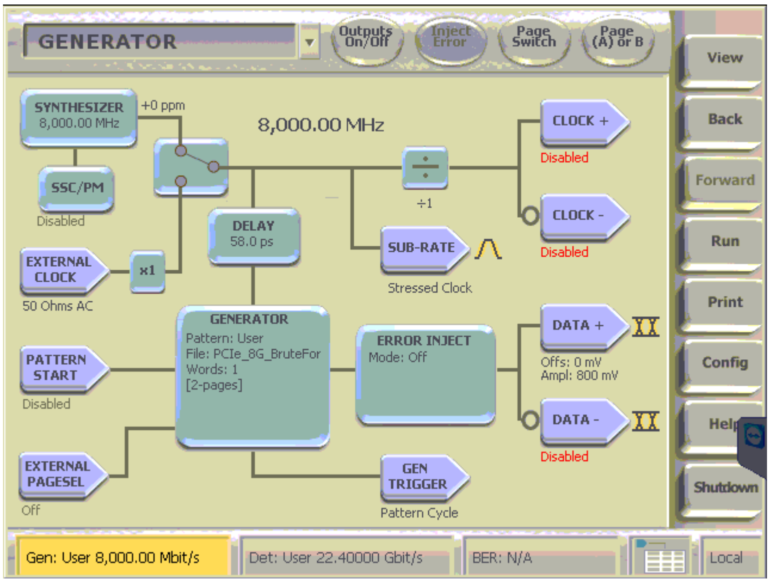


FIGURE 121. RECEIVER STRESSED JITTER TEST – BERTSCOPE SETUP #1

10.4.3.2 Configure for Stressed Jitter at 100MHz

1. Set the Calibrated SJ for 0.1UI at 100MHz.
2. Set the Calibrated RJ that is calibrated during Stressed Jitter Calibration that achieved EW and EH.
3. Set the Calibrated Sine Interference to 0mV.
4. Set the DPP Output to the calibrated amplitude to achieve EH and EW.

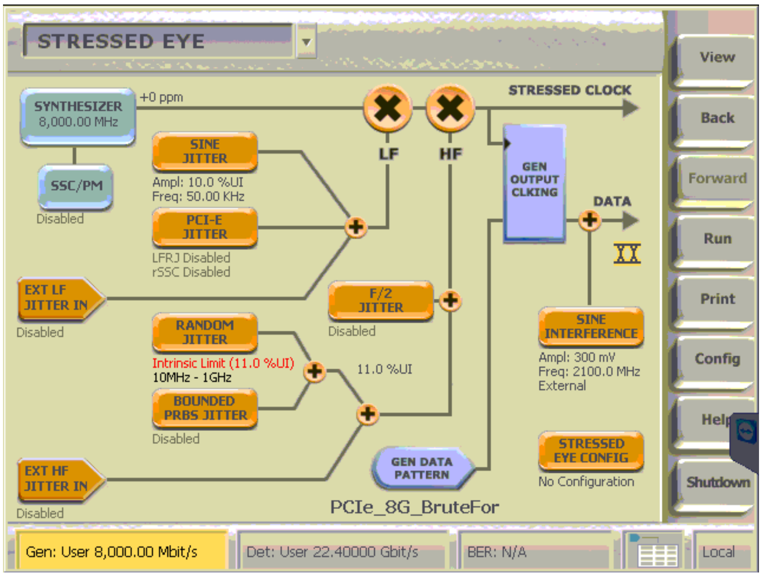


FIGURE 122. RECEIVER STRESSED JITTER TEST – BERTSCOPE SETUP #2

5. Configure the ISI by setting the Artek ISI % value to the calibrated channel type.
6. Configure the AFG by setting the Output1 of AFG to OFF.
7. Set up the BERTScope Detector by clicking on Auto Align.

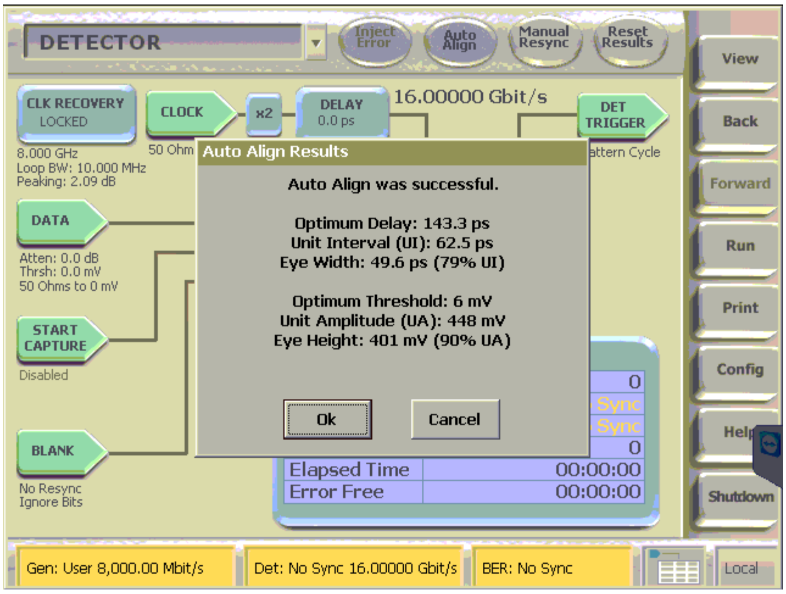


FIGURE 123. RECEIVER STRESSED JITTER TEST – BERTSCOPE DETECTOR

10.4.3.3 Bit Error Rate Test

1. With the DUT in loopback mode, and the BERTScope synchronized with pattern, the compliance test may begin.
2. Click Reset Result.
3. Click RUN.
4. Let the Detector runs, and stop when the bits are more than 1xE12.
5. Read the Error value.
6. If the error is 0, the test passes.

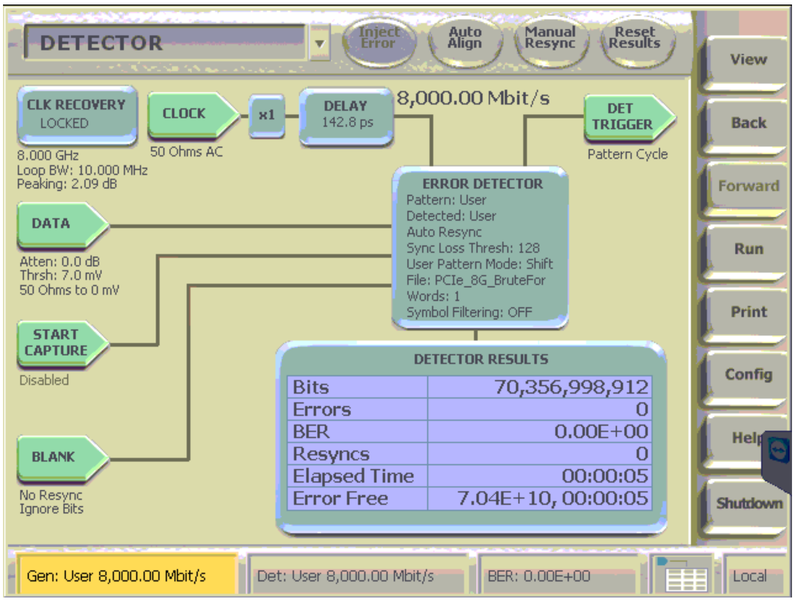


FIGURE 124. RECEIVER STRESSED JITTER – PERFORM BER TEST

11 Appendix E: PVT Automation Features

The GRL PCIe3-BASE & PCIe4-BASE (8 GT/s) Rx software provides support for repeated testing within sequences of parameter values, which are applied to the DUT during the tests. These features are enabled by the Advanced Mode in the Configurations page. Advanced sequencing can be used to manage repetitive test loops needed when performing PVT (Process, Voltage, Temperature) characterization on PCIe3 transceiver silicon.

11.1 Available Parameters

Table 6 lists the parameters which can be controlled by the PVT Automation. Up to eight values may be specified for each parameter.

TABLE 6. AVAILABLE PARAMETERS

Symbol	Parameter	Units
RJ	Random Jitter	Picoseconds
ISI	Inter Symbol Interference	Per cent of UI
SJ	Sinusoidal Jitter	Picoseconds
Amplitude	Launch Voltage	Millivolts, peak-to-peak
CM	Common Mode (noise source)	
DM	Differential Mode (noise source)	

11.2 Applicable Tests

Table 7 lists the tests which can be controlled by the PVT Automation. PVT parameters have no effect on other available tests in the software.

TABLE 7. APPLICABLE TESTS

Test Title
Stress Voltage Sweep Test (none)
Stress Voltage Sweep Test (short)
Stress Voltage Sweep Test (long)
Stress Jitter Sweep Test (long)

11.3 Setting Up PVT Value Sequences

1. To enable Advanced PVT features in the GRL software, in the Configurations page, set the Advanced Mode to 'True'.

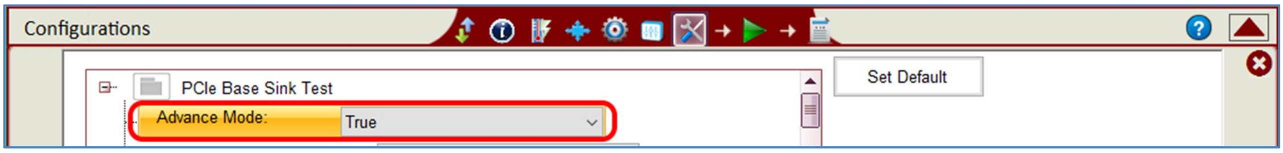


FIGURE 125. ENABLE ADVANCED PVT AUTOMATION

2. The Advanced PVT configuration icon  will appear on the toolbar menu. Select the icon to access the PVT Configuration page.

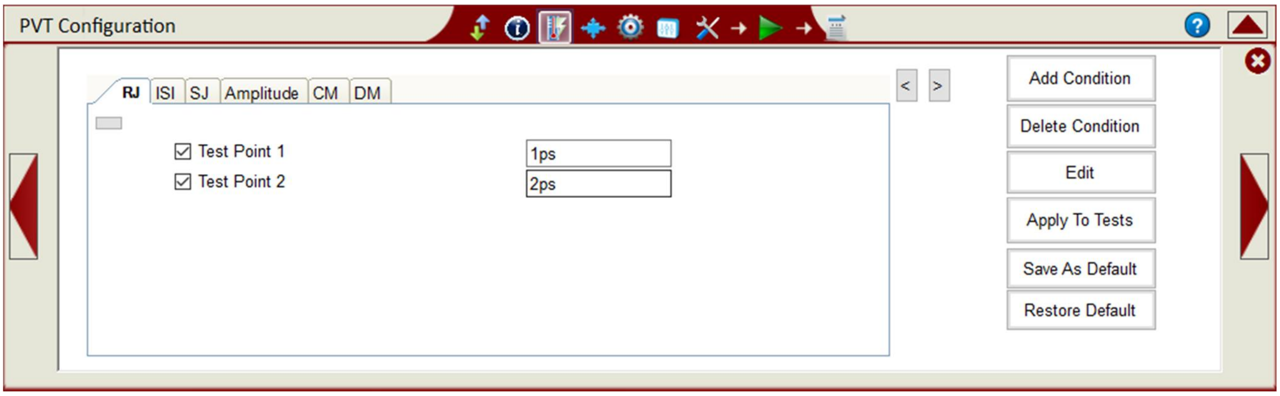


FIGURE 126. PVT CONFIGURATION PAGE

3. Add a parameter to the selected test by selecting "Add Condition". See Figure 127, which selects 'SJ_1' as the new condition group. No drop-down menu of allowed parameter names is provided. Refer to Table 6. A short description may be provided. This description, and the names of the individual step 'Variables' are all included in the test Report.

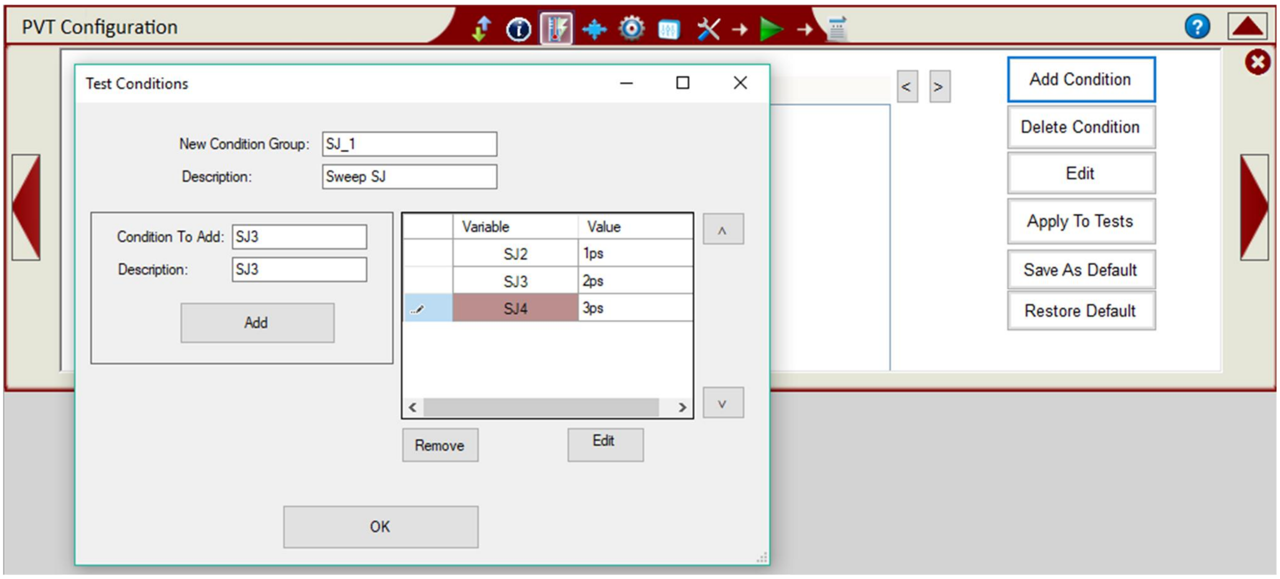


FIGURE 127. ADD FIRST PVT AUTOMATION PARAMETER

4. Enter one or more parameter value for the steps of the test condition sequence. Take care to include the suffix for the units, and to assign values which are appropriate for that parameter according to the PCIE3 specification. See figure below, which shows four steps for parameter 'SJ', named 'SJ1', 'SJ2', 'SJ3' and 'SJ4', and assigned values 1ps, 1.2ps, 1.8ps and 3ps, respectively. When finished editing the Test Conditions, select "OK". Note that individual steps may be selected, then edited or removed from the list.

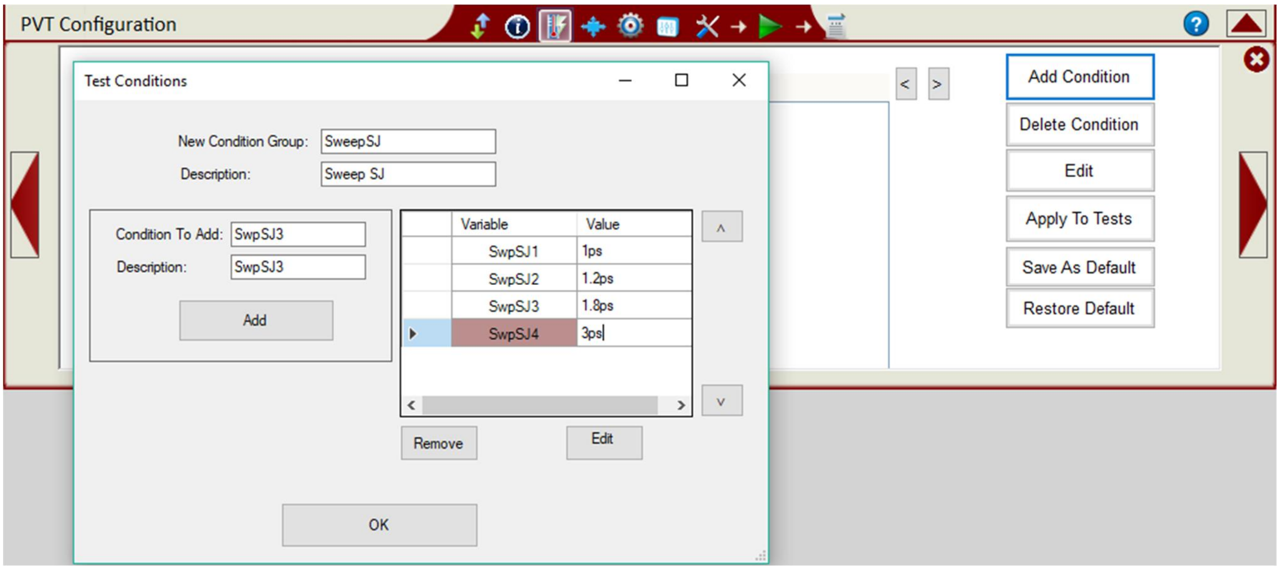


FIGURE 128. SET EACH PVT PARAMETER VALUE IN SEQUENCE

5. Add a second parameter. See figure below, which adds 'SweepISI', with three values, each expressed as a percentage.

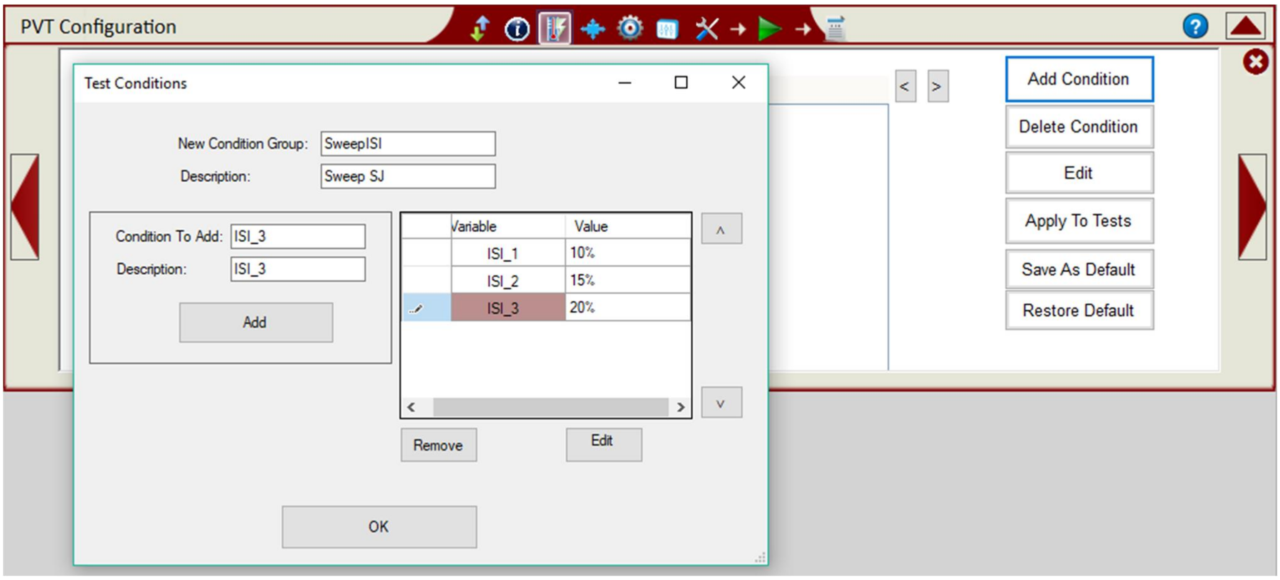


FIGURE 129. ADD SECOND PVT PARAMETER

6. Repeat setting values to each of the allowed parameters. Those parameters which are not set up with explicit values will use the default value.

7. Apply the sequences of parameters to the selected tests (see figure below), which builds a “Stress Test Plan”.

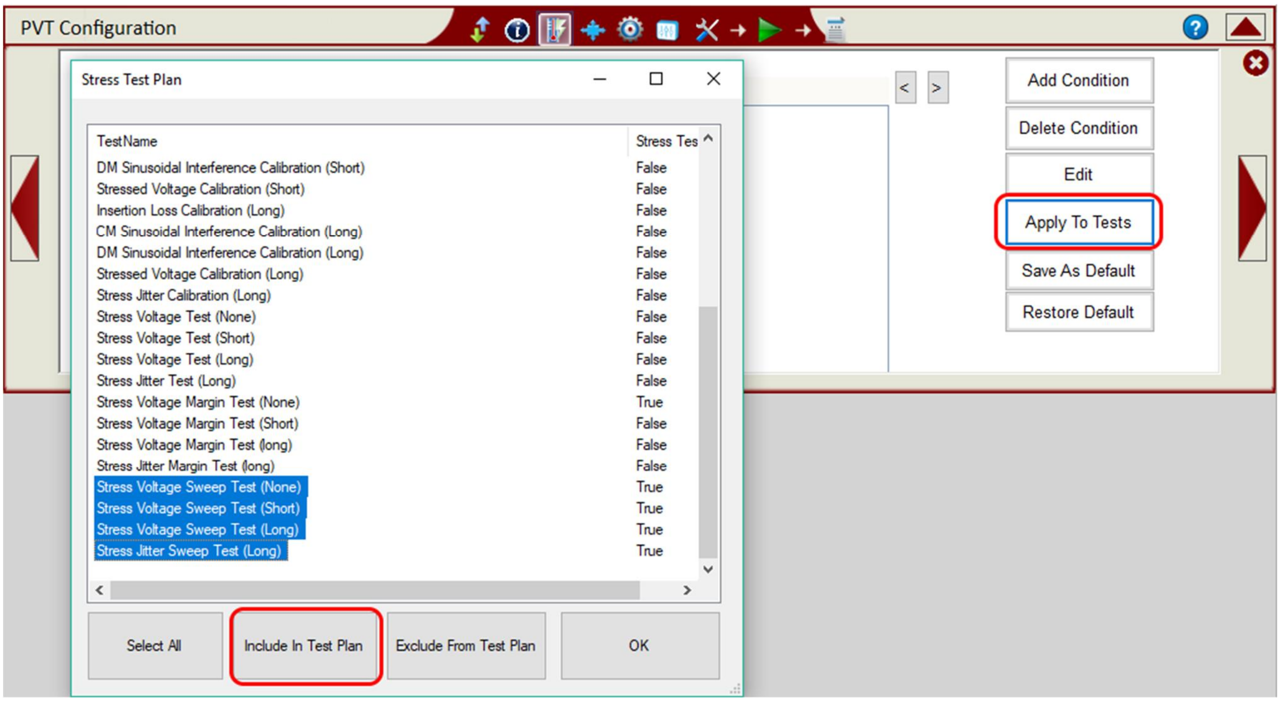


FIGURE 130. APPLY TO TESTS AND SELECT APPLICABLE TESTS

8. Select the PVT tests to run (see figure below).

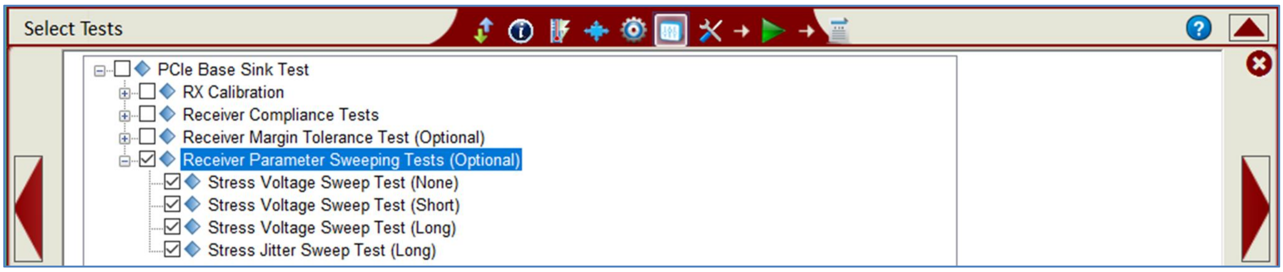


FIGURE 131. SELECT PVT TESTS TO RUN

9. Run the tests using the “Run Tests with PVT” button (see figure below).

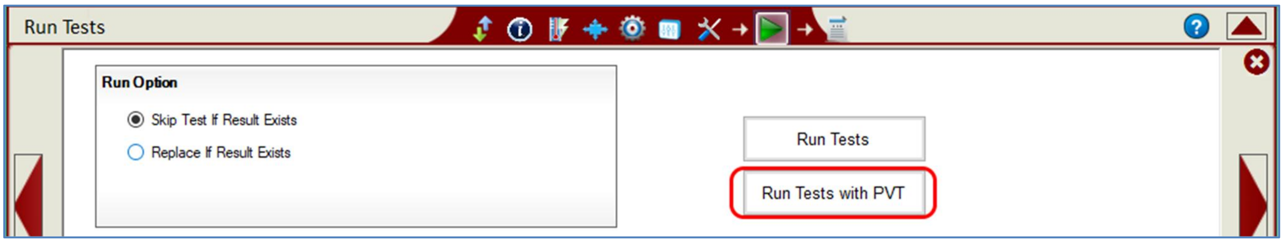


FIGURE 132. RUN TESTS WITH PVT

11.4 Search Algorithm

11.4.1 Jitter Margin Testing

After selecting the parameters and their ranges, the user may select from a list of search algorithms to find the bounds of jitter margin.

TABLE 8. PVT AUTOMATION – INTERNAL JITTER MARGIN SEARCH ALGORITHMS

Symbol	Algorithm
	Bottom-Up
	Top-Down
	Binary

11.5 Test Results

Results from the selected PVT tests, each using the one or more defined PVT parameters, are collected in the Test Report.

The selected tests are all run, one after the other, for each permutation of the parameters. The parameter defined first is varied most slowly; the last-defined parameter is defined most quickly.

For example, considering the parameters and tests defined and selected in the above will iterate as shown in Table 9. (Individual parameter step names are not shown.)

TABLE 9. PVT AUTOMATION – ITERATION SEQUENCE EXAMPLE

Seq.	SJ	ISI	Tests
1	1.0ps	10%	All 4 Parameter Sweeping Tests
2	1.2ps	15%	All 4 Parameter Sweeping Tests
3	1.8ps	20%	All 4 Parameter Sweeping Tests
4	3.0ps	10%	All 4 Parameter Sweeping Tests
5	1.0ps	15%	All 4 Parameter Sweeping Tests
6	1.2ps	20%	All 4 Parameter Sweeping Tests
7	1.8ps	10%	All 4 Parameter Sweeping Tests
8	3.0ps	15%	All 4 Parameter Sweeping Tests
9	1.0ps	20%	All 4 Parameter Sweeping Tests
10	1.2ps	10%	All 4 Parameter Sweeping Tests
11	1.8ps	15%	All 4 Parameter Sweeping Tests
12	3.0ps	20%	All 4 Parameter Sweeping Tests

11.6 Saving and Loading a PVT Session

When using the PVT Automation control, the "Save As Default" and "Restore Default" buttons are not used. To save a session, with all of the PVT parameter information, test results, and any waveforms, use the "Options" drop-down on the main software menu bar, followed by "Save Session".

To load a session back into the software, including the saved parameter settings, select "Options" -> "Load Session".

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

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