# Granite River Labs

# GRL-PCIE-TX PCI Express® 4.0 & 5.0 Transmitter Compliance Test Automation Solution Quick Start/User Guide

## for Physical Layer Transmitter Test Application

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# 1 Introduction

This Quick Start/User Guide provides information using the GRL-PCIE-TX test solution to set up and test an electrical transmitter (Tx) device for PCI Express (PCI-SIG SEG) certification.

The main body of this documentation describes how to configure the GRL-PCIE-TX solution to capture and test waveforms in a PCIe 5.0 (or below) system (lane, data rate, preset), or individual waveforms, and perform SigTest signal quality and de-emphasis compliance tests. The test automation is carried out based on PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's).

The GRL-PCIE-TX solution consists of the GRL PCIe "GRL-P1" hardware controller and automation software (GRL-PCIE-TX). The GRL-PCIE-TX software when run from the computer or oscilloscope enables automation control to test the device under test (DUT) for Tx electrical compliance. The GRL-P1 hardware controller is designed to work primarily with the software to provide compliance toggle to control the state of the DUT. Alternatively, an arbitrary function generator can also be used as a secondary option for compliance toggle control. The GRL test solution also extends support for RF switch integration to automate switching or selection of the lane under test.

The GRL automation control enabled PC or scope automates power and signal quality test sequencing and processing of captured waveforms for the DUT at the selected PCIe data rate. The Tx path is tested with worst case eye to ensure a Bit Error Ratio (BER) of less than 1E-12 can be achieved. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

This documentation covers the following major components for PCIe Tx testing.

1. GRL-P1 hardware controller setup.
2. GRL-PCIE-TX software configuration and test setup.

*Note: For manual test methodology, please refer to PCI-SIG SEG for approved vendor specific Method of Implementation (MOI's) as technical reference.*

# 2 Resource Requirements

*Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.*

## 2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

| Equipment | Qty. | Description/Key Spec Requirement |
|---|---|---|
| High Performance Real-time Oscilloscope [a] | 1 | ≥ 25 GHz bandwidth (For PCIe Gen 4)<br>≥ 33 GHz bandwidth (For PCIe Gen 5) |
| "GRL-P1" PCIe Compliance Test Hardware Controller (Optional) | 1 | For PCIe compliance toggle control |
| Advanced Technology eXtended (ATX) Power Supply | 1 | For power supply to the DUT |
| GRL Switch (Optional) | 1 | For multi-lane automated testing |
| PCI-SIG Compliance Base Board (CBB)<br>or<br>PCI-SIG Compliance Load Board (CLB) | 1 | For add-in cards<br><br>For hosts |
| Computer (laptop or desktop) | 1 | Windows 7+ OS<br>For automation control of the DUT state |

*[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.*

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

| Cable | Qty. |
|---|---|
| Power Control Adapter Cable | 1 |
| USB Type-A to micro Type-A/B Cable | 1 |
| Test Fixture Control Cable (2-conductor power control only cable or 6-conductor fixture control cable) | 1 |
| Clock Compliance Toggle Cables (matched SMA-to-SMP cables) | 1 pair |
| SMA-to-SMP Cables | 4 pairs[a] |

*[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.*

## 2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

| Software | Description/Source |
|---|---|
| GRL-PCIE-TX | Granite River Labs PCI Express® 4.0 & 5.0 Automated Transmitter Compliance Test Solution (hardware & software) – www.graniteriverlabs.com<br>Further automation license for Custom DUT, RF Switch, or other bench automation – www.graniteriverlabs.com |
| VISA (Virtual Instrument Software Architecture) API Software | VISA Software is required to be installed on the controller PC running GRL-GRL-PCIE-TX software. GRL's software framework has been tested to work with all three versions of VISA available on the Market:<br>1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/<br>2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)*<br>3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)* |
| SigTest | Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html |

# 3 Setting Up GRL-PCIE-TX Automation Software

This section provides the procedures to start up and pre-configure the GRL-PCIE-TX automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

*Note: The GRL-PCIE-TX software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.*

To start using the GRL-PCIE-TX software, follow the procedures in the following sections.

## 3.1 Download GRL-PCIE-TX Software

Download and install the GRL-PCIE-TX software as follows:

1. If the GRL-PCIE-TX software is to be installed on a PC (where is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIETxTestApplicationxxxxxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the GRL-PCIE-TX application.
   - **PCIe4_TxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

## 3.2 Launch and Set Up GRL-PCIE-TX Software

1. Once the GRL-PCIE-TX software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

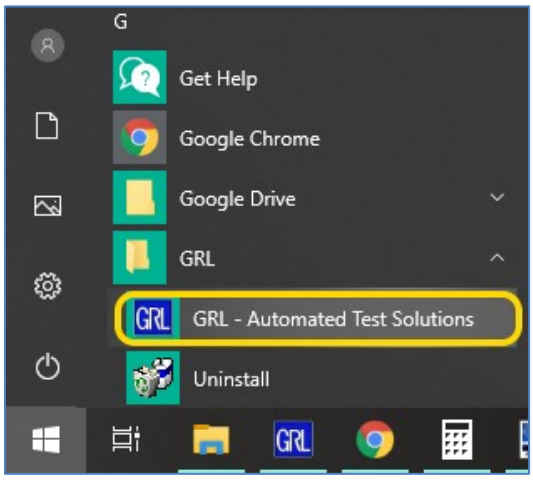



FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

2. From the **Application→Framework Test Solution** drop-down menu, select "**PCIE Tx Test Application**" to start the PCIe Tx Test Application. If the selection is grayed out, it means that your license has expired.

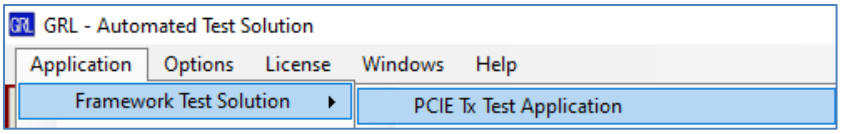



FIGURE 2. START PCIE TX TEST APPLICATION

3. To enable license, go to License→License Details.

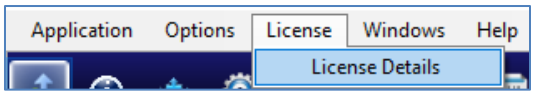



FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

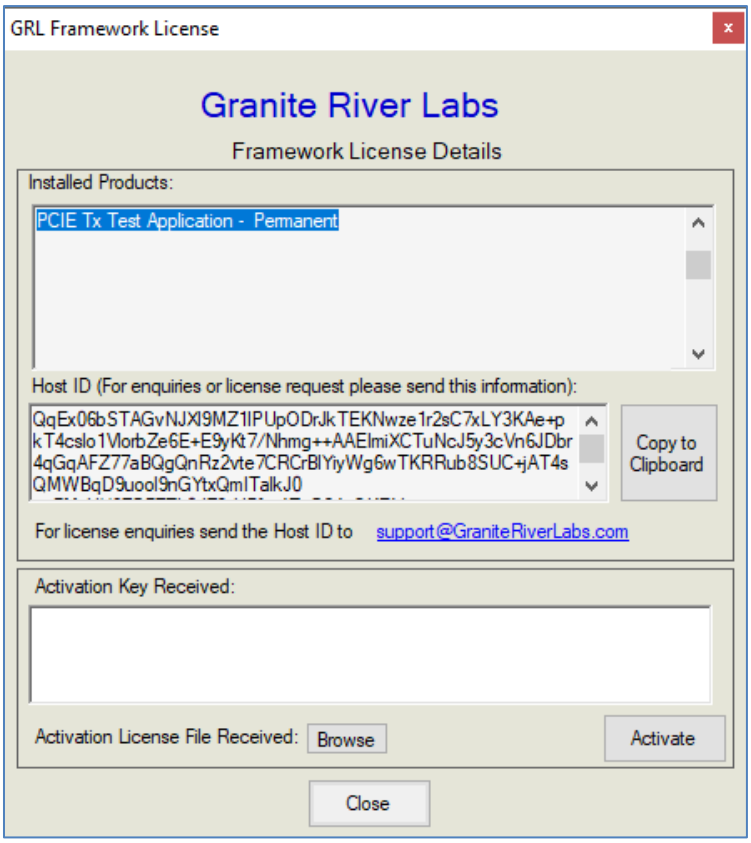



FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select "Activate".
- If you do not have an Activation Key, select "Close" to use a demo version of the software over a free 10-day trial period.

***Note:*** *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

4. Select the Equipment Setup icon on the PCIe Tx Test Application menu.
5. Connect the oscilloscope with the controller PC through either GPIB, USB or LAN. *(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the controller PC is provided in the Appendix of this document.)*
6. If using an RF Switch, connect the switch via GPIB to the GRL automation control enabled Scope or PC.
7. If using an Arbitrary Function Generator (AFG) as the compliance toggle control, connect the AFG via USB to the GRL automation control enabled Scope or PC.
8. On the Scope or PC, obtain the network addresses for all the connected instruments from the device settings. These addresses will be used to connect the instruments to the GRL automation software.
9. If using the GRL-P1 hardware controller, connect the controller via USB to the GRL automation control enabled Scope or PC.
10. On the Scope or PC, obtain the network address for the connected GRL-P1 from the device settings. For example, if GRL-P1 is connected to the PC, open the Device Manager which should detect the controller as a Controller Serial (COM) Port, e.g. "GRL PCIe34 P1 (COM10)".
11. On the Equipment Setup page of the GRL PCIe Tx Test Application, type in the address of each connected instrument into the "Address" field.

    Then select the "lightning" button ( ) for each connected instrument.

    The "lightning" button should turn green ( ) once the application has successfully established connection with each instrument.

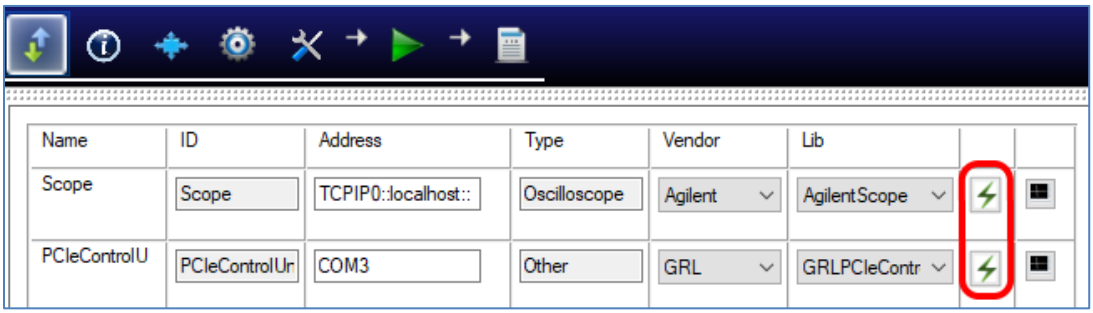



FIGURE 5. CONNECT INSTRUMENTS WITH GRL-PCIE-TX SOFTWARE

13. *(Note: If the GRL-PCIE-TX software is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR.)* If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to omit the Port number from the address. The "lightning" button should turn green if successfully connected to the instrument.

## 3.3 Pre-Configure GRL-PCIE-TX Software before Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced test setup.

### 3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

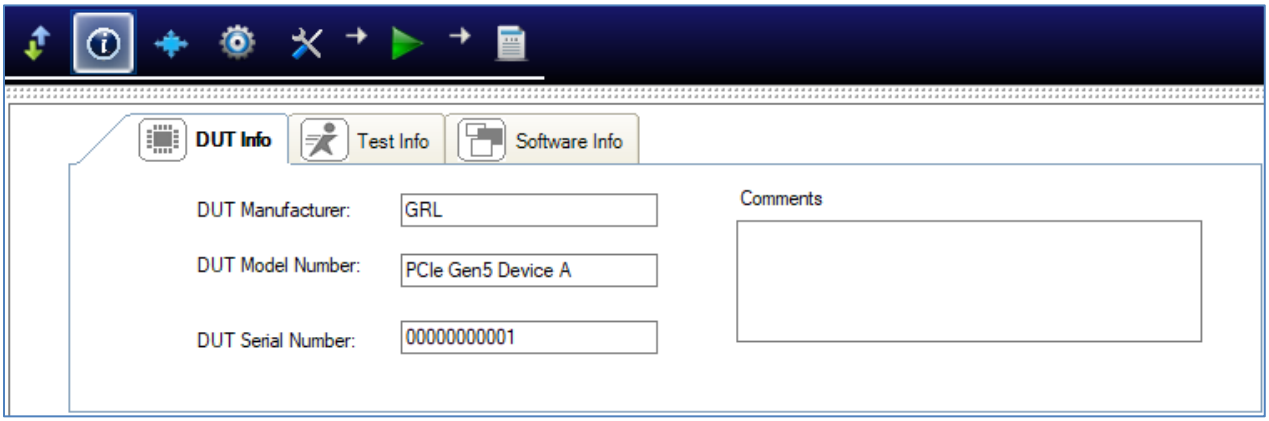



FIGURE 6. SESSION INFO PAGE

### 3.3.2 Set Test Conditions

Select  from the menu to access the **Conditions** page to set the conditions for testing. The software will run tests for the PCIe data lanes, data rates, and preset settings that are selected.

a) **Lane** tab: Select the desired data lanes to be tested.

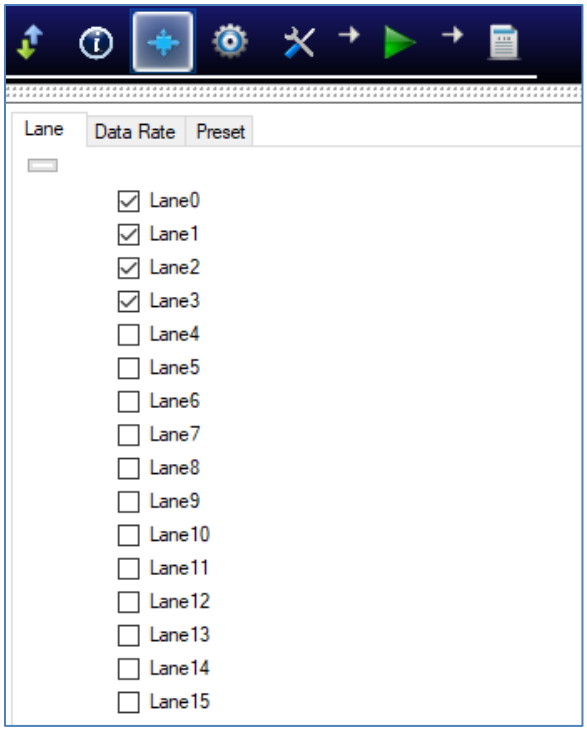



FIGURE 7. SELECT LANE UNDER TEST

b) **Data Rate** tab: Select the desired PCIe data rates for testing.

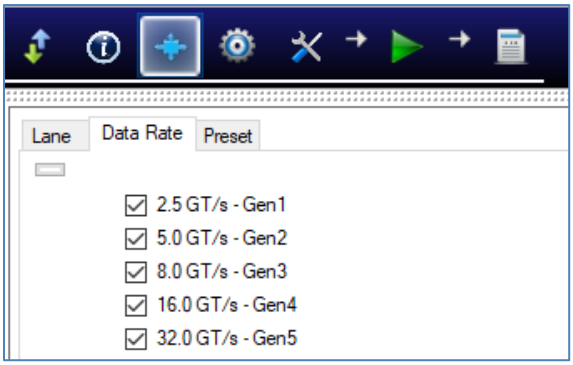



FIGURE 8. SELECT DATA RATES

c) **Preset** tab: Select the pre-defined Tx presets as required for Tx equalization.

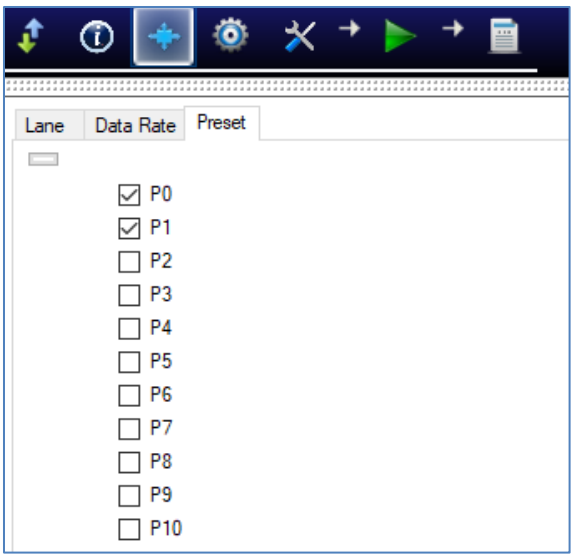



FIGURE 9. SELECT PRESETS

# 4 Testing Using GRL-PCIE-TX

The GRL-PCIE-TX test solution supports automated Tx compliance testing using the SigTest signal quality/de-emphasis and stress tolerance analysis application for PCIe system board and add-in card DUT's. In a typical test environment, the GRL-PCIE-TX automation software is run from the PC/oscilloscope and communicates with the GRL-P1 hardware controller. This enables automation control for the DUT's power and signal quality test sequence, as well as waveform acquisition (for PCIe Gen1, Gen2, Gen3, Gen4 and Gen5). Optionally an arbitrary function generator can also be used as an alternative compliance toggle controller.

The GRL-P1 controller can be connected to either a PCI-SIG compliance load board (CLB) test fixture for the system board DUT or compliance base board (CBB) test fixture for the add-in card DUT. The GRL automation control enabled PC/Scope will send commands to GRL-P1 which controls the power to the DUT and provides a compliance toggle signal to cause the DUT to enter the next compliance state.

The DUT will transmit the test signal to the oscilloscope that is used to validate the test pattern of the signal. The compliance signal will be captured and saved as a waveform file which is then measured for stress tolerance and preset test compliance. In between, an optional RF switch can be used and controlled by the GRL-PCIE-TX software to automate selection of the lane under test. When testing is completed, the software will generate a test report detailing all results from all lanes tested.

## 4.1 GRL-PCIE-TX Advantage

The GRL-PCIE-TX test solution provides a more efficient way to perform PCIe Tx compliance testing rather than using traditional manually-driven methods that are generally both time-consuming and error prone, tying up valuable equipment and resources.

To increase test efficiency, the GRL-P1 controller will first quickly capture waveforms on the oscilloscope. Then using a separate computer, the GRL-PCIE-TX software will run PCIe compliance tests for the waveforms, SigTest signal quality, and de-emphasis.

Through this offline processing of captured waveforms, the oscilloscope can be freed up for other work. The test time can also be further reduced with the software's multi-threading of SigTest. Another advantage is that GRL-P1 can be programmed to automatically capture only the waveforms for the test that the user wants to perform.

## 4.2 Set Up DUT Tx Test with Automation

Once pre-configuration has been completed from Section 3.3, continue with the test setup. The following procedures show how to set up the test environment to perform automated Tx compliance testing for both the System Board and Add-In Card DUT's.

### 4.2.1 Connect Equipment for System Board DUT Test

The connection diagrams below show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe System Board DUT using a GRL automation control enabled Scope and different test controller methods.

#### 4.2.1.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using GRL-P1 with the PCIe Gen 4 & Gen 5 Compliance Load Boards.

##### *4.2.1.1.1 PCIe Gen 4 System Setup*

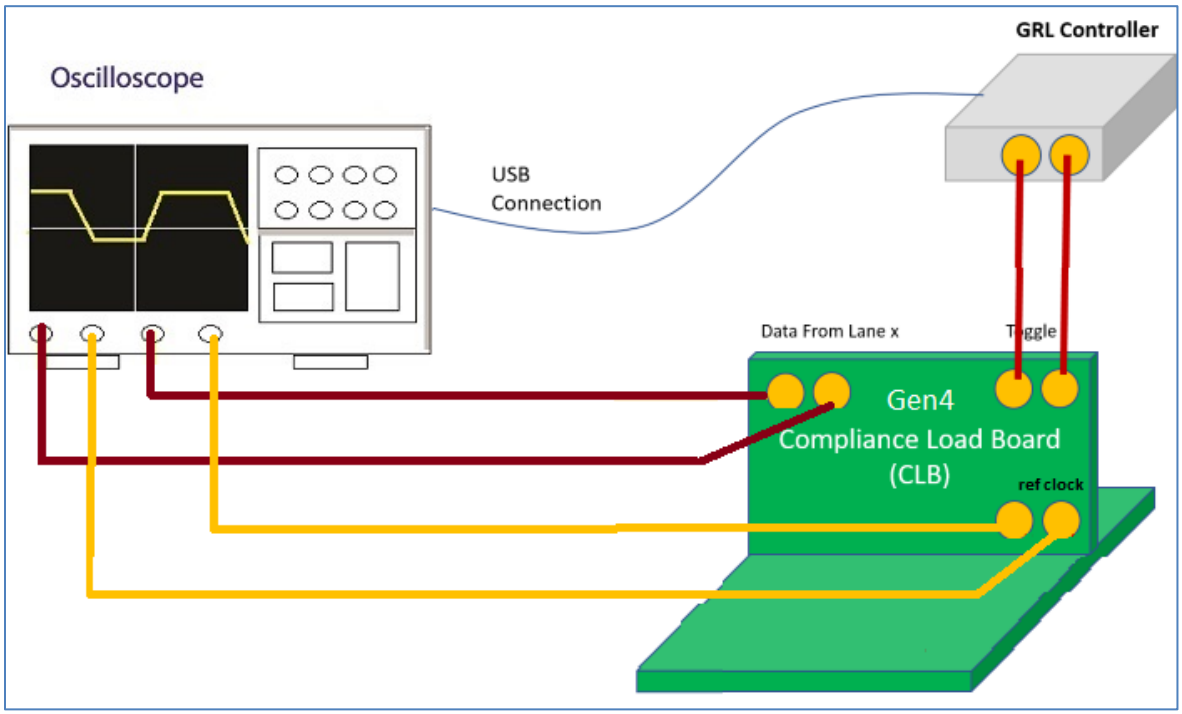



FIGURE 10. CONCEPTUAL PCIE GEN 4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the PCIe Gen 4 Compliance Load Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the PCIe Gen 4 Compliance Load Board to Channel 3 of the Scope.
3. Connect Ref Clk+ from the PCIe Gen 4 Compliance Load Board to Channel 2 of the Scope.
4. Connect Ref Clk- from the PCIe Gen 4 Compliance Load Board to Channel 4 of the Scope.
5. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
6. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
7. Connect GRL-P1 to the Scope using a USB cable.

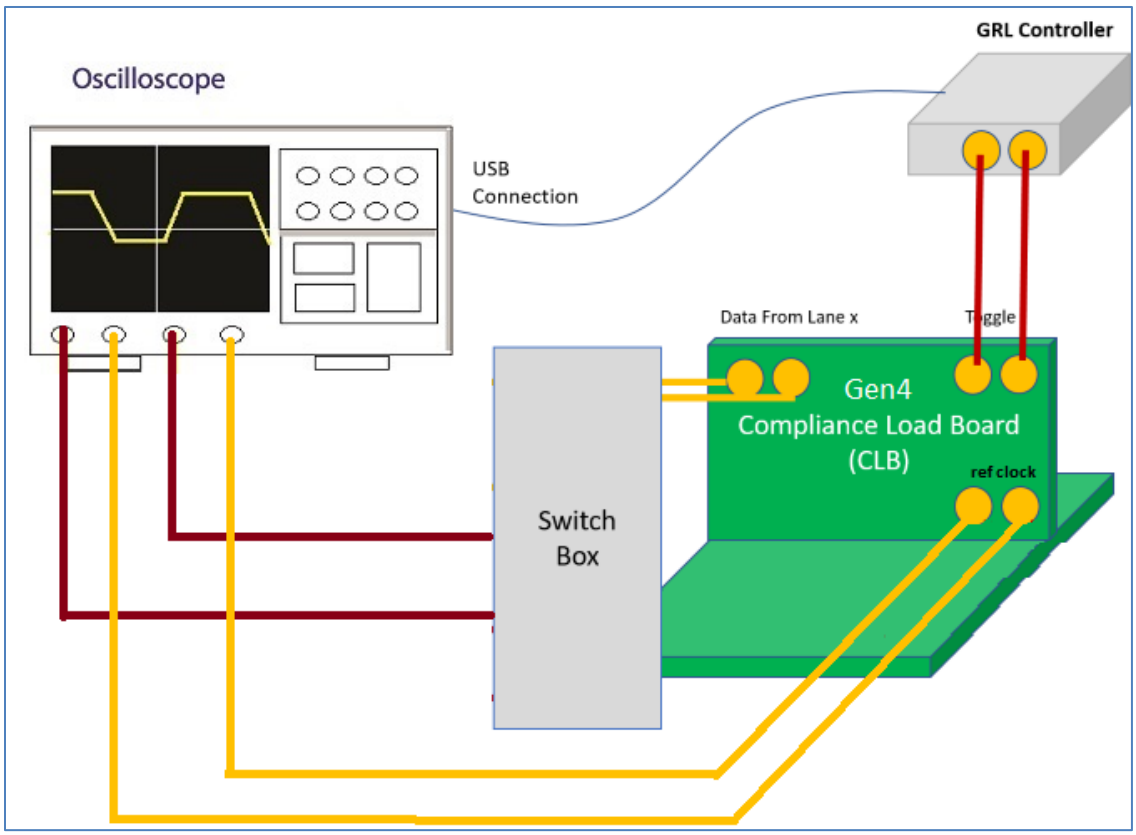



FIGURE 11. CONCEPTUAL PCIE GEN 4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the PCIe Gen 4 Compliance Load Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the PCIe Gen 4 Compliance Load Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.
5. Connect Ref Clk+ from the PCIe Gen 4 Compliance Load Board to Channel 2 of the Scope.
6. Connect Ref Clk- from the PCIe Gen 4 Compliance Load Board to Channel 4 of the Scope.
7. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
8. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
9. Connect GRL-P1 to the Scope using a USB cable.

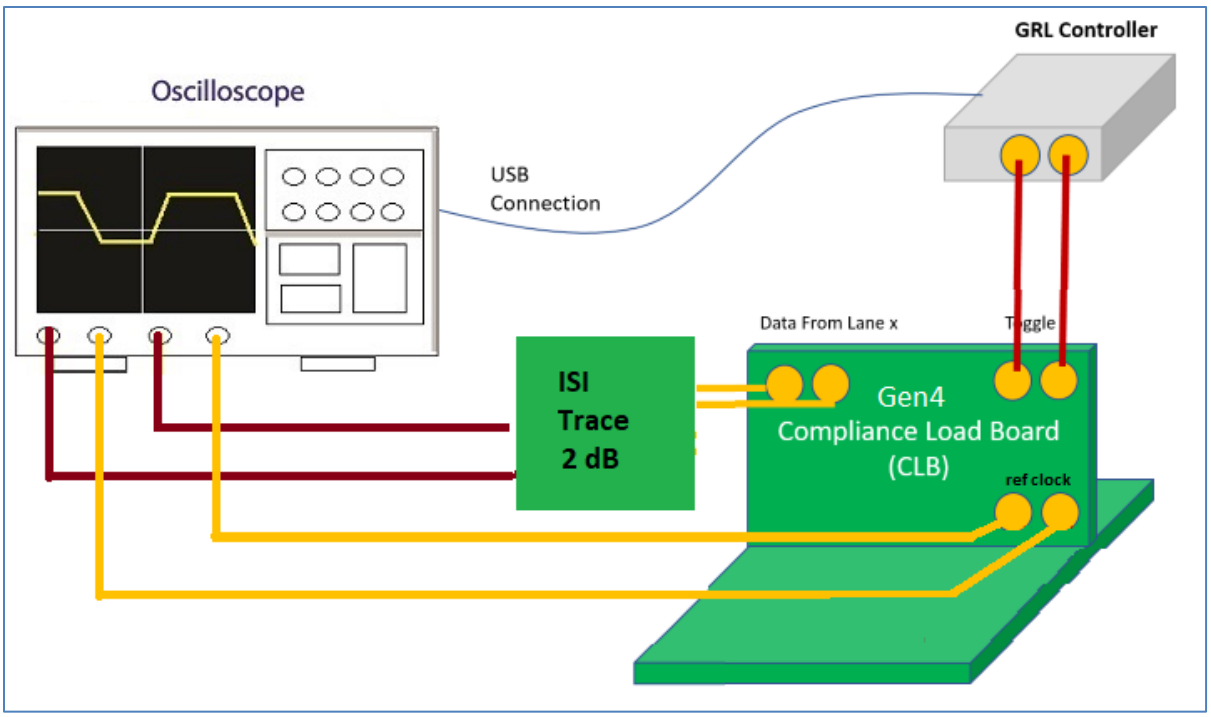



FIGURE 12. CONCEPTUAL PCIE GEN 4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ and Tx- from the PCIe Gen 4 Compliance Load Board to a ISI Channel (2 dB ISI trace).
2. Connect the ISI Channel to Channels 1 and 3 of the Scope.
3. Connect Ref Clk+ from the PCIe Gen 4 Compliance Load Board to Channel 2 of the Scope.
4. Connect Ref Clk- from the PCIe Gen 4 Compliance Load Board to Channel 4 of the Scope.
5. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
6. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
7. Connect GRL-P1 to the Scope using a USB cable.

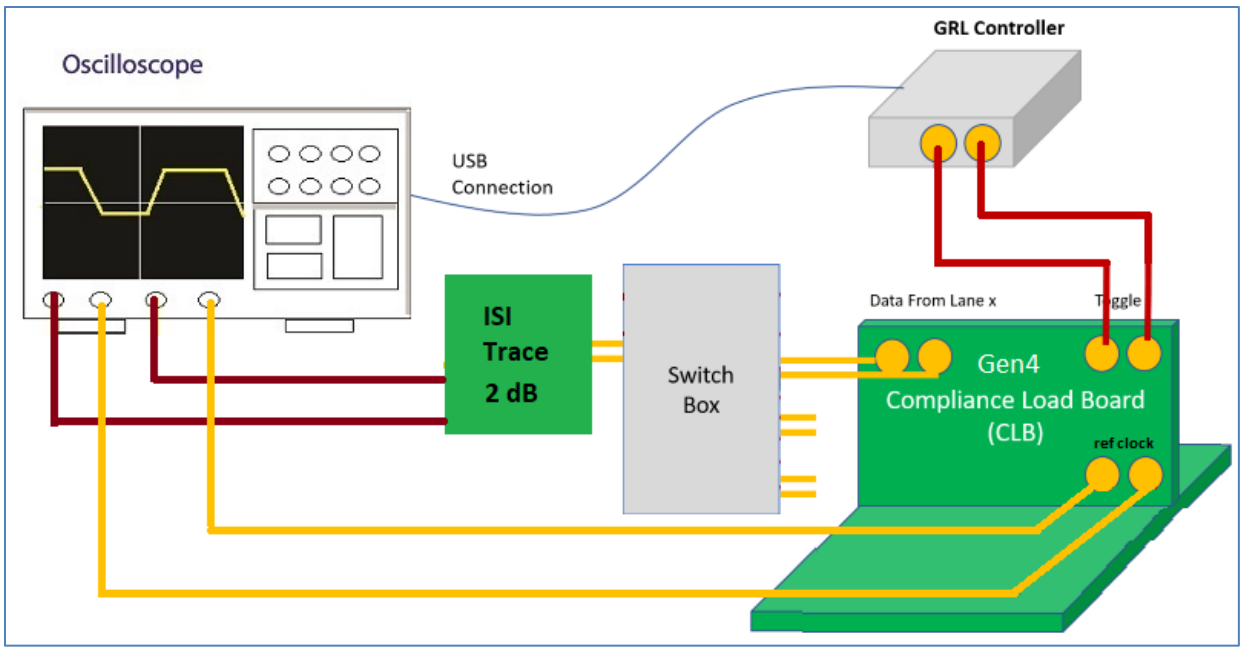



FIGURE 13. CONCEPTUAL PCIE GEN 4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITH RF SWITCH)

1. Connect Tx+ and Tx- Data Lanes from the PCIe Gen 4 Compliance Load Board to the RF Switch Input.
2. Connect Output+ and Output- from the RF Switch to a ISI Channel (2 dB ISI trace).
3. Connect the ISI Channel to Channels 1 and 3 of the Scope.
4. Connect Ref Clk+ from the PCIe Gen 4 Compliance Load Board to Channel 2 of the Scope.
5. Connect Ref Clk- from the PCIe Gen 4 Compliance Load Board to Channel 4 of the Scope.
6. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
7. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
8. Connect GRL-P1 to the Scope using a USB cable.

#### *4.2.1.1.2 PCIe Gen 5 System Setup*

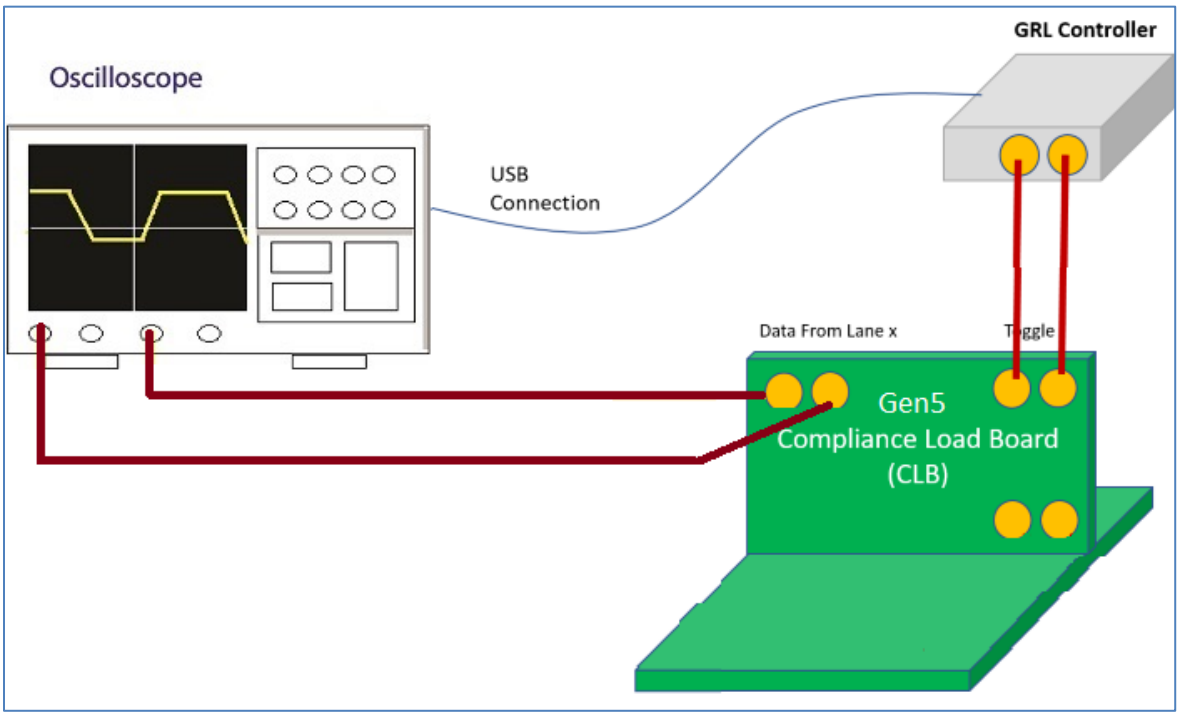



FIGURE 14. CONCEPTUAL PCIE GEN 5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the PCIe Gen 5 Compliance Load Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the PCIe Gen 5 Compliance Load Board to Channel 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

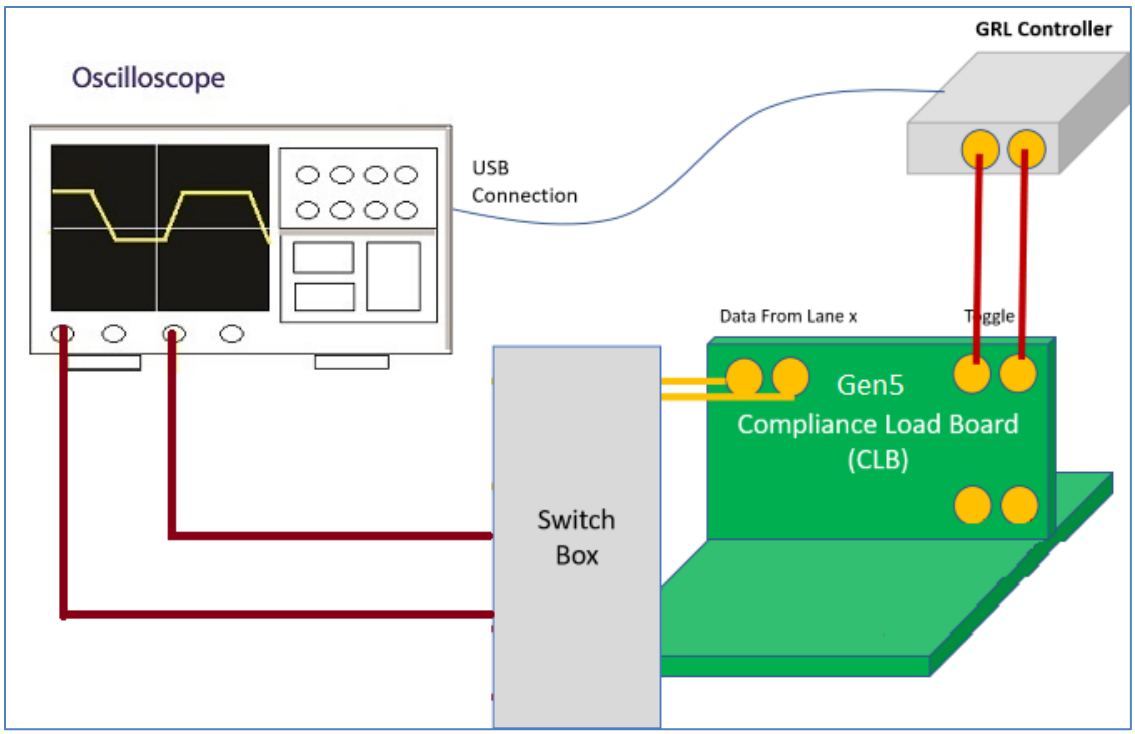



FIGURE 15. CONCEPTUAL PCIE GEN 5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the PCIe Gen 5 Compliance Load Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the PCIe Gen 5 Compliance Load Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.
5. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
6. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
7. Connect GRL-P1 to the Scope using a USB cable.

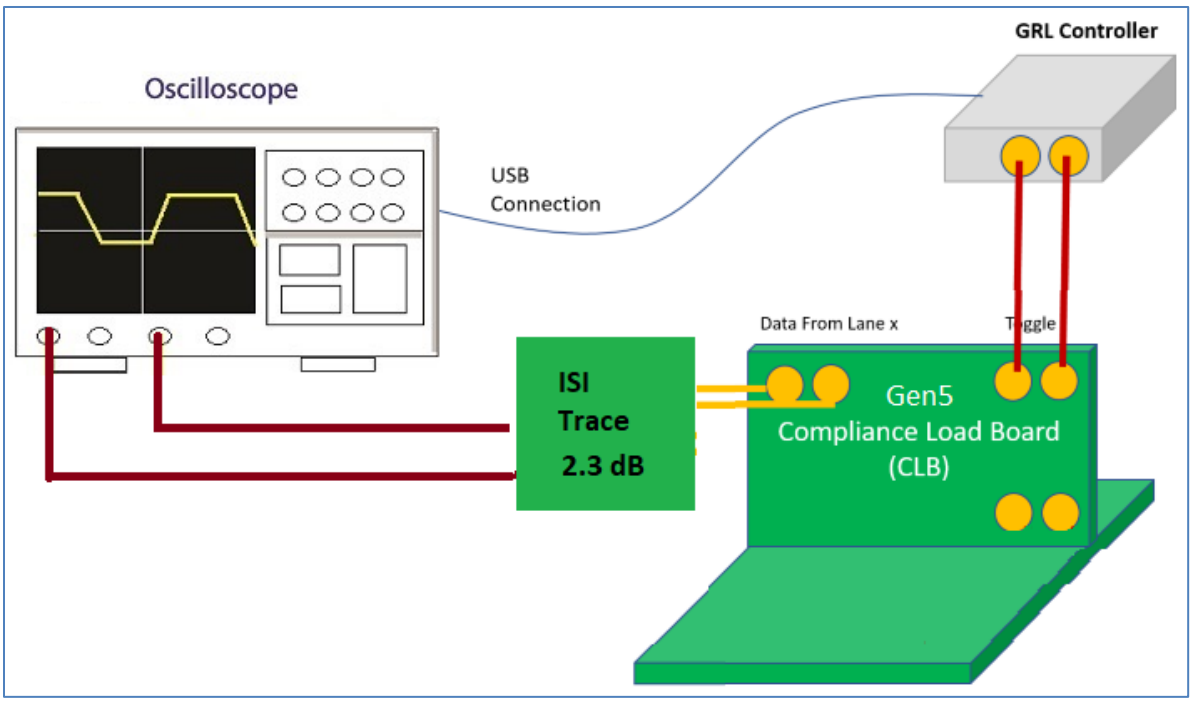



FIGURE 16. CONCEPTUAL PCIE GEN 5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ and Tx- from the PCIe Gen 5 Compliance Load Board to a ISI Channel (2.3 dB ISI trace).
2. Connect the ISI Channel to Channels 1 and 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

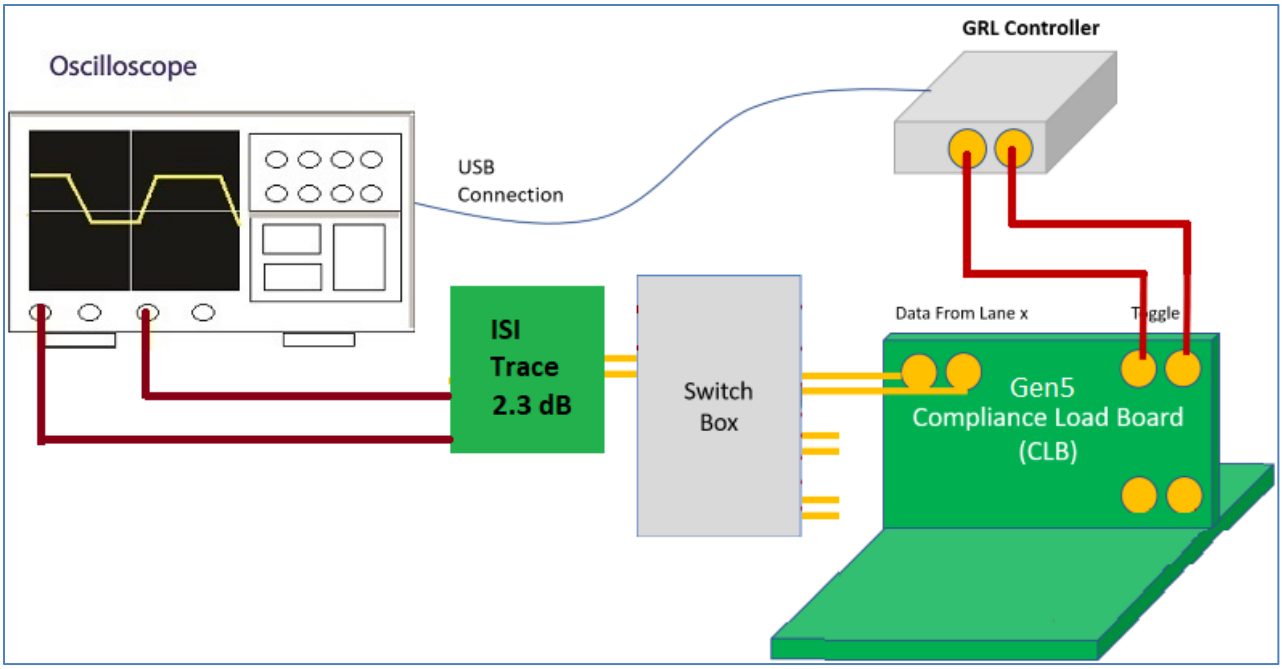



FIGURE 17. CONCEPTUAL PCIE GEN 5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITH RF SWITCH)

1. Connect Tx+ and Tx- Data Lanes from the PCIe Gen 5 Compliance Load Board to the RF Switch Input.
2. Connect Output+ and Output- from the RF Switch to a ISI Channel (2.3 dB ISI trace).
3. Connect the ISI Channel to Channels 1 and 3 of the Scope.
4. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
5. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
6. Connect GRL-P1 to the Scope using a USB cable.

#### 4.2.1.2 Setup Using Manual Compliance Toggle

The following diagrams describe how to connect the equipment if not using any controller with the PCIe Gen 3 Compliance Load Board. *Note: With no controller connected, the compliance toggle must be initiated manually by pressing the compliance toggle button on the Compliance Load Board.*

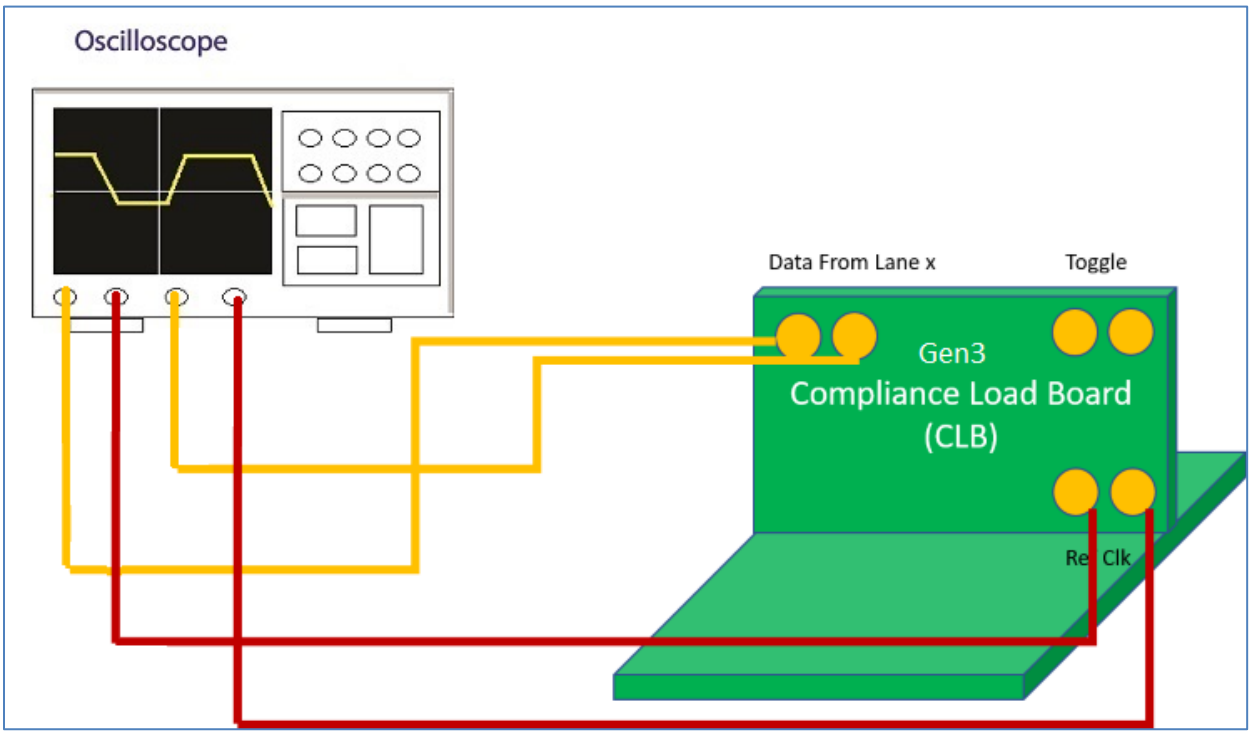



FIGURE 18. CONCEPTUAL PCIE GEN 3 SYSTEM BOARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the PCIe Gen 3 Compliance Load Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the PCIe Gen 3 Compliance Load Board to Channel 3 of the Scope.
3. Connect Ref Clk+ from the PCIe Gen 3 Compliance Load Board to Channel 2 of the Scope.
4. Connect Ref Clk- from the PCIe Gen 3 Compliance Load Board to Channel 4 of the Scope.

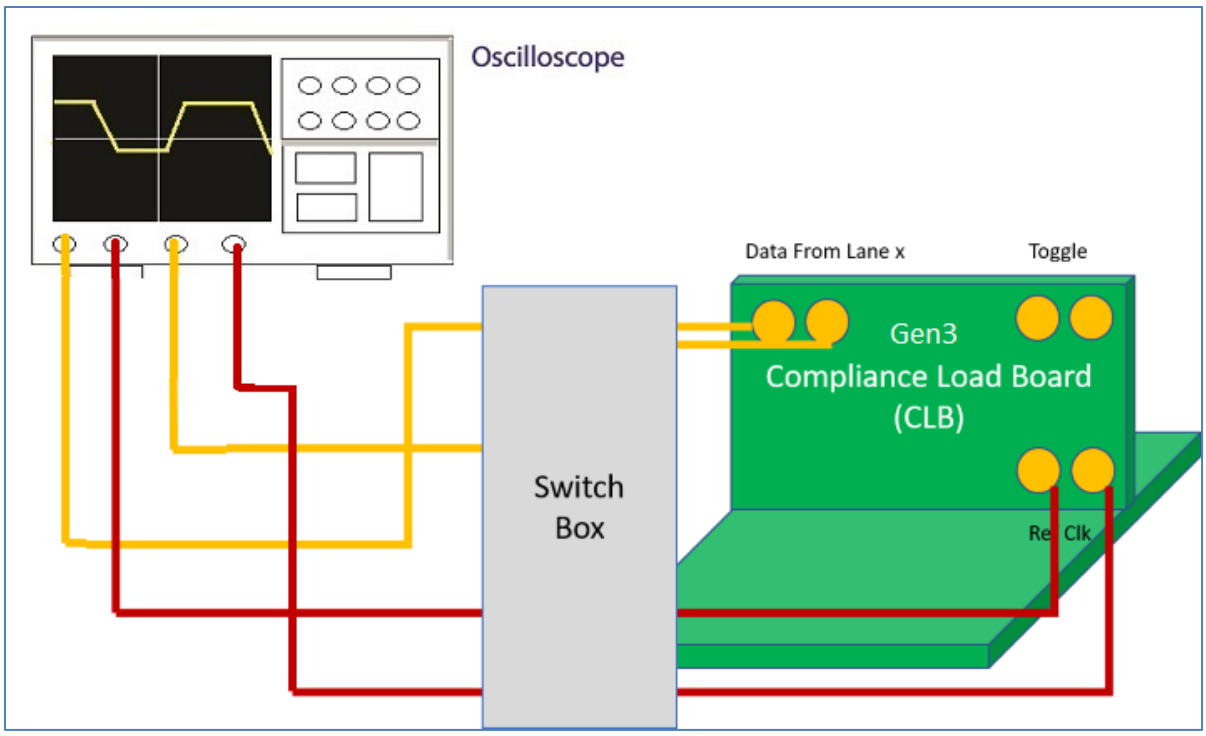



FIGURE 19. CONCEPTUAL PCIE GEN 3 SYSTEM BOARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the PCIe Gen 3 Compliance Load Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the PCIe Gen 3 Compliance Load Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.
5. Connect Ref Clk+ from the PCIe Gen 3 Compliance Load Board to Channel 2 of the Scope.
6. Connect Ref Clk- from the PCIe Gen 3 Compliance Load Board to Channel 4 of the Scope.

### 4.2.2 Connect Equipment for Add-In Card DUT Test

The following connection diagrams show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe Add-In Card DUT using a GRL automation control enabled Scope and different test controller methods.

#### 4.2.2.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using GRL-P1 with the PCIe Gen 4 & Gen 5 Compliance Base Boards.

##### *4.2.2.1.1 PCIe Gen 4 Add-In Card Setup*

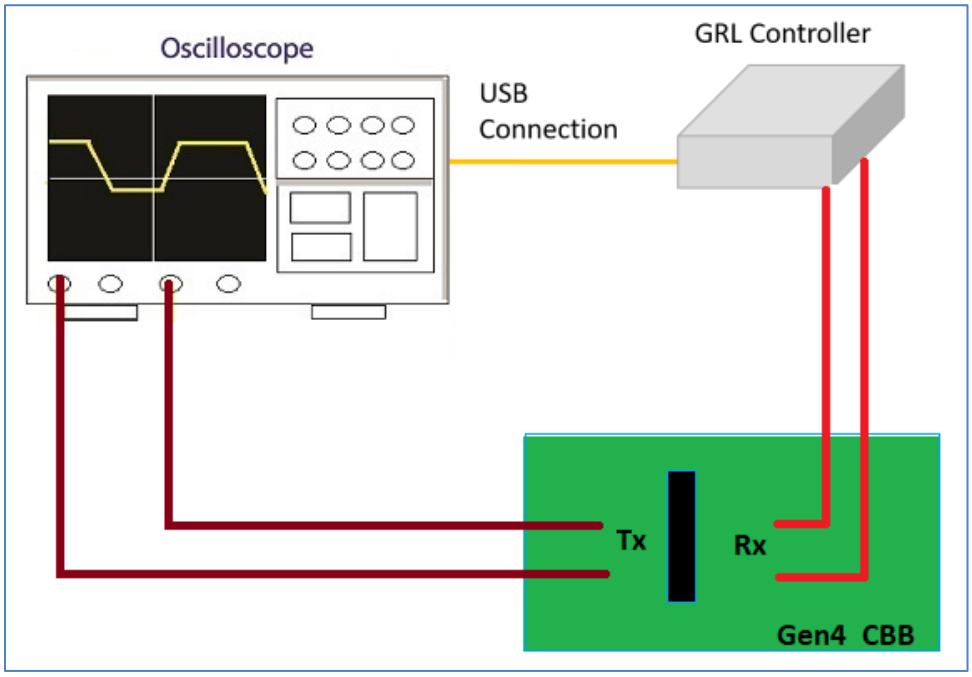



FIGURE 20. CONCEPTUAL PCIE GEN 4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the PCIe Gen 4 Compliance Base Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the PCIe Gen 4 Compliance Base Board to Channel 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

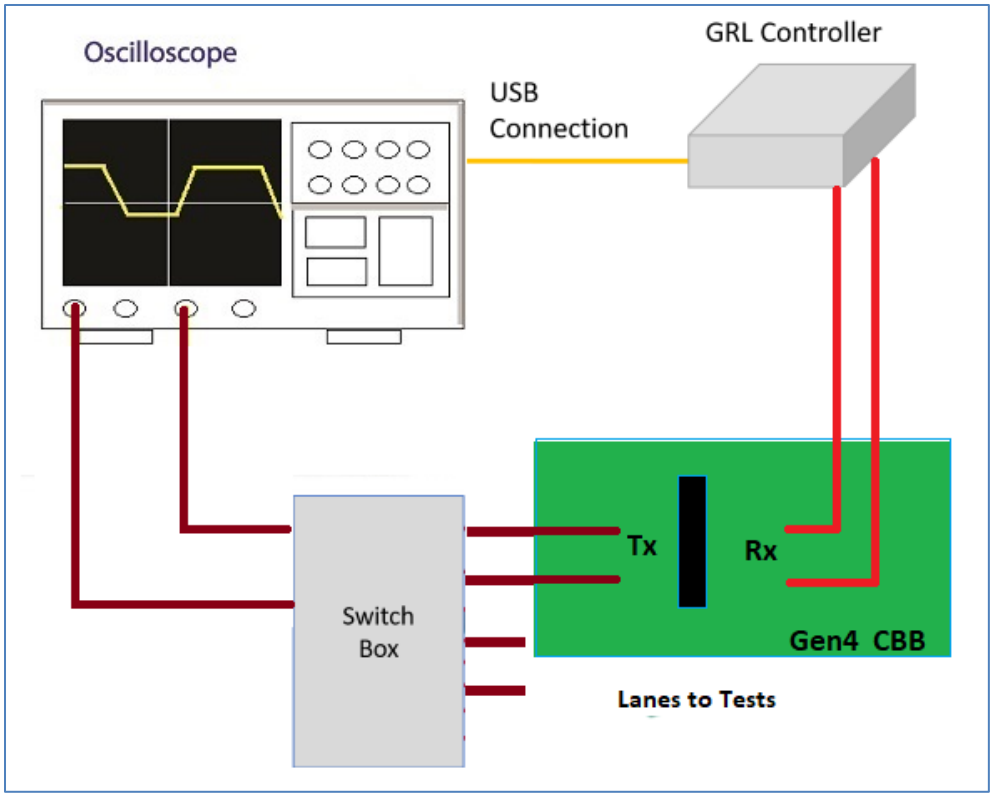



FIGURE 21. CONCEPTUAL PCIE GEN 4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the PCIe Gen 4 Compliance Base Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the PCIe Gen 4 Compliance Base Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.
5. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
6. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
7. Connect GRL-P1 to the Scope using a USB cable.

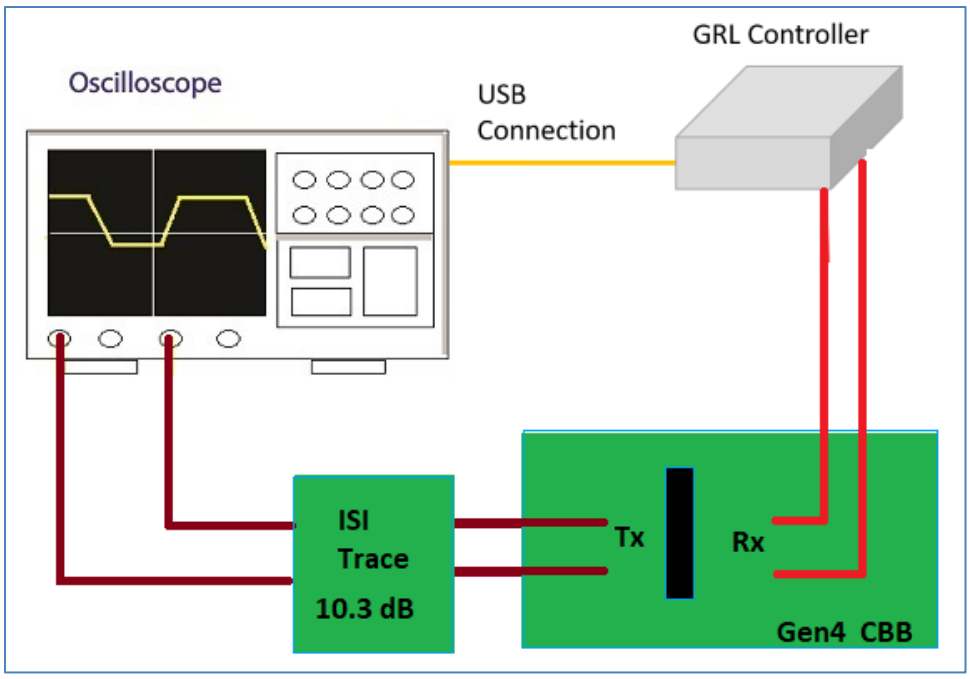



FIGURE 22. CONCEPTUAL PCIE GEN 4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ and Tx- from the PCIe Gen 4 Compliance Base Board to a ISI Channel (10.3 dB ISI trace).
2. Connect the ISI Channel to Channels 1 and 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

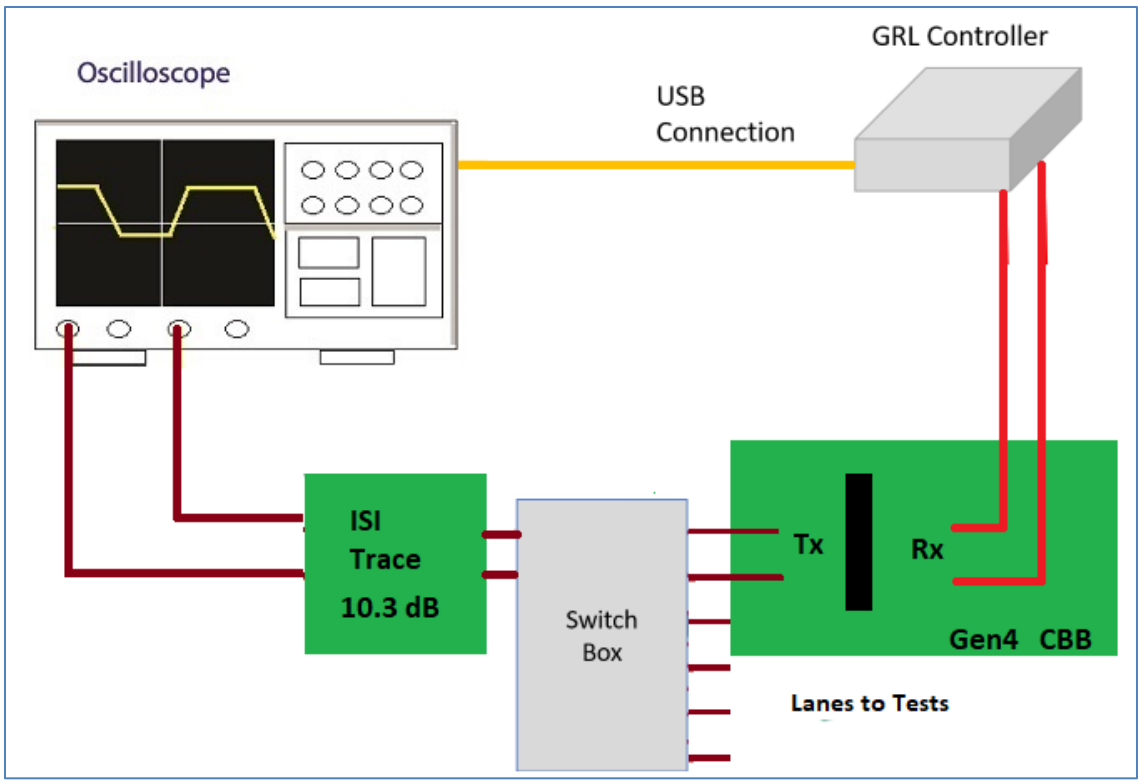



FIGURE 23. CONCEPTUAL PCIE GEN 4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITH RF SWITCH)

1. Connect Tx+ and Tx- Data Lanes from the PCIe Gen 4 Compliance Base Board to the RF Switch Input.
2. Connect Output+ and Output- from the RF Switch to a ISI Channel (10.3 dB ISI trace).
3. Connect the ISI Channel to Channels 1 and 3 of the Scope.
4. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
5. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
6. Connect GRL-P1 to the Scope using a USB cable.

#### *4.2.2.1.2 PCIe Gen 5 Add-In Card Setup*

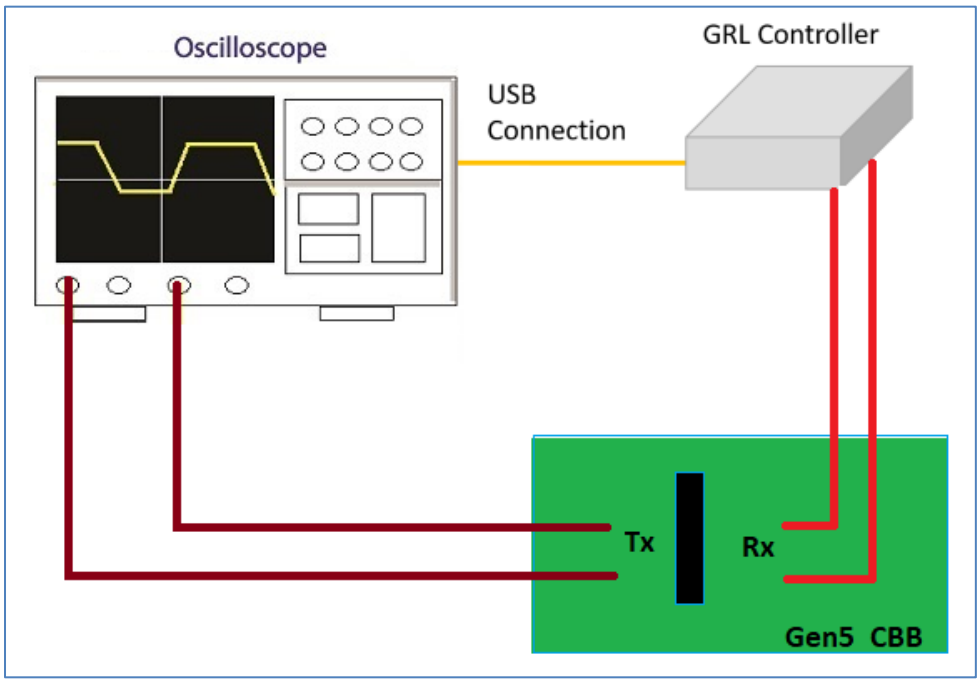



FIGURE 24. CONCEPTUAL PCIE GEN 5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the PCIe Gen 5 Compliance Base Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the PCIe Gen 5 Compliance Base Board to Channel 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

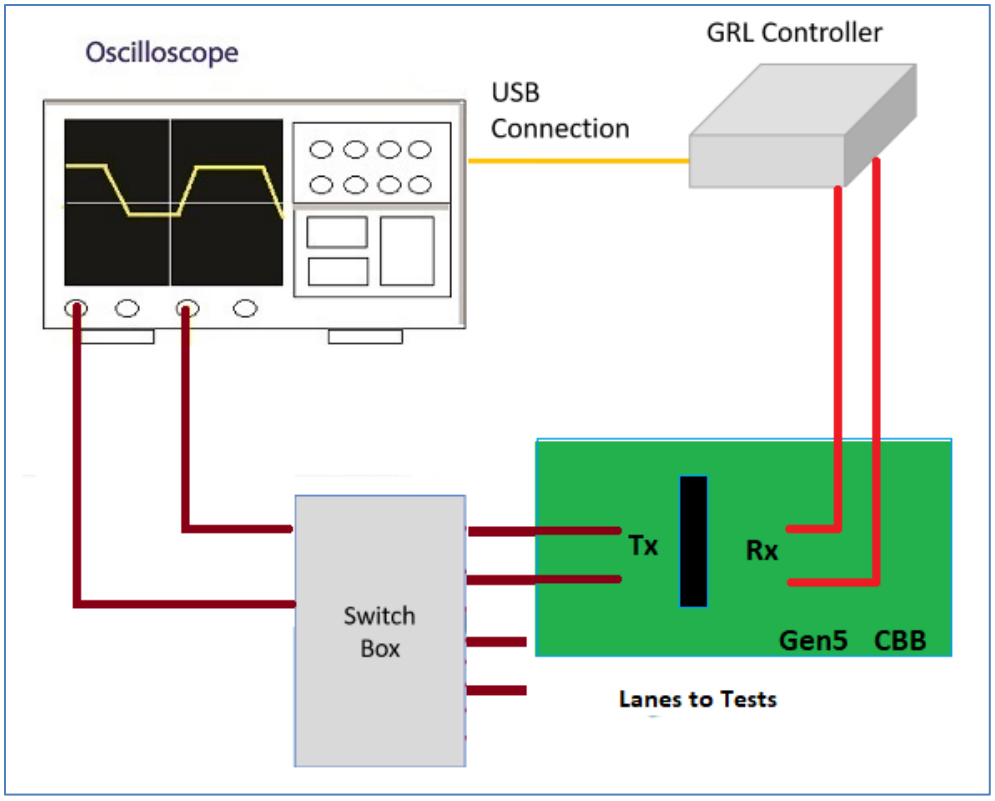



FIGURE 25. CONCEPTUAL PCIE GEN 5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the PCIe Gen 5 Compliance Base Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the PCIe Gen 5 Compliance Base Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.
5. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
6. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
7. Connect GRL-P1 to the Scope using a USB cable.

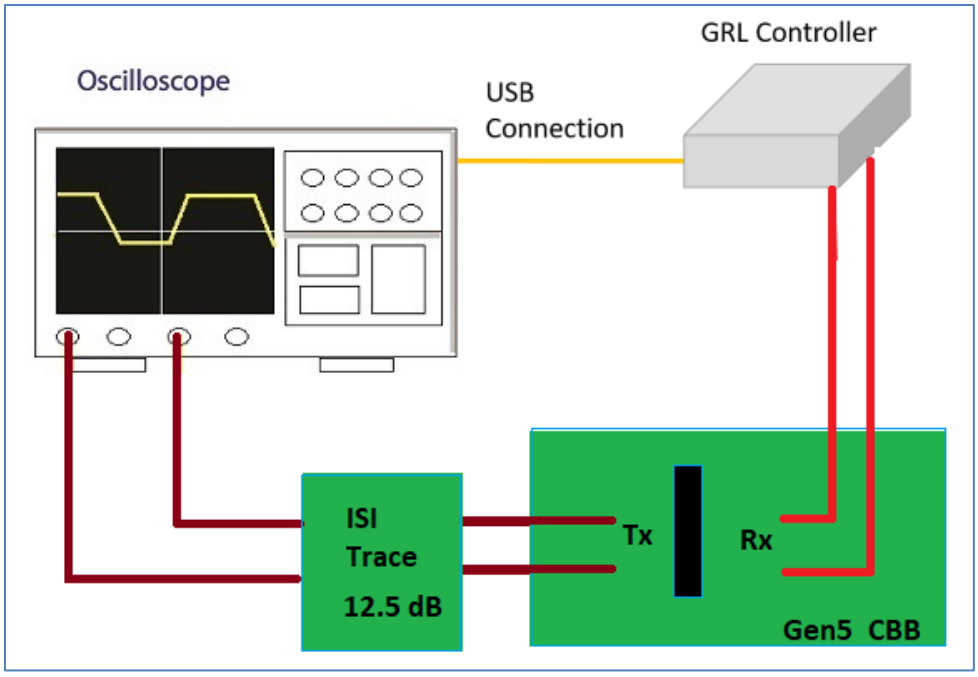



FIGURE 26. CONCEPTUAL PCIE GEN 5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ and Tx- from the PCIe Gen 5 Compliance Base Board to a ISI Channel (12.5 dB ISI trace).
2. Connect the ISI Channel to Channels 1 and 3 of the Scope.
3. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
4. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
5. Connect GRL-P1 to the Scope using a USB cable.

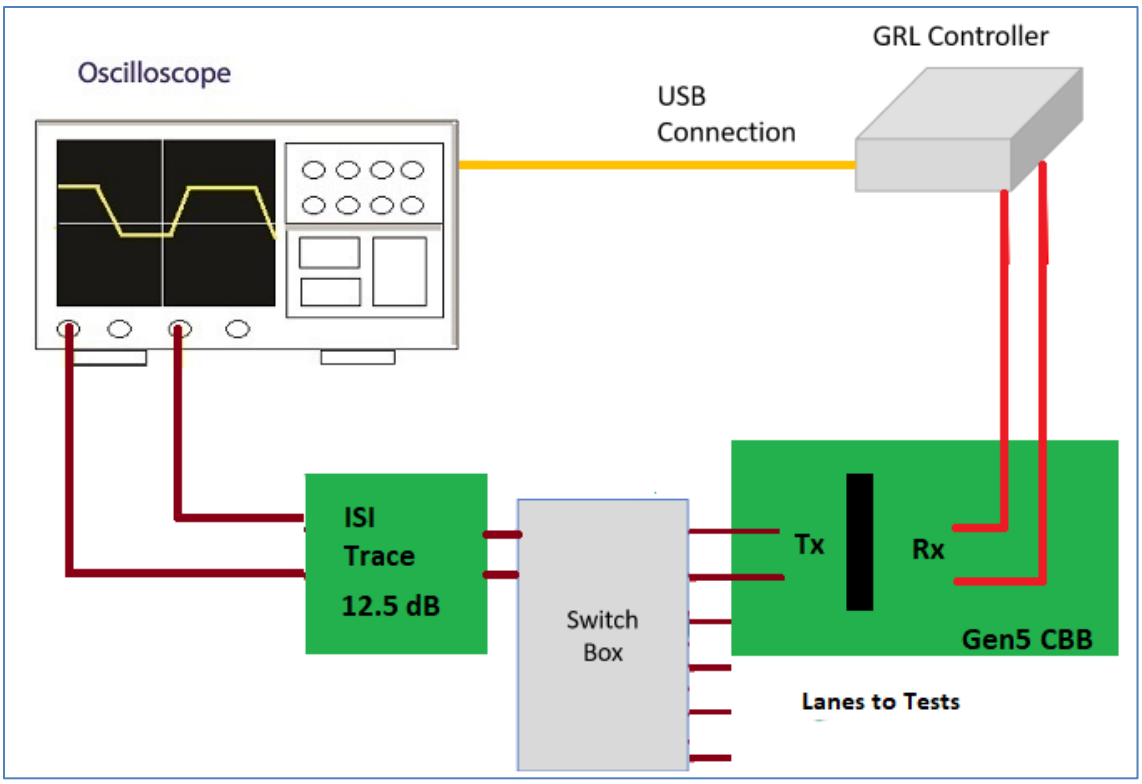



FIGURE 27. CONCEPTUAL PCIE GEN 5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 WITH ISI CHANNEL (WITH RF SWITCH)

1. Connect Tx+ and Tx- Data Lanes from the PCIe Gen 5 Compliance Base Board to the RF Switch Input.
2. Connect Output+ and Output- from the RF Switch to a ISI Channel (12.5 dB ISI trace).
3. Connect the ISI Channel to Channels 1 and 3 of the Scope.
4. Connect Rx+ from the Riser Board to the GRL-P1 Output 1.
5. Connect Rx- from the Riser Board to the GRL-P1 Output 2.
6. Connect GRL-P1 to the Scope using a USB cable.

#### 4.2.2.2 Setup Using Manual Compliance Toggle

The following diagrams describe how to connect the equipment if not using any controller.
*Note: With no controller connected, the compliance toggle must be initiated manually by pressing the compliance toggle button on the Compliance Base Board.*

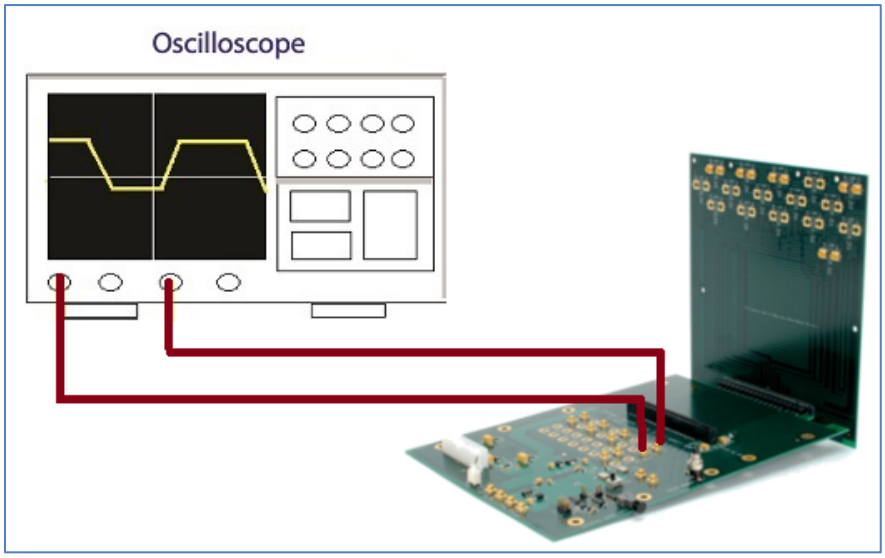



FIGURE 28. CONCEPTUAL PCIE ADD-IN CARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITHOUT RF SWITCH)

1. Connect Data Lane 0's Tx+ from the Compliance Base Board to Channel 1 of the Scope.
2. Connect Data Lane 0's Tx- from the Compliance Base Board to Channel 3 of the Scope.

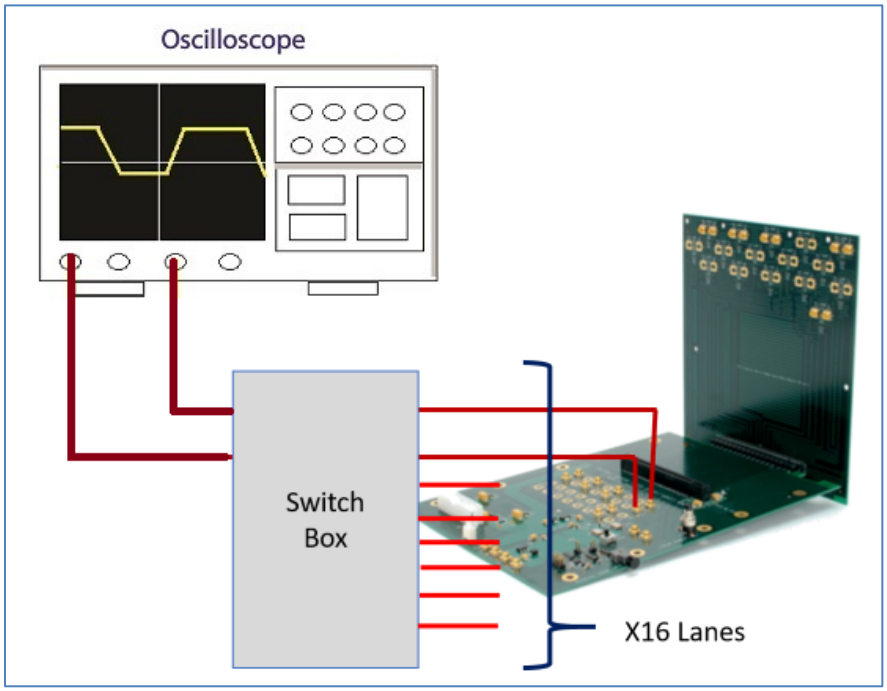



FIGURE 29. CONCEPTUAL PCIE ADD-IN CARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITH RF SWITCH)

1. Connect Tx+ Data Lanes from the Compliance Base Board to the RF Switch Input.
2. Connect Tx- Data Lanes from the Compliance Base Board to the RF Switch Input.
3. Connect Output+ from the RF Switch to Channel 1 of the Scope.
4. Connect Output- from the RF Switch to Channel 3 of the Scope.

### 4.2.3 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL PCIe Tx Test Application menu to access the Setup Configuration page. Select the DUT to be tested, set up and run SigTest, and set up waveform processing to be applied for testing.

a) **Device Type** tab: Select to use either a PCIe System Board or Add-In Card as the DUT.

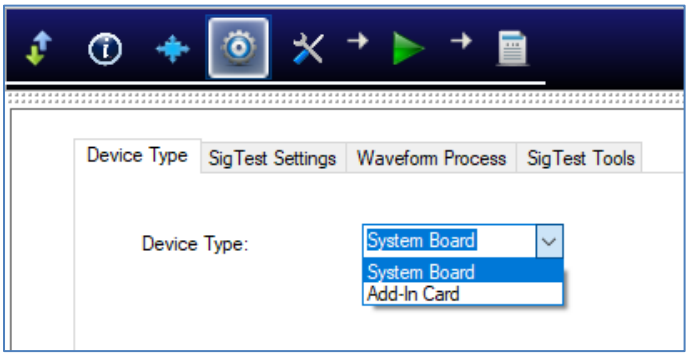



FIGURE 30. SELECT DUT TYPE

b) **SigTest Settings** tab:

- *PCIE Gen1 (2.5Gb/s), Gen2 (5Gb/s) and Gen3 (8Gb/s)* – Select to run either the pre-defined Version "3.2.0.3" or a "Custom" Version of the SigTest. If "Custom" is selected, enter the Version number of the Custom SigTest and also make sure that the SigTest is already installed in the system.
- *PCIE Gen4 (16Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.
- *PCIE Gen5 (32Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.

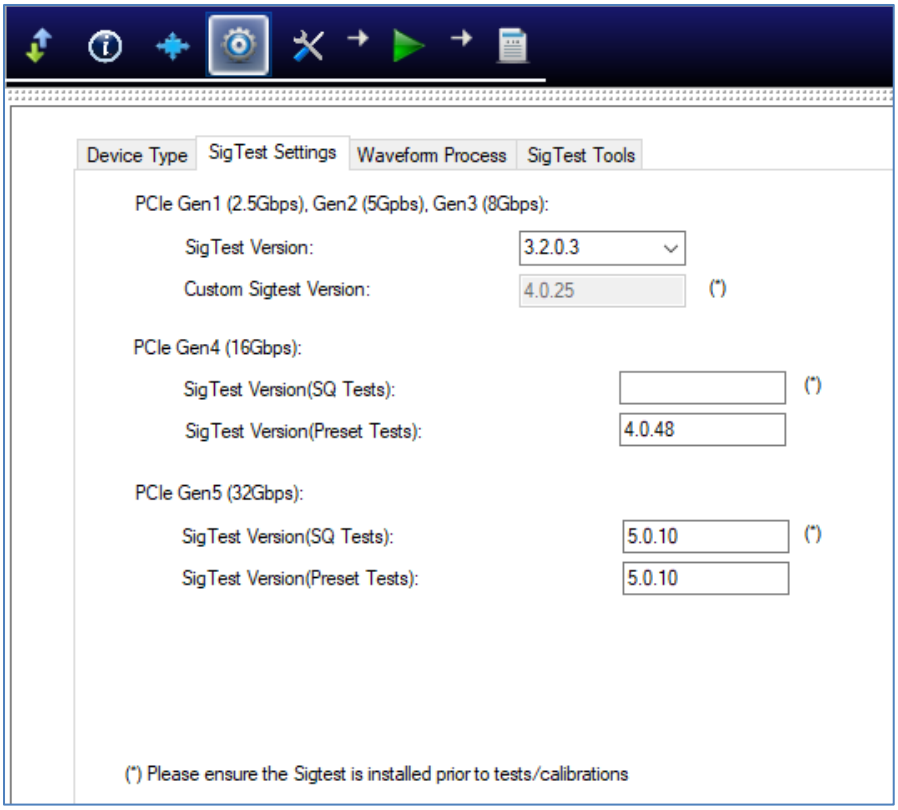



FIGURE 31. SET UP SIGTEST

c) **Waveform Process** tab: Select "Live Capture" to acquire PCIe waveforms by the software, or select "Process Pre-captured waveforms" to use existing waveforms that have been previously captured and saved for analysis. *Note that selecting "Process Pre-captured waveforms" will remove the "Waveform Acquisition" group from the Select Tests page. See Section 4.2.4.1.*

If "Process Pre-captured waveforms" is selected, enter the directory of the saved waveform file in the Pre-Captured Waveform Path field.

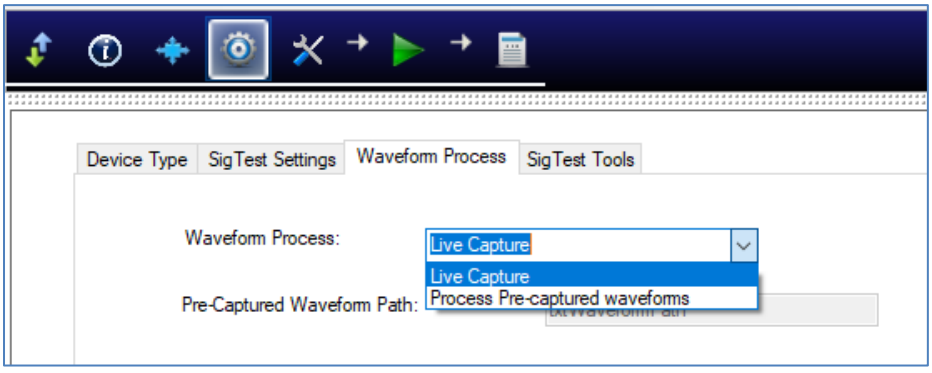



FIGURE 32. SET UP WAVEFORM PROCESSING

### 4.2.4 Select Compliance Tests

Once test requirements are defined, select **Test List** from the top "Windows" drop-down menu to display and access all tests available for the selected DUT type. User can select any of these tests to perform DUT compliance testing for all PCIe parameters.

*Note: The Select Tests page will only list DUT-specific tests. For example, if System Board is selected as the DUT, only those tests applicable for System Board will be shown. Other test parameters such as desired data rates and presets that were previously configured may also affect the test selection.*

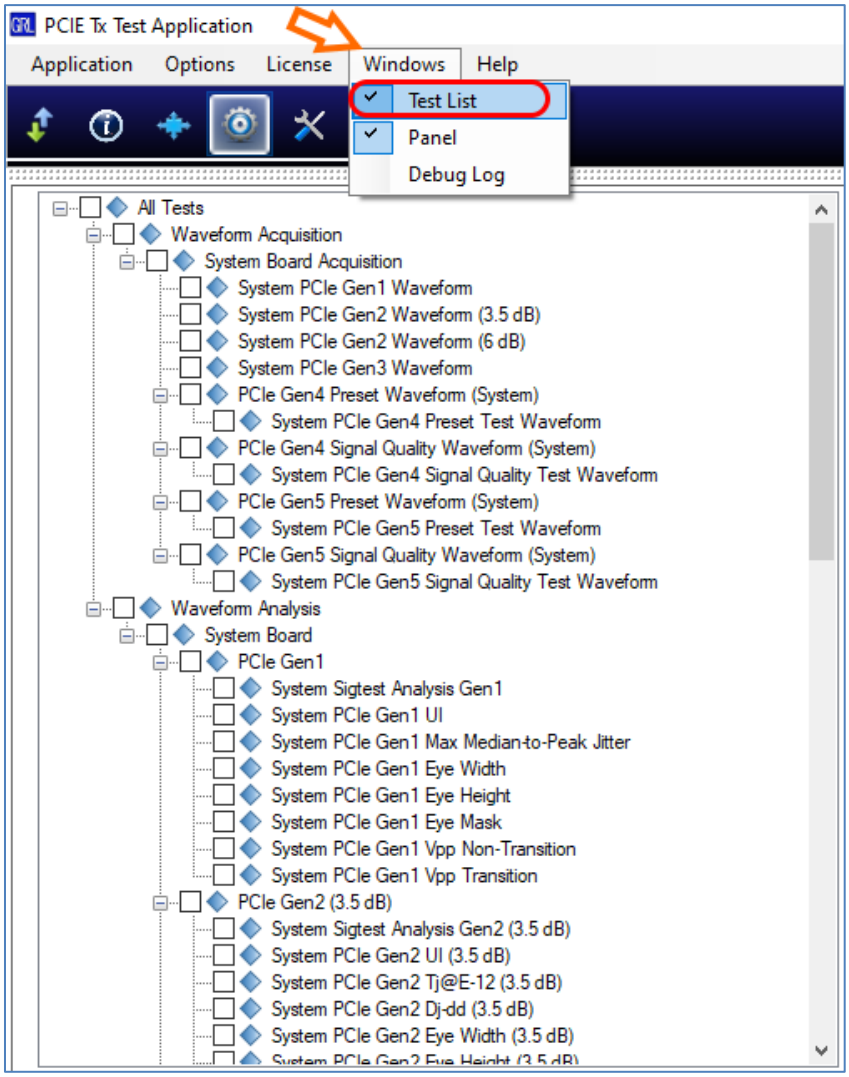



FIGURE 33. SELECT TESTS PAGE

#### 4.2.4.1 Select to Acquire Waveforms

Under "Waveform Acquisition", select the waveforms to capture for the required PCIe data rates. The software will run a live capture of the selected waveforms prior to analysis.

*Note: Waveform Acquisition can only be selected if "Live Capture" is set under the Waveform Process tab on the Setup Configuration page. See Section 4.2.3.*

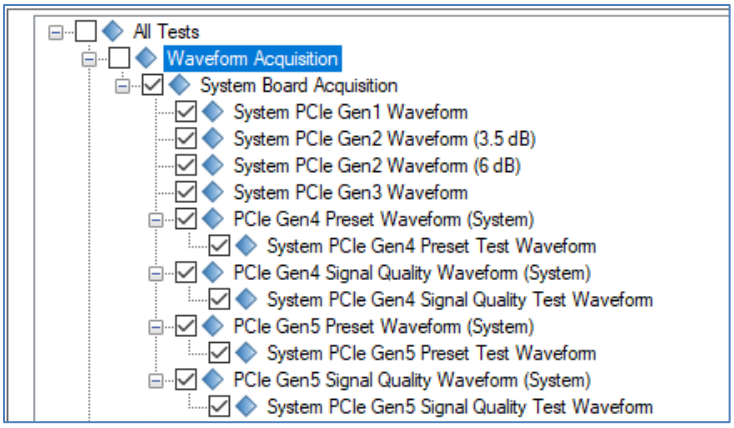



FIGURE 34. SELECT WAVEFORM TO CAPTURE

#### 4.2.4.2 Select Waveform Analysis Tests

Under "Waveform Analysis", select to perform the SigTest analysis, jitter and eye measurements, and preset test for the applicable PCIe waveform. The software will automatically run the selected tests when initiated.

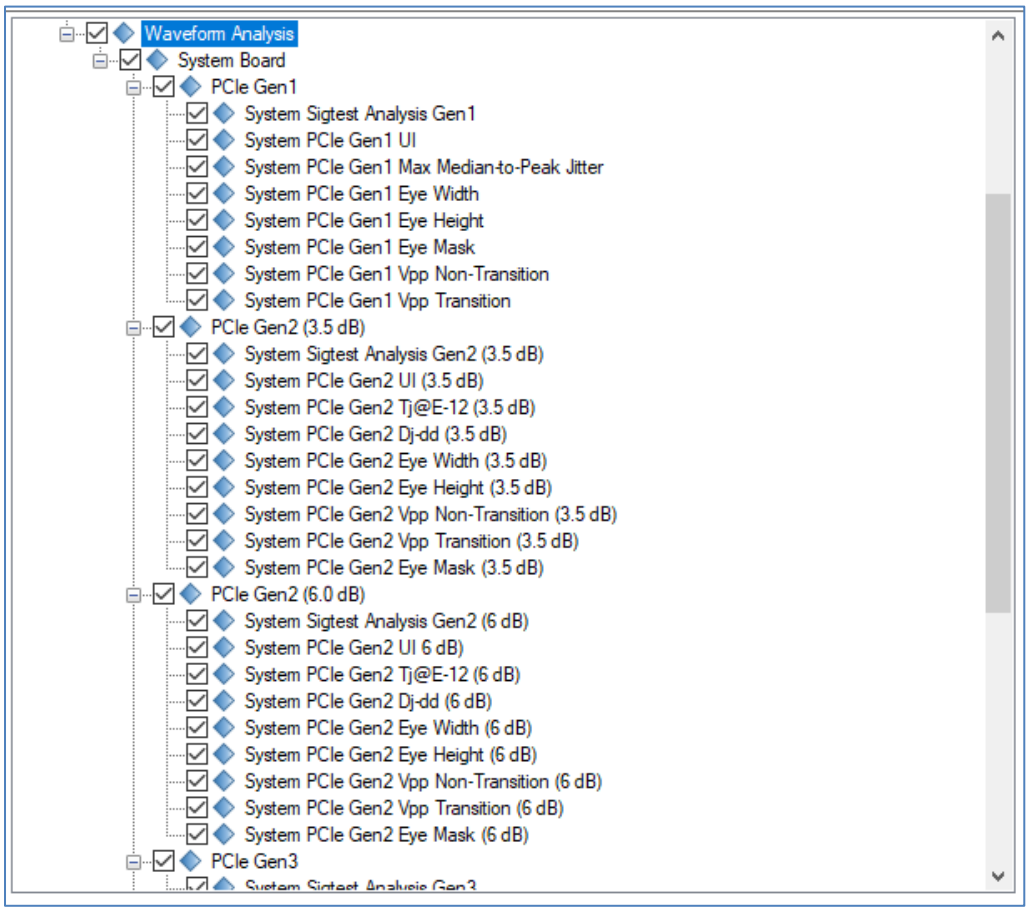



FIGURE 35. SELECT WAVEFORM ANALYSIS TESTS

### 4.2.5 Configure Test Parameters

After selecting the desired tests, select  from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.

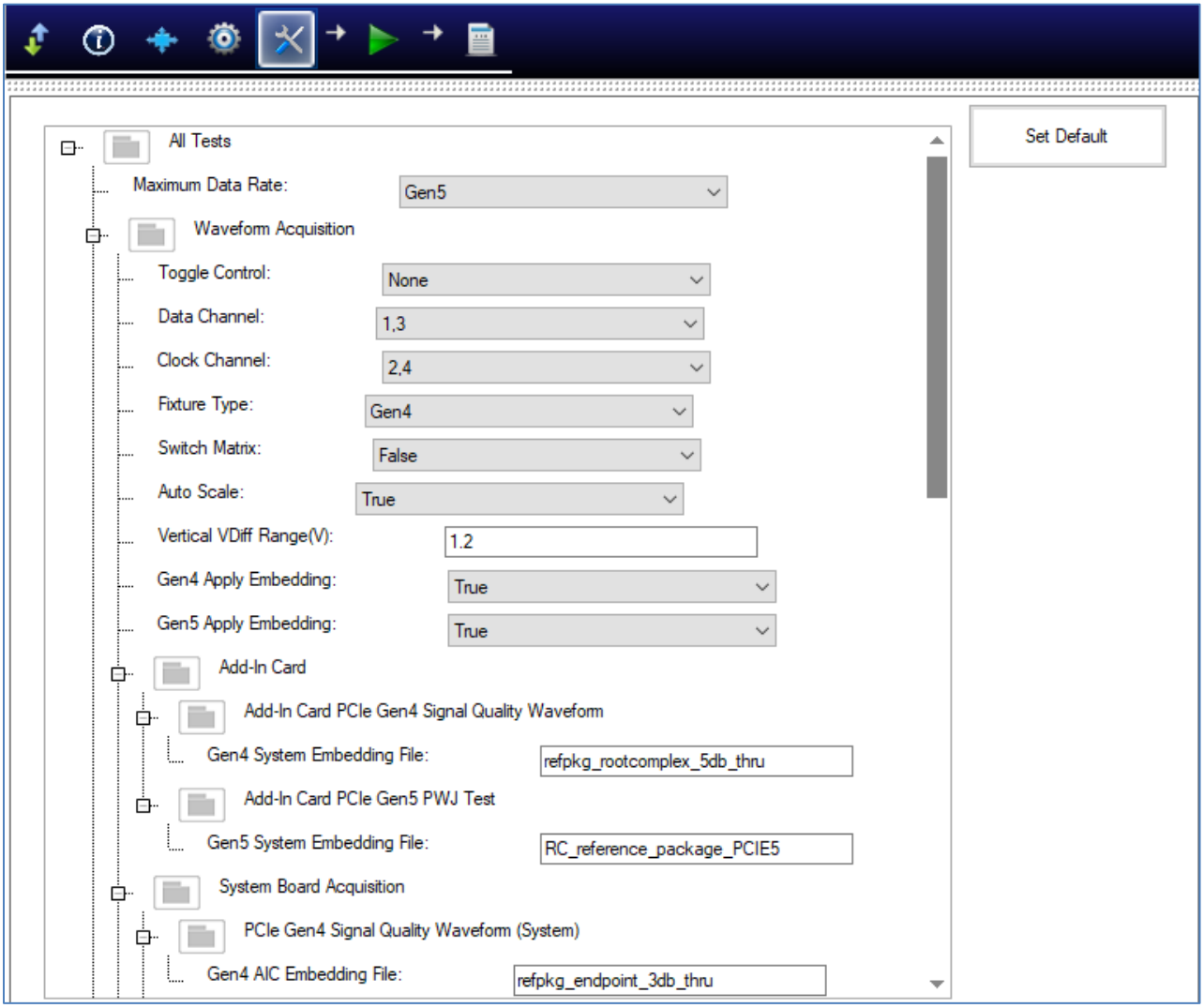



FIGURE 36. TEST PARAMETERS CONFIGURATION PAGE

TABLE 4. TEST PARAMETERS DESCRIPTION

| Parameter | Description |
|---|---|
| **Maximum Data Rate** | Select the highest level for the PCIe data rate to perform tests. |
| **Toggle Control** | Select to use the GRL-P1 hardware controller to provide compliance toggle signal to control the compliance state of the DUT.<br>Select "None" if using manual compliance toggle. |

| | |
|---|---|
| **Data/Clock Channel** | Select the Scope channels that are connected to the Data Lanes and Reference Clock of the respective test fixture. |
| **Fixture Type** | Select a PCIe compliance test fixture in use. |
| **Switch Matrix** | Select "True" to enable using an RF switch in the test setup. |
| **Auto Scale** | Select "True" to enable auto scaling during tests. |
| **Vertical $V_{Diff}$ Range (V)** | Set the vertical range of the Scope to easily detect a change to the voltage level when running tests. |
| **Gen4 Apply Embedding** | Select "True" to enable embedding to be performed during tests for PCIe Gen 4. |
| **Gen5 Apply Embedding** | Select "True" to enable embedding to be performed during tests for PCIe Gen 5. |
| **Gen4 System/AIC Embedding File** | If "Gen4 Apply Embedding" has been set to "True", enter the name of the file to be used for embedding of the PCIe Gen 4 system board or add-in card. |
| **Gen5 System/AIC Embedding File** | If "Gen5 Apply Embedding" has been set to "True", enter the name of the file to be used for embedding of the PCIe Gen 5 system board or add-in card. |
| **UI (M) [Gen1/Gen2/Gen3/Gen4/ Gen5]** | Specify the number of sample points to capture for each data rate. |
| **Sample Rate (Gb/s) [Gen1/Gen2/Gen3/Gen4/ Gen5]** | Specify the real-time sample rate in Gb/s to capture the required waveform data. |
| **Gen3/Gen4/Gen5 Signal Quality Test Preset** | Select the preset to be applied for Gen 3, Gen 4 or Gen5 signal quality test. |
| **User Real Edge (Gen5)** | Select "True" to use real edge channels for PCIe Gen5 compliance testing. |
| **SigTest Run Mode** | Select the SigTest to run Sequential or Parallel signal quality testing to ensure waveform compliance. |
| **SigTest Max Thread** | Specify the maximum number of threads for each SigTest run. |
| **SSC Support** | Select "True" to enable Spread Spectrum Clock (SSC) capabilities for testing (if supported by the DUT). |

## 4.3 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE-TX software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

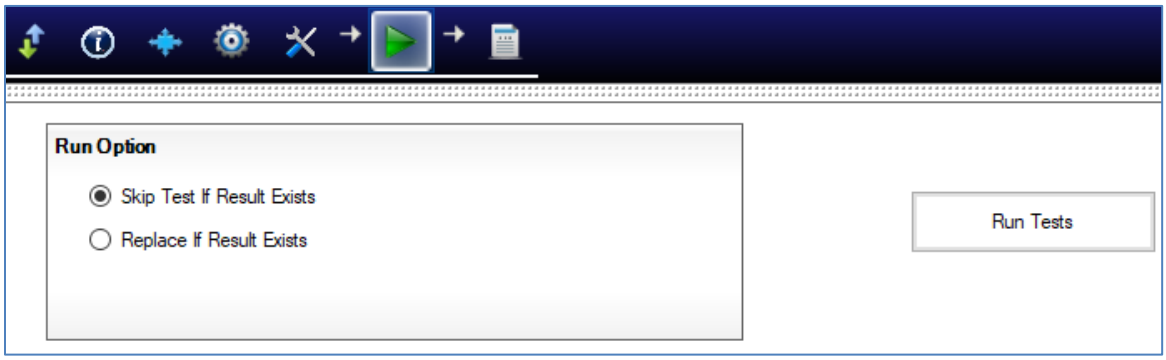



FIGURE 37. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed. Follow the step by step instructions to complete the entire testing.

# 5 Interpreting GRL-PCIE-TX Test Report

When all test runs have completed from Section 4, the GRL-PCIE-TX software will automatically display the test results on the **Report** page.

Select  from the menu to access the Report page to view the results from each test run.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

Also select the **Generate report** button to generate a detailed test report in the PDF format.

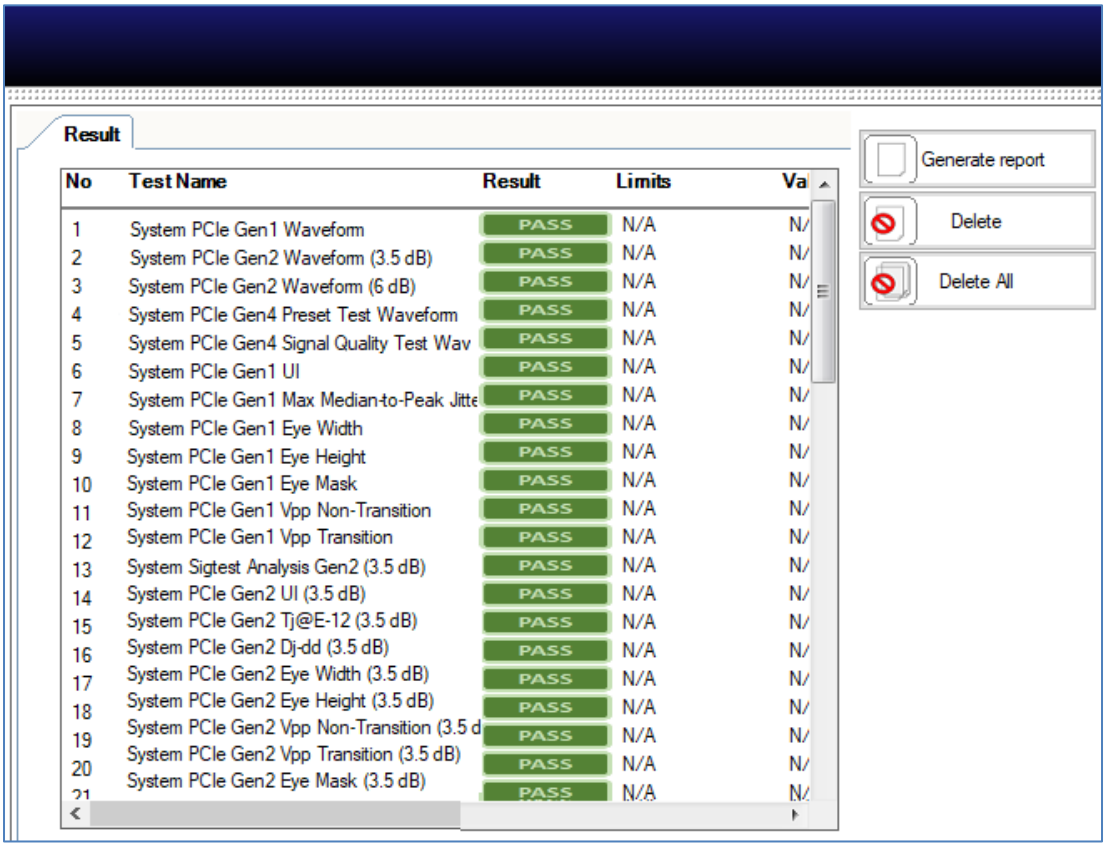


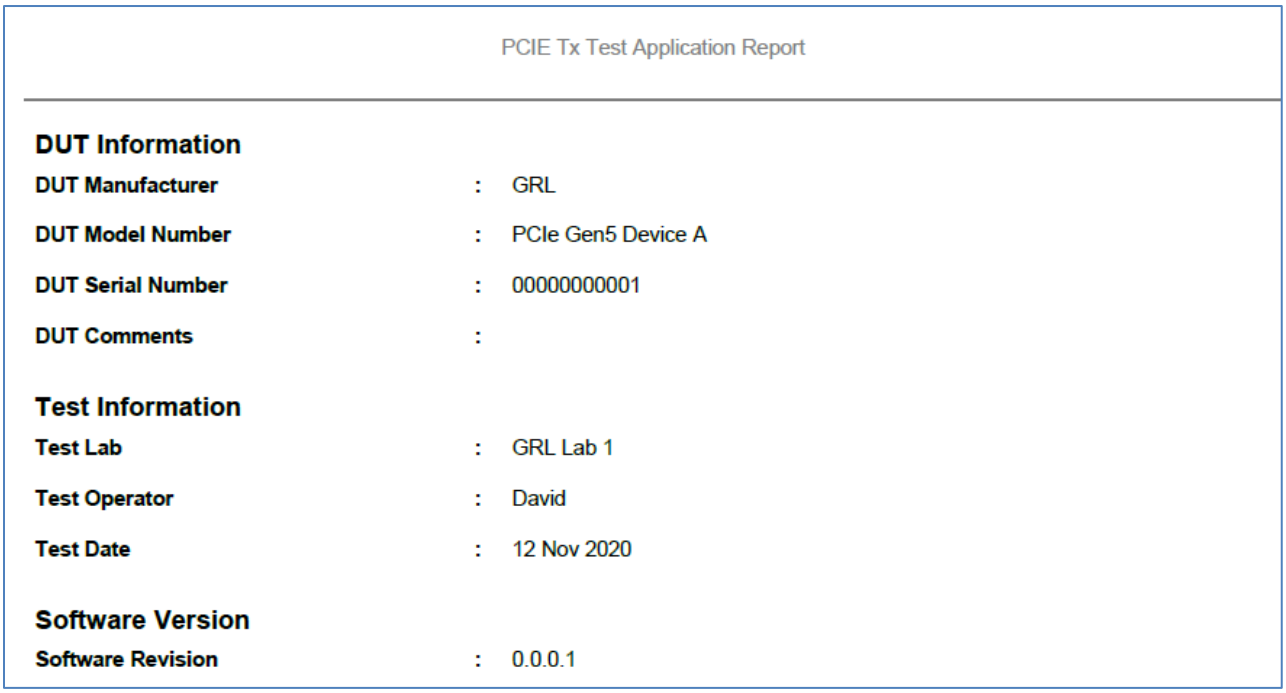

FIGURE 38. TEST REPORT PAGE

## 5.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

### 5.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.


PCIE Tx Test Application Report

**DUT Information**

| | | |
|---|---|---|
| **DUT Manufacturer** | : | GRL |
| **DUT Model Number** | : | PCIe Gen5 Device A |
| **DUT Serial Number** | : | 00000000001 |
| **DUT Comments** | : | |

**Test Information**

| | | |
|---|---|---|
| **Test Lab** | : | GRL Lab 1 |
| **Test Operator** | : | David |
| **Test Date** | : | 12 Nov 2020 |

**Software Version**

| | | |
|---|---|---|
| **Software Revision** | : | 0.0.0.1 |

FIGURE 39. TEST SESSION INFORMATION EXAMPLE

### 5.1.2 Test Summary Table

This table provides an overall view of all the tests performed along with their test conditions and results.

| No | TestName | Limits | Value | Results | Lane | Data Rate | Preset |
|---|---|---|---|---|---|---|---|
| 1 | Add-In Card PCIe Gen1 Waveform | N/A | N/A | Pass | Lane0 | Gen1 | N/A |
| 2 | Add-In Card PCIe Gen2 Waveform (3.5 dB) | N/A | N/A | Pass | Lane0 | Gen2 | N/A |
| 3 | Add-In Card PCIe Gen2 Waveform (6 dB) | N/A | N/A | Pass | Lane0 | Gen2 | N/A |
| 4 | Add-In Card PCIe Gen3 Waveform | N/A | N/A | Pass | Lane0 | Gen3 | P4 |
| 5 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P0 |
| 6 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P1 |
| 7 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P2 |
| 8 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P3 |
| 9 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P4 |
| 10 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P5 |
| 11 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P6 |
| 12 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P7 |
| 13 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P8 |
| 14 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P9 |
| 15 | Add-In Card PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P10 |
| 16 | Add-In Card PCIe Gen4 PWJ Waveform | N/A | N/A | Pass | Lane0 | Gen4 | N/A |
| 17 | Add-In Card PCIe Gen4 Add In Card Signal Quality Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P4 |
| 18 | Add-In Card PCIe Gen4 Add In Card Signal Quality Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P0 |
| 19 | System PCIe Gen1 Waveform | N/A | N/A | Pass | Lane0 | Gen1 | N/A |
| 20 | System PCIe Gen2 Waveform (3.5 dB) | N/A | N/A | Pass | Lane0 | Gen2 | N/A |
| 21 | System PCIe Gen2 Waveform (6 dB) | N/A | N/A | Pass | Lane0 | Gen2 | N/A |
| 22 | System PCIe Gen3 Waveform | N/A | N/A | Pass | Lane0 | Gen3 | P4 |
| 23 | System PCIe Gen4 Preset Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P4 |
| 24 | System PCIe Gen4 Signal Quality Test Waveform | N/A | N/A | Pass | Lane0 | Gen4 | P4 |
| 25 | Add-In Card PCIe Gen1 UI | 399.8800< X < 402.1200 ps | 399.9998 ps | Pass | Lane0 | Gen1 | N/A |
| 26 | Add-In Card PCIe Gen1 Max Median-to-Peak Jitter | < 56.0000 ps | 17.4189 ps | Pass | Lane0 | Gen1 | N/A |
| 27 | Add-In Card PCIe Gen1 Eye Width | N/A | 381.2836 ps | InfoOnly | Lane0 | Gen1 | N/A |
| 28 | Add-In Card PCIe Gen1 Eye Height | N/A | 0.2335 V | InfoOnly | Lane0 | Gen1 | N/A |
| 29 | Add-In Card PCIe Gen1 Eye Mask | N/A | N/A | Fail | Lane0 | Gen1 | N/A |
| 30 | Add-In Card PCIe Gen1 Vpp Non-Transition | < 1.2000 V | 0.7136 V | Pass | Lane0 | Gen1 | N/A |
| 31 | Add-In Card PCIe Gen1 Vpp Transition | < 1.2000 V | 0.7291 V | Pass | Lane0 | Gen1 | N/A |
| 32 | Add-In Card PCIe Gen2 UI (3.5 dB) | 199.9400< X < 201.0600 ps | 199.9999 ps | Pass | Lane0 | Gen2 | N/A |
| 33 | Add-In Card PCIe Gen2 TJ@E-12 (3.5 dB) | N/A | 15.2605 ps | InfoOnly | Lane0 | Gen2 | N/A |
| 34 | Add-In Card PCIe Gen2 Dj-dd (3.5 dB) | < 57.0000 ps | 9.8680 ps | Pass | Lane0 | Gen2 | N/A |
| 35 | Add-In Card PCIe Gen2 Eye Wdith (3.5 dB) | N/A | 184.7395 ps | InfoOnly | Lane0 | Gen2 | N/A |
| 36 | Add-In Card PCIe Gen2 Eye Height (3.5 dB) | N/A | 0.2159 V | InfoOnly | Lane0 | Gen2 | N/A |
| 37 | Add-In Card PCIe Gen 2 Eye Mask (3.5 dB) | N/A | N/A | Fail | Lane0 | Gen2 | N/A |

FIGURE 40. TEST SUMMARY TABLE EXAMPLE

### 5.1.3 Test Results

This portion displays the results of each test performed in detail along with supporting data points and screenshots.

| 102. System PCIe Gen4 Eye Mask [Lane0,Gen4,P4] | | |
|---|---|---|
| Pass/Fail Stats | : | Pass |
| SigTest Version | : | 4.0.48 |
| DUT Type: | : | System Board |
| Transition Eye Violations | : | 0 |
| Non Transition Eye Violations | : | 0 |
| Total Eye Violations | : | 0 |
| Extrapolated Eye Height | : | 170.9318 mV |
| Eye Width | : | 40.2587 ps |
| Composite Eye Height | : | 182.3066 mV |
| Dj-dd | : | 0.0000 s |
| Rj (RMS) | : | 0.0000 s |
| Tj@E-12 | : | 0.0000 s |
| Minimum Transition Eye Voltage Margin Above Eye | : | 100.6610 mV |
| Minimum Transition Eye Voltage Margin Below Eye | : | -100.4805 mV |
| Minimum Non Transition Eye Voltage Margin Above Eye | : | 84.8030 mV |
| Minimum Non Transition Eye Voltage Margin Below Eye | : | -84.4703 mV |
| Minimum Transition Eye Voltage | : | -201.3482 mV |
| Maximum Transition Eye Voltage | : | 202.8798 mV |
| Minimum Non Transition Eye Voltagee | : | -198.0414 mV |
| Maximum Non Transition Eye Voltag | : | 197.3573 mV |
| Test completed time | : | 12 November 2019 3:14:25 AM |

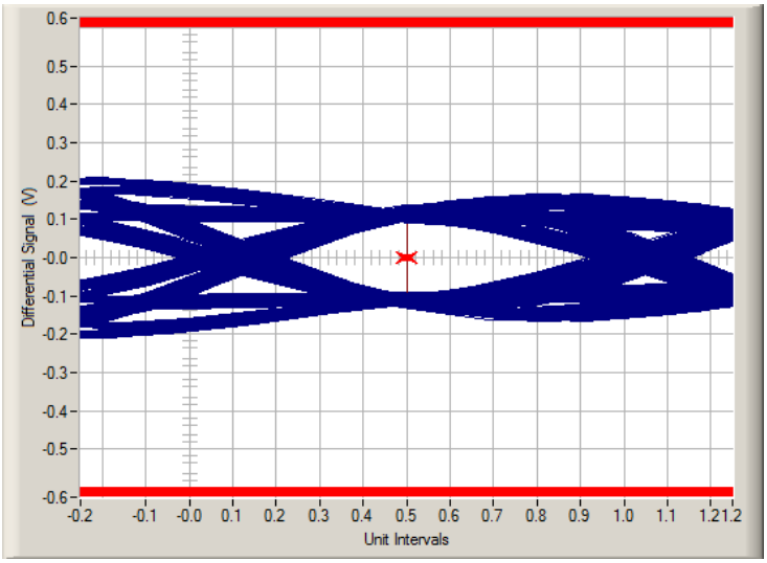



FIGURE 41. TEST RESULTS EXAMPLE

## 5.2 Delete Test Results

Select the **Delete** button to delete individual test results or **Delete All** to delete all test results.

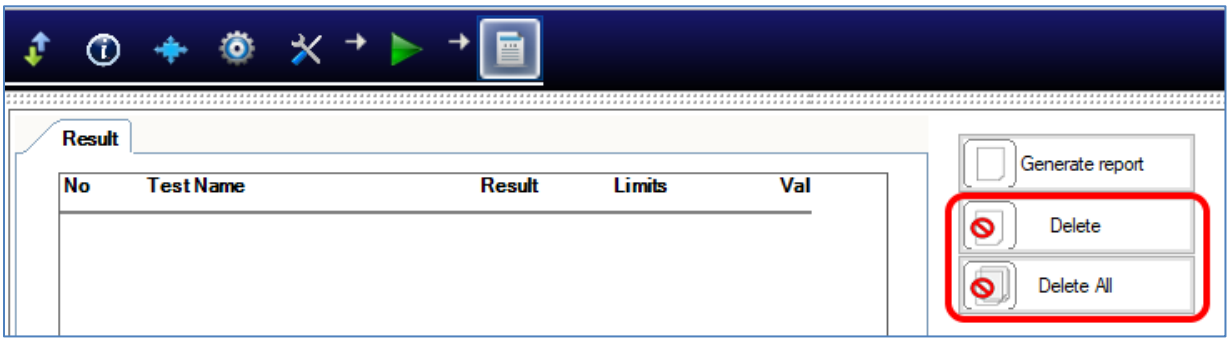



FIGURE 42. DELETE TEST RESULTS

# 6 Saving and Loading GRL-PCIE-TX Test Sessions

The usage model for the GRL-PCIE-TX software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select "Save Session".
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → "Load Session".
- To ***create a new test session*** and return the application back to the default configuration, select Options → "New Session".

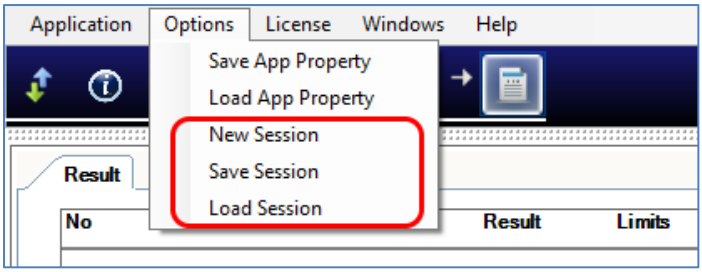



FIGURE 43. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

# 7 Appendix A: SigTest Tool Tab

The SigTest Tool allows the user to manually perform SigTest verification tests for the DUT using appropriate offline PCIe compliant SigTest template and waveform files. This function is used for debugging purposes.

1. Select  from the GRL PCIe Tx Test Application menu to access the Setup Configuration page.

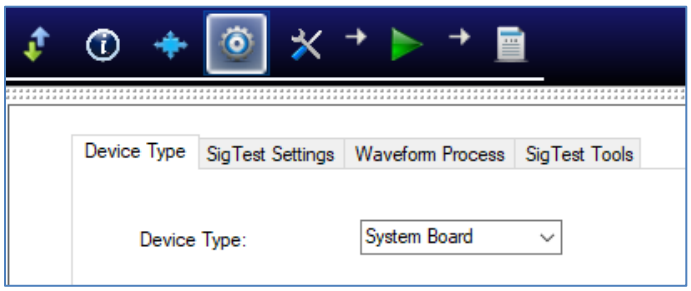



FIGURE 44. SETUP CONFIGURATION PAGE

2. Select the **SigTest Tools** tab.

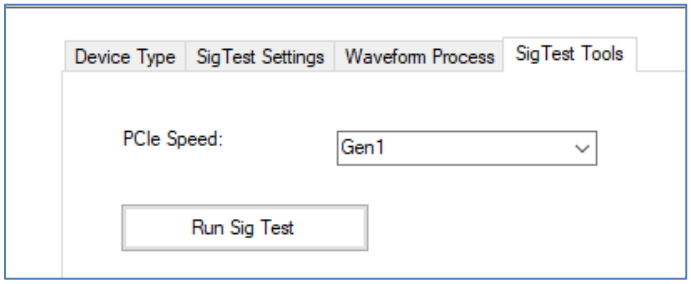



FIGURE 45. PERFORM SIGTEST DEBUGGING

3. Select the **PCIe Speed** for the appropriate waveform data rate to be used and then select the **Run Sig Test** button to perform SigTest using a selected saved offline waveform file. When selected, the GRL software will automatically run the SigTest for the waveform as shown in below example.

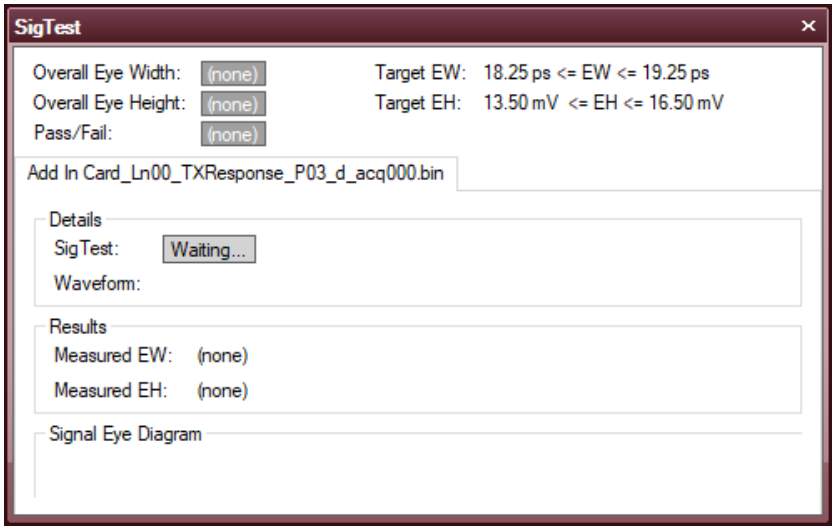



FIGURE 46. RUNNING OFFLINE SIGTEST VERIFICATION

4. Once test is completed, the results will be displayed like in the following example.

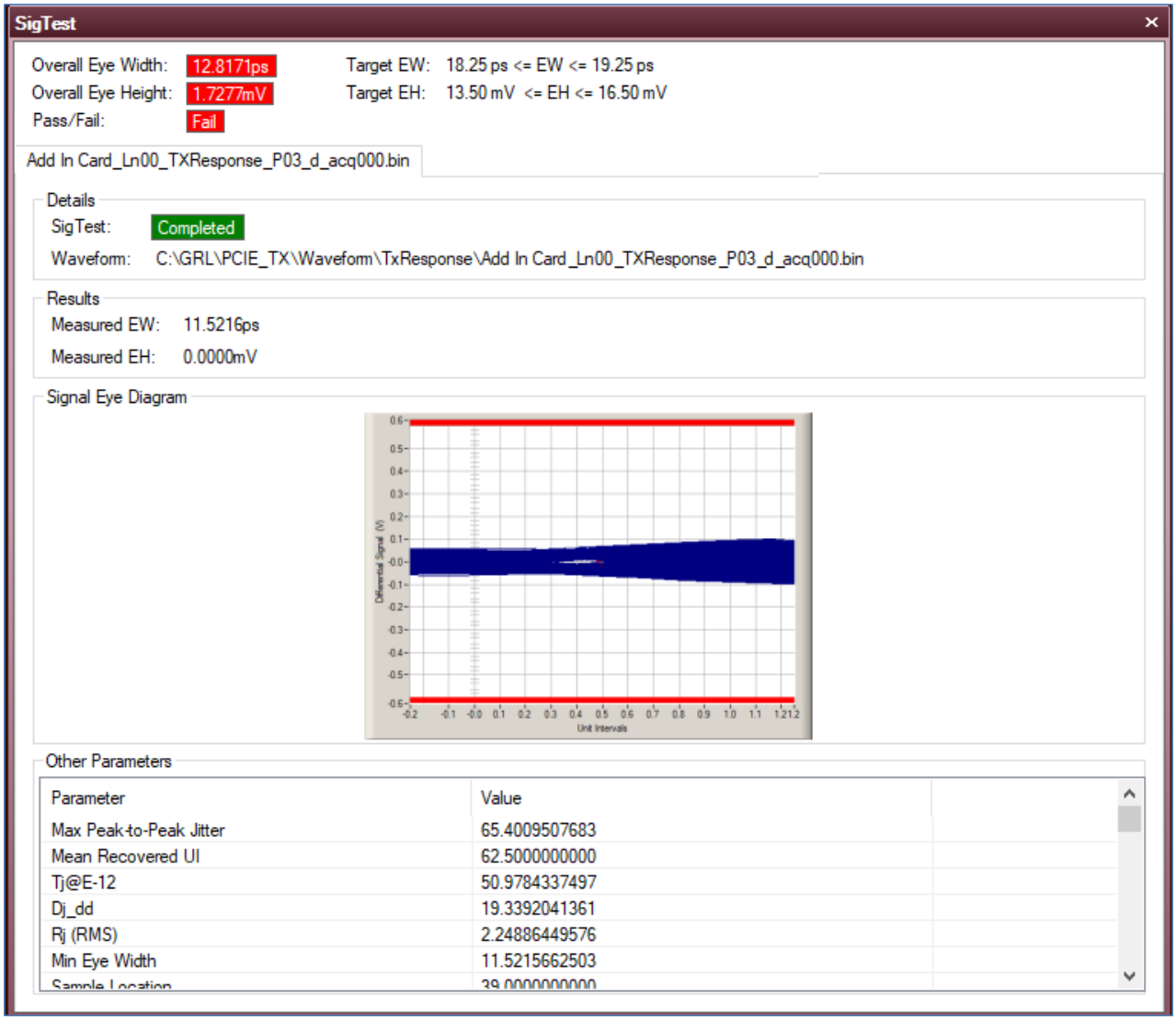



FIGURE 47. VIEWING SIGTEST ANALYSIS RESULTS

# 8 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

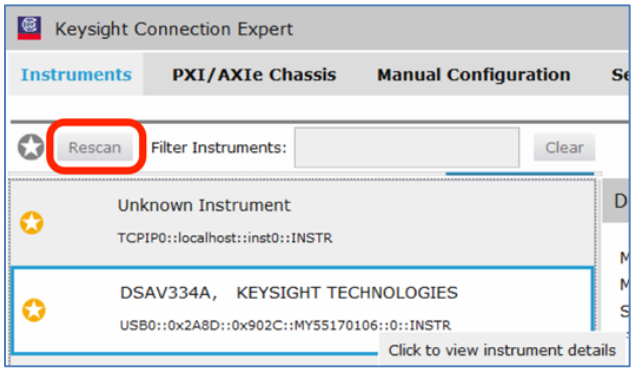



FIGURE 48. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

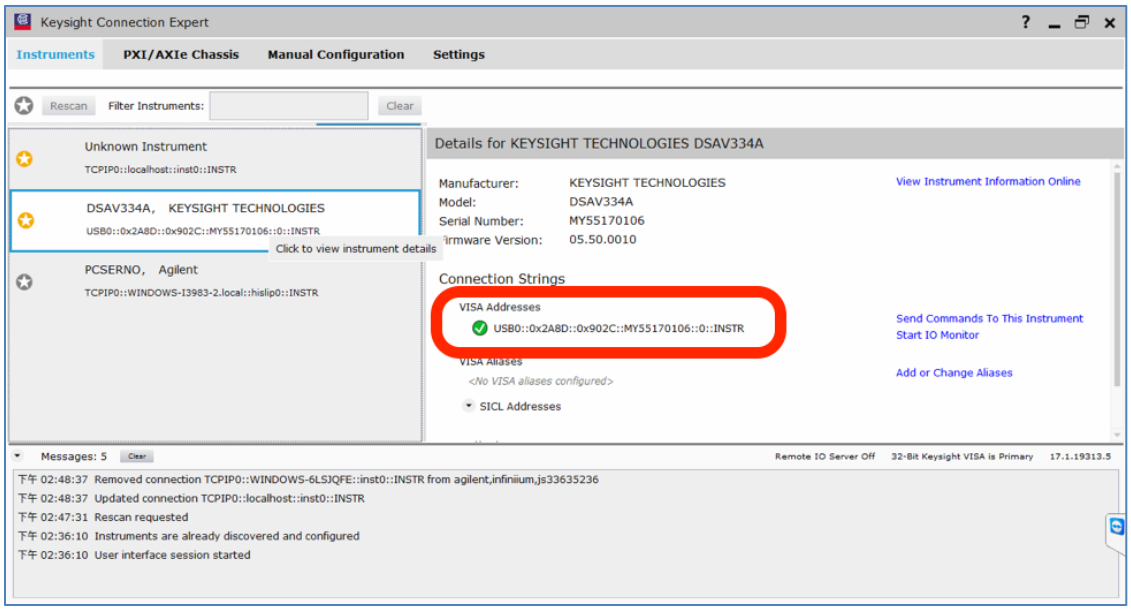



FIGURE 49. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe Tx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

# 9 Appendix C: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

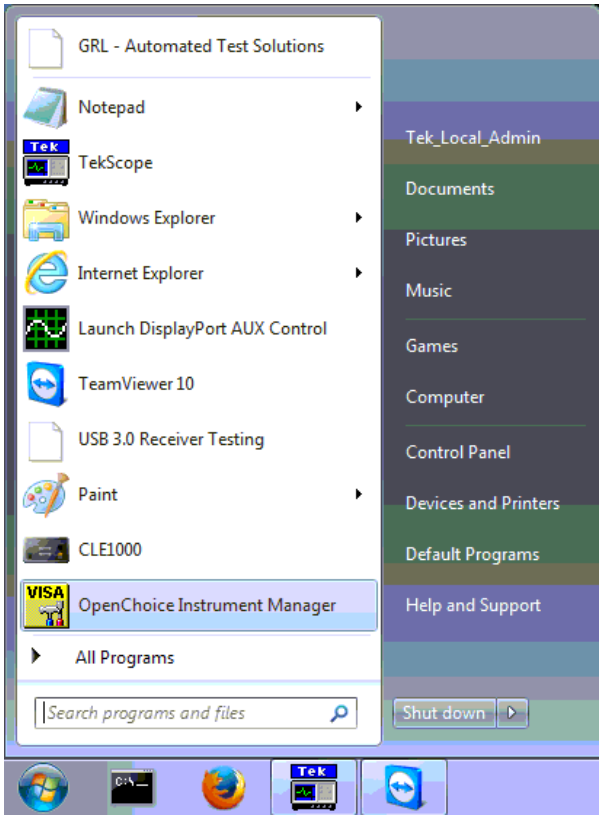



FIGURE 50. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left "Instruments" panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the "Instruments" panel – "Instrument List Update", "Search Criteria", "Instrument Identify" and "Properties" can be used to detect the Scope in case it does not initially appear under "Instruments".
   a) "Instrument List Update": Select to refresh the instrument list and locate new instruments connected to the PC.
   b) "Search Criteria": Select to configure the instrument search function.
   c) "Instrument Identify": Select to use a supported programming language to send a query to identify the selected instrument.
   d) "Properties": Select to display and view the selected instrument properties.

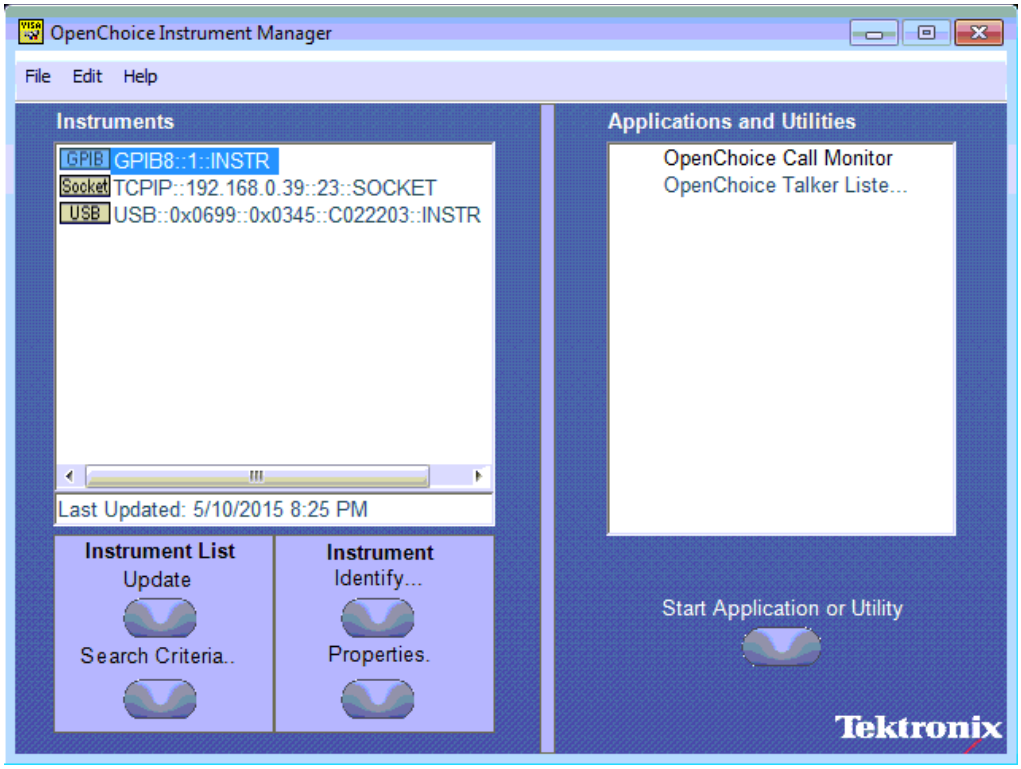



FIGURE 51. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe Tx Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe Tx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

**END_OF_DOCUMENT**