GRL-PCIE-TX PCI Express® 5.0 Transmitter Compliance Test Automation Solution
Quick Start/User Guide/Method of Implementation (MOI)
for PCIe Gen5 Physical Layer Transmitter Test Application

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TABLE OF CONTENTS

TABLE OF CONTENTS 3

1 INTRODUCTION 5

2 RESOURCE REQUIREMENTS 6

2.1 Equipment Requirements 6

2.2 Software Requirements 7

3 SETTING UP GRL-PCIE-TX AUTOMATION SOFTWARE 8

3.1 Download GRL-PCIE-TX Software 8

3.2 Launch and Set Up GRL-PCIE-TX Software 8

3.3 Pre-Configure GRL-PCIE-TX Software Before Testing 11

3.3.1 Enter Test Session Information 11

3.3.2 Set Test Conditions 11

4 TESTING USING GRL-PCIE-TX 14

4.1 GRL-PCIE-TX Advantage 14

4.2 Set Up DUT Tx Test with Automation 14

4.2.1 Connect Equipment for System Board DUT Test 15

4.2.2 Connect Equipment for Add-In Card DUT Test 16

4.2.3 Connect Equipment for System Ref Clock Jitter Test 19

4.2.4 Set Up Test Requirements 20

4.2.5 Select Compliance Tests 22

4.2.6 Configure Test Parameters 25

4.3 Run Automation Tests 27

5 INTERPRETING GRL-PCIE-TX TEST REPORT 28

5.1 Understand Test Report Information 28

5.1.1 Test Session Information 28

5.1.2 Test Summary Table 29

5.1.3 Test Results 29

5.2 Delete Test Results 32

6 SAVING AND LOADING GRL-PCIE-TX TEST SESSIONS 33

7 APPENDIX A: METHOD OF IMPLEMENTATION (MOI) FOR MANUAL PCIE 5.0 TRANSMITTER MEASUREMENTS 34

7.1 System Board Tx Signal Quality Test 34

7.2 Add-in Card Tx Signal Quality Test 37

7.3 SYSTEM BOARD TX PRESET TEST 39
7.4 ADD-IN CARD TX PRESET TEST 39
7.5 SYSTEM BOARD TX BASE JITTER (UPW-TJ, UPW-DJDD, UTJ AND UDJDD) TEST 41
7.6 ADD-IN CARD TX BASE JITTER (UPW-TJ, UPW-DJDD, UTJ AND UDJDD) TEST 42
7.7 SYSTEM BOARD REF CLOCK (100 MHZ) JITTER TEST 44
8 APPENDIX B: CONNECTING KEYSIGHT OSCILLOSCOPE TO PC 45
9 APPENDIX C: CONNECTING TEKTRONIX OSCILLOSCOPE TO PC 46

1 Introduction

This Quick Start/User Guide/MOI provides information using the GRL-PCIE-TX test solution to set up and test an electrical transmitter (Tx) device for PCI Express (PCI-SIG SEG) certification.

The main body of this documentation describes how to configure the GRL-PCIE-TX solution to capture and test waveforms in a PCIe 5.0 system (lane, data rate, preset), or individual waveforms, and perform SigTest signal quality and de-emphasis compliance tests. The test automation is carried out based on PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's).

The GRL-PCIE-TX solution consists of the GRL PCIe "GRL-P1" hardware controller and automation software (GRL-PCIE-TX). The GRL-PCIE-TX software when run from the computer or oscilloscope enables automation control to test the device under test (DUT) for Tx electrical compliance. The GRL-P1 hardware controller is designed to work primarily with the software to provide compliance toggle to control the state of the DUT. Alternatively, an arbitrary function generator can also be used as a secondary option for compliance toggle control. The GRL test solution also extends support for RF switch integration to automate switching or selection of the lane under test.

The GRL automation control enabled PC or scope automates power and signal quality test sequencing and processing of captured waveforms for the DUT at the selected PCIe data rate. The Tx path is tested with worst case eye to ensure a Bit Error Ratio (BER) of less than 1E-12 can be achieved. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

This documentation covers the following major components for PCIe Tx testing.

1. GRL-P1 hardware controller setup.
2. GRL-PCIE-TX software configuration and test setup.

Note: For manual test methodology, please refer to PCI-SIG SEG for approved vendor specific Method of Implementation (MOI's) as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

Equipment	Qty.	Description/Key Spec Requirement
High Performance Real-time Oscilloscope [a]	1	≥ 33 GHz bandwidth (For PCIe Gen5) Sample rate: ≥ 128 Gb/s with 2x interpolation
"GRL-P1" PCIe Compliance Test Hardware Controller (Optional)	1	For PCIe compliance toggle control
Advanced Technology eXtended (ATX) Power Supply	1	For power supply to the DUT
GRL Switch (Optional)	1	For multi-lane automated testing
PCI-SIG Compliance Base Board (CBB) or PCI-SIG Compliance Load Board (CLB)	1	For add-in cards For hosts
Computer (laptop or desktop)	1	Windows 7+ OS For automation control of the DUT state

[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable	Qty.
Power Control Adapter Cable	1
USB Type-A to Type-A/B Micro Cable	1
Test Fixture Control Cable (2-conductor power control only cable or 6-conductor fixture control cable)	1
Clock Compliance Toggle Cables (matched SMA-to-SMP cables)	1 pair
SMA-to-SMP Cables	4 pairs[a]

[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
GRL-PCIE-TX	Granite River Labs PCI Express® 5.0 Automated Transmitter Compliance Test Solution (hardware & software) – www.graniteriverlabs.com Further automation license for Custom DUT, RF Switch, or other bench automation – www.graniteriverlabs.com
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-GRL-PCIE-TX software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
SigTest	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html

3 Setting Up GRL-PCIE-TX Automation Software

This section provides the procedures to start up and pre-configure the GRL-PCIE-TX automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL-PCIE-TX software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the GRL-PCIE-TX software, follow the procedures in the following sections.

3.1 Download GRL-PCIE-TX Software

Download and install the GRL-PCIE-TX software as follows:

1. If the GRL-PCIE-TX software is to be installed on a PC (where is referred to as 'controller PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL software is to be used (see Section 2.2).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIETxTestApplicationxxxxxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the GRL-PCIE-TX application.
   - **PCIe4_TxTestScopeSetupFilesInstallationxxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

3.2 Launch and Set Up GRL-PCIE-TX Software

4. Once the GRL-PCIE-TX software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

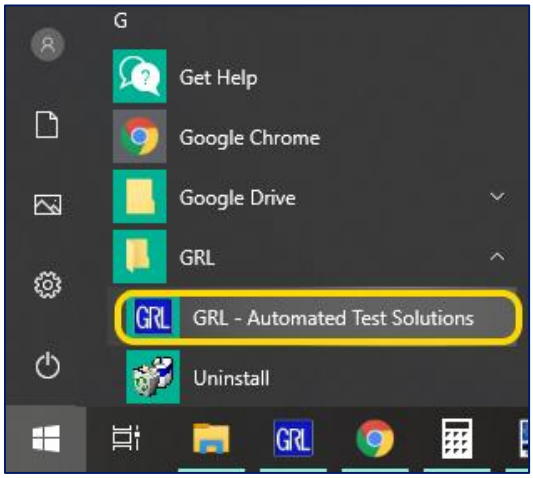


FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

5. From the **Application→Framework Test Solution** drop-down menu, select "**PCIE Tx Test Application**" to start the PCIe Tx Test Application. If the selection is grayed out, it means that your license has expired.

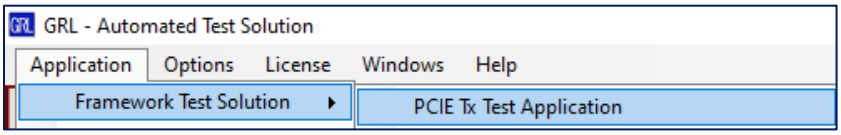


FIGURE 2. START PCIE TX TEST APPLICATION

6. To enable license, go to License→License Details.

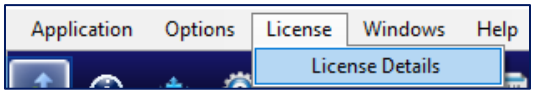


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

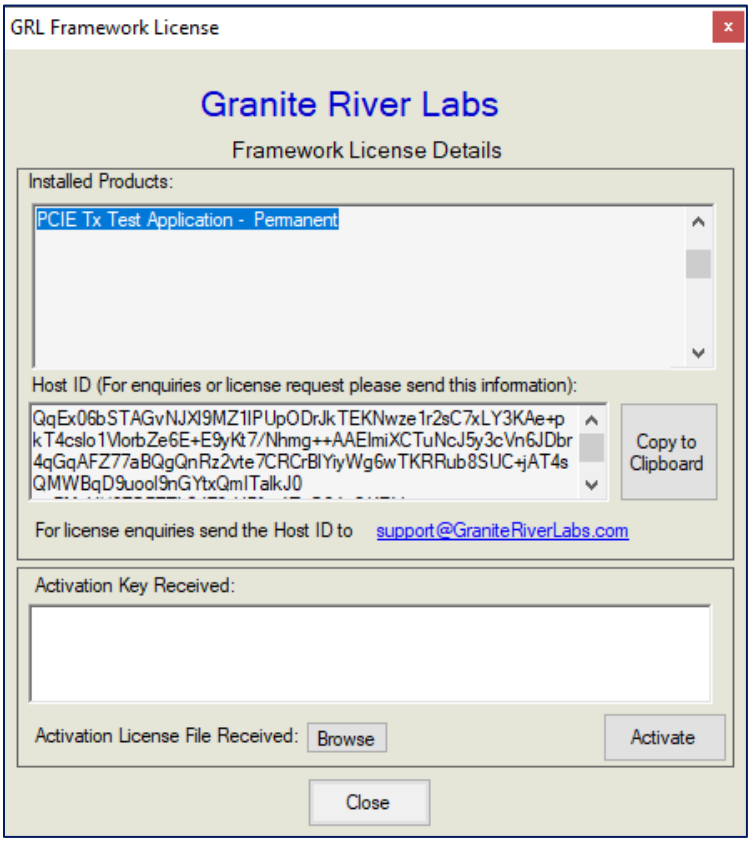


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select "Activate".
- If you do not have an Activation Key, select "Close" to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

7. Select the Equipment Setup icon on the PCIe Tx Test Application menu.
8. Connect the oscilloscope with the controller PC through either GPIB, USB or LAN. *(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the controller PC is provided in the Appendix of this document.)*
9. If using an RF Switch, connect the switch via GPIB to the GRL automation control enabled Scope or PC.
10. If using an Arbitrary Function Generator (AFG) as the compliance toggle control, connect the AFG via USB to the GRL automation control enabled Scope or PC.
11. On the Scope or PC, obtain the network addresses for all the connected instruments from the device settings. These addresses will be used to connect the instruments to the GRL automation software.
12. If using the GRL-P1 hardware controller, connect the controller via USB to the GRL automation control enabled Scope or PC.
13. On the Scope or PC, obtain the network address for the connected GRL-P1 from the device settings. For example, if GRL-P1 is connected to the PC, open the Device Manager which should detect the controller as a Controller Serial (COM) Port, e.g. “GRL PCIe34 P1 (COM10)”.
14. On the Equipment Setup page of the GRL PCIe Tx Test Application, type in the address of each connected instrument into the “Address” field.

    Then select the “lightning” button ( ) for each connected instrument.

    The “lightning” button should turn green ( ) once the application has successfully established connection with each instrument.

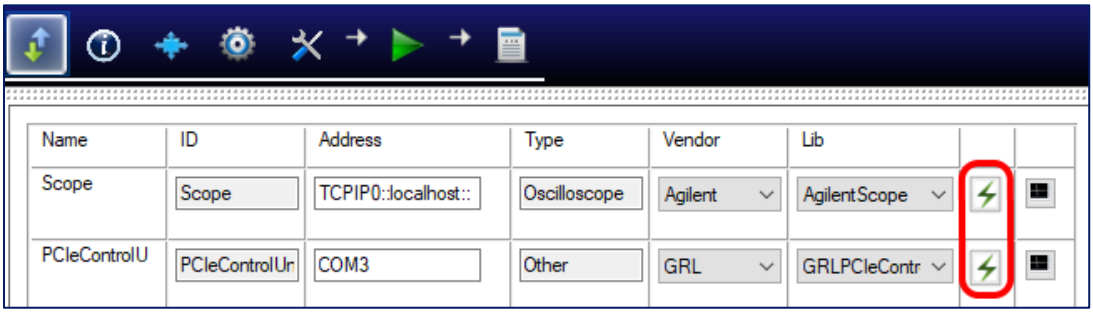


FIGURE 5. CONNECT INSTRUMENTS WITH GRL-PCIE-TX SOFTWARE

13. *(Note: If the GRL-PCIE-TX software is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR.)* If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to omit the Port number from the address. The “lightning” button should turn green if successfully connected to the instrument.

3.3 Pre-Configure GRL-PCIE-TX Software Before Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced test setup.

3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

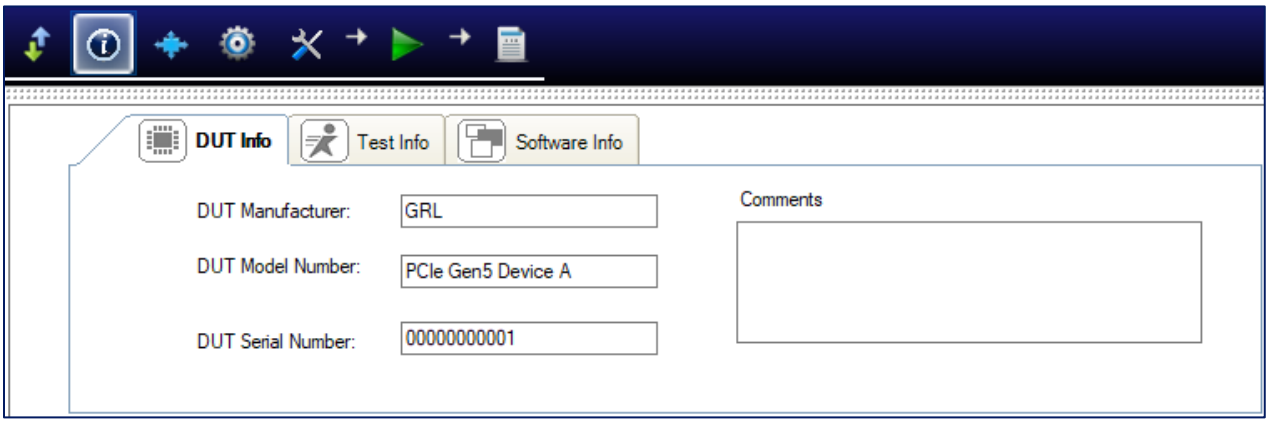


FIGURE 6. SESSION INFO PAGE

3.3.2 Set Test Conditions

Select  from the menu to access the **Conditions** page to set the conditions for testing. The software will run tests for the PCIe data lanes, data rates, and preset settings that are selected.

a) **Lane** tab: Select the desired data lanes to be tested.

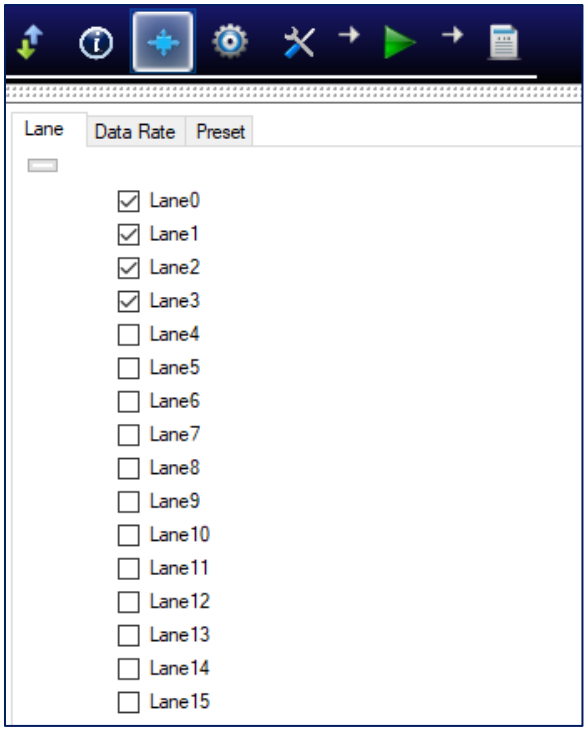


FIGURE 7. SELECT LANE UNDER TEST

b) **Data Rate** tab: Select the desired PCIe data rates for testing.

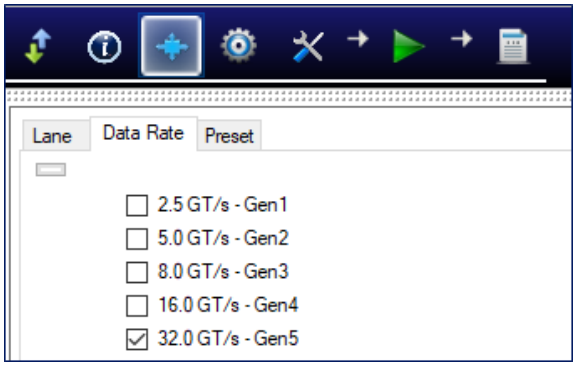


FIGURE 8. SELECT DATA RATES

c) **Preset** tab: Select the pre-defined Tx presets as required for Tx equalization.

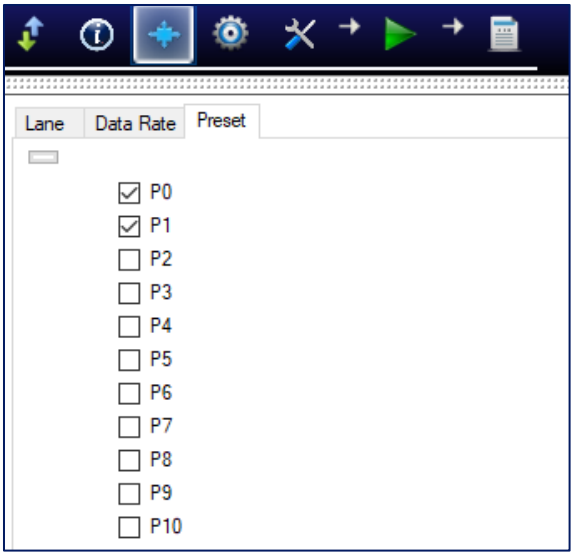


FIGURE 9. SELECT PRESETS

4 Testing Using GRL-PCIE-TX

The GRL-PCIE-TX test solution supports automated Tx compliance testing using the SigTest signal quality/de-emphasis and stress tolerance analysis application for PCIe system board and add-in card DUT's. In a typical test environment, the GRL-PCIE-TX automation software is run from the PC/oscilloscope and communicates with the GRL-P1 hardware controller. This enables automation control for the DUT's power and signal quality test sequence, as well as waveform acquisition for PCIe Gen5. Optionally an arbitrary function generator can also be used as an alternative compliance toggle controller.

The GRL-P1 controller can be connected to either a PCI-SIG compliance load board (CLB) test fixture for the system board DUT or compliance base board (CBB) test fixture for the add-in card DUT. The GRL automation control enabled PC/Scope will send commands to GRL-P1 which controls the power to the DUT and provides a compliance toggle signal to cause the DUT to enter the next compliance state.

The DUT will transmit the test signal to the oscilloscope that is used to validate the test pattern of the signal. The compliance signal will be captured and saved as a waveform file which is then measured for stress tolerance and preset test compliance. In between, an optional RF switch can be used and controlled by the GRL-PCIE-TX software to automate selection of the lane under test. When testing is completed, the software will generate a test report detailing all results from all lanes tested.

4.1 GRL-PCIE-TX Advantage

The GRL-PCIE-TX test solution provides a more efficient way to perform PCIe Tx compliance testing rather than using traditional manually-driven methods that are generally both time-consuming and error prone, tying up valuable equipment and resources.

To increase test efficiency, the GRL-P1 controller will first quickly capture waveforms on the oscilloscope. Then using a separate computer, the GRL-PCIE-TX software will run PCIe compliance tests for the waveforms, SigTest signal quality, and de-emphasis.

Through this offline processing of captured waveforms, the oscilloscope can be freed up for other work. The test time can also be further reduced with the software's multi-threading of SigTest. Another advantage is that GRL-P1 can be programmed to automatically capture only the waveforms for the test that the user wants to perform.

4.2 Set Up DUT Tx Test with Automation

Once pre-configuration has been completed from Section 3.3, continue with the test setup. The following procedures show how to set up the test environment to perform automated Tx compliance testing for both the System Board and Add-In Card DUT's.

4.2.1 Connect Equipment for System Board DUT Test

The connection diagrams below show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe System Board DUT using a GRL automation control enabled Scope and test controller method.

4.2.1.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using GRL-P1 with the PCIe Gen5 Compliance Load Board (CLB). *Note the use of GRL-P1 in the setup is optional.*

4.2.1.1.1 PCIe Gen5 System Board Connection Setup

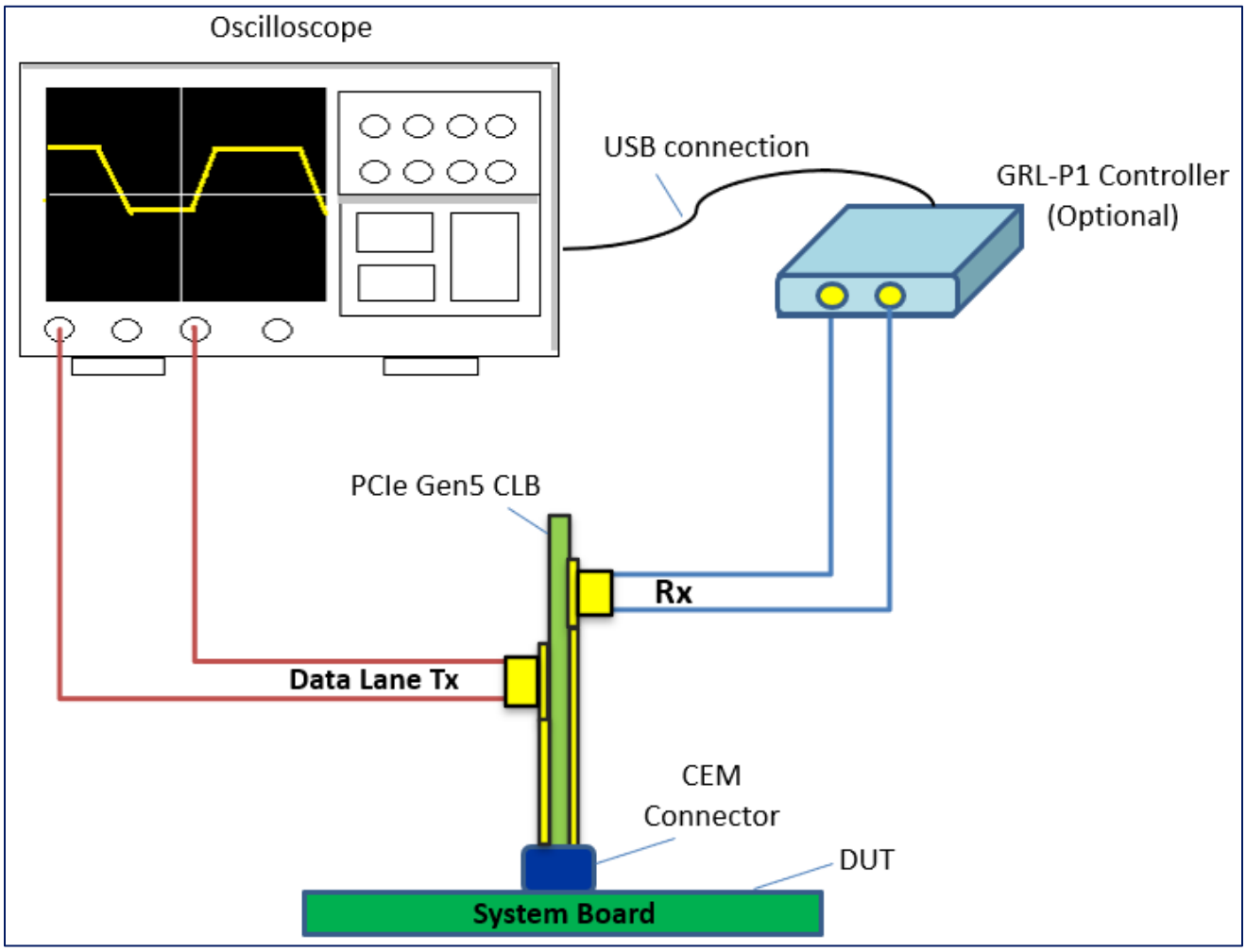


FIGURE 10. CONCEPTUAL PCIE GEN5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1

1. Insert the CLB into the designated slot on the DUT.
2. Connect the Tx+ Data Lane from the CLB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CLB to Channel 3 of the Scope.
4. Connect the CLB Rx+ Lane to the GRL-P1 Output 1.
5. Connect the CLB Rx- Lane to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the DUT.

7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.
9. If using ISI, connect a 2.3 dB ISI in between the CLB Tx outputs and Scope channels (Figure 11 below).

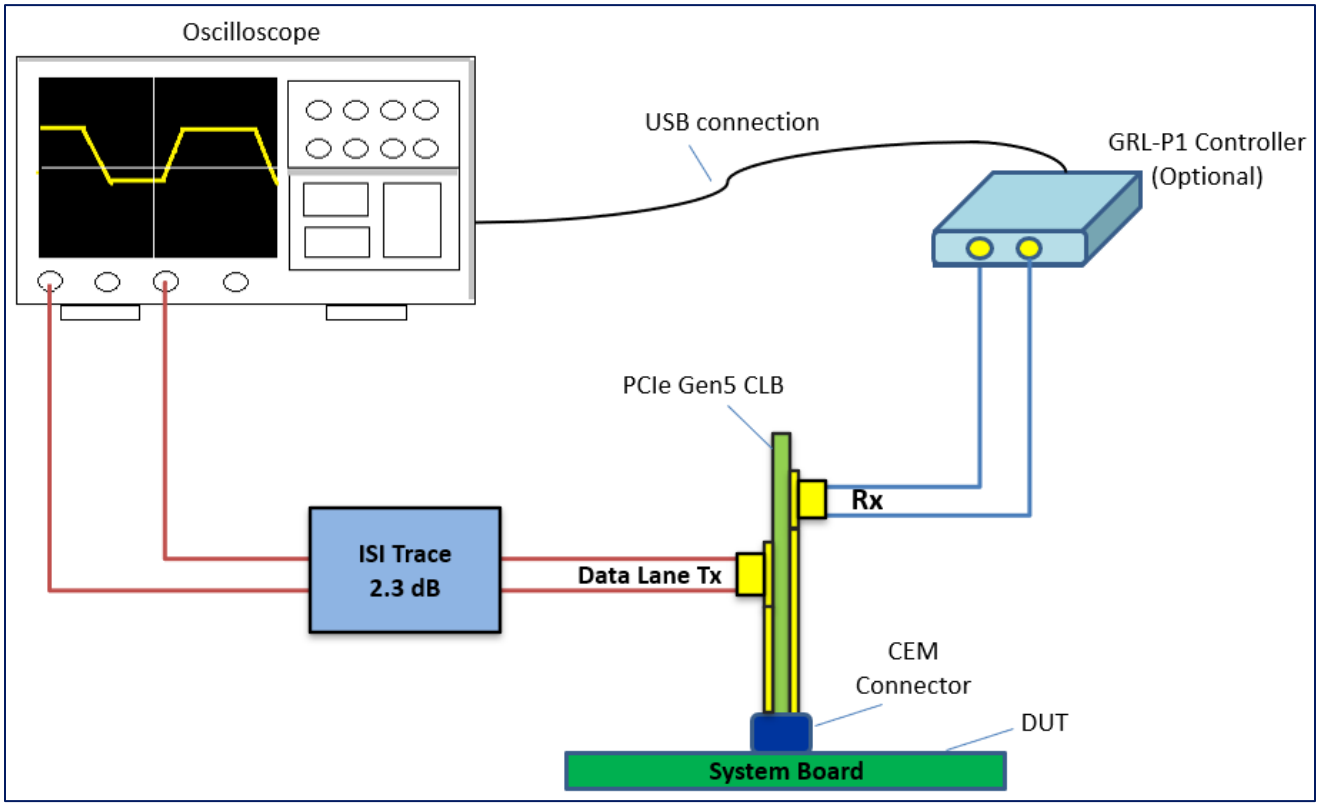


FIGURE 11. CONCEPTUAL PCIE GEN5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH ISI)

4.2.2 Connect Equipment for Add-In Card DUT Test

The following connection diagrams show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe Add-In Card DUT using a GRL automation control enabled Scope and test controller method.

4.2.2.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using GRL-P1 with the PCIe Gen5 Compliance Base Board (CBB). *Note the use of GRL-P1 in the setup is optional.*

4.2.2.1.1 PCIe Gen5 Add-In Card Connection Setup

Note: The use of GRL-P1 in the setup is optional.

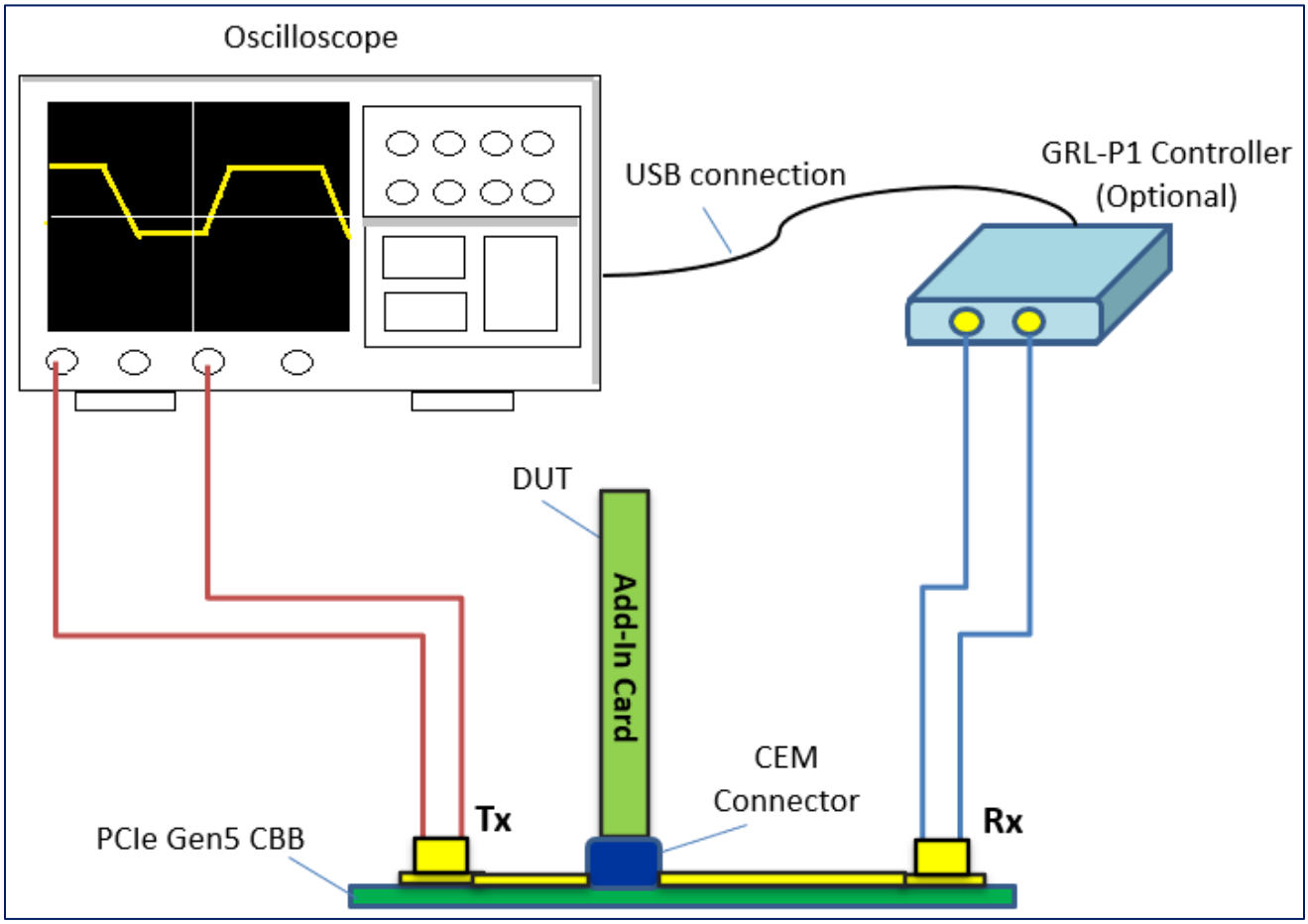


FIGURE 12. CONCEPTUAL PCIE GEN5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1

1. Attach the DUT to the designated slot on the CBB.
2. Connect the Tx+ Data Lane from the CBB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CBB to Channel 3 of the Scope.
4. Connect the Rx+ Lane from the CBB to the GRL-P1 Output 1.
5. Connect the Rx- Lane from the CBB to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the CBB.
7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.
9. If using ISI, connect a 12.5 dB ISI in between the CBB Tx outputs and Scope channels (Figure 13 below).

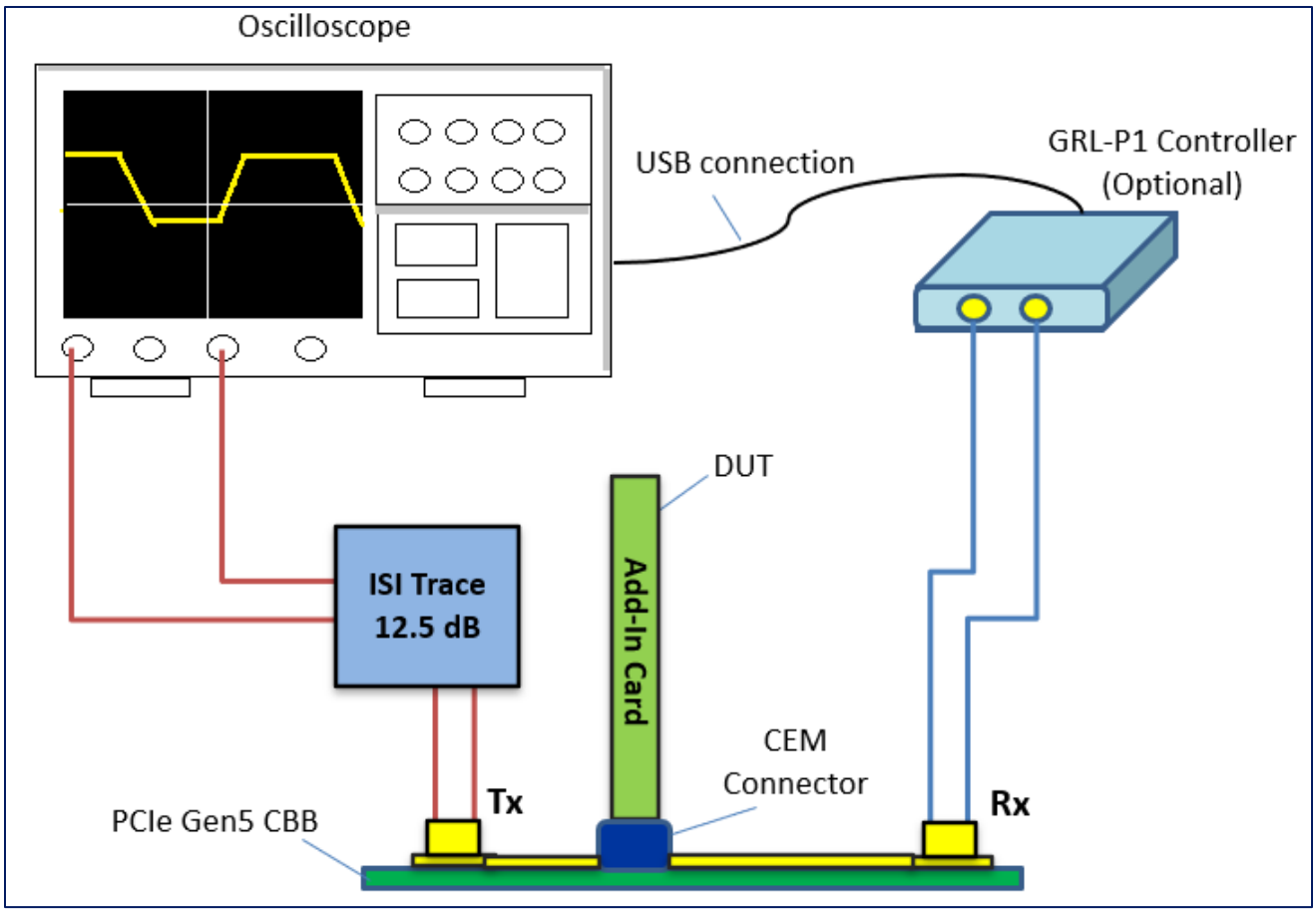


FIGURE 13. CONCEPTUAL PCIE GEN5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH ISI)

4.2.3 Connect Equipment for System Ref Clock Jitter Test

The following connection diagram shows the recommended equipment setup to perform waveform acquisition and analysis for the PCIe Gen5 System Ref Clock Jitter Test.

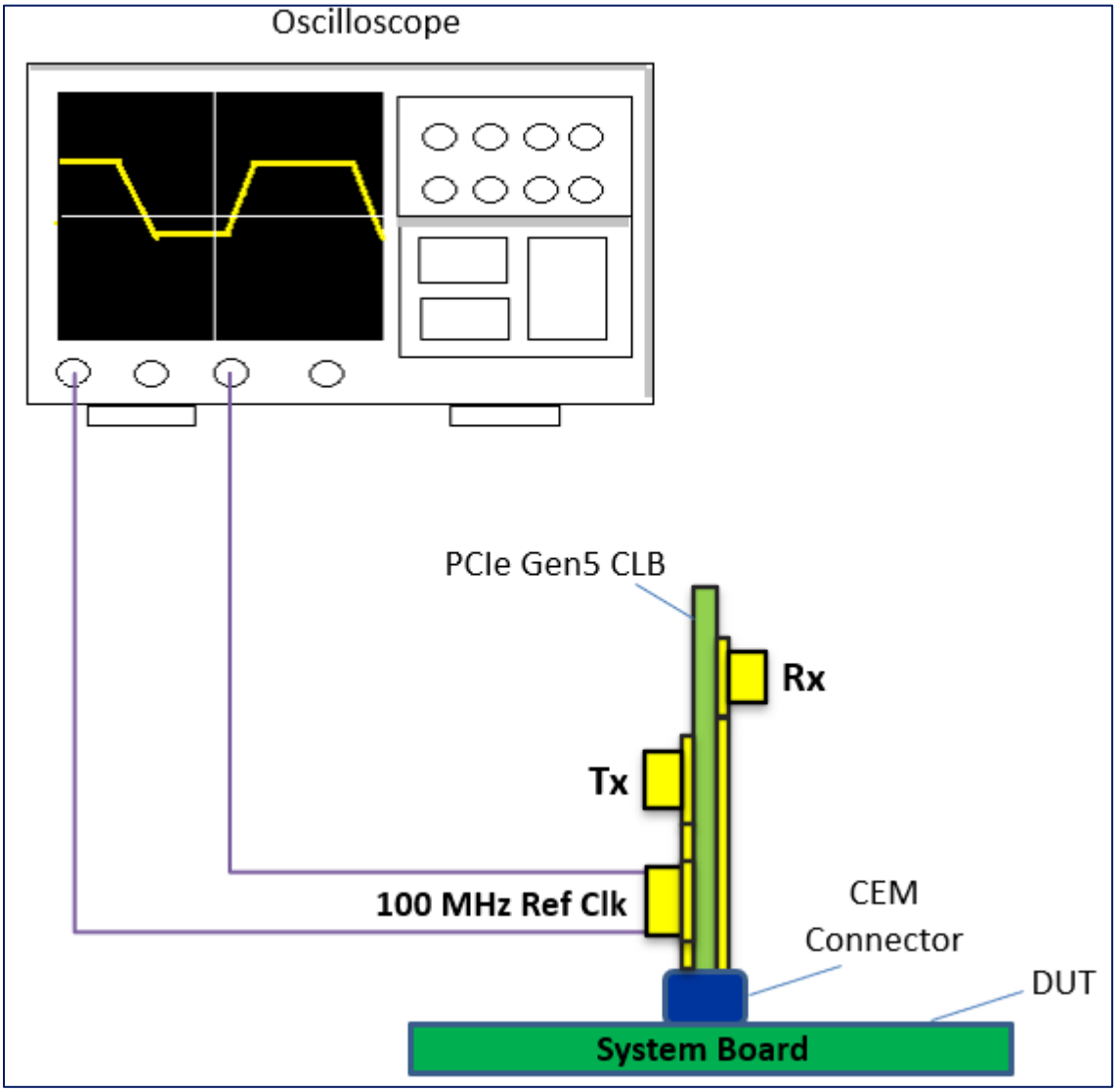


FIGURE 14. CONCEPTUAL PCIE GEN5 SYSTEM REF CLOCK JITTER TEST SETUP DIAGRAM

1. Insert the CLB into the designated slot on the DUT.
2. Connect Ref Clk+ from the CLB to Channel 1 of the Scope.
3. Connect Ref Clk- from the CLB to Channel 3 of the Scope.
1. Connect the power control adapter cable from the ATX power supply to the DUT.

4.2.4 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL PCIe Tx Test Application menu to access the Setup Configuration page. Select the DUT to be tested, set up and run SigTest, and set up waveform processing to be applied for testing.

a) **Device Type** tab: Select to use either a PCIe System Board or Add-In Card as the DUT. Select to use either the PCIe CEM, PCIe Gen3 U.2 (SFF-8639) or PCIe Gen3 M.2 fixture connector as supported by the DUT.

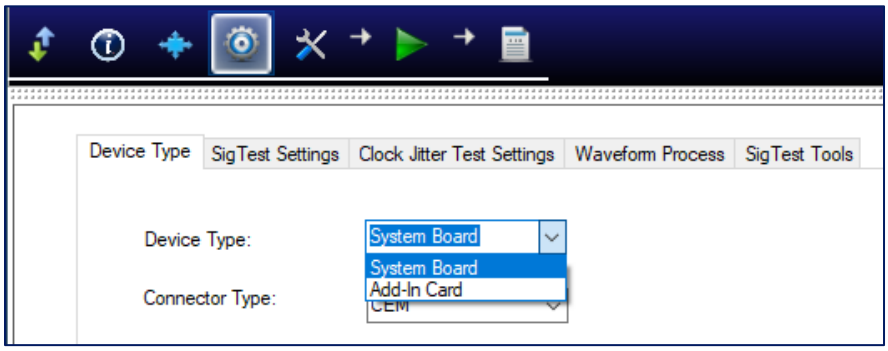


FIGURE 15. SELECT DUT TYPE

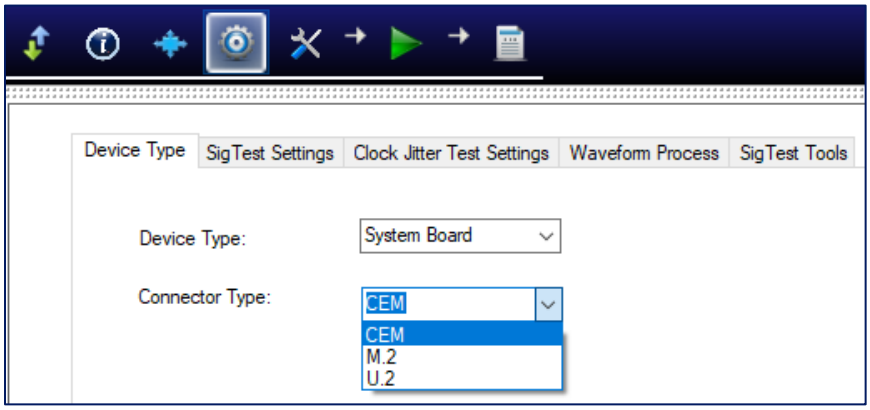


FIGURE 16. SELECT DUT FIXTURE CONNECTOR TYPE

b) **SigTest Settings** tab:

- *PCIE Gen1 (2.5Gb/s), Gen2 (5Gb/s) and Gen3 (8Gb/s)* – Select to run either the pre-defined Version "3.2.0.3" or a "Custom" Version of the SigTest. If "Custom" is selected, enter the Version number of the Custom SigTest and also make sure that the SigTest is already installed in the system.
- *PCIE Gen4 (16Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.
- *PCIE Gen5 (32Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.

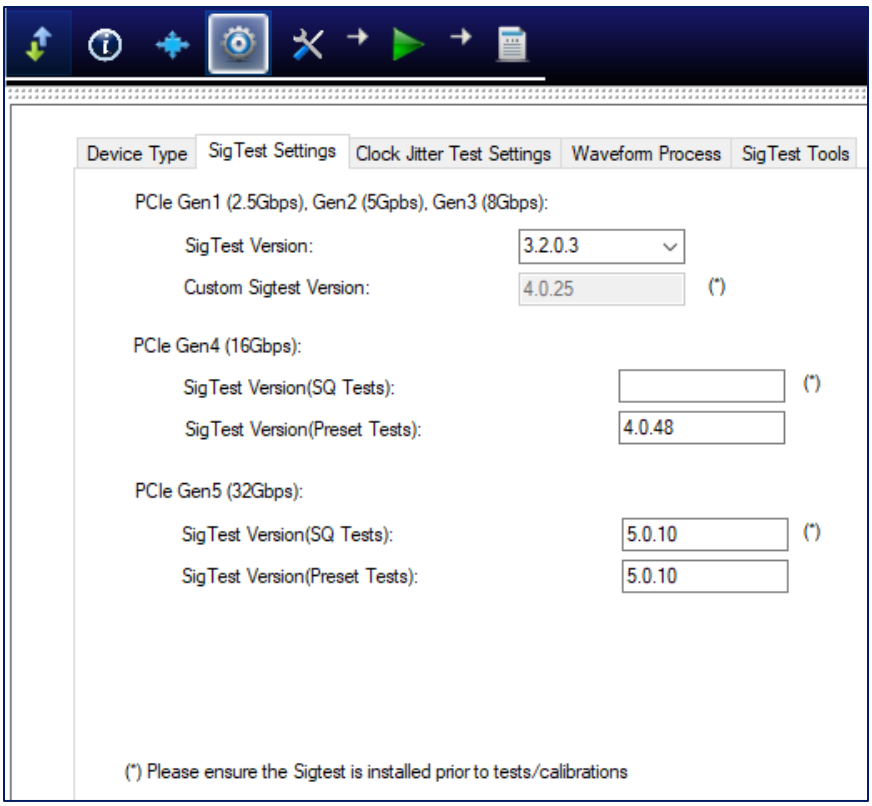


FIGURE 17. SET UP SIGTEST

c) **Clock Jitter Test Settings** tab: Enter the version of the Clock Jitter Tool, and select the type and file directory of the template to be used for the System Ref Clock Jitter Test.

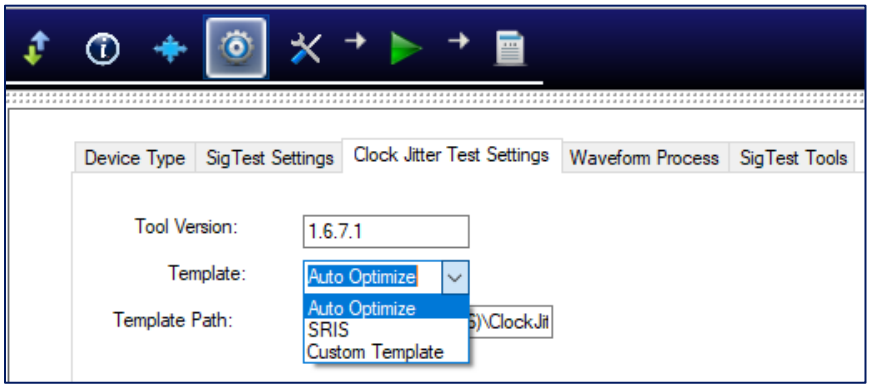


FIGURE 18. CONFIGURE SETTINGS FOR SYSTEM REF CLOCK JITTER TEST

d) **Waveform Process** tab: Select "Live Capture" to acquire PCIe waveforms by the GRL software, or select "Process Pre-captured waveforms" to use existing waveforms that have been previously captured and saved for analysis. *Note that selecting "Process Pre-captured waveforms" will remove the "Waveform Acquisition" group from the Select Tests page. See Section 4.2.5.1.*

If "Process Pre-captured waveforms" is selected, enter the directory of the saved waveform file in the Pre-Captured Waveform Path field.

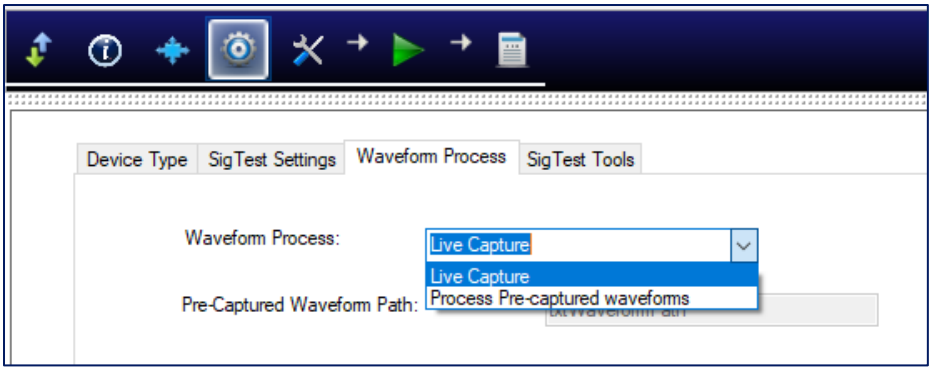


FIGURE 19. SET UP WAVEFORM PROCESSING

4.2.5 Select Compliance Tests

Once test requirements are defined, select **Test List** from the top "Windows" drop-down menu to display and access all tests available for the selected DUT type. User can select any of these tests to perform DUT compliance testing for all PCIe parameters.

Note: The Select Tests page will only list DUT-specific tests. For example, if System Board is selected as the DUT, only those tests applicable for System Board will be shown. Other test parameters such as desired data rates and presets that were previously configured may also affect the test selection.

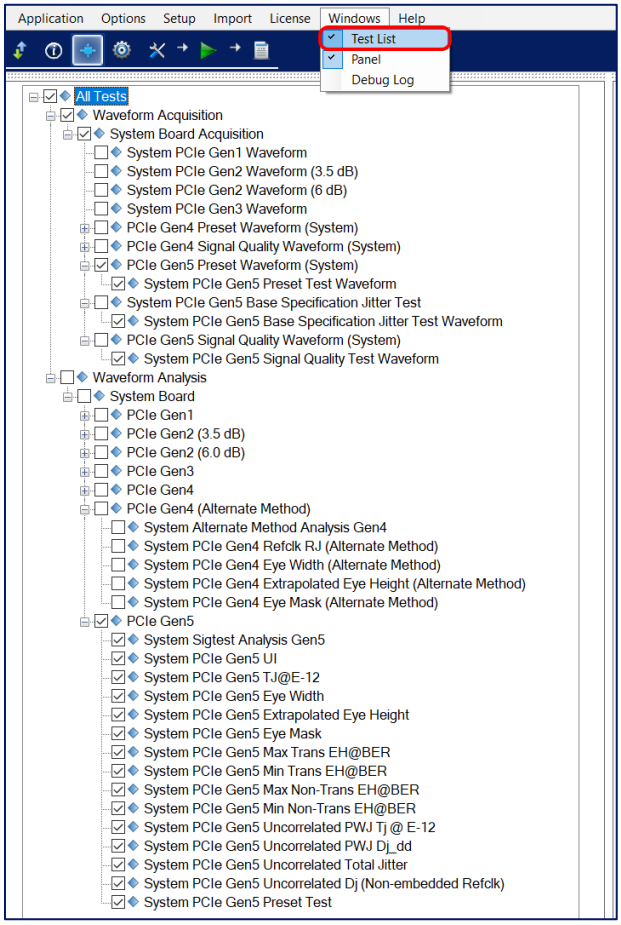


FIGURE 20. SELECT TESTS PAGE

4.2.5.1 Select to Acquire Waveforms

Under “Waveform Acquisition”, select the waveforms to capture for the required PCIe Gen5 DUT tests. The software will run a live capture of the selected waveforms prior to analysis.

Note: Waveform Acquisition can only be selected if “Live Capture” is set under the Waveform Process tab on the Setup Configuration page. See Section 4.2.4.

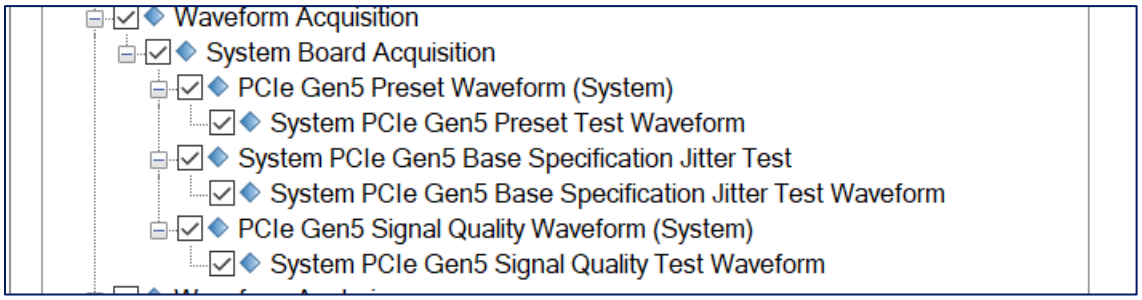


FIGURE 21. SELECT WAVEFORM TO CAPTURE FOR SYSTEM BOARD

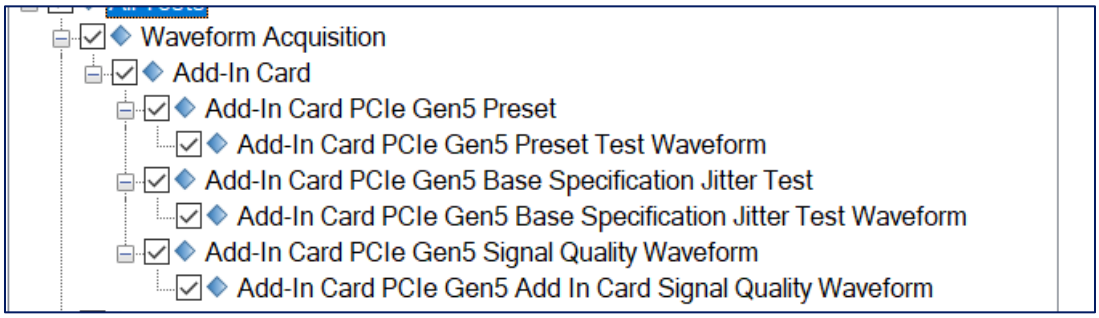


FIGURE 22. SELECT WAVEFORM TO CAPTURE FOR ADD-IN CARD

4.2.5.2 Select Waveform Analysis Tests

Under “Waveform Analysis”, select to perform the SigTest analysis, jitter and eye measurements, and preset test for the applicable PCIe Gen5 waveform. The software will automatically run the selected tests when initiated.

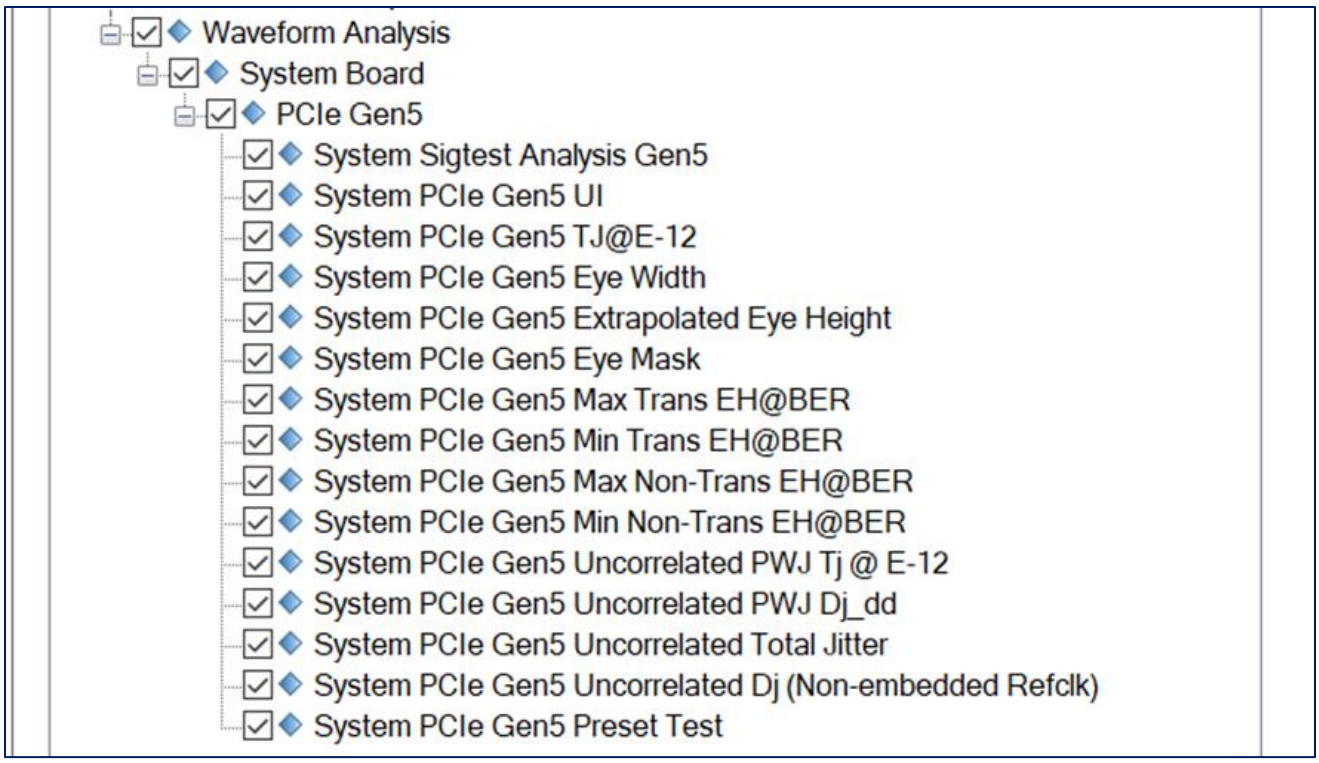


FIGURE 23. SELECT WAVEFORM ANALYSIS TESTS FOR SYSTEM BOARD

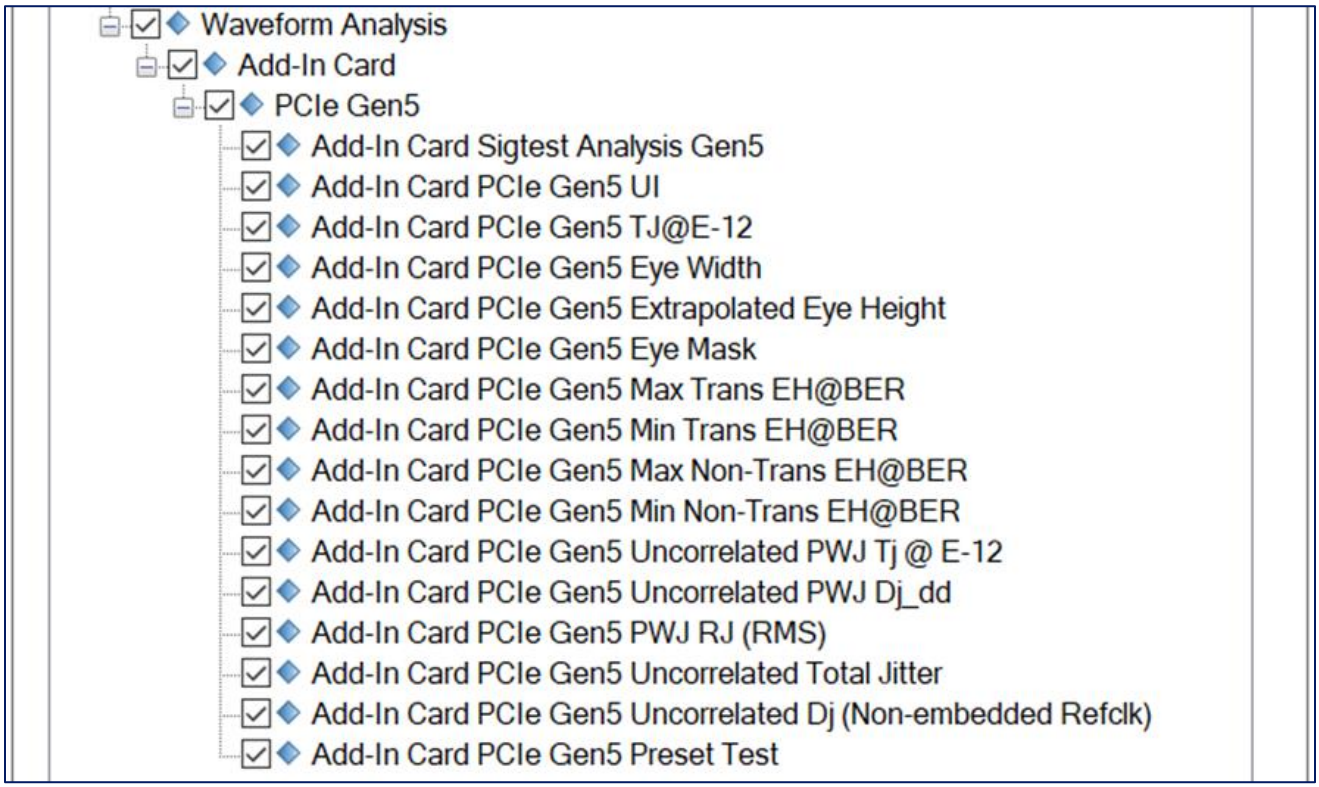


FIGURE 24. SELECT WAVEFORM ANALYSIS TESTS FOR ADD-IN CARD

4.2.6 Configure Test Parameters

After selecting the desired tests, select  from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.

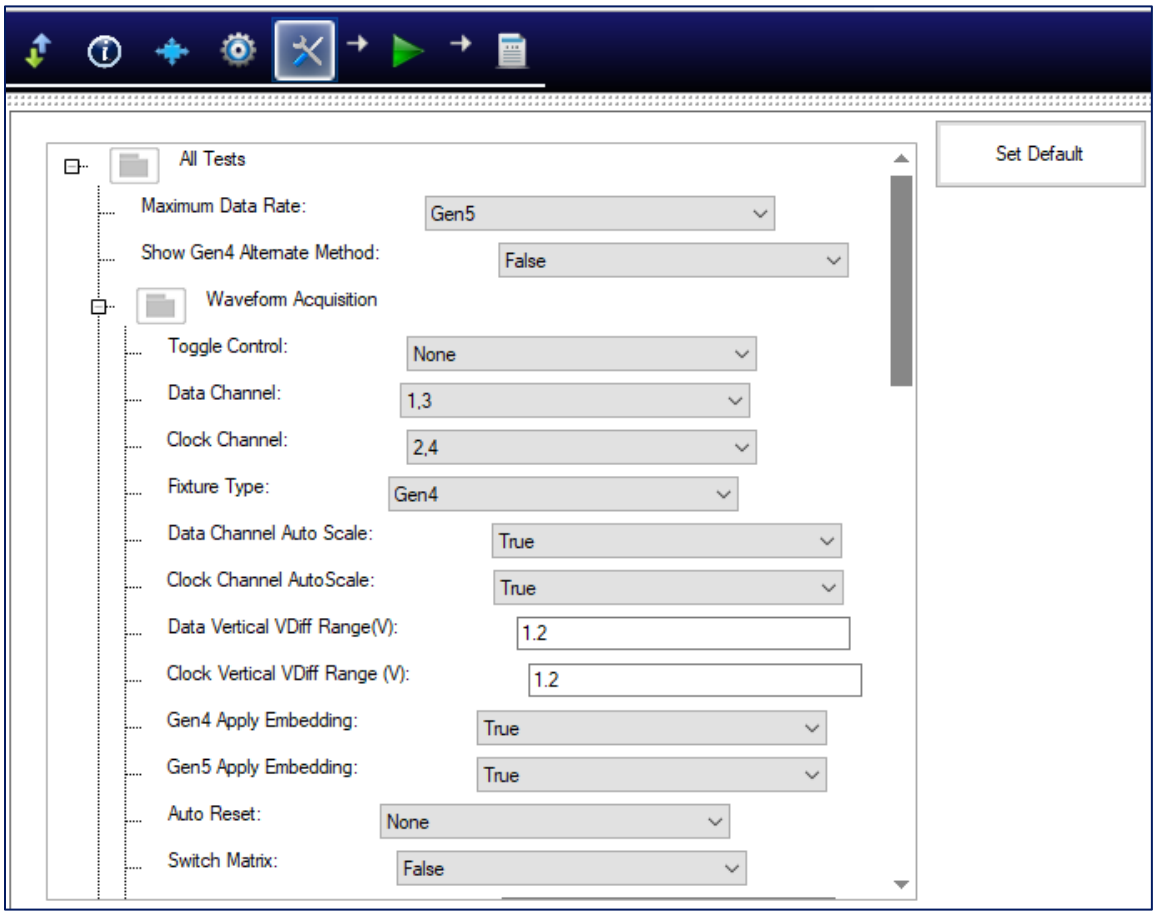


FIGURE 25. TEST PARAMETERS CONFIGURATION PAGE

TABLE 4. TEST PARAMETERS DESCRIPTION

Parameter	Description
Maximum Data Rate	Select the highest level for the PCIe data rate to perform tests.
Show Gen4 Alternate Method	Select "True" to enable the alternate method of performing PCIe Gen4 System Signal Quality test where the Data and 100 MHz Reference Clock can be captured and post-processed separately.
Toggle Control	Select to use the GRL-P1 hardware controller to provide compliance toggle signal to control the compliance state of the DUT. Select "None" if using manual compliance toggle.

Data/Clock Channel	Select the Scope channels that are connected to the Data Lanes and Reference Clock of the respective test fixture.
Fixture Type	Select a PCIe compliance test fixture in use.
Data/Clock Channel Auto Scale	Select “True” to enable autoscaling for connected Data or Reference Clock channels on the Scope.
Data/Clock Vertical V_{Diff} Range (V)	Set the vertical range of the Scope to easily detect a change to the voltage level when running tests.
Gen4 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen4.
Gen5 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen5.
Auto Reset	Select the option to automatically power cycle the controller during tests.
Switch Matrix	Select “True” to enable using an RF switch in the test setup.
Wait Time After Reset (ms)	If “Auto Reset” has been enabled for the controller, specify the time interval in milliseconds to stand by after reset.
Gen4 System/AIC Embedding File	If “Gen4 Apply Embedding” has been set to “True”, enter the name of the file to be used for embedding of the PCIe Gen4 system board or add-in card.
Gen5 System/AIC Embedding File	If “Gen5 Apply Embedding” has been set to “True”, enter the name of the file to be used for embedding of the PCIe Gen5 system board or add-in card.
UI (M) [Gen1/Gen2/Gen3/Gen4/Gen5]	Specify the number of sample points to capture for each data rate.
Sample Rate (Gb/s) [Gen1/Gen2/Gen3/Gen4/Gen5]	Specify the real-time sample rate in Gb/s to capture the required waveform data.
Gen3/Gen4/Gen5 Signal Quality Test Preset	Select the preset to be applied for PCIe Gen3, Gen4 or Gen5 signal quality test.
User Real Edge (Gen5)	Select “True” to use real edge channels for PCIe Gen5 compliance testing.
SigTest Run Mode	Select the SigTest to run Sequential or Parallel signal quality testing to ensure waveform compliance.
SigTest Max Thread	Specify the maximum number of threads for each SigTest run.

SSC Support	Select “True” to enable Spread Spectrum Clock (SSC) capabilities for testing (if supported by the DUT).

4.3 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PCIE-TX software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

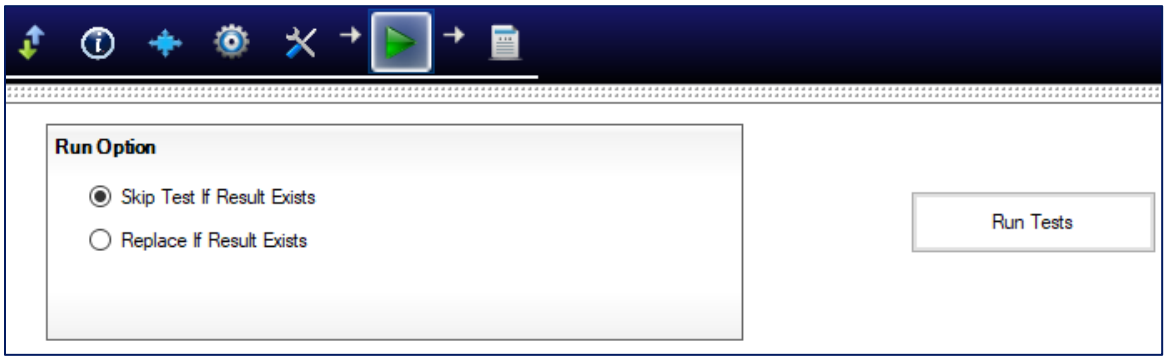


FIGURE 26. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed. Follow the step by step instructions to complete the entire testing.

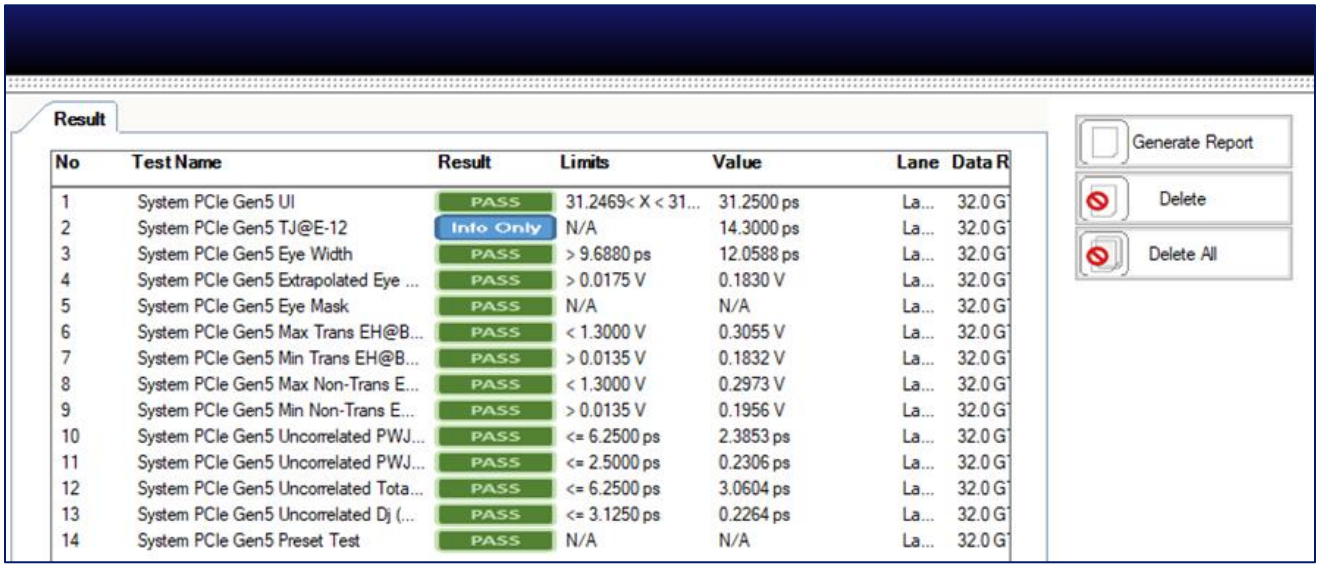
5 Interpreting GRL-PCIE-TX Test Report

When all test runs have completed from Section 4, the GRL-PCIE-TX software will automatically display the test results on the **Report** page.

Select  from the menu to access the Report page to view the results from each test run.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

Also select the **Generate report** button to generate a detailed test report in the PDF format.



No	Test Name	Result	Limits	Value	Lane	Data R
1	System PCIe Gen5 UI	PASS	31.2469< X < 31...	31.2500 ps	La...	32.0 G
2	System PCIe Gen5 TJ@E-12	Info Only	N/A	14.3000 ps	La...	32.0 G
3	System PCIe Gen5 Eye Width	PASS	> 9.6880 ps	12.0588 ps	La...	32.0 G
4	System PCIe Gen5 Extrapolated Eye ...	PASS	> 0.0175 V	0.1830 V	La...	32.0 G
5	System PCIe Gen5 Eye Mask	PASS	N/A	N/A	La...	32.0 G
6	System PCIe Gen5 Max Trans EH@B...	PASS	< 1.3000 V	0.3055 V	La...	32.0 G
7	System PCIe Gen5 Min Trans EH@B...	PASS	> 0.0135 V	0.1832 V	La...	32.0 G
8	System PCIe Gen5 Max Non-Trans E...	PASS	< 1.3000 V	0.2973 V	La...	32.0 G
9	System PCIe Gen5 Min Non-Trans E...	PASS	> 0.0135 V	0.1956 V	La...	32.0 G
10	System PCIe Gen5 Uncorrelated PWJ...	PASS	<= 6.2500 ps	2.3853 ps	La...	32.0 G
11	System PCIe Gen5 Uncorrelated PWJ...	PASS	<= 2.5000 ps	0.2306 ps	La...	32.0 G
12	System PCIe Gen5 Uncorrelated Tota...	PASS	<= 6.2500 ps	3.0604 ps	La...	32.0 G
13	System PCIe Gen5 Uncorrelated Dj (...	PASS	<= 3.1250 ps	0.2264 ps	La...	32.0 G
14	System PCIe Gen5 Preset Test	PASS	N/A	N/A	La...	32.0 G

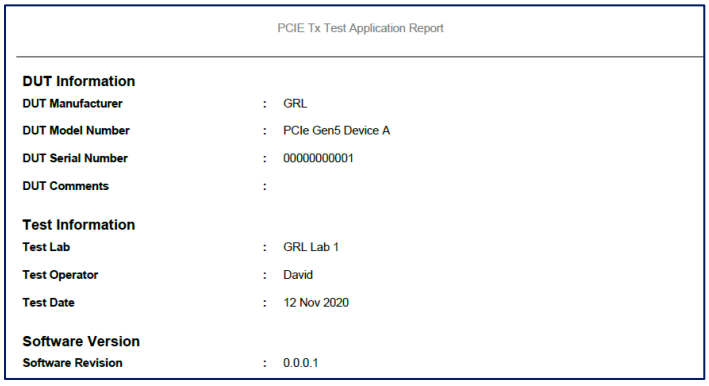
FIGURE 27. TEST REPORT PAGE

5.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

5.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.



PCIE Tx Test Application Report

DUT Information

DUT Manufacturer	:	GRL
DUT Model Number	:	PCIe Gen5 Device A
DUT Serial Number	:	00000000001
DUT Comments	:	

Test Information

Test Lab	:	GRL Lab 1
Test Operator	:	David
Test Date	:	12 Nov 2020

Software Version

Software Revision	:	0.0.0.1

FIGURE 28. TEST SESSION INFORMATION EXAMPLE

5.1.2 Test Summary Table

This table provides an overall view of all the tests performed along with their test conditions and results.

PCIE Tx Test Application Report

No	TestName	Limits	Value	Results	Lane	Data Rate	Preset
1	System PCIe Gen5 UI	31.2469< X < 31.2531 ps	31.2500 ps	Pass	Lane0	Gen5	P9
2	System PCIe Gen5 TJ@E-12	N/A	14.3000 ps	InfoOnly	Lane0	Gen5	P9
3	System PCIe Gen5 Eye Width	> 9.6880 ps	12.0588 ps	Pass	Lane0	Gen5	P9
4	System PCIe Gen5 Extrapolated Eye Height	> 0.0175 V	0.1830 V	Pass	Lane0	Gen5	P9
5	System PCIe Gen5 Eye Mask	N/A	N/A	Pass	Lane0	Gen5	P9
6	System PCIe Gen5 Max Trans EH@BER	< 1.3000 V	0.3055 V	Pass	Lane0	Gen5	P9
7	System PCIe Gen5 Min Trans EH@BER	> 0.0135 V	0.1832 V	Pass	Lane0	Gen5	P9
8	System PCIe Gen5 Max Non-Trans EH@BER	< 1.3000 V	0.2973 V	Pass	Lane0	Gen5	P9
9	System PCIe Gen5 Min Non-Trans EH@BER	> 0.0135 V	0.1956 V	Pass	Lane0	Gen5	P9
10	System PCIe Gen5 Uncorrelated PWJ Tj @ E-12	<= 6.2500 ps	2.3853 ps	Pass	Lane0	Gen5	N/A
11	System PCIe Gen5 Uncorrelated PWJ Dj_dd	<= 2.5000 ps	0.2306 ps	Pass	Lane0	Gen5	N/A
12	System PCIe Gen5 Uncorrelated Total Jitter	<= 6.2500 ps	3.0604 ps	Pass	Lane0	Gen5	N/A
13	System PCIe Gen5 Uncorrelated Dj (Non-embedded Refclk)	<= 3.1250 ps	0.2264 ps	Pass	Lane0	Gen5	N/A
14	System PCIe Gen5 Preset Test	N/A	N/A	Pass	Lane0	Gen5	N/A

FIGURE 29. TEST SUMMARY TABLE EXAMPLE

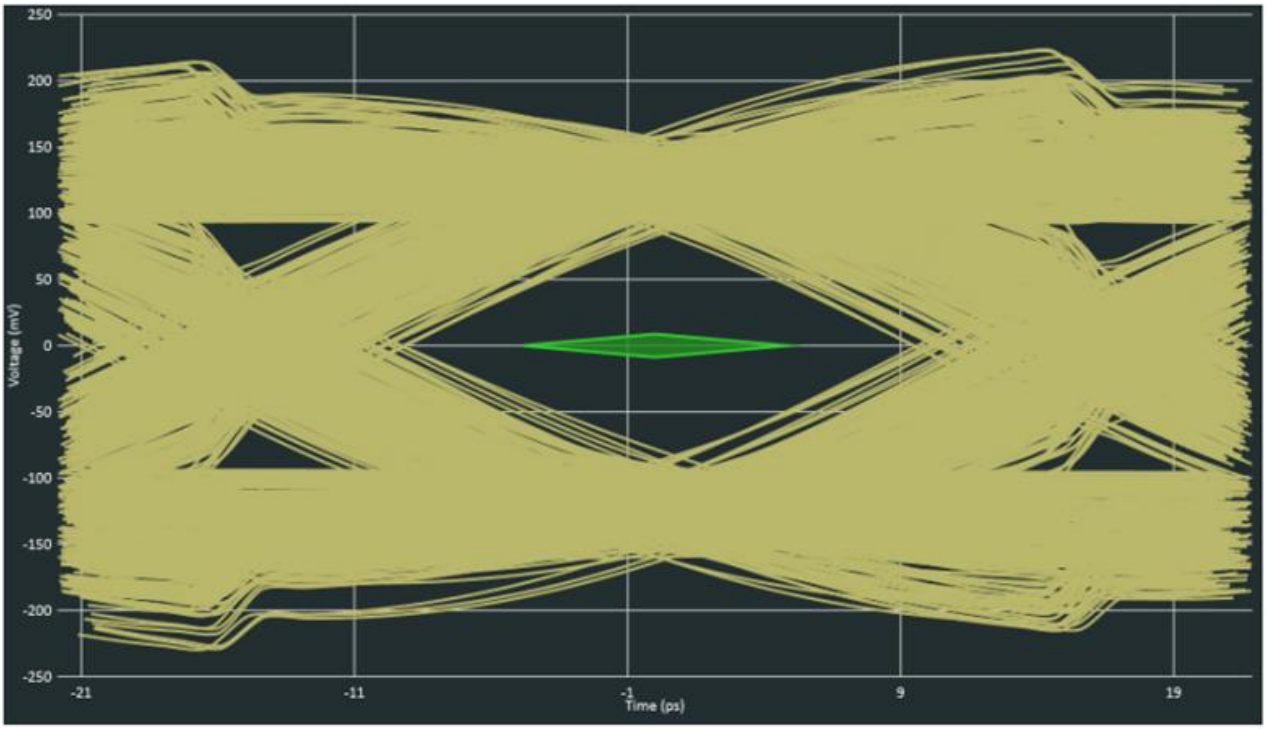
5.1.3 Test Results

This portion displays the results of each test performed in detail along with supporting data points and screenshots.

17. System PCIe Gen5 Eye Mask [Lane0,Gen5,P9]

Pass/Fail Stats	:	Pass
SigTest Version	:	5.1.01
DUT Type:	:	System Board
Composite Eye Height	:	205.8006 mV
Composite Eye Width	:	17.2100 ps
EH @ BER	:	180.8013 mV
EW @ BER	:	12.1100 ps
Connector Type	:	CEM
Test completed time	:	16 December 2021 2:22:19 AM

Composite Eyes (Best CTLE -5.00000000050129)



10. System PCIe Gen5 Uncorrelated PWJ Tj @ E-12 [Lane0,Gen5]

Pass/Fail Stats	:	Pass
Test Limits	:	<= 6.2500 ps
Result	:	2.3853 ps
SigTest Version	:	5.0.24
DUT Type:	:	System Board
PWJ TJ	:	2.385313E-12
Connector Type	:	CEM
Test completed time	:	31 August 2021 22:18:30 PM

11. System PCIe Gen5 Uncorrelated PWJ Dj_dd [Lane0,Gen5]

Pass/Fail Stats	:	Pass
Test Limits	:	<= 2.5000 ps
Result	:	0.2306 ps
SigTest Version	:	5.0.24
DUT Type:	:	System Board
PWJ DjDD	:	0.230616E-12
Connector Type	:	CEM
Test completed time	:	31 August 2021 22:18:31 PM

12. System PCIe Gen5 Uncorrelated Total Jitter [Lane0,Gen5]

Pass/Fail Stats	:	Pass
Test Limits	:	<= 6.2500 ps
Result	:	3.0604 ps
SigTest Version	:	5.0.24
DUT Type:	:	System Board
TIE TJ	:	3.060381E-12
Connector Type	:	CEM
Test completed time	:	31 August 2021 22:18:31 PM

13. System PCIe Gen5 Uncorrelated Dj (Non-embedded Refclk) [Lane0,Gen5]

Pass/Fail Stats	:	Pass
Test Limits	:	<= 3.1250 ps
Result	:	0.2264 ps
SigTest Version	:	5.0.24
DUT Type:	:	System Board
TIE DjDD	:	0.226376E-12
Test completed time	:	31 August 2021 22:18:31 PM

14. System PCIe Gen5 Preset Test [Lane0,Gen5]

Pass/Fail Stats	:	Pass
P0 Pass/Fail	:	PASS
P0 Preshoot	:	-363.4200 mdB
P0 De Emphasis	:	-6.0069 dB
P1 Pass/Fail	:	PASS
P1 Preshoot	:	-271.6500 mdB
P1 De Emphasis	:	-3.4873 dB
P2 Pass/Fail	:	PASS
P2 Preshoot	:	-277.6200 mdB
P2 De Emphasis	:	-4.3406 dB
P3 Pass/Fail	:	PASS
P3 Preshoot	:	-125.5800 mdB
P3 De Emphasis	:	-2.4308 dB
P4 Pass/Fail	:	PASS
P4 Preshoot	:	0.00000E+000 dB
P4 De Emphasis	:	0.00000E+000 dB
P5 Pass/Fail	:	PASS
P5 Preshoot	:	1.6587 dB
P5 De Emphasis	:	70.0000 mdB
P6 Pass/Fail	:	PASS
P6 Preshoot	:	2.3270 dB
P6 De Emphasis	:	49.7100 mdB
P7 Pass/Fail	:	PASS
P7 Preshoot	:	3.1536 dB
P7 De Emphasis	:	-6.0173 dB
P8 Pass/Fail	:	PASS
P8 Preshoot	:	3.3240 dB

FIGURE 30. TEST RESULTS EXAMPLE

5.2 Delete Test Results

Select the **Delete** button to delete individual test results or **Delete All** to delete all test results.

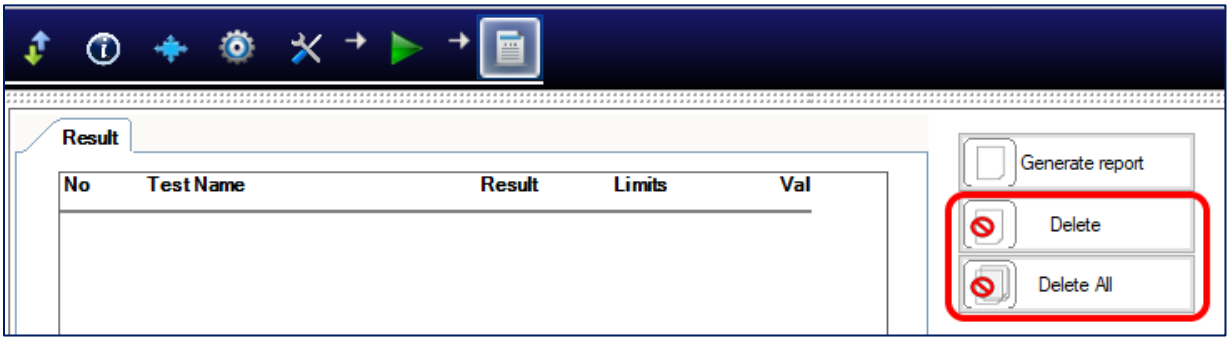


FIGURE 31. DELETE TEST RESULTS

6 Saving and Loading GRL-PCIE-TX Test Sessions

The usage model for the GRL-PCIE-TX software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select "Save Session".
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → "Load Session".
- To ***create a new test session*** and return the application back to the default configuration, select Options → "New Session".

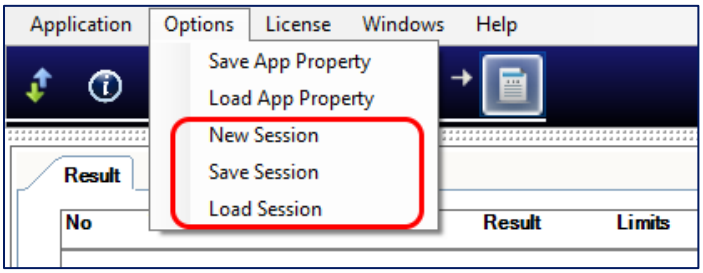


FIGURE 32. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

7 Appendix A: Method of Implementation (MOI) for Manual PCIe 5.0 Transmitter Measurements

This section describes how to manually perform PCIe 5.0 CEM based Tx compliance testing following the recommended test procedure from the PCI Express Architecture PHY Test Specification Rev 5.0.

The following steps give a general overview for testing the PCIe 5.0 CEM based Tx DUT:

i) Test for System Board & Add-in Card DUT Tx Signal Quality compliance:
   - 2.0M UI acquisition for any Tx EQ Preset (P0-P10)
   - Post-processing of acquired waveforms with SigTest Phoenix for:
     - Eye Width ≥ 10.625 ps and Eye Height ≥ 22 mV (for Add-In Card DUT)
     - Eye Width ≥ 9.688 ps and Eye Height ≥ 17.5 mV (for System Board DUT)

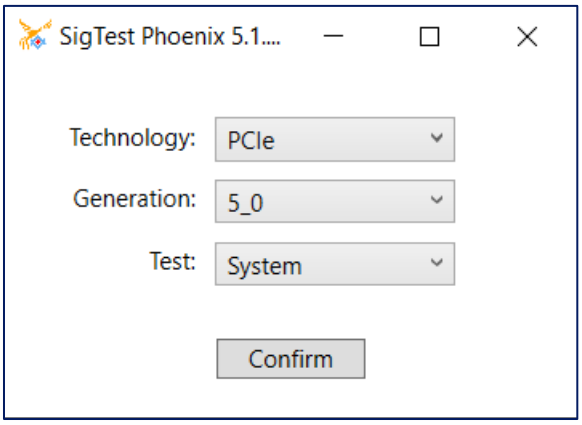
ii) Test for System Board & Add-in Card DUT Base Jitter (UPW-TJ, UPW-DJDD, UTJ and UDJDD) compliance:
   - 2.0M UI acquisition and post-processing of acquired waveforms with SigTest Phoenix for:
     - UPW-TJ ≤ 6.25 ps
     - UPW-DJDD ≤ 2.5 ps
     - UTJ ≤ 6.25 ps
     - UDJDD ≤ 3.125 ps

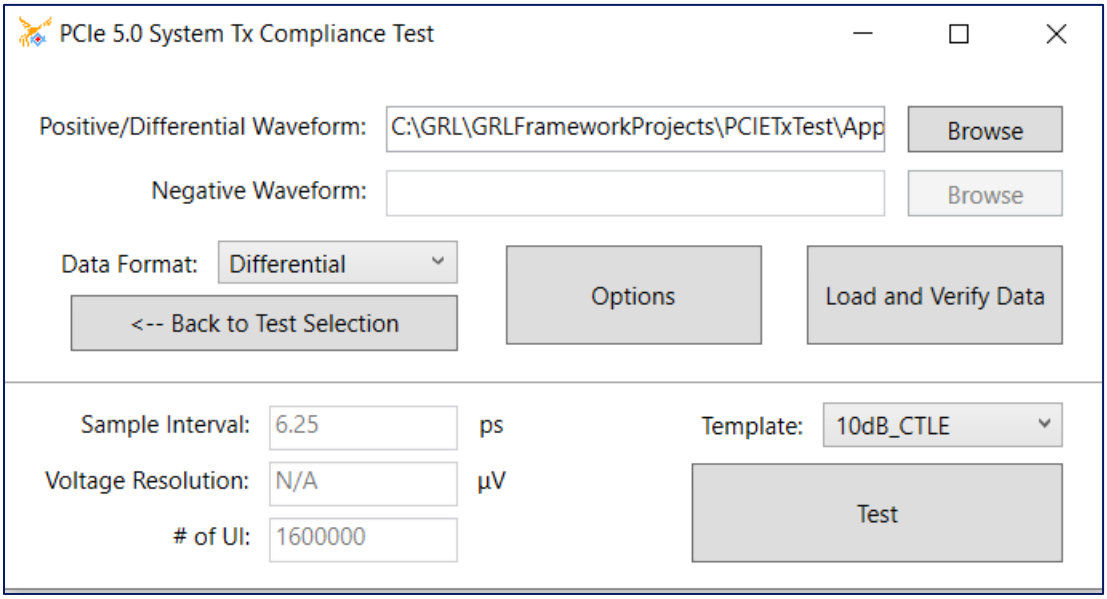
7.1 System Board Tx Signal Quality Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

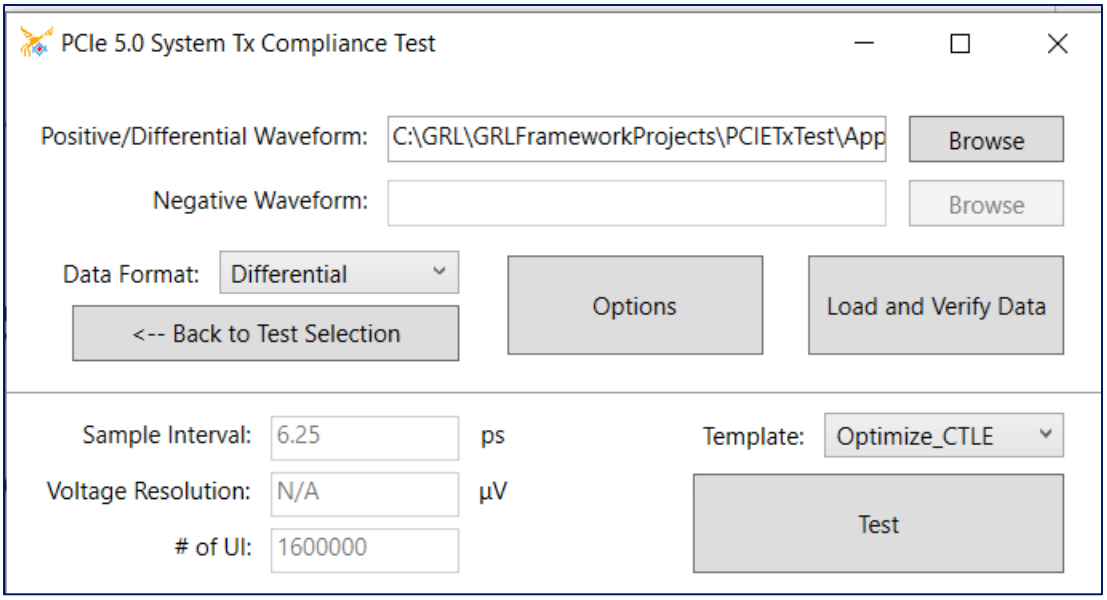
1. Set up the test equipment as described in Section 4.2.1.
2. Adjust the Scope to capture 2M UI's using the following configuration:
   - Bandwidth: 33 GHz
   - Sampling Rate: ≥ 128 GS/s (2x interpolation allowed)
3. Refer to "Appendix B, Section B.11, Target Loss Values – Tx Signal Quality" in the *PCI Express Architecture PHY Test Specification, Revision 5.0, Version 0.9* to determine the target loss and locate the S4P file to be embedded on the Scope.
4. Push the compliance toggle on the DUT to transmit 32 GT/s compliance pattern by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
5. On the Scope, capture 2.0M UI's for any Tx EQ Preset (P0-P10). Save the captured waveforms to be used for post-processing.

6. To test for signal quality, load the saved waveform files in SigTest Phoenix (by selecting **PCIe → 5_0 → System → Browse → Load and Verify Data**). *[Make sure the file contains the appropriate trace loss and package model losses embedded with the captured waveform as well as both data and clock.]*

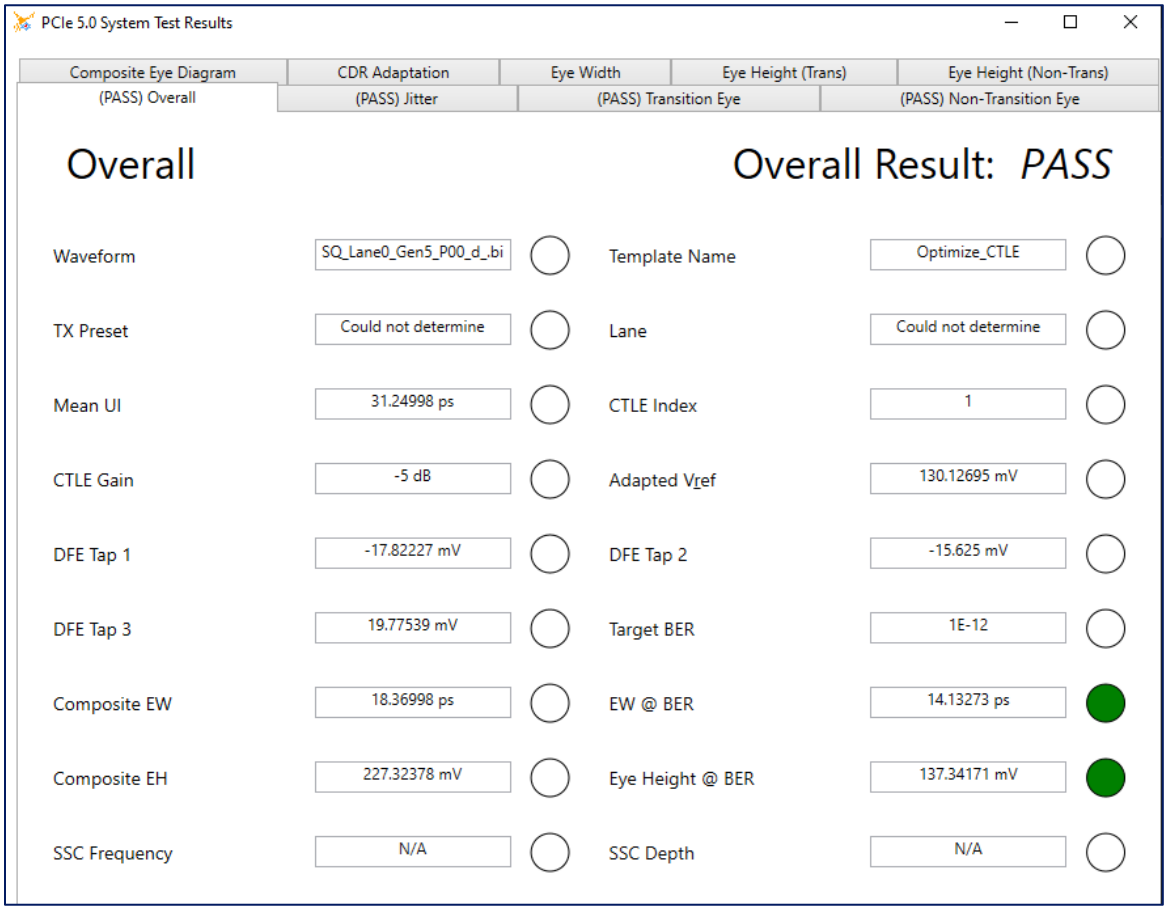




7. Measure both the Eye Height and Eye Width @1e-12 on SigTest Phoenix using the ***"PCIe\5_0\System\Optimize_CTLE"*** template file.



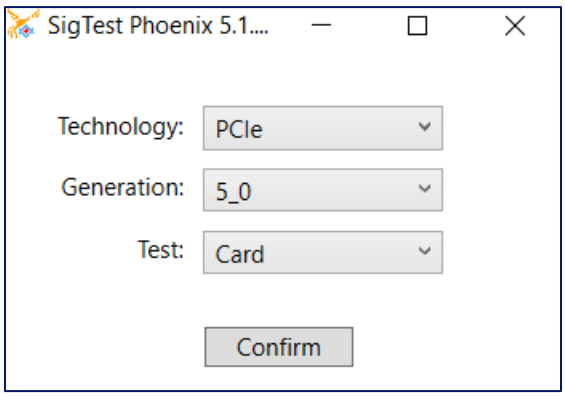
8. Make sure that each DUT test lane achieves the following target Eye Height and Eye Width values for at least one Tx EQ Preset:
   - Eye Width ≥ 9.688 ps ±0.5 ps
   - Eye Height ≥ 17.5 mV ±1.5 mV

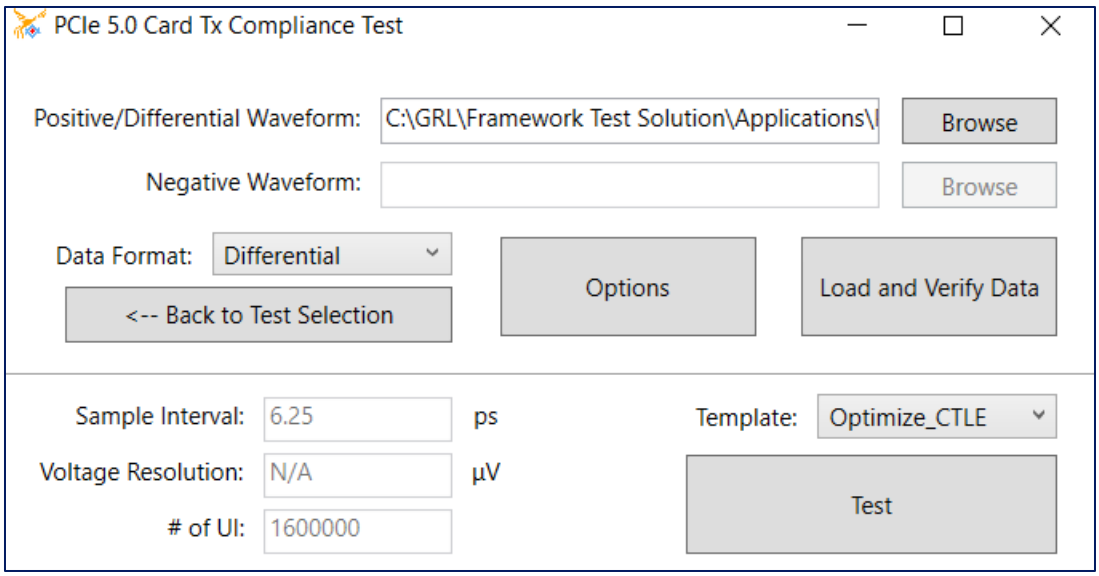


7.2 Add-in Card Tx Signal Quality Test

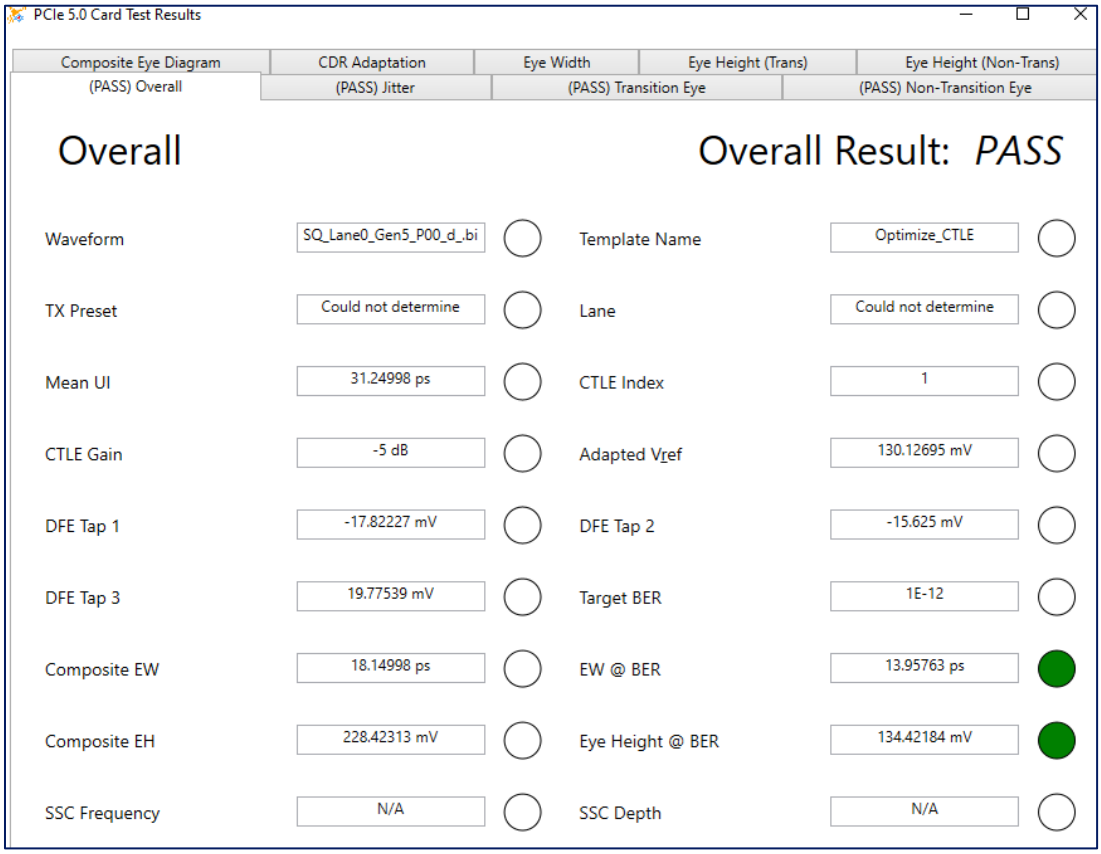
Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.2.
2. Turn on SSC on the CBB (-0.5% SSC down-spread).
3. Adjust the Scope to capture 2M UI's using the following configuration:
    - Bandwidth: 33 GHz
    - Sampling Rate: ≥ 128 GS/s (2x interpolation allowed)
4. Refer to "Appendix B, Section B.11, Target Loss Values – Tx Signal Quality" in the *PCI Express Architecture PHY Test Specification, Revision 5.0, Version 0.9* to determine the target loss and locate the S4P file to be embedded on the Scope.
5. Push the compliance toggle on the DUT to transmit 32 GT/s compliance pattern by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
6. On the Scope, capture 2.0M UI's for any Tx EQ Preset (P0-P10). Save the captured waveforms to be used for post-processing.
7. To test for signal quality, load the saved waveform files in SigTest Phoenix (by selecting **PCIe → 5_0 → Card → Browse → Load and Verify Data**) *(Make sure the file contains the appropriate trace loss and package model losses embedded with the captured waveform as well as both data and clock.)*





8. Measure both the Eye Height and Eye Width @1e-12 on SigTest Phoenix using the **"*PCIe\5_0\Card\Optimize_CTLE*"** template file.
9. Make sure that each DUT test lane achieves the following target Eye Height and Eye Width values for at least one Tx EQ Preset:
   - Eye Width ≥ 10.625 ps ±0.5 ps
   - Eye Height ≥ 22 mV ±1.5 mV



7.3 System Board Tx Preset Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.1.
2. Adjust the Scope to display Preset 0 (P0) at 32 GT/s with the following configuration:
    - Bandwidth: 33 GHz
    - Sampling Rate: ≥ 128 GS/s (2x interpolation allowed)
    - No embedding
3. Push the compliance toggle on the DUT to capture Presets 0 to 10 (P0-P10) on Lane 0. Save the captured presets to be used for post-processing.
4. Save waveforms of all presets as "System_Lane**X**_Gen5_P0**Y**_d_.**wtf**", where:
    - X = Lane number (0 to 15)
    - Y = Preset number (0 to 10)
    - wtf = waveform format (for example, .wfm for Tekscope waveform or .bin for Keysight waveform)
5. To test the presets, load the saved preset files in SigTest Phoenix (by selecting **PCIe → 5_0 → PresetTestAC → Template "No_CTLE" → Browse**) and run the preset tests (by selecting **Test**).
6. When the preset tests have completed, select **Exit** to save the test results.

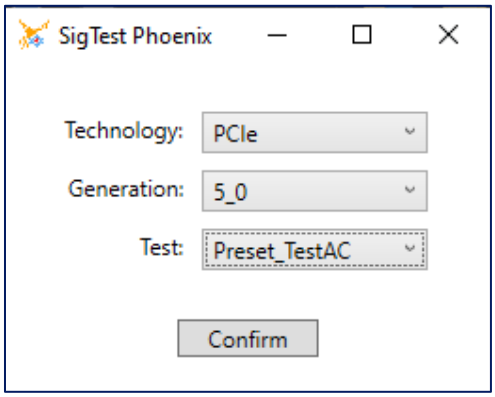
7.4 Add-In Card Tx Preset Test

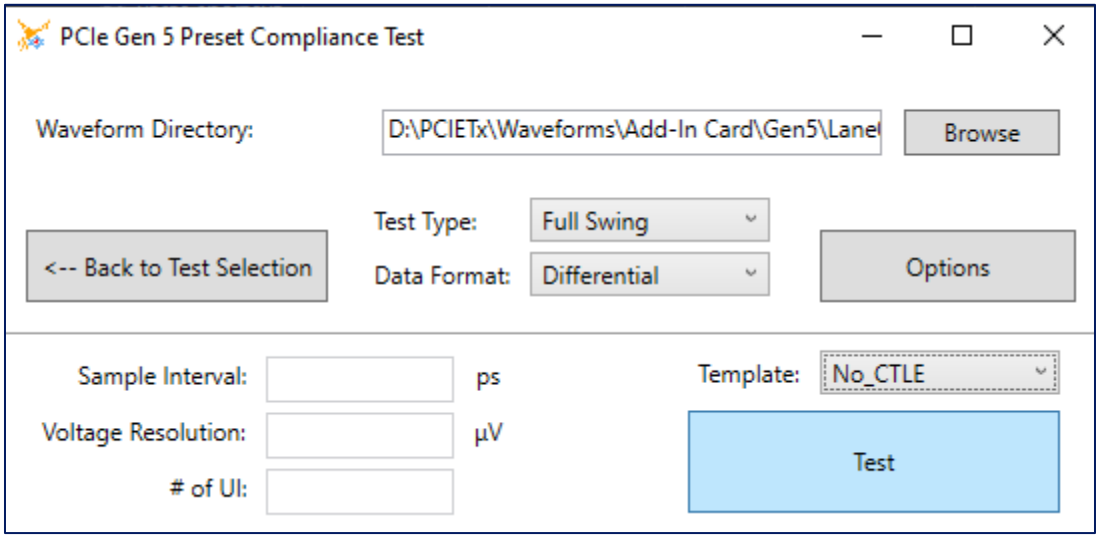
Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

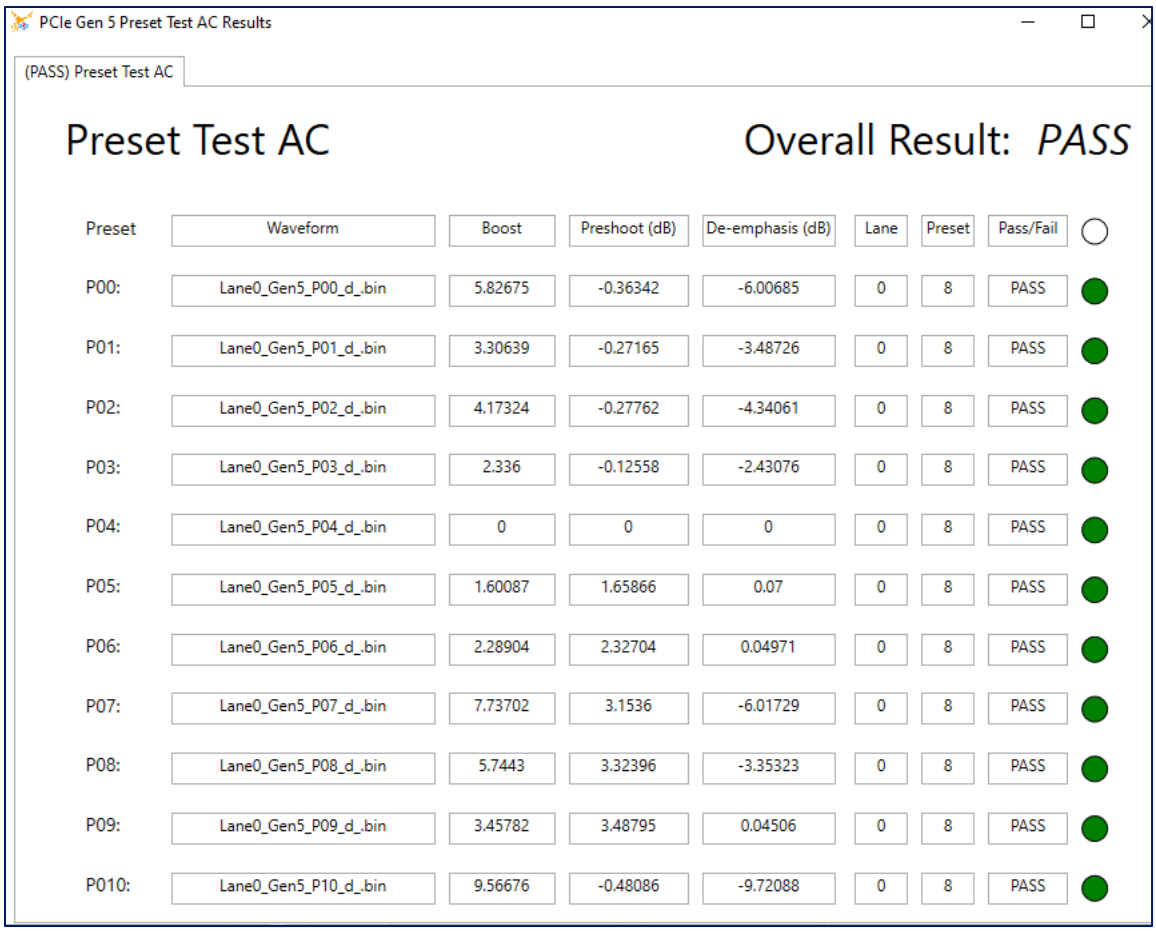
1. Set up the test equipment as described in Section 4.2.2.
2. Turn on SSC on the CBB (-0.5% SSC down-spread).
3. Adjust the Scope to display Preset 0 (P0) at 32 GT/s with the following configuration:
    - Bandwidth: 33 GHz
    - Sampling Rate: ≥ 128 GS/s (2x interpolation allowed)
    - No embedding
4. Push the compliance toggle on the DUT to capture Presets 0 to 10 (P0-P10) on Lane 0. Save the captured presets to be used for post-processing.
5. Save waveforms of all presets as "AIC_Lane**X**_Gen5_P0**Y**_d_.**wtf**", where:
    - X = Lane number (0 to 15)
    - Y = Preset number (0 to 10)

- wtf = waveform format (for example, .wfm for Tekscope waveform or .bin for Keysight waveform)

6. To test the presets, load the saved preset files in SigTest Phoenix (by selecting **PCIe → 5_0 → PresetTestAC → Template "No_CTLE" → Browse**) and run the preset tests (by selecting **Test**).







Preset	Waveform	Boost	Preshoot (dB)	De-emphasis (dB)	Lane	Preset	Pass/Fail
P00:	Lane0_Gen5_P00_d_.bin	5.82675	-0.36342	-6.00685	0	8	PASS
P01:	Lane0_Gen5_P01_d_.bin	3.30639	-0.27165	-3.48726	0	8	PASS
P02:	Lane0_Gen5_P02_d_.bin	4.17324	-0.27762	-4.34061	0	8	PASS
P03:	Lane0_Gen5_P03_d_.bin	2.336	-0.12558	-2.43076	0	8	PASS
P04:	Lane0_Gen5_P04_d_.bin	0	0	0	0	8	PASS
P05:	Lane0_Gen5_P05_d_.bin	1.60087	1.65866	0.07	0	8	PASS
P06:	Lane0_Gen5_P06_d_.bin	2.28904	2.32704	0.04971	0	8	PASS
P07:	Lane0_Gen5_P07_d_.bin	7.73702	3.1536	-6.01729	0	8	PASS
P08:	Lane0_Gen5_P08_d_.bin	5.7443	3.32396	-3.35323	0	8	PASS
P09:	Lane0_Gen5_P09_d_.bin	3.45782	3.48795	0.04506	0	8	PASS
P010:	Lane0_Gen5_P10_d_.bin	9.56676	-0.48086	-9.72088	0	8	PASS

7. When the preset tests have completed, select **Exit** to save the test results.

7.5 System Board Tx Base Jitter (UPW-TJ, UPW-DJDD, UTJ and UDJDD) Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

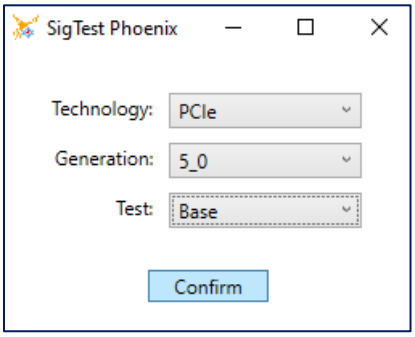
1. Set up the test equipment as described in Section 4.2.1.
2. Adjust the Scope to capture 2M UI's with the following configuration:
    - Bandwidth: 33 GHz
    - Sampling Rate: ≥ 128 GS/s
    - No embedding
3. Push the compliance toggle on the DUT to transmit 32 GT/s Jitter Measurement pattern (setting #47 on Lane 0 in the PCIe 5.0 Base Specification and COMPAT on adjacent lanes) by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
4. On the Scope, capture 2.0M UI's and save the captured waveforms to be used for post-processing.
5. To measure UPW-TJ, UPW-DJDD, UTJ, and UDJDD, load the saved waveform files in SigTest Phoenix (by selecting **PCIe → 5_0 → Base → Browse → Load and Verify Data**).

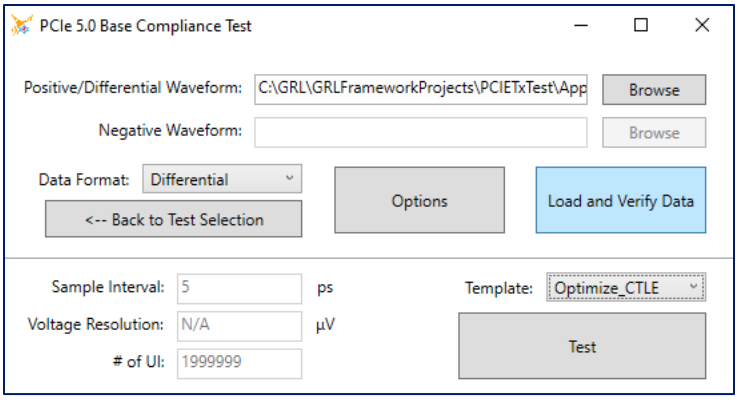
6. Measure UPW-TJ, UPW-DJDD, UTJ, and UDJDD @1e-12 on SigTest Phoenix using the **"*Templates**PCIe**5_0**Base**Optimize_CTLE*"** template file and select **Test** to start the measurements.
7. The test is considered as Pass if the following target jitter parameter values are met:
    - UPW-TJ ≤ 6.25 ps
    - UPW-DJDD ≤ 2.5 ps
    - UTJ ≤ 6.25 ps
    - UDJDD ≤ 3.125 ps

7.6 Add-In Card Tx Base Jitter (UPW-TJ, UPW-DJDD, UTJ and UDJDD) Test

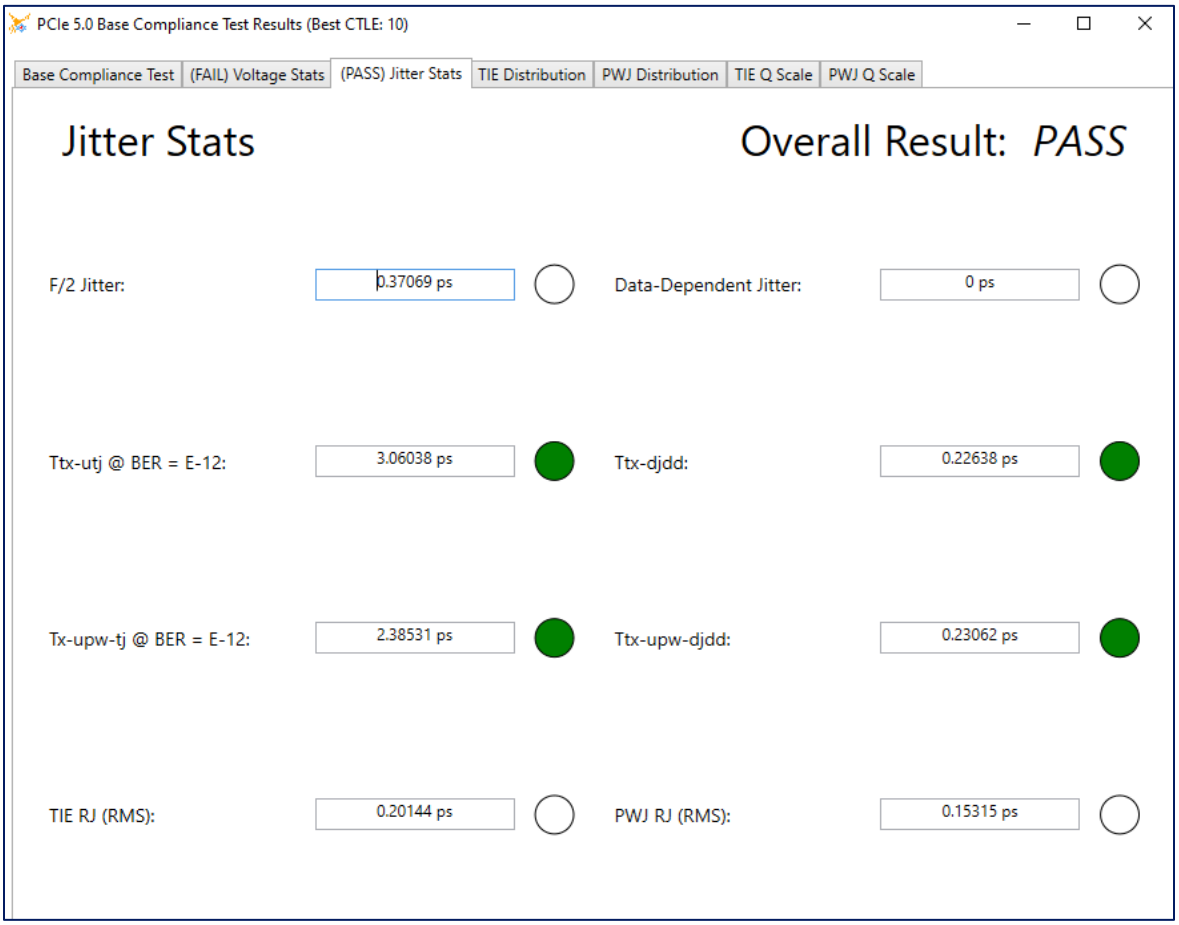
Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.2.
2. Adjust the Scope to capture 2M UI's with the following configuration:
    - Bandwidth: 33 GHz
    - Sampling Rate: ≥ 128 GS/s
    - No embedding
3. Turn on SSC on the CBB (-0.5% SSC down-spread).
4. Push the compliance toggle on the DUT to transmit 32 GT/s Jitter Measurement pattern (setting #47 on Lane 0 in the PCIe 5.0 Base Specification and COMPAT on adjacent lanes) by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
5. On the Scope, capture 2.0M UI's and save the captured waveforms to be used for post-processing.
6. To measure UPW-TJ, UPW-DJDD, UTJ, and UDJDD, load the saved waveform files in SigTest Phoenix (by selecting **PCIe → 5_0 → Base → Browse → Load and Verify Data**).
7. Measure UPW-TJ, UPW-DJDD, UTJ, and UDJDD @1e-12 on SigTest Phoenix using the **"*Templates**PCIe**5_0**Base**Optimize_CTLE*"** template file and select **Test** to start the measurements.





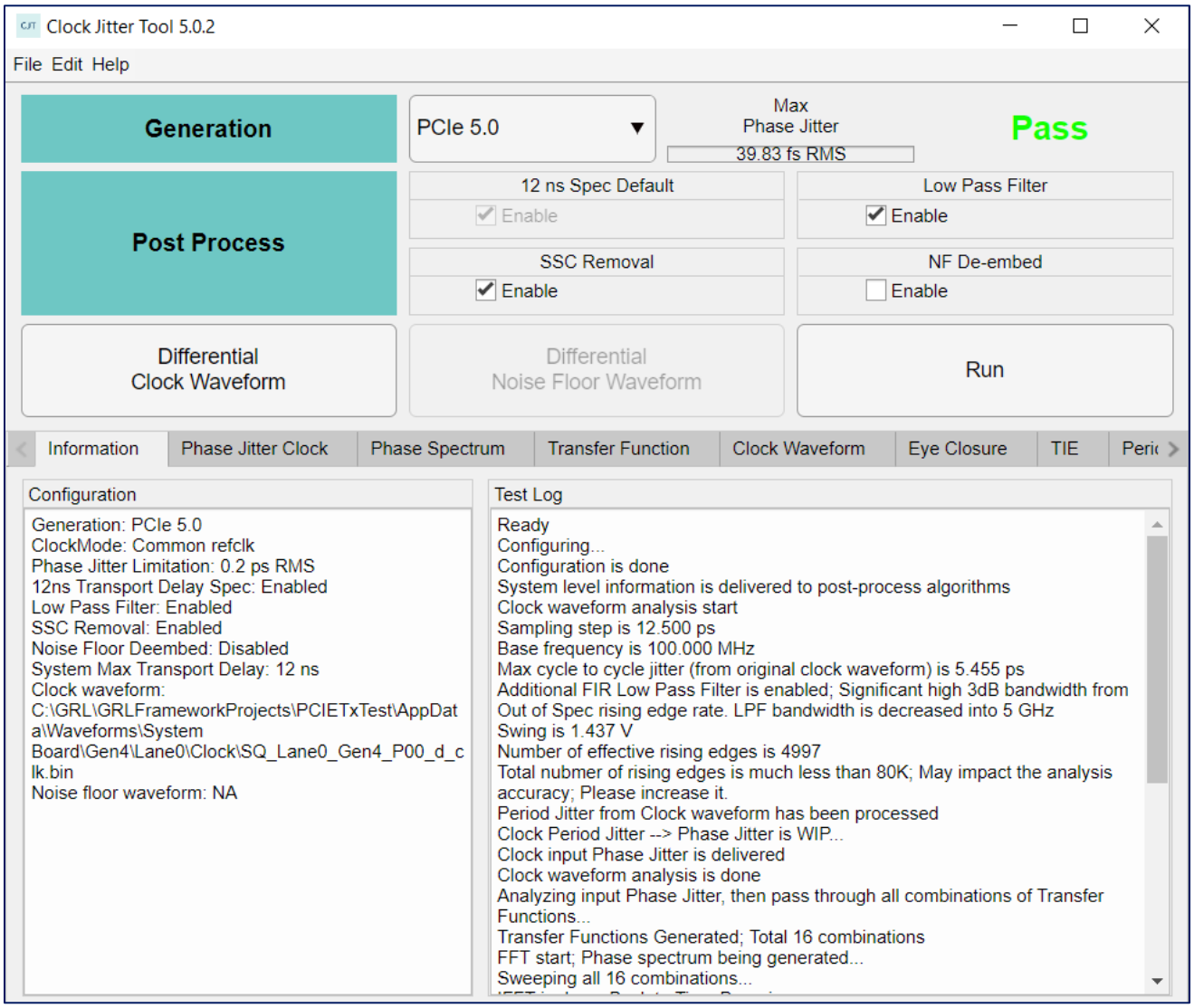
8. The test is considered as Pass if the following target jitter parameter values are met:
   - UPW-TJ ≤ 6.25 ps
   - UPW-DJDD ≤ 2.5 ps
   - UTJ ≤ 6.25 ps
   - UDJDD ≤ 3.125 ps



7.7 System Board Ref Clock (100 MHz) Jitter Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.3.
2. Adjust the Scope to capture >80K Clock Cycle (80000 * 10 ns = 0.8 ms).
3. SSC can be turned ON or OFF depending on the system board DUT.
4. Using the Clock Jitter Tool, measure the HF RJ RMS (Max Phase Jitter) as shown in figure below.



5. The test is considered as Pass if the HF RJ RMS (Max Phase Jitter) is ≤ 200 fs.

8 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

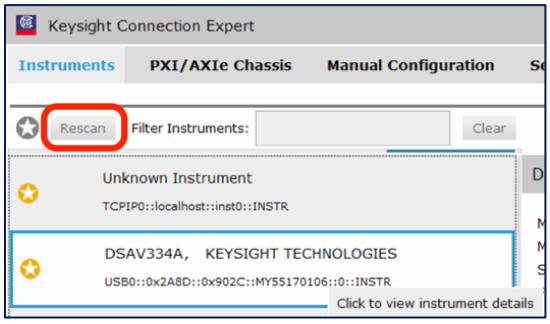


FIGURE 33. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

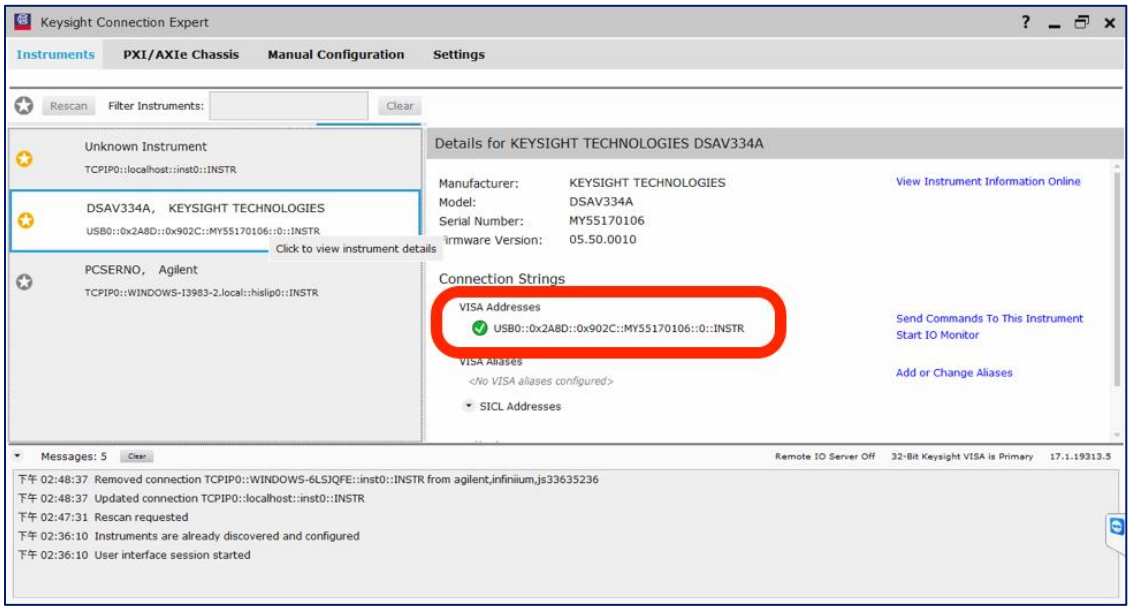


FIGURE 34. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe Tx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

9 Appendix C: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

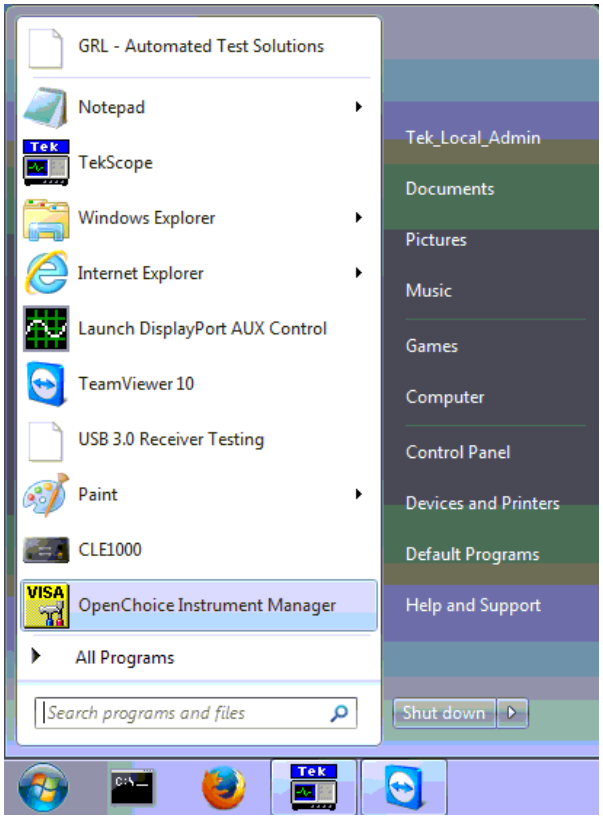


FIGURE 35. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
   a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
   b) “Search Criteria”: Select to configure the instrument search function.
   c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
   d) “Properties”: Select to display and view the selected instrument properties.

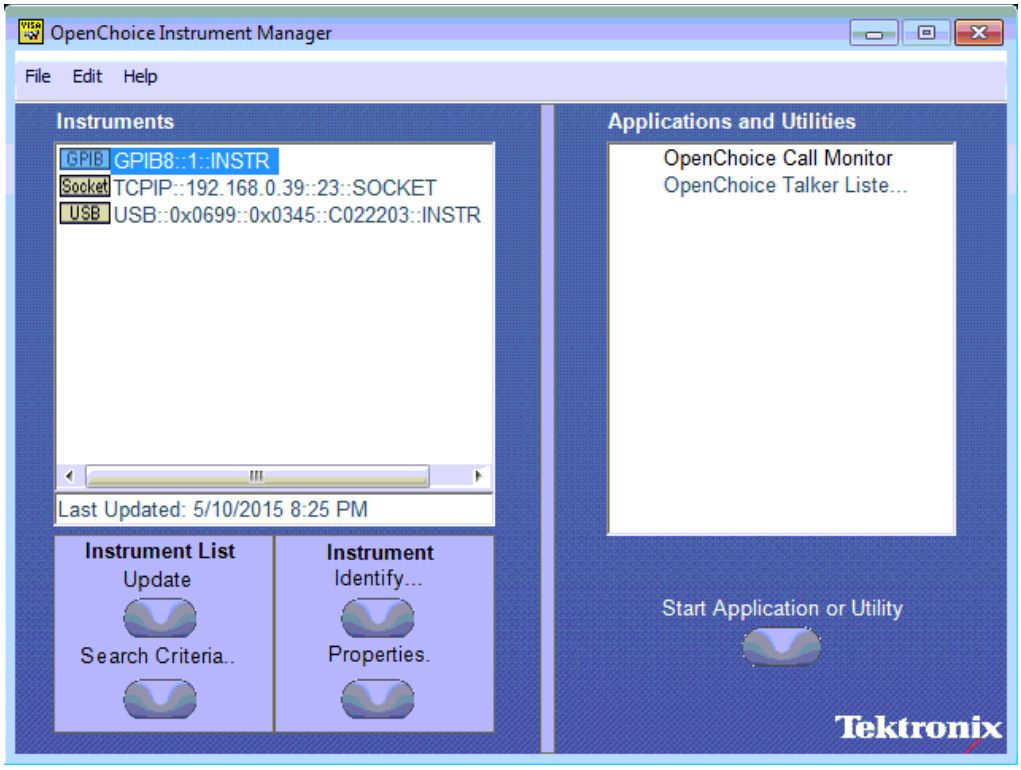


FIGURE 36. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe Tx Test Application, type in the Scope address into the ‘Address’ field. If the GRL PCIe Tx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to ***omit*** the Port number from the address.

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