Granite River Labs

GRL-PCIE-PLL Phase-Locked Loop (PLL) Calibration and Test Automation Software

User Guide/Method of Implementation (MOI)

Using
Anritsu High Performance BERT,
High Performance Real-Time Oscilloscope
with
GRL-PCIE-PLL Automation Software

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1 Introduction

This MOI & User Guide describes how to set up and test a PCIe Add-In Card device using the GRL-PCIE-PLL automation software for the PCIe Gen1 to Gen5 data rates. The PCIe PLL test is one of the test items defined for PCIe Add-In Card Tx compliance testing. The bandwidth and peaking of the PLL is measured and checked against the compliance values defined in the PCIe specification.

The GRL-PCIE-PLL software when run from a control computer or oscilloscope automates calibration and tests for PLL bandwidth compliance of the Add-In Card DUT. The test automation is carried out based on PCI-SIG-approved Methods of Implementation (MOI's) with the Anritsu BERT Model (MP1900A) and high performance real-time oscilloscopes using existing PCI-SIG Compliance Base Boards (CBB's). Optionally, the GRL PCIe hardware controller ("GRL-P1") or an arbitrary function generator can be used in the test setup to provide compliance toggle to control the state of the DUT. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

Note: For manual test methodology, refer to Appendix of this documentation or approved vendor-specific MOI's as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT type. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description/Key Specification Requirement
GRL-PCIE-PLL	1	Granite River Labs PCI Express PLL Compliance Calibration & Test Automation Software – www.graniteriverlabs.com *– with Node Locked License to single Oscilloscope/PC OS*
High Performance Real-Time Oscilloscope [a]	1	≥ 33 GHz bandwidth with Windows 7+ OS [b]
Anritsu BERT [c]	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 32G bit/s SI Pulse Pattern Generator, or MU196020A 64.2G bit/s or 64.2G baud PAM4 Pulse Pattern Generator [d] • MU195050A Noise Generator *(Optional)*

System	Qty.	Description/Key Specification Requirement
PCI-SIG Compliance Base Board (CBB)	1	For add-in card DUT
[Optional]: GRL-PCIE4-P1 "GRL-P1" PCIe Compliance Test Hardware Controller	1	For PCIe 3.0 and 4.0 compliance toggle control
Advanced Technology eXtended (ATX) Power Supply	1	For power supply to the DUT
VISA (Virtual Instrument Software Architecture) API Software	1	VISA Software is required to be installed on the host PC running GRL-PCIE-PLL software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
Computer	1	Laptop or desktop PC running Windows 7+ OS for automation control

[a] *Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.*

[b] *Oscilloscope with scope bandwidth as specified in vendor specific MOI's.*

[c] *BERT PCIe PLL test patterns are distributed with GRL-PCIE-PLL software and are installed during installation process.*

[d] *The GRL-PCIE-PLL software supports PAM4 PPG in NRZ mode.*

TABLE 2. EQUIPMENT REQUIREMENTS – ACCESSORIES

Accessory	Qty.	Description/Key Specification Requirement
Phase-matched SMA cables	3 pairs	*– DUT connector type and test configuration dependent*
V(m) - K(f) Adapter	*2*	*34VKF50A Coaxial Adapter, only required if using a PAM4 Pulse Pattern Generator*
1-meter SMA coaxial cables	1 pair	*– DUT connector type and test configuration dependent*
Phase-matched K-K coaxial cables	1 pair	*– DUT connector type and test configuration dependent*
SMA-to-SMA cables	2	*– DUT connector type and test configuration dependent*

Accessory	Qty.	Description/Key Specification Requirement
Power Control Adapter Cable	1	
LAN cable	1	

3 Setting Up GRL-PCIE-PLL Automation Software

This section provides the procedures to start up and pre-configure the GRL-PCIE-PLL automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the GRL software, follow the procedures in the following sections.

3.1 Download GRL-PCIE-PLL Software

Download and install the GRL-PCIE-PLL software on a PC or an oscilloscope (where GRL-PCIE-PLL is referred to as 'Controller PC' or 'Scope' respectively in this User Guide & MOI):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-PCIE-PLL is to be used (see Section 2.1).
2. Download the software ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   - **PCIEPLLPatternFilesInstallation0000000xSetup.exe** – Run this on the Anritsu MP1900A BERT Signal Quality Analyzer to install the PCIE PLL test pattern setup files.
   - **PCIePLLTestApplication0000000xSetup.exe** – Run this on the Controller PC or Scope to install the GRL-PCIE-PLL application.
   - **PCIe_PLL_TestScopeSetupFilesInstallation0000000xSetup.exe** – Run this on the Scope to install the scope setup files.

3.2 Launch and Set Up GRL-PCIE-PLL Software

1. Once the GRL-PCIE-PLL software is installed, open the **GRL** folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

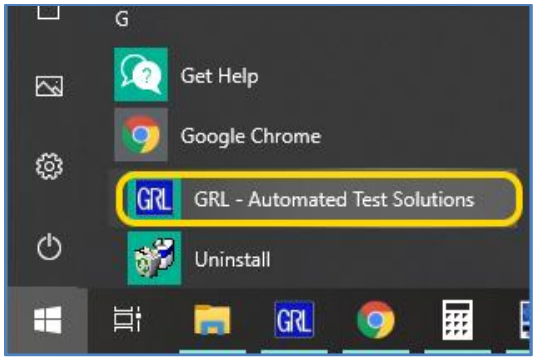


FIGURE 1. SELECT AND LAUNCH GRL FRAMEWORK

2. From the **Application → Framework Test Solution** drop-down menu, select **PCIE PLL Test Application** to start the GRL PCIe PLL Test Application. If the selection is grayed out, it means that your license has expired.

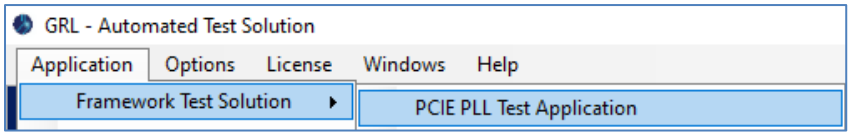


FIGURE 2. START GRL PCIE PLL TEST APPLICATION

3. To enable license, go to License→License Details.

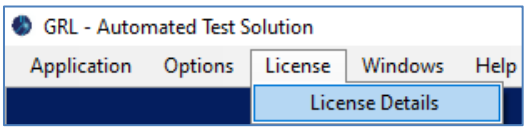


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

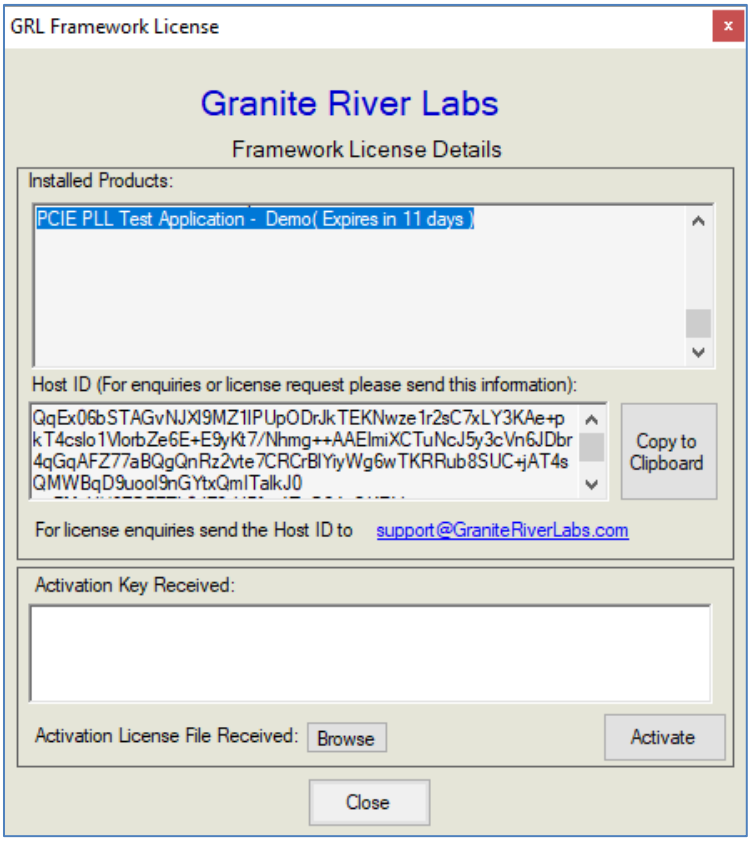


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the field provided and select “Activate”.

- If you do not have an Activation Key, select “Close” to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

4. Select the Equipment Setup icon  on the GRL PCIe PLL Test application menu.
4. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC. The BERT and MX183000A software can be connected using connection string formats similar to the following examples:
    - BERT: “TCPIP0::192.168.0.14::5001::SOCKET” or “192.168.0.14:5001”
    - MX183000A: “TCPIP0::192.168.0.14::5000::SOCKET” or “192.168.0.14:5000”

    Note the IP addresses listed above are only examples and should be changed according to the actual network connection being used.
5. Connect the oscilloscope with the GRL automation control enabled PC through either GPIB, USB or LAN. *(Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the controller PC is provided in the Appendix of this document.)*
6. If using the GRL-P1 hardware controller as the compliance toggle control, connect the GRL-P1 via USB to the GRL automation control enabled Scope or PC.
7. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Take note of these addresses as they will be used to connect the instruments to the GRL automation software.
8. On the Equipment Setup page of the GRL PCIe PLL Test application, type in the address of each connected instrument into the ‘Address’ field.

    *(Note: If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”.)*

    If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to ***omit*** the Port number from the address.

    *(Note: If the GRL software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as “TCPIP0::192.168.0.4::5025::SOCKET”.)*
9. Select the “lightning” button () for each connected instrument.

    The “lightning” button should turn green () once the GRL software has successfully established connection with each instrument.

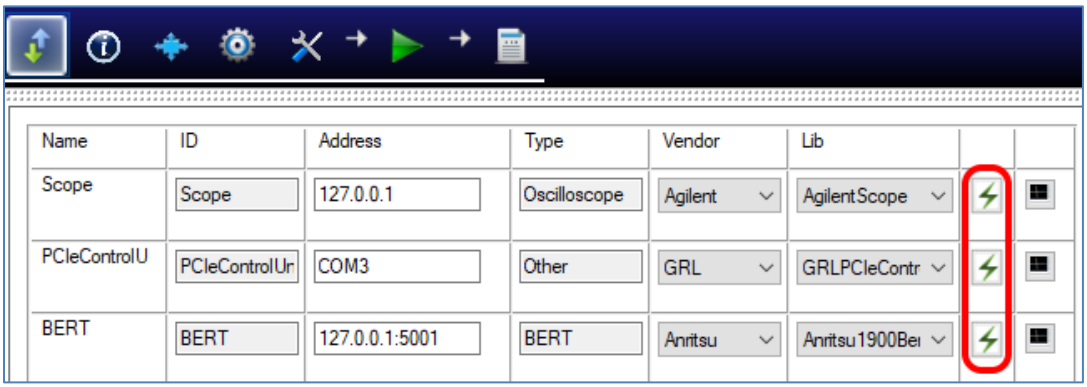


FIGURE 5. CONNECT INSTRUMENTS WITH GRL SOFTWARE

3.3 Pre-Configure GRL-PCIE-PLL Software Before Calibration/Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced measurement setup.

3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the GRL software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

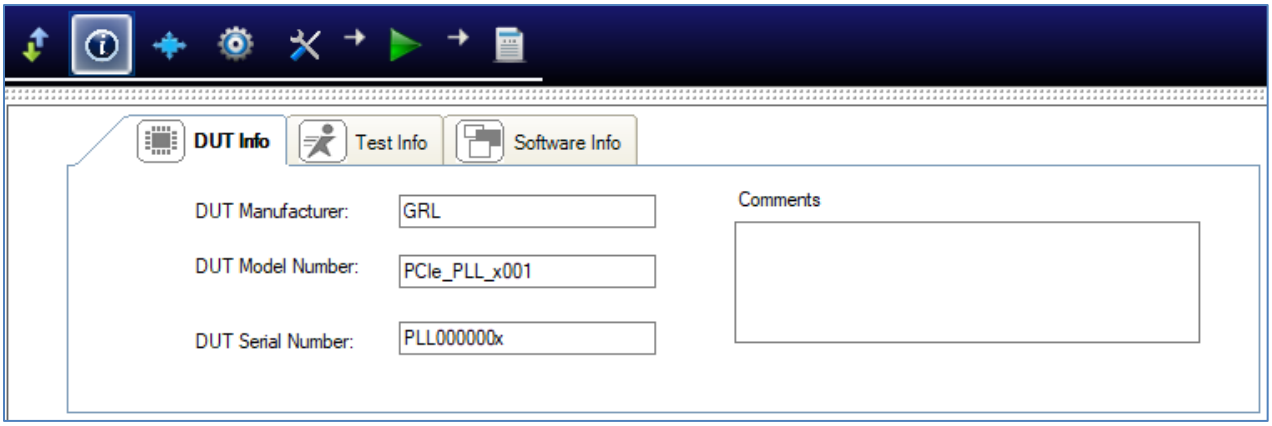


FIGURE 6. SESSION INFO PAGE

3.3.2 Set Measurement Conditions

Select  from the menu to access the **Conditions** page to set the conditions for calibration and compliance testing. The GRL software will perform calibration and testing using selected presets, PCIe Gen2 de-emphasis levels and sinusoidal jitter (SJ) frequencies for selected PCIe data rates.

Recommended procedure:

- *Step 1*: When calibrating, select all conditions that may be used for testing, and perform the calibration.
- *Step 2*: Once calibration is completed and ready for testing, re-select the necessary test conditions. For example, if required to test only at specific SJ frequencies, then select the appropriate conditions for testing.

a) **Data Rate** tab: Select the PCIe data rates as supported by the DUT for calibration and testing:

- For the PCIe Gen1 PLL test, select "2.5GT/s"
- For the PCIe Gen2 PLL test, select "5.0GT/s"
- For the PCIe Gen3 PLL test, select "8.0GT/s"
- For the PCIe Gen4 PLL test, select "16.0GT/s"
- For the PCIe Gen5 PLL test, select "32.0GT/s"

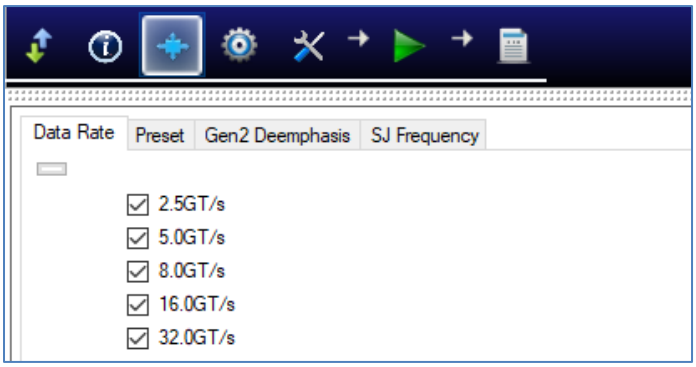


FIGURE 7. SELECT DATA RATES

b) **Preset** tab: Select the required pre-defined Tx EQ presets for testing. *Note: If you are not sure of which preset to use, select all presets.*

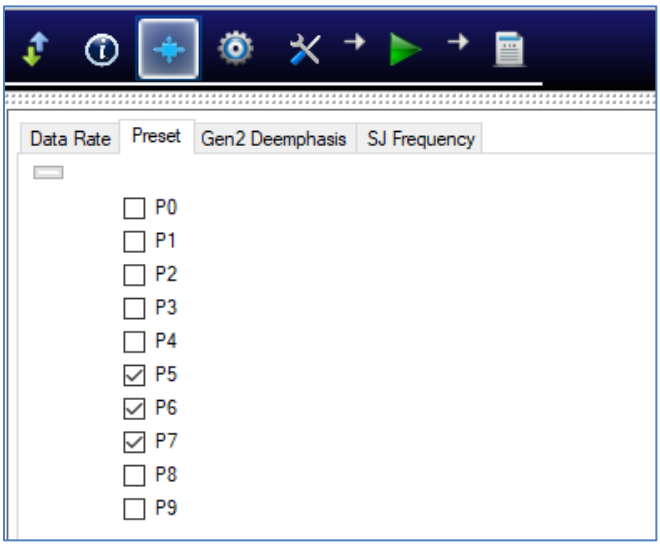


FIGURE 8. SELECT TX EQ PRESETS

c) **Gen2 Deemphasis** tab: Select the required de-emphasis levels for the PCIe Gen2 based DUT.

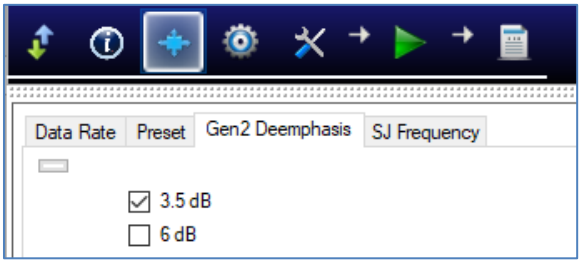


FIGURE 9. SELECT PCIE GEN2 DE-EMPHASIS LEVELS

d) **SJ Frequency** tab: Select the required SJ frequencies for calibration and testing. *[Note: The value of each SJ frequency can be configured through the Setup Configuration page. See Section 6.1 for more details.]*

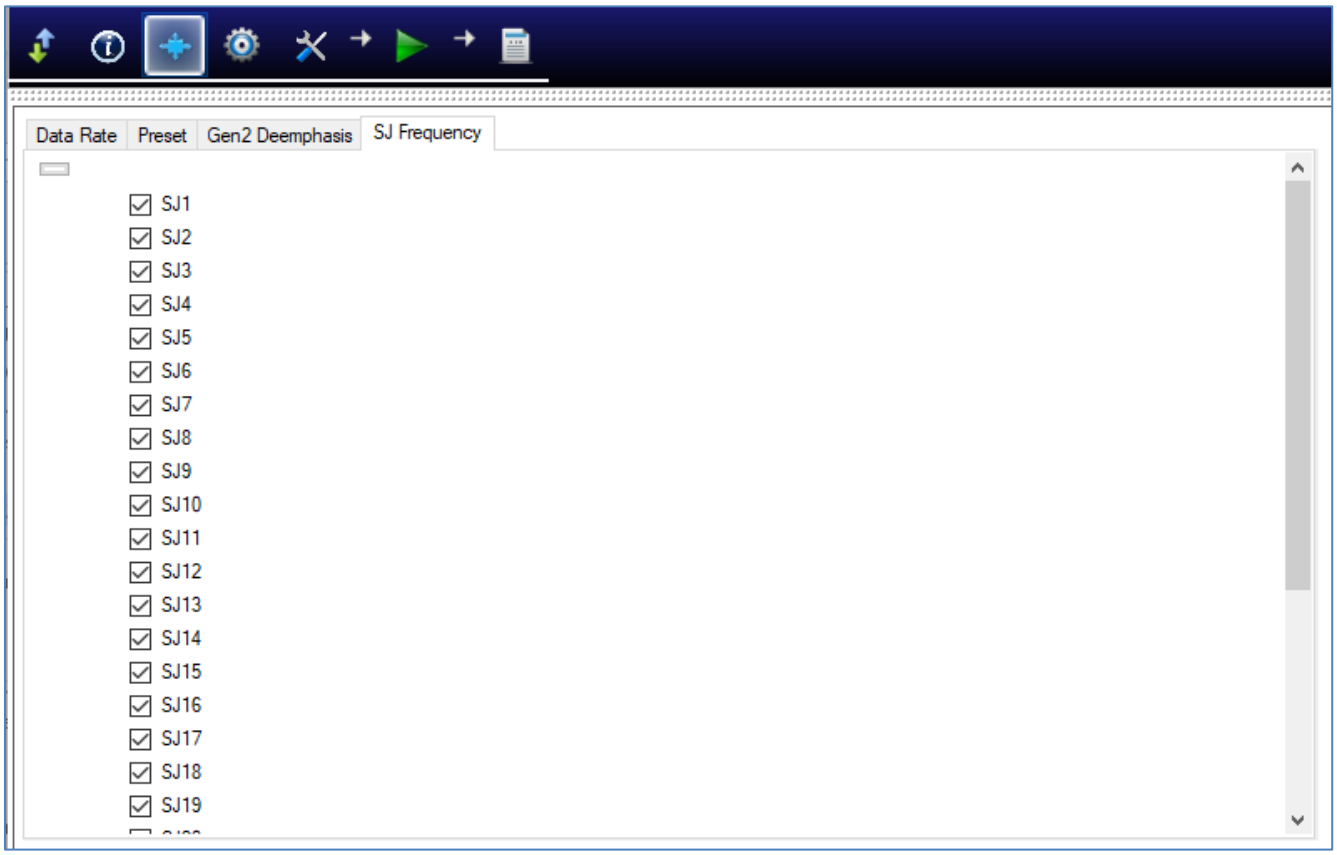


FIGURE 10. SELECT SJ FREQUENCIES

4 Calibrating Using GRL-PCIE-PLL Software

The GRL-PCIE-PLL test solution when run from the oscilloscope or an external controller PC enables automation control for each step of SJ calibration to ensure that the BERT is transmitting SJ at a correct value.

Calibration is performed by connecting the Scope to the BERT directly in the setup. By default, SJ is measured using a simple TIE method. The TIE without SJ or stressors is measured to obtain the intrinsic jitter of the setup. The subsequent TIE measurements will be subtracted by the TIE without stressors to obtain the SJ.

The GRL-PCIE-PLL software provides SJ calibration that can be selected and run as described in Section 6.2.1.

When calibration is completed, the GRL software will generate a test report detailing all results obtained from the calibration.

4.1 Connection Setup for MP1900A BERT Generator Set

Figure 11 shows the connection setup between each module of the Anritsu MP1900A BERT Generator Set. *Note that the cable models used in this setup are examples and can be replaced with their equivalent.*

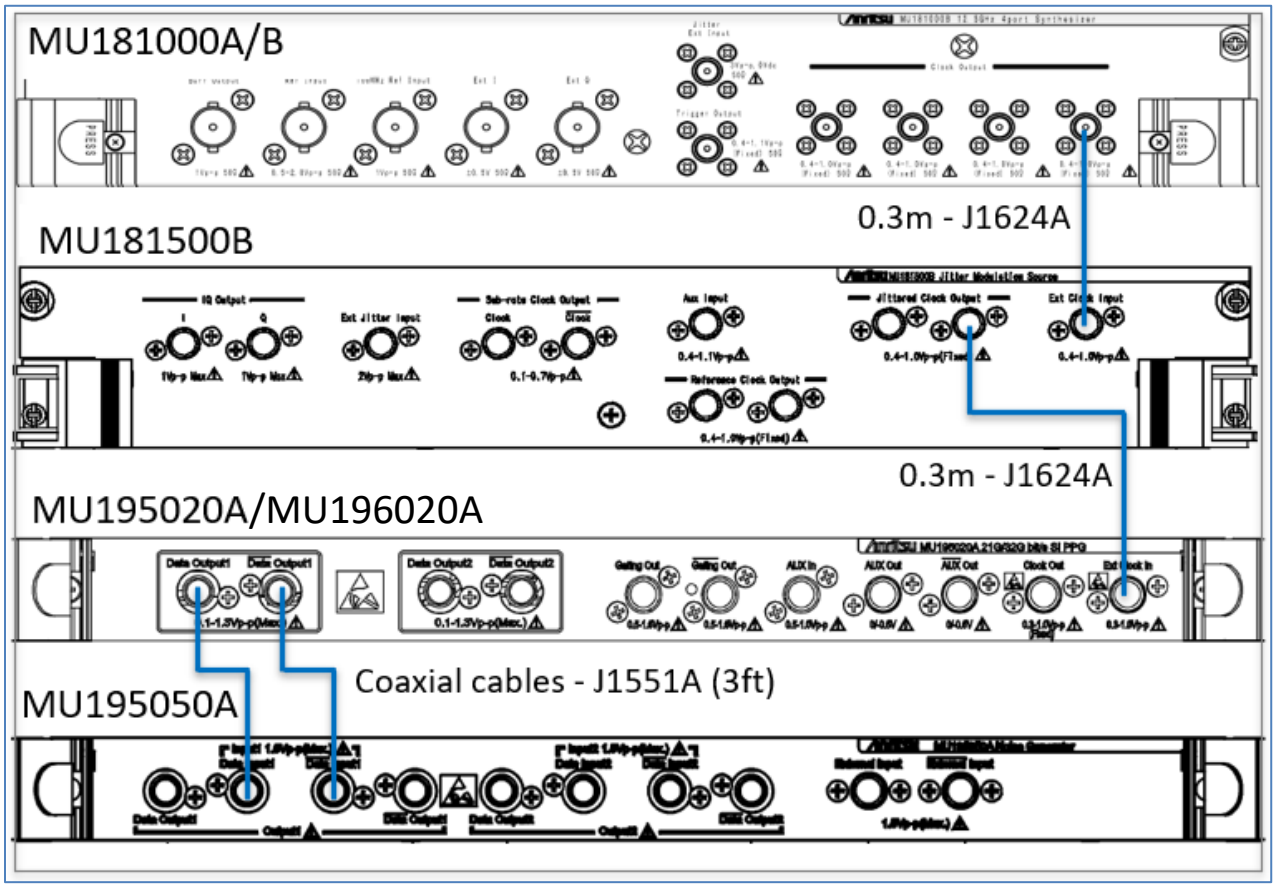


FIGURE 11. CONNECTION SETUP FOR MP1900A BERT GENERATOR SET MODULES

Connection Steps:

1. Using the J1624A SMA-SMA (0.3m) cable, connect the Clock Output of the MU181000A/B Synthesizer to the Ext Clock Input of the MU181500B Jitter Modulator.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU195020A/MU196020A Pulse Pattern Generator.
3. Using the J1551A coaxial cables (3ft), connect the MU195020A/MU196020A Data Outputs to the MU195050A Data Inputs.

4.2 Set Up SJ Calibration with Automation

After the GRL software has been pre-configured from Section 3.3, continue with the calibration setup. The following procedures show how to set up the physical connections to perform automated SJ calibration.

4.2.1 Connect Equipment for Sinusoidal Jitter (SJ) Calibration

The connection diagram below shows the recommended equipment setup to calibrate for SJ.

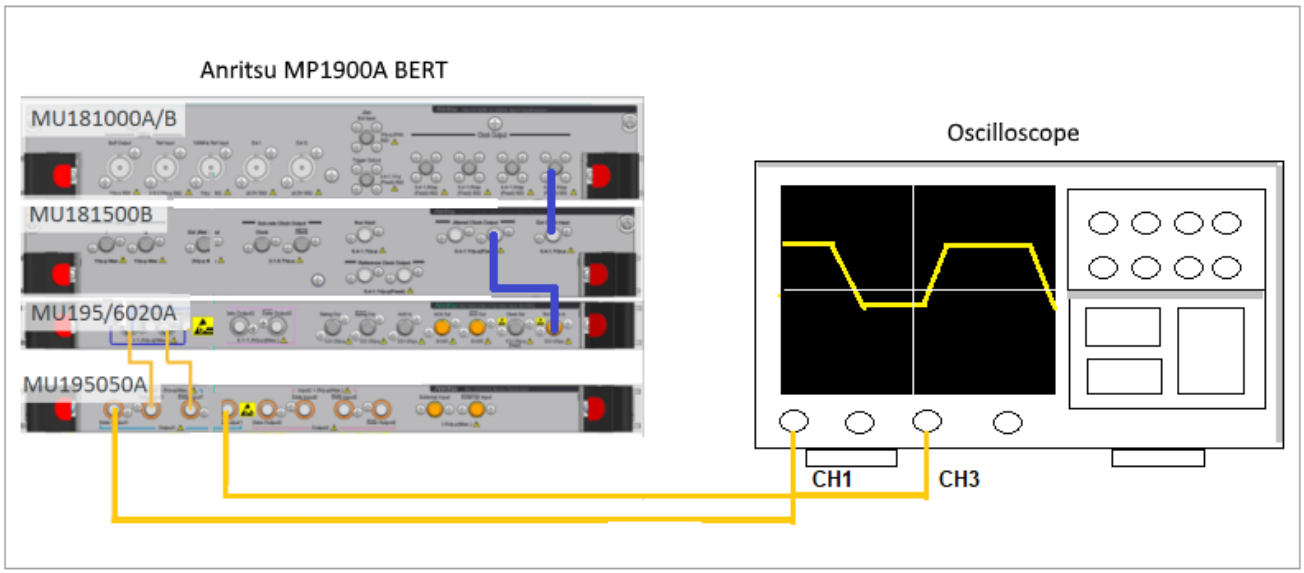


FIGURE 12. SJ CALIBRATION SETUP

Connection Steps:

1. Set up the MP1900A BERT connections as described in Section 4.1 above.
2. Connect the MU195050A data outputs to Channels 1 and 3 on the oscilloscope using phase-matched K-K coaxial cables.

5 Compliance Testing Using GRL-PCIE-PLL Software

After calibration has completed, the PCIe PLL Bandwidth Test can be performed by connecting the Add-In Card DUT to the PCIe Compliance Base Board (CBB). The GRL-PCIE-PLL software automates testing by measuring the jitter transfer of the PLL and obtaining the JTF.

The BERT is used to apply SJ at the Ref Clk input of the DUT through the CBB. The GRL-P1 hardware controller can be connected to the CBB to be used as an option for compliance toggle control of the DUT. The resulting SJ from the Tx output is then measured on the Scope. The jitter transfer (ratio of output jitter to input jitter) is plotted and the bandwidth and peaking of the PLL is determined from the plot.

5.1 Set Up PCIE PLL Add-In Card DUT Test with Automation

5.1.1 Connect Equipment for PLL Bandwidth Test

The connection diagram below shows the recommended equipment setup to test the Add-In Card DUT for PCIe PLL Bandwidth compliance. *Note: This applies for all PCIe data rates, 2.5GT/s (Gen1) to 32.0 GT/s (Gen5).*

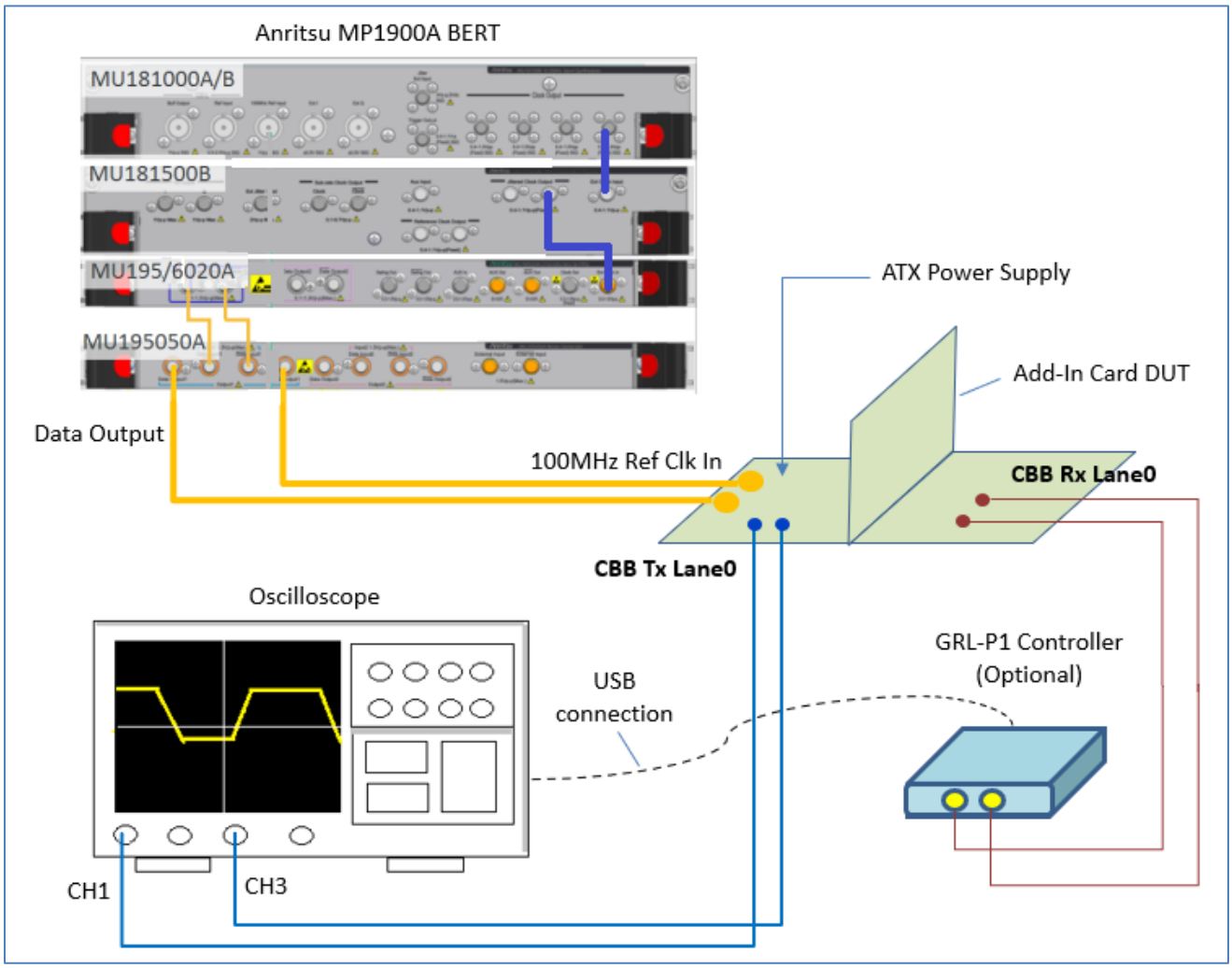


FIGURE 13. PCIE PLL BANDWIDTH TEST SETUP FOR ADD-IN CARD DUT

Connection Steps:

1. Using back the same setup connections from the SJ calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect an ATX power supply to the Add-In Card DUT through the CBB.
3. Connect the MU195050A data outputs to the 100MHz Ref Clk In of the CBB using a pair of phase-matched SMA cables.
4. Connect another pair of phase-matched SMA cables from the GRL-P1 controller outputs to the Rx Lane pins on the CBB for DUT compliance toggle control. *(Note this is optional.)* Connect the GRL-P1 to the oscilloscope via a USB cable.
5. Connect the Tx Lane pins on the CBB to Channels 1 and 3 on the oscilloscope using a pair of phase-matched SMA cables.
6. Insert the Add-In Card DUT into the designated slot on the CBB.

6 Configuring and Selecting Calibration and Compliance Tests Using GRL-PCIE-PLL Software

6.1 Set Up Calibration and Compliance Test Requirements

After setting up the physical equipment, select  from the GRL PCIe PLL Test Application menu to access the Setup Configuration page.

Use this page to configure the necessary measurement-related settings prior to running tests.

6.1.1 Test Setup Tab

Specify the Reference Clock Amplitude and Offset in the **RefClk Amplitude Setting (V)** and **RefClk Offset Setting (V)** fields respectively.

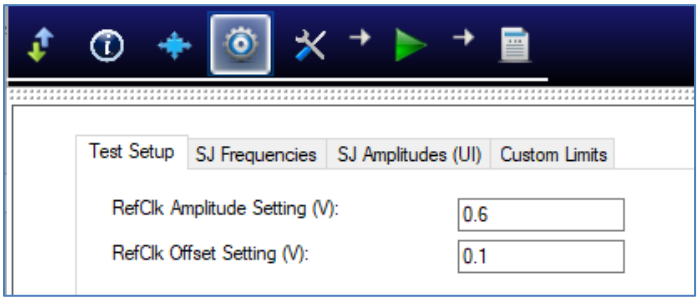


FIGURE 14. CONFIGURE LAUNCH AMPLITUDE

6.1.2 SJ Frequencies Tab

Specify custom limit values for each SJ frequency.

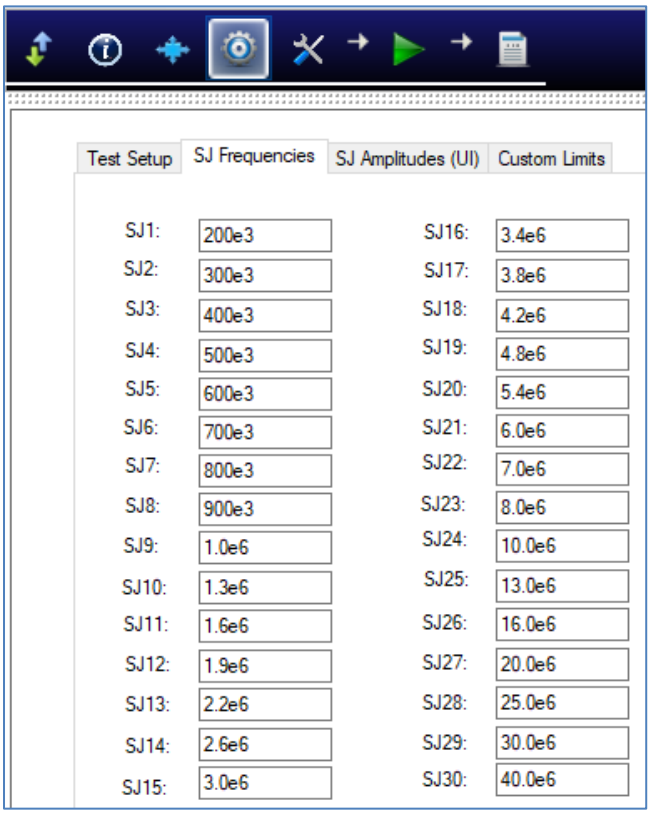


FIGURE 15. CONFIGURE CUSTOM SJ FREQUENCY LIMITS

6.1.3 **SJ Amplitudes (UI) Tab**

Specify custom values for each SJ level in UI if the “Override Individual Amplitude” checkbox is selected.

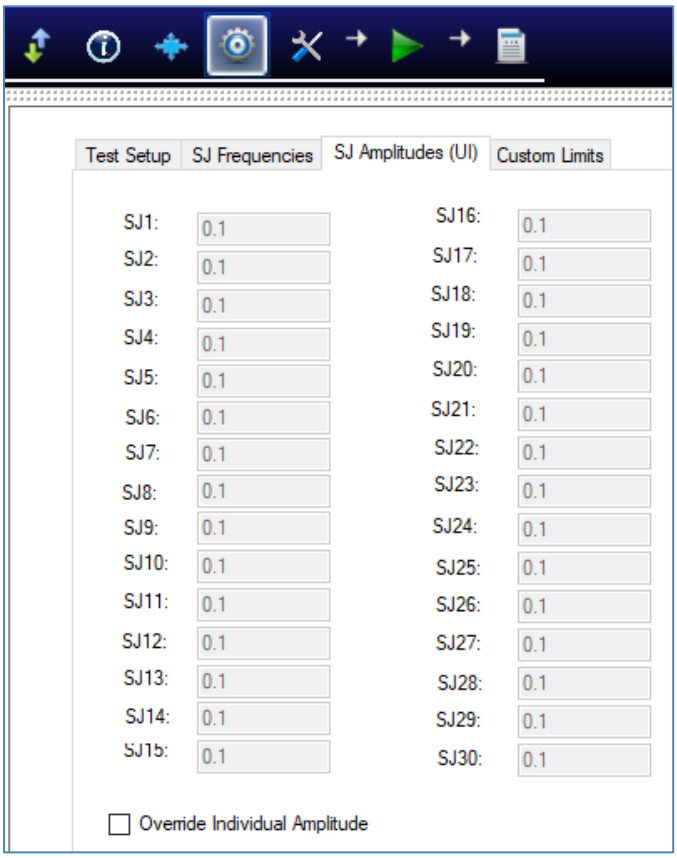


FIGURE 16. CONFIGURE CUSTOM SJ LEVELS

6.1.4 **Custom Limits Tab**

Specify the range of PLL bandwidth and peaking values for PCIe Gen1 to Gen5 data rates if the "Custom Limits" checkbox is selected.

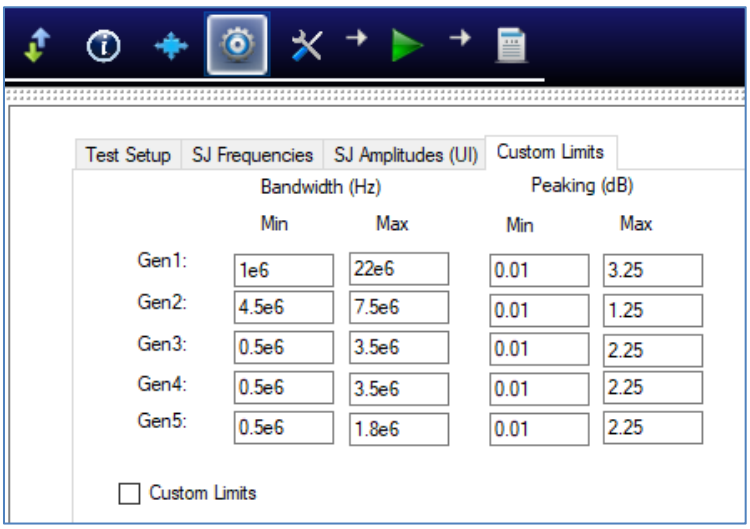


FIGURE 17. CONFIGURE CUSTOM LIMITS FOR BANDWIDTH AND PEAKING

6.2 Select Calibration and Compliance Tests

After setting up test requirements, go to the test selection page which allows all available calibration and DUT compliance tests to be selected. Select the check boxes of the respective calibration and tests to be performed.

Note: When running tests for the first time or changing anything in the setup, it is suggested to perform calibration first. If calibration is not completed, attempting to run the tests will throw errors.

6.2.1 Select Calibration

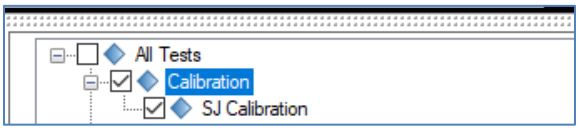


FIGURE 18. CALIBRATION SELECTION

6.2.2 Select DUT PLL Bandwidth Tests

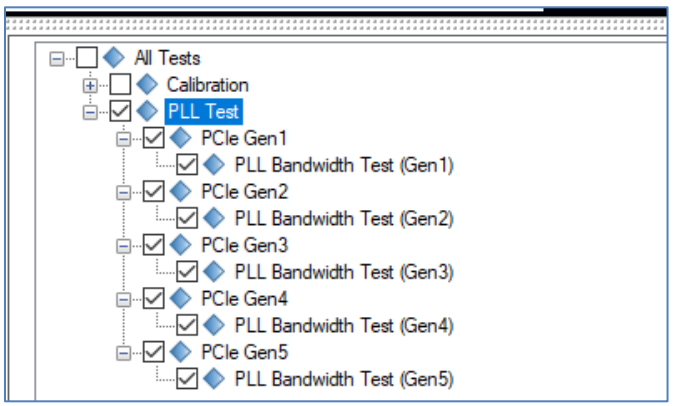


FIGURE 19. DUT PLL BANDWIDTH TEST SELECTION

6.3 Calibration/Compliance Test Parameters Configuration Page

Select  from the menu to access the Configurations page.

Set any of the available parameters required for measurement as described below. To return all parameters to their default values, select the 'Set Default' button.

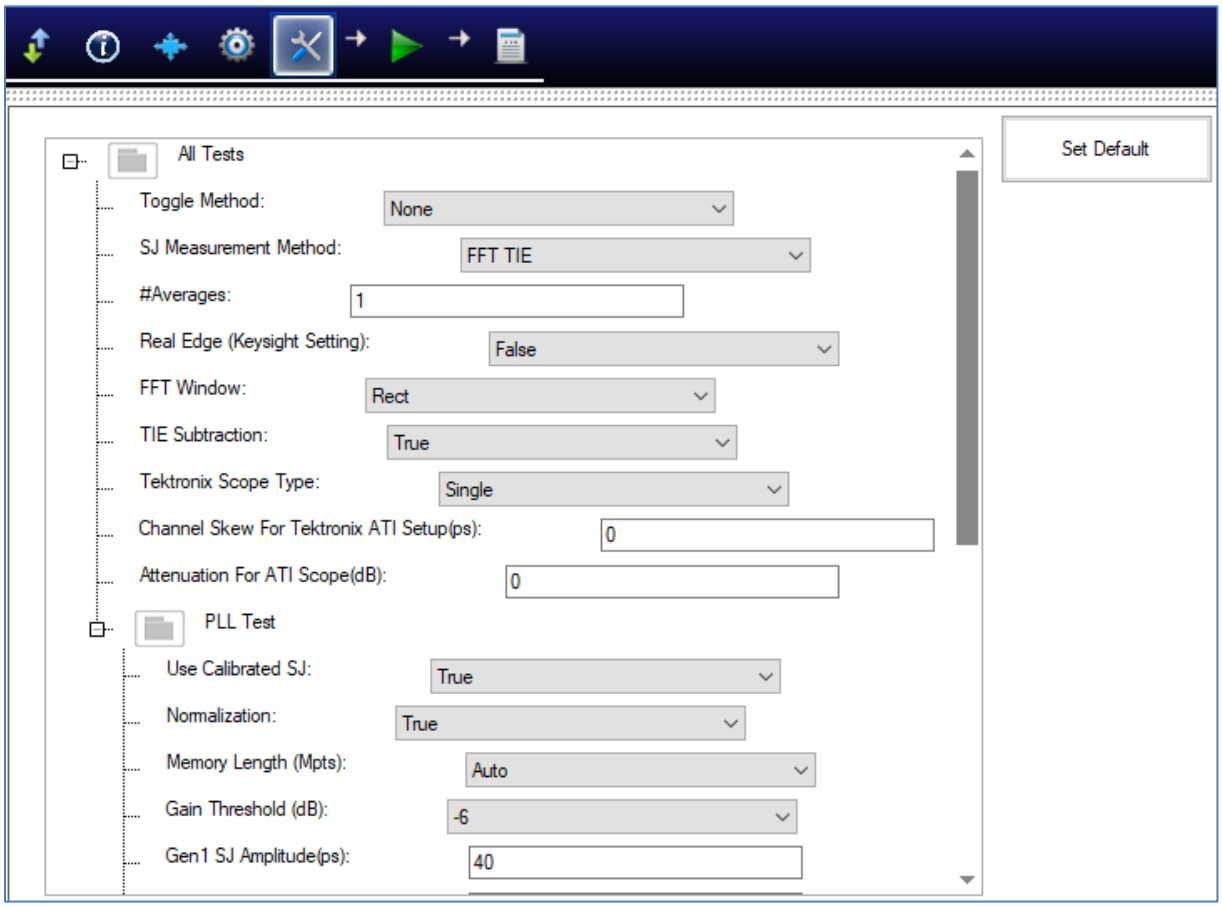


FIGURE 20. CALIBRATION/COMPLIANCE TEST PARAMETERS CONFIGURATION

TABLE 3. CALIBRATION/COMPLIANCE TEST PARAMETERS DESCRIPTION

Parameter	Description
Toggle Method	Select one of the following options to provide compliance toggle signal to control the compliance state of the DUT: • 'None': Select "None" if using manual compliance toggle. • 'GRLController': This is provided as an Option. The GRL-P1 hardware controller can be used in the setup for compliance toggle control.
SJ Measurement Method	Select the Scope Fast Fourier Transform (FFT) TIE filter or a system-defined based methodology to be applied during calibration of SJ. • If the 'System Defined' option is selected, the Vendor-specific method (Tektronix or Keysight Scope jitter measurement) will be used for calibration of all SJ frequencies. • If the 'FFT TIE' option is selected, the relative TIE will be measured using amplitude of TIE of the desired frequency in the FFT domain.
#Averages	Specify the number of times to apply averaging to achieve correct average frequency. *This setting is optional.*

Real Edge (Keysight Setting)	If using the Keysight Scope, select 'True' to enable the clock signal to be supplied on the Real Edge channel for test setup, or 'False' to disable Real Edge connection on the scope. *This setting is only applicable for the Keysight Scope.*
FFT Window	Select one of the following FFT windowing options for offline FFT processing: • 'Rect': Use the Rectangular window for offline FFT processing. • 'Hanning': Use the Hanning window for offline FFT processing. • 'Hamming': Use the Hamming window for offline FFT processing.
TIE Subtraction	Select 'True' to enable the TIE subtraction method to be applied or 'False' to disable TIE subtraction.
Tektronix Scope Type	If using the Tektronix Scope, select either the Single-shot based Scope or the Tektronix' owned Dual Asynchronous Time Interleaving (Dual ATI) based Scope.
Channel Skew For Tektronix ATI Setup (ps)	If using the Tektronix ATI based Scope, enter the channel skew or timing to perform alignment of the Scope channels.
Attenuation For ATI Scope (dB)	If using the Tektronix ATI based Scope, specify the attenuation factor of the probe to be applied.
Use Calibrated SJ	Select 'True' to enable or 'False' to disable calibrated SJ values to be used in the PLL test, respectively.
Normalization	Select 'True' to enable normalization to be applied which normalizes the Jitter Transfer Function by setting the first point to zero, or 'False' to disable normalization.
Memory Length (Mpts)	Select the length of signal to capture for measurement.
Gain Threshold (dB)	Select the gain threshold value which when reached will trigger the PLL test to be stopped.
Gen1 – Gen5 SJ Amplitude (ps)	Use the default values or specify custom values for the high frequency SJ amplitude limits for PCIe Gen1 to Gen5 data rates. By default, the values are those defined in the specification. In case the default values are required again, just select the "Set Default" button to allow all configuration to be reset to default.
Override Low Frequency Setting	Select 'True' for the SJ amplitude limits with low frequencies below the selected cut-off frequency to use the values defined for the low frequency SJ amplitude limits. Or, select 'False' for all SJ amplitude limits to use the values defined for the high frequency SJ amplitude limits. This also means that all low frequency SJ amplitude limits will not be applicable. *Note: This setting applies for PCIe Gen1 to Gen5 data rates.*
Low Frequency Cut Off Range (Hz)	Select the cut-off frequency for the signal that contains a certain range of frequencies where low frequencies above the selected cut-off frequency are

	filtered.
Low Frequency Acquisitions	Specify the number of acquisitions for the low frequency within the selected range.
Low Frequency Gen1 – Gen5 SJ Amplitude (ps)	Use the default values or specify custom values for the low frequency SJ amplitude limits for PCIe Gen1 to Gen5 data rates. By default, the values are those defined in the specification. In case the default values are required again, just select the “Set Default” button to allow all configuration to be reset to default.

7 Running Automation Calibration and Tests Using GRL-PCIE-PLL Software

Once calibration and tests have been selected and set up from the previous sections, they are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL software automatically runs the selected calibration and tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration/tests exist, the software will *skip* those calibration/tests, or
- **Replace if Result Exists** – If results from previous calibration/tests exist, the software will *replace* those calibration/tests with new results.

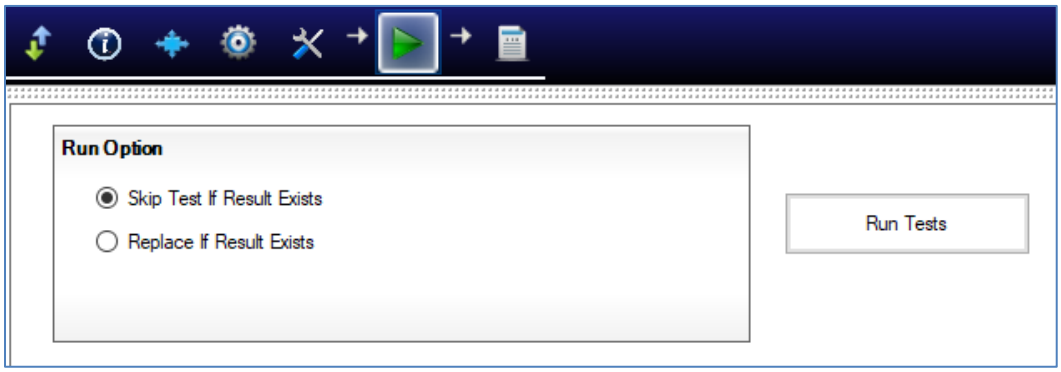


FIGURE 21. RUN TESTS PAGE

Select the **Run Tests** button to automatically start running the selected calibration and tests. At the start of a specific calibration/test, the corresponding connection diagram will initially appear to allow the user to verify with the recommended physical setup before continuing with the next step. Below shows an example of a connection diagram pop-up window.

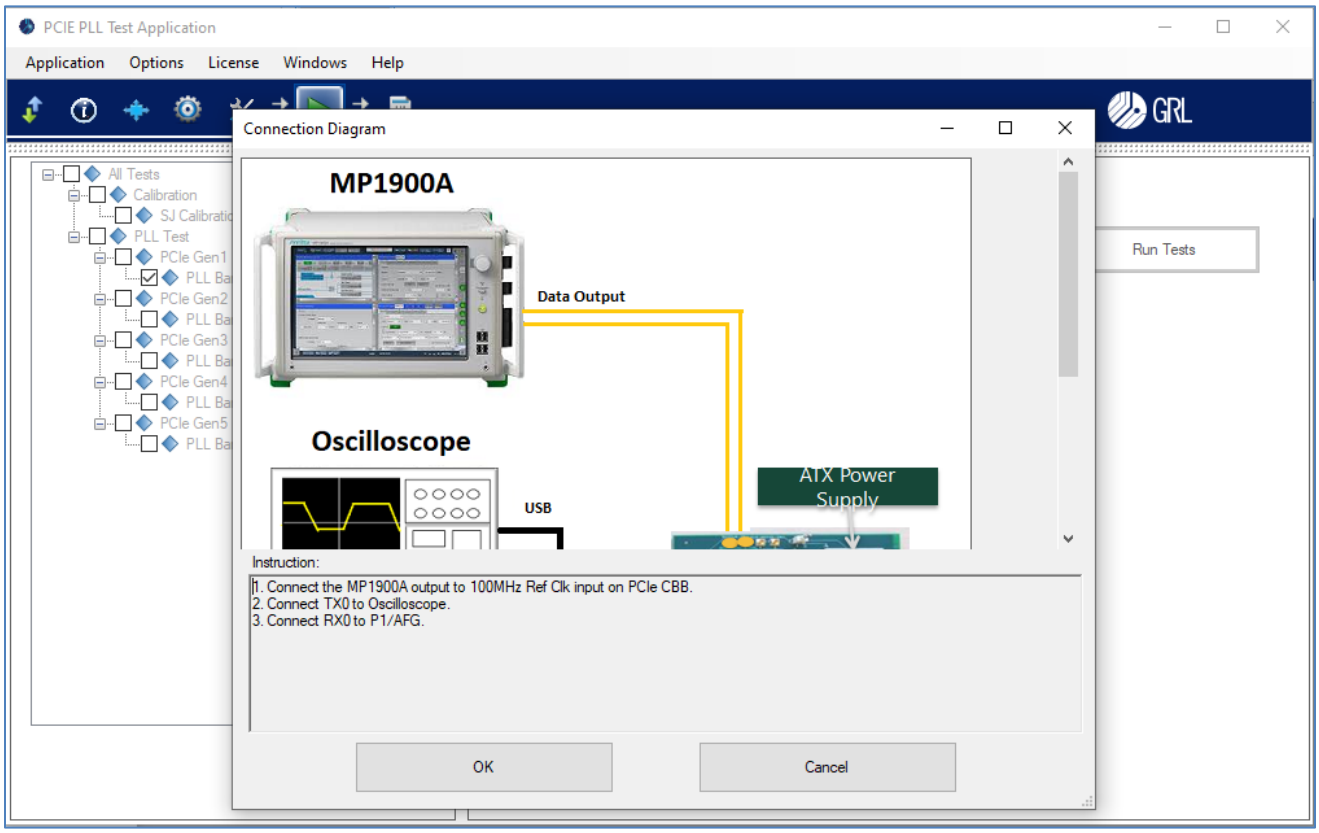


FIGURE 22. CONNECTION DIAGRAM POP-UP WINDOW EXAMPLE

8 Interpreting GRL-PCIE-PLL Test Report

When all calibration and test runs have completed from the previous section, the GRL-PCIE-PLL software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

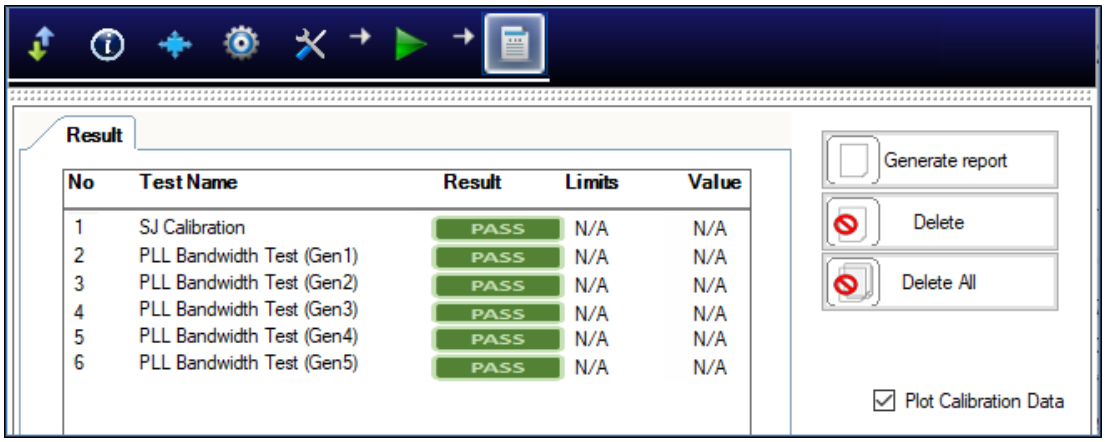


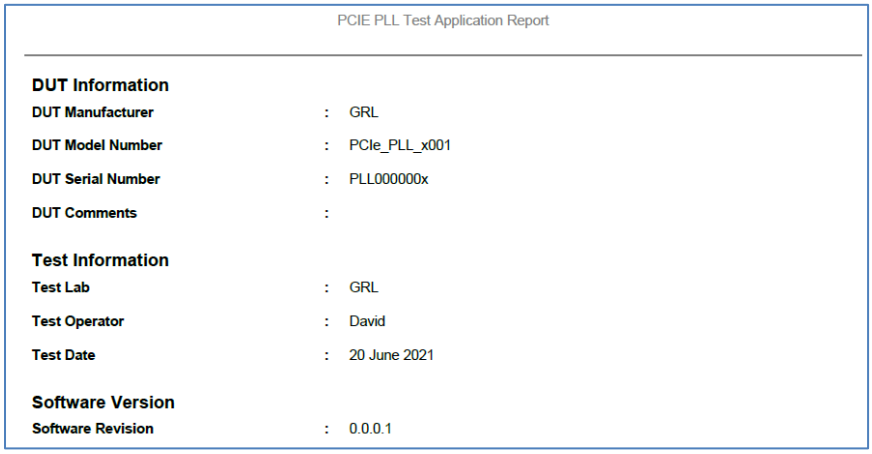
FIGURE 23. TEST REPORT PAGE

8.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

8.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.


PCIE PLL Test Application Report

DUT Information

DUT Manufacturer	:	GRL
DUT Model Number	:	PCIe_PLL_x001
DUT Serial Number	:	PLL000000x
DUT Comments	:	

Test Information

Test Lab	:	GRL
Test Operator	:	David
Test Date	:	20 June 2021

Software Version

Software Revision	:	0.0.0.1

FIGURE 24. TEST SESSION INFORMATION EXAMPLE

8.1.2 Test Summary Table

This table provides an overall view of all the calibration and tests performed along with their conditions and results.

No	TestName	Limits	Value	Results	Data Rate	Preset	SJ Frequency	Gen2 Deemphasis
1	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ1	N/A
2	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ2	N/A
3	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ3	N/A
4	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ4	N/A
5	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ5	N/A
6	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ6	N/A
7	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ7	N/A
8	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ8	N/A
9	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ9	N/A
10	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ10	N/A
11	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ11	N/A
12	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ12	N/A
13	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ13	N/A
14	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ14	N/A
15	SJ Calibration	N/A	N/A	Pass	N/A	N/A	SJ15	N/A
16	PLL Bandwidth Test	N/A	N/A	Fail	N/A	P0	N/A	N/A
17	PLL Bandwidth Test	N/A	N/A	Fail	N/A	P9	N/A	N/A

FIGURE 25. TEST SUMMARY TABLE EXAMPLE

8.1.3 Calibration & Test Results

This portion displays the results in detail along with supporting data points and screenshots for each calibration/test run.

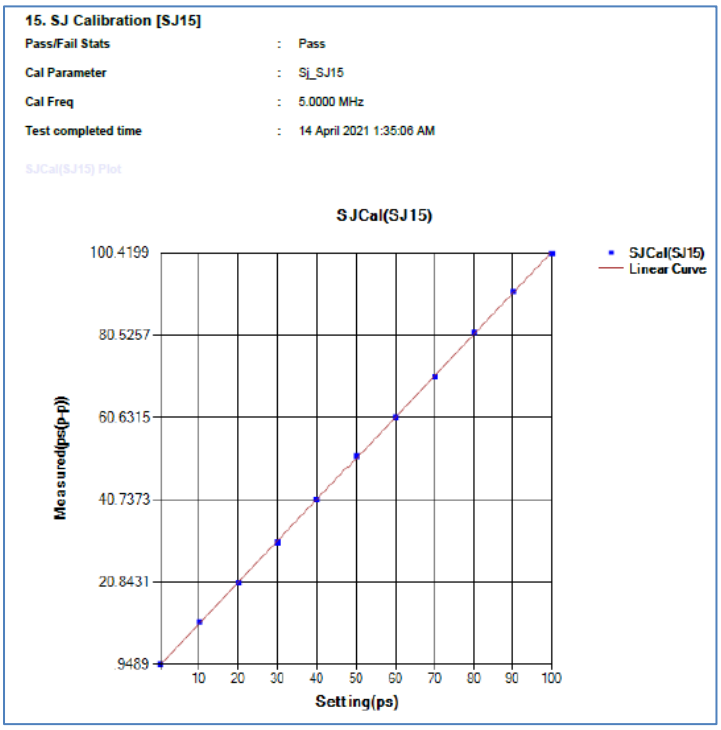


FIGURE 26. SJ CALIBRATION RESULTS EXAMPLE

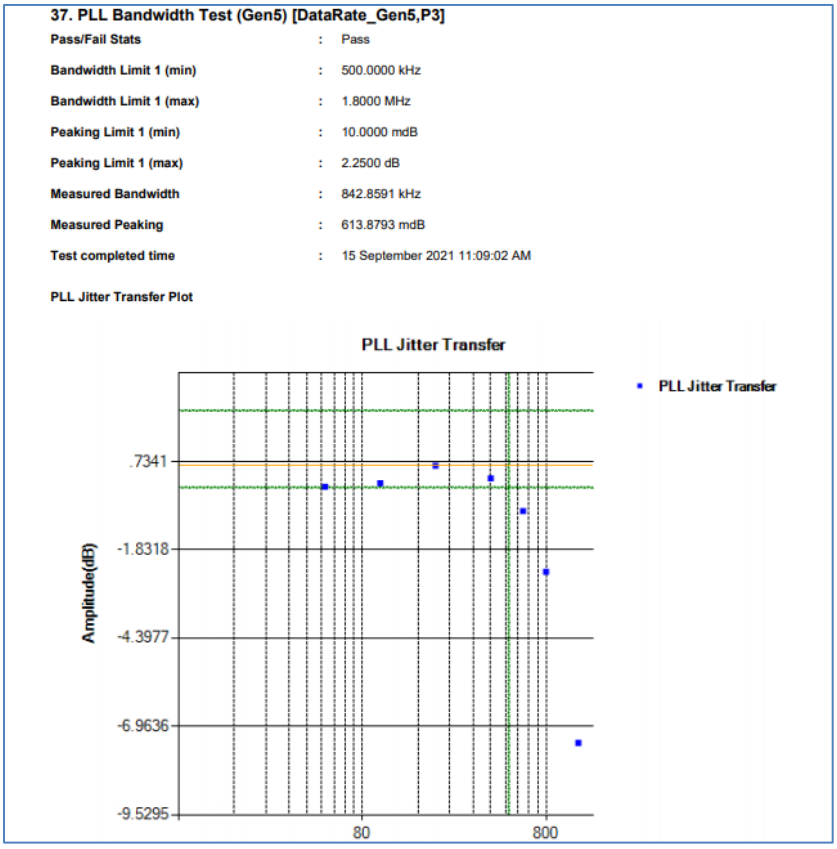


FIGURE 27. PLL BANDWIDTH TEST RESULTS EXAMPLE

8.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

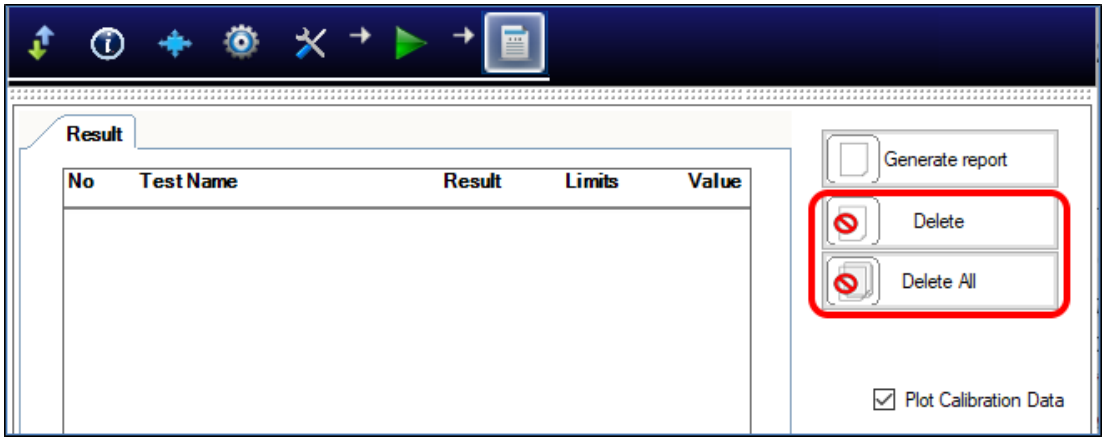


FIGURE 28. TEST REPORT DELETED

9 Saving and Loading GRL-PCIE-PLL Test Sessions

The usage model for the GRL-PCIE-PLL software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To ***save a test session***, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To ***load a test session*** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To ***create a new test session*** and return the application back to the default configuration, select Options → 'New Session'.

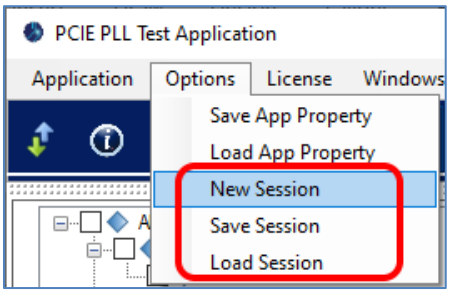


FIGURE 29. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

10 Appendix A: Method of Implementation (MOI) for Manual PCIE PLL Measurements

This section provides the manual PCIe PLL calibration and compliance test methodology based on the PCIe Standard.

10.1 SJ Calibration Procedure

Set up the equipment connections as described in Section 4.2.1 before proceeding with the following steps.

1. Initialize BERT.
2. Set the BERT Differential Amplitude to within the range of 300 mV to 800 mV. If a Noise module is used, the range should be within 424 mV to 1.13 V differential.
3. Disable All Stresses.
4. Set BERT to transmit 100 MHz clock signal as follows:
   - Set the BERT Data Rate to 8 GHz.
   - Load the “100MHzRefClockGen3.txt” Pattern File.
5. Set the SJ Frequency of the first SJ point to calibrate.
6. Set 0 ps (p-p) as base value in SJ, measure SJ (in ps (p-p)) from scope using the GRL MeasureSJ script and record the values.
7. Increase the SJ by 10 ps and repeat steps 5 to 6 until SJ is more than 40 ps.
8. Plot a linear graph.
9. Proceed to the next SJ Frequency and repeat steps 5 to 8.

10.2 PLL Bandwidth Test Procedure

Set up the equipment connections as described in Section 5.1.1 before proceeding with the following steps.

1. Initialize BERT.
2. Set BERT to transmit 100 MHz clock signal as follows:
   - Set the BERT Data Rate to 8 GHz.
   - Load the “100MHzRefClockGen3.txt” Pattern File.
3. Set the BERT Differential Amplitude to within the range of 300 mV to 800 mV. If a Noise module (3 dB loss) is used, the range should be within 424 mV to 1.13 V differential.
4. Set the BERT Offset to within the range of 250 mV to 550 mV. If a Noise module (3 dB loss) is used, the offset range should be within 350 mV to 777 mV.
5. Disable All Stresses.
6. Toggle the DUT to output the compliance pattern at the desired data rate and preset.
7. Set the SJ Frequency of the first SJ point to test.
8. Set the SJ Amplitude to the settings defined, measure SJ (in ps (p-p)) from scope and record the values. Averaging may be optionally performed.
9. The jitter transfer is calculated using the following equation:

Jitter Transfer = 20 * Log (Measured SJ / Applied SJ)

10. Proceed to the next SJ Frequency and repeat steps 7 to 9.
11. Plot the Jitter Transfer vs Frequency plot.
12. The 3 dB bandwidth and peaking of the PLL is determined from the plot.
13. Ensure that the DUT complies to the target range of Bandwidth and Peaking value in Table 4 from the PCI Express PLL Specifications for the respective data rate.
14. If the DUT fails to achieve the target results, repeat the test using different presets until the target results are obtained.
15. A passing result with any preset is sufficient to pass this test.

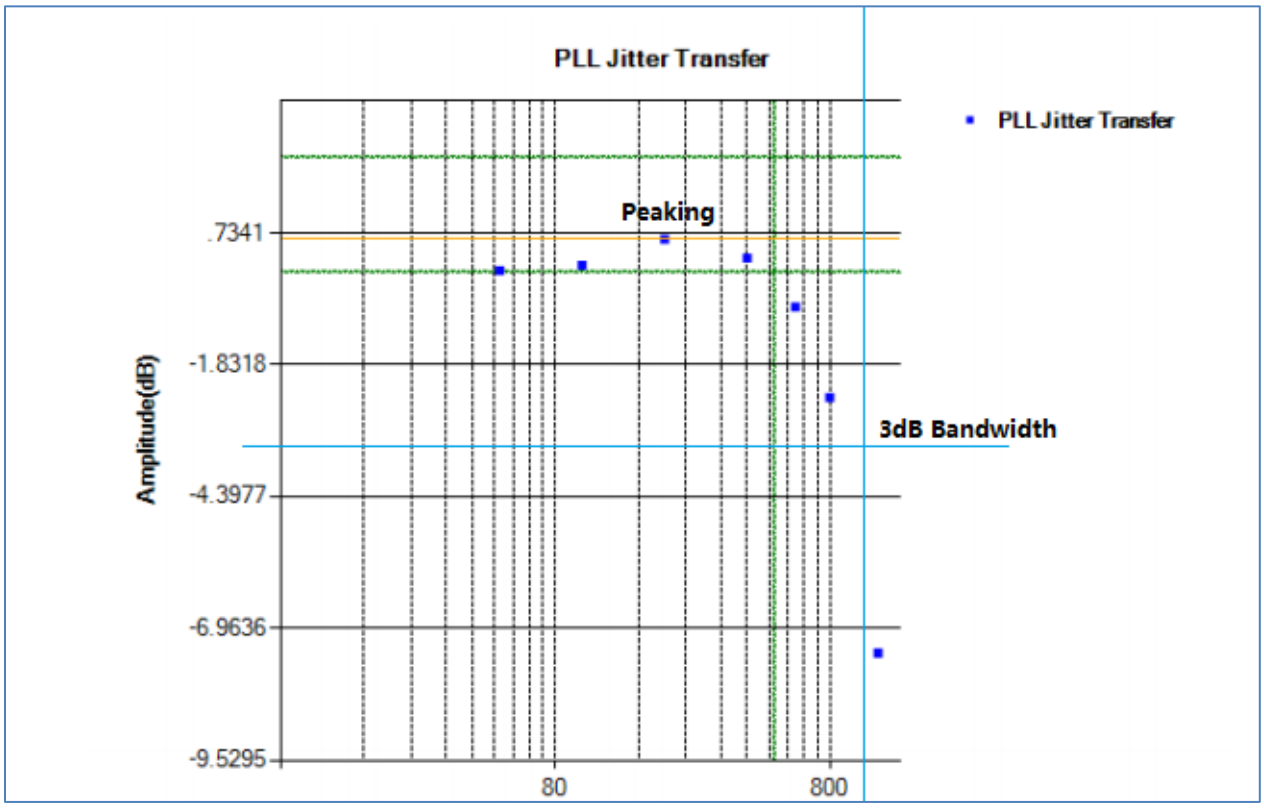
TABLE 4. TARGET BANDWIDTH AND PEAKING VALUES FROM PCIE EXPRESS PLL SPECIFICATION

Max Data Rate	Bandwidth (MHz)	Bandwidth Tolerance (MHz)	Max Peaking (dB)	Peaking Tolerance (dB)
2.5 GT/s	1.5-22.0	±0.5	3.0	+ 0.25
5.0 GT/s	8.0-16.0	±0.5	3.0	+ 0.25
5.0 GT/s	5.0-16.0	±0.5	1.0	+ 0.25
8.0 GT/s	0.5*-4.0	-0.2/+0.5	2.0	+ 0.25
8.0 GT/s	0.5*-5.0	-0.2/+0.5	1.0	+ 0.25
8.0 GT/s	2.0**-4.0	±0.5	2.0	+ 0.25
8.0 GT/s	2.0**-5.0	±0.5	1.0	+ 0.25
16.0 GT/s	0.5*-4.0	-0.2/+0.5	2.0	+ 0.25
16.0 GT/s	0.5*-5.0	-0.2/+0.5	1.0	+ 0.25
16.0 GT/s	2.0**-4.0	±0.5	2.0	+ 0.25
16.0 GT/s	2.0**-5.0	±0.5	1.0	+ 0.25
32.0 GT/s	0.5-1.8	-0.2/+0.5	2.0	+ 0.25

Table 1: PLL Testing Limits

*: *PCIe 5.0 Base Specification* allows lower PLL bandwidth limit to be 0.5 MHz at 8.0 GT/s and 16.0 GT/s

**: PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as the Min PLL BW at both 8.0 GT/s and 16.0 GT/s



11 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a controller PC. The Keysight Scope can be connected to the controller PC through GPIB, USB or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the controller PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the controller PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

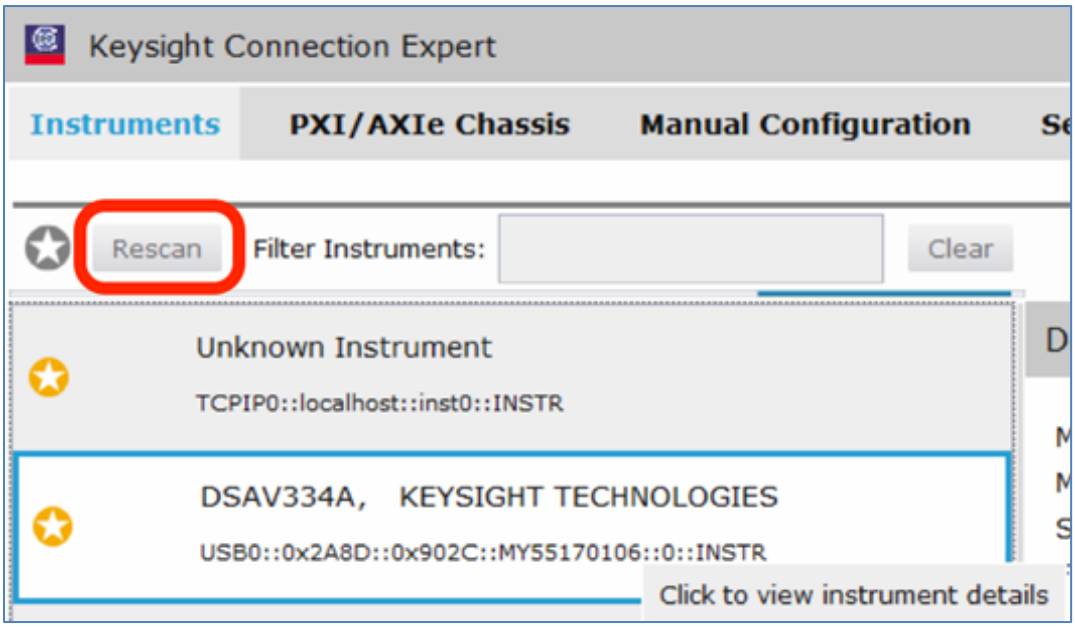


FIGURE 30. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

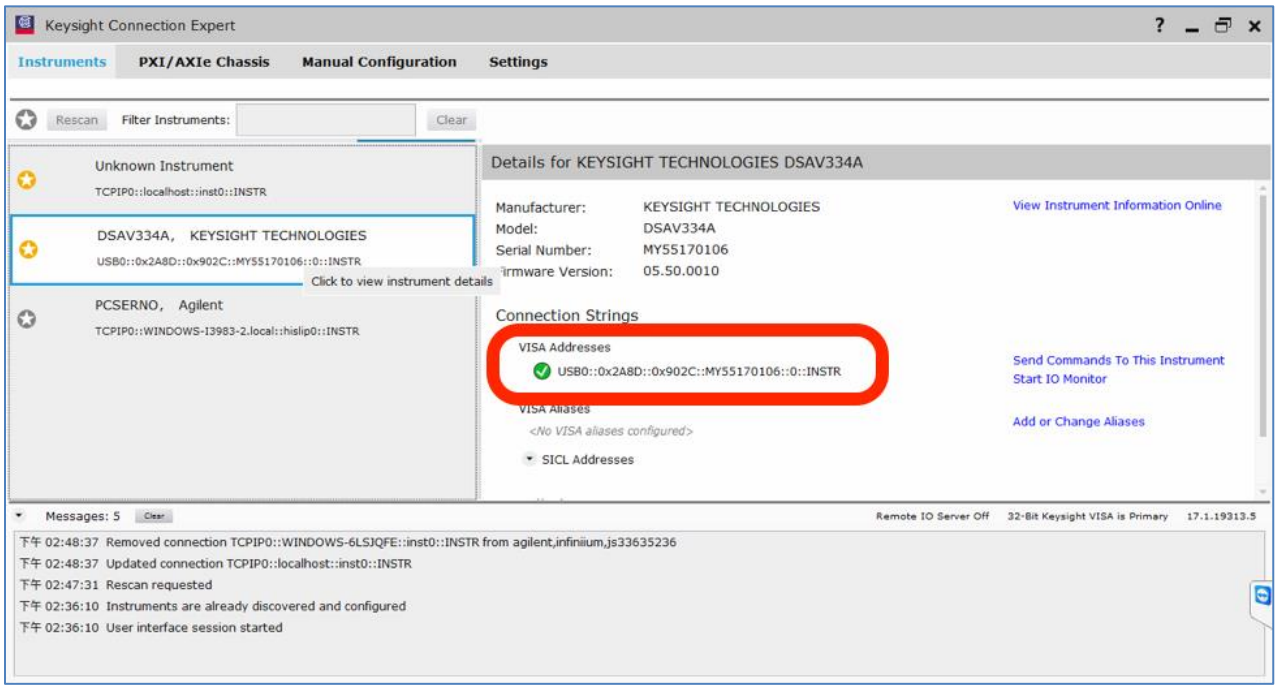


FIGURE 31. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL PCIe PLL Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

   If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".

12 Appendix C: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

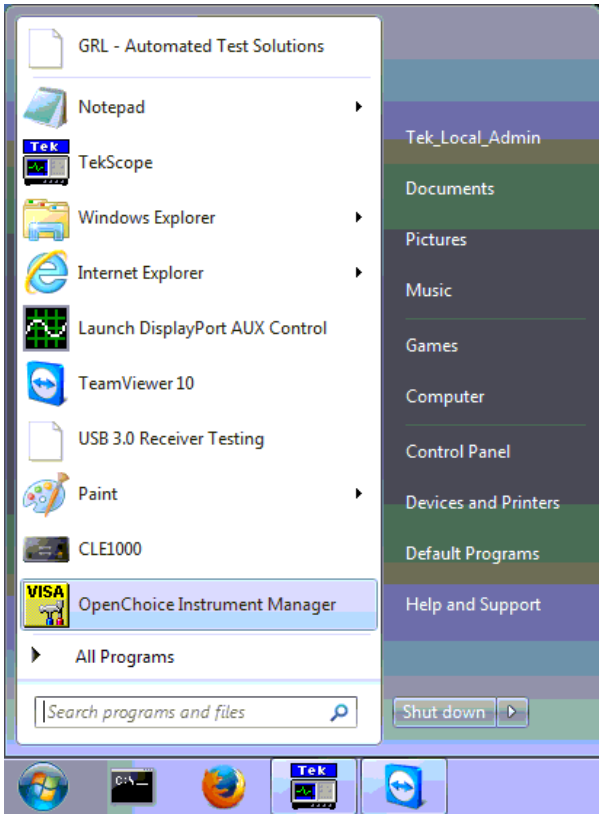


FIGURE 32. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
   a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
   b) “Search Criteria”: Select to configure the instrument search function.
   c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
   d) “Properties”: Select to display and view the selected instrument properties.

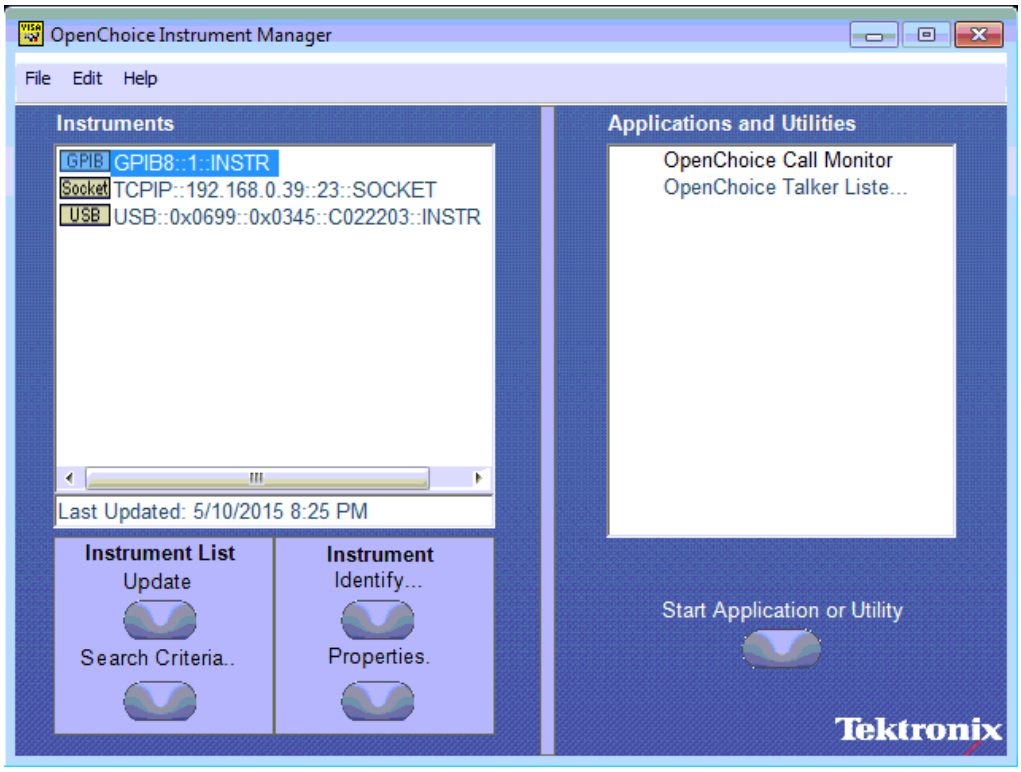


FIGURE 33. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL PCIe PLL Test Application, type in the Scope address into the 'Address' field. If the GRL PCIe PLL Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

END_OF_DOCUMENT