Granite River Labs

DisplayPort™ PHY 2.1 Receiver Calibration and Test User Guide & Method of Implementation (MOI)

Using

Anritsu MP1900A BERT and High Performance Real-Time Oscilloscope

with

GRL-DP21-SINK-AN DisplayPort 2.1 Receiver Calibration and Test Automation Software

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1 Introduction

This User Guide & MOI describes the procedures to perform DisplayPort 2.1 Sink (or Receiver) calibration and tests of the VESA DisplayPort Logo Compliance Program using the Anritsu MP1900A BERT and High Performance Real-Time Oscilloscopes in conformance with the DisplayPort PHY 2.1 Compliance Test Specification (CTS). Sink tests are required to qualify a Sink product or silicon building block for Logo certification and listing on the DP Integrators List.

This User Guide & MOI explains how to set up and use the GRL-DP21-SINK-AN software to automate receiver calibration and compliance testing for DisplayPort 2.1 Sink conformance. The GRL-DP21-SINK-AN software is used with the Anritsu MP1900A BERT for testing DisplayPort receivers per the Jitter Tolerance requirements of the DisplayPort PHY CTS and DisplayPort over USB Type-C® CTS respectively.

The GRL-DP21-SINK-AN software automates stressed signal calibration and jitter tolerance testing at the following DisplayPort data rates– UHBR 10 (10.0 Gbit/s per lane), UHBR 13.5 (13.5 Gbit/s per lane) & UHBR 20 (20.0 Gbit/s per lane) and supports USB Type-C and standard DisplayPort sink device-under-tests (DUT's). For link training, compliance, and margin testing through DPCD registers, the software provides automation control using a compatible DisplayPort AUX controller.

The following are the main topics covered by this User Guide & MOI:

1. Equipment required for calibration and testing.
2. GRL-DP21-SINK-AN software setup for calibration and test automation.
3. Manual DisplayPort PHY CTS Sink calibration and test methodology.

2 Resource Requirements

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description	Key Specification Requirement
GRL-DP21-SINK-AN	1	Granite River Labs DisplayPort 2.1 Sink Compliance Calibration & Test Automation Software for the Anritsu MP1900A BERT – www.graniteriverlabs.com (Support > Download Center) *– with Node Locked License to single Oscilloscope/PC OS*	
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator • MU195050A Noise Generator	• Option STR for stress generation • Proper test patterns [a]
Real-time Oscilloscope [b]	1	Keysight (InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization) Oscilloscope Or Tektronix DPO/MSO70000DX or 70000SX Series Oscilloscope with DPOJET (Jitter and Eye Analysis) software	> 16 GHz bandwidth [c]

[a] MP1900A DisplayPort patterns are distributed with GRL-DP21-SINKAN software and are installed during installation process.

[b] Infiniium / DPOJET setup files and SDLA filters are distributed with the GRL-DP14-SINKAN software and are installed during installation process.

[c] For UHBR 13.5 / UHBR 20 data rates, at least 21 GHz of oscilloscope bandwidth is required.

TABLE 2. EQUIPMENT REQUIREMENTS – ACCESSORIES

Accessory	Qty.	Description	Key Specification Requirement
TP1 Plug Test Fixture	1	Test Point 1 DisplayPort USB Type-C Plug Test Fixture	
	1	Test Point 1 Standard/Mini DisplayPort Plug Test Fixture	

Accessory	Qty.	Description	Key Specification Requirement
TP3 Channel Components	2	Test Point 3 DisplayPort USB Type-C Receptacle Fixture	
	2	Test Point 3 Standard/Mini DisplayPort Receptacle Fixture	
TP3 Fixed ISI Trace	1	Test Point 3 Fixed ISI Board	
TP3 Test Cables	1	2 m USB Type-C Cable	Insertion Loss -18.5 dB at 5 GHz
	1	0.8 m USB Type-C Cable	Insertion Loss -17.5 dB at 6.75 GHz
	1	0.8 m USB Type-C Cable	Insertion Loss -16.5 dB at 10 GHz
	1	2 m Standard/Mini DisplayPort Cable	Insertion Loss -19 dB at 5 GHz
	1	0.8 m Standard/Mini DisplayPort Cable	Insertion Loss -16.5 dB at 6.75 GHz
	1	0.8 m Standard/Mini DisplayPort Cable	Insertion Loss -16.5 dB at 10 GHz
DisplayPort Control Board	1	DisplayPort USB Type-C Mode Control Board	
DisplayPort AUX Controller	1	Compatible vendor specific AUX controller	For link training and error detection
Cable Deskew Fixture	1	Anritsu Splitter	K241B
DC Block	2		Bandwidth of at least 33 GHz
÷4 RF Splitter	1	Anritsu AN44182A 4-Way Power Divider or equivalent	
Computer	1	Laptop or Desktop PC	Windows 7+ OS For automation control (running GRL-DP21-SINK-AN software)

***Note**: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table below is a recommended list. Please also refer to the respective manufacturer for detailed cabling recommendations related to DisplayPort 2.1.*

TABLE 3. EQUIPMENT REQUIREMENTS – CONNECTION CABLES

Connection Cable	Qty.	Key Specification Requirement
MU181000A/B to MU181500B	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU181500B to MU195020A	1	Anritsu J1624A SMA-SMA cable (0.3 m)

Connection Cable	Qty.	Key Specification Requirement
MU195020A to MU195050A	1 pair	Anritsu J1746A K-K skew matched pair short semirigid cable
Matched Cable Pairs	6	Phase Matched ±5° at 40 GHz Insertion Loss 1 dB maximum in 10 GHz
RPC-2.92 Jack to SMP Jack	4	Rosenberger 02K119-K00E3
JTAG Ribbon Cable	1	For connecting AUX controller and test fixture

2.2 Software Requirements

Software	Source
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-DP21-SINK-AN software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com *(Search on IO Libraries)* 3. Tektronix TekVISA: www.tek.com *(Downloads > Software > TekVisa)*
MX190000A	Anritsu High-Speed Serial Data Test Software – Mainframe MX190000A SQA Control Software (Version 4.00.00 or above). This software is located on the BERT.

3 Installing and Setting Up GRL-DP21-SINK-AN Software

This section provides the procedure for installing, configuring and verifying the operation of the GRL-DP21-SINK-AN software. It also helps you familiarize yourself with the basic operation of the software.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the software application, follow the procedure in the following section.

3.1 Download and Set Up GRL-DP21-SINK-AN Software

Install, launch and set up the GRL-DP21-SINK-AN software on a PC or an oscilloscope (where GRL-DP21-SINK-AN is referred to as 'Controller PC' or 'Scope' respectively in this MOI & User Guide):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-DP21-SINK-AN is to be used (see Section 2.1).
2. Download the GRL-DP21-SINK-AN ZIP file package from the Granite River Labs support site.
3. The ZIP file contains:
   a) **DPSink21_ANPatternFilesInstallationxxxxxxxxxSetup** – Run this on the Anritsu MP1900A BERT to install the DisplayPort 2.1 test pattern setup files. This will place the DisplayPort Configuration and Pattern files on the MP1900A BERT in the *'C:\Configurations\Anritsu DisplayPort Sink Test 2.1'* directory hierarchy.
   b) **DPSinkTest21_ANApplicationxxxxxxxxxSetup** – Run this on the Controller PC or Oscilloscope to install the GRL-DP21-SINK-AN application. This application will create the *'C:\GRL\Rx Test Solution\Applications\DPSinkTest20_AN'* directory hierarchy.
   c) **DPSinkTest21_ANScopeSetupFilesInstallationxxxxxxxxxSetup** – Run this on the Oscilloscope to install the Infiniium setup files. This will place the DisplayPort Setup and Filter folders in the *'C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 2.1'* of the Keysight Scope or *C:\TekApplications\DPOJET* of the Tektronix Scope directory hierarchy.

3.1.1 On the Anritsu MP1900A BERT

1. Launch the Signal Quality Analyzer-R Control Software.
2. Select the "Expert BERT" button to turn on the Miscellaneous System. This will allow you to remotely control the MP1900A BERT.

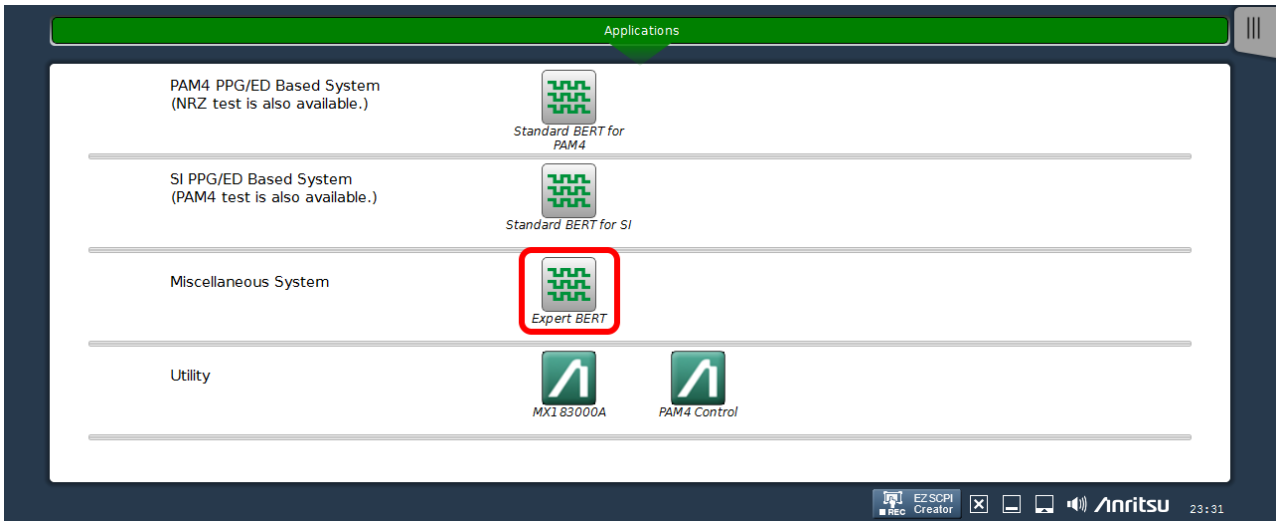


FIGURE 1. TURN ON MISCELLANEOUS SYSTEM

3. Note the IP Address as it will be used to connect the MP1900A BERT with the GRL-DP21-SINK-AN software.

3.1.2 On the PC Used for GRL Framework Installation

1. Open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

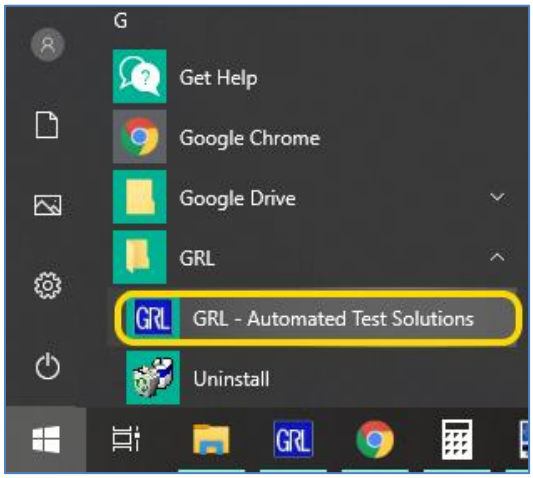


FIGURE 2. SELECT AND LAUNCH GRL FRAMEWORK

2. From the **Application → Rx Test Solution** drop-down menu, select **Anritsu DisplayPort Sink Test 2.1** to start the application. If the selection is grayed out, it means that your license has expired.

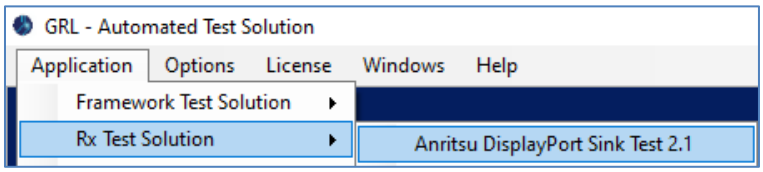


FIGURE 3. START DISPLAYPORT SINK TEST 2.1 APPLICATION

3. To enable license, go to License→License Details.

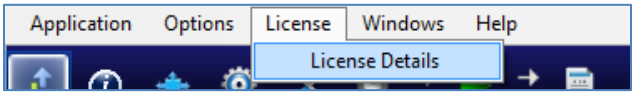


FIGURE 4. SEE LICENSE DETAILS

a) Check the license status for the installed application.

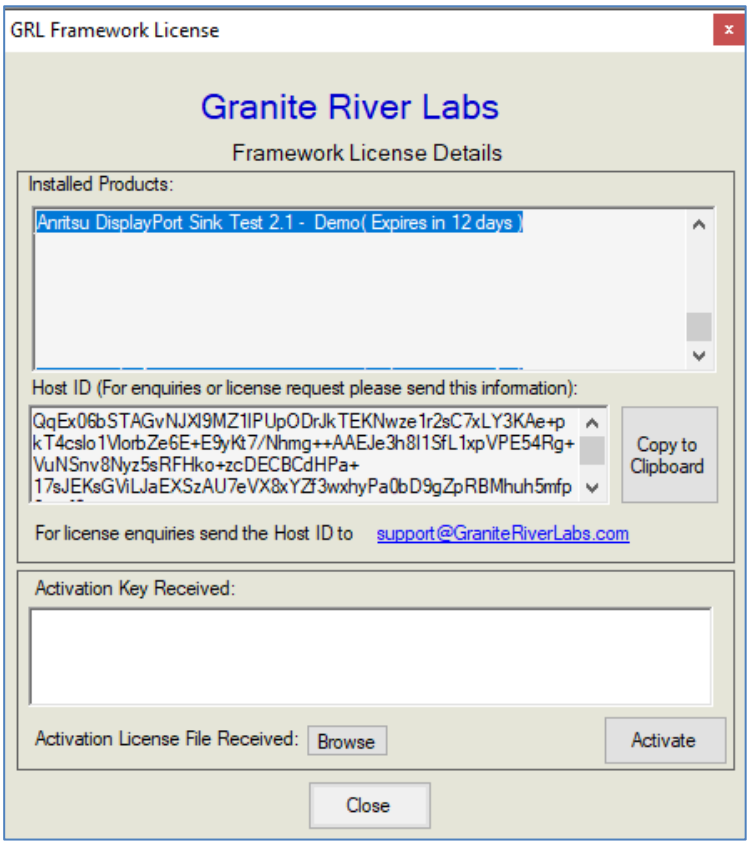


FIGURE 5. CHECK LICENSE FOR INSTALLED APPLICATION

4. Activate License:

a) If you have an Activation Key, please enter in the box provided and select **Activate**.
b) If you do not have an Activation Key, select **Close** to use a demo version of the software over a free 10-day trial period.

Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its*

capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.

5. Select the Equipment Setup icon on the DisplayPort Sink Test 2.1 Application menu.
4. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC. Enter the MP1900A IP address and Port number to match what is shown in the MP1900A *Remote Client* window in Section 3.1.1. For example, the BERT can be connected using a connection string in the following format: "TCPIP0::192.168.0.14::5001::SOCKET" or "192.168.0.14:5001". Note the IP address listed is only example and should be changed according to the actual network connection being used.
6. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.

   *(Note: The Scope IP address can be obtained, if not known, by typing CMD → IPCONFIG on the Scope and observe the IP address listed. If the GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR".) If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to **omit** the Port number from the address.)*
7. Then select the "lightning" button ( ) for each connected instrument.

   The "lightning" button should turn green ( ) once the GRL software has successfully established connection with each instrument.

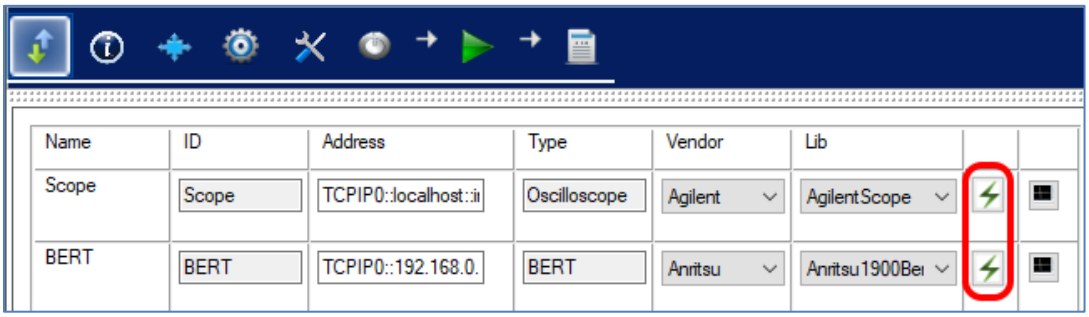


FIGURE 6. CONNECT INSTRUMENTS WITH GRL SOFTWARE

Note: Further information for connecting the Keysight and Tektronix oscilloscopes to the PC is provided in the Appendix of this document.

3.2 Configure the GRL-DP21-SINK-AN Software Before Calibration and Testing

3.2.1 Enter Calibration/Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

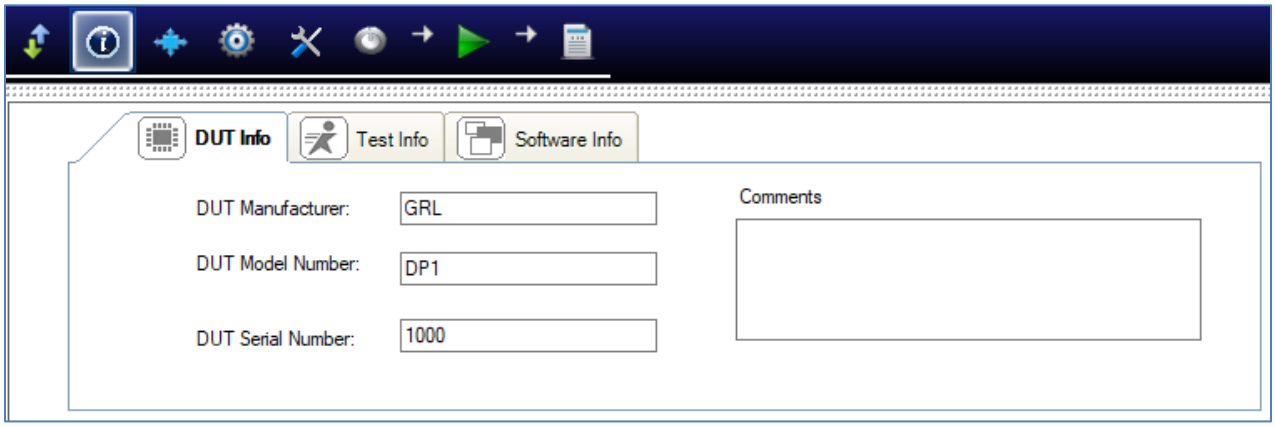


FIGURE 7. SESSION INFO PAGE

3.2.2 Set Up Conditions for Calibration/Testing

Select  from the menu to access the **Conditions** page to set the conditions for calibration and testing.

Recommended procedure:

- *Step 1*: When calibrating, select the desired conditions and perform the calibration tests.
- *Step 2*: When ready for testing, re-select the desired test conditions. For example, if required to test only one Lane at one SJ Frequency for the UHBR10 Data Rate, then select the appropriate conditions for testing.

a) **Lane tab**: Select the desired Lanes for testing. *[Note: This is only applicable for DUT compliance test and NOT for calibration.]*

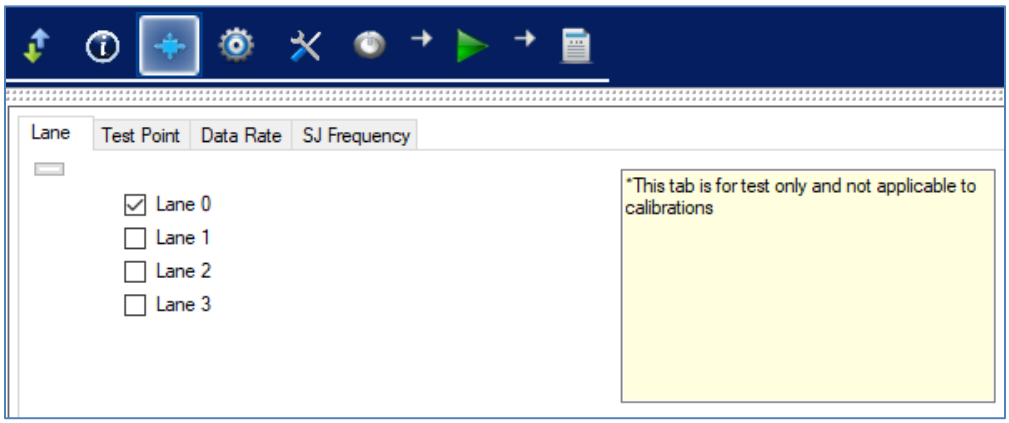


FIGURE 8. SELECT LANE UNDER TESTS

b) **Test Point tab**: Select the test points for calibration and testing. *[Note: TP1 calibration (Total Jitter & Eye Height) must be performed first prior to TP3_EQ calibration (Optimized EQ Lookup, Eye Height & Eye Width).]*

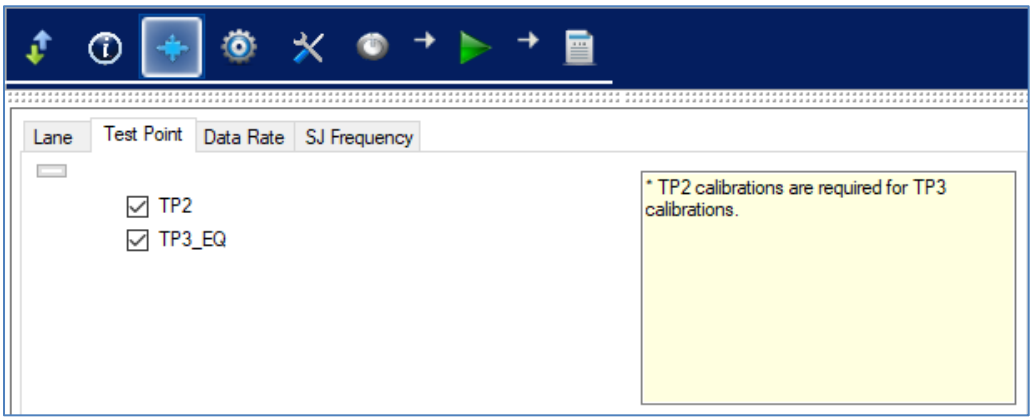


FIGURE 9. SELECT TEST POINTS

c) **Data Rate tab**: Select the desired data rates for calibration or testing:

- UHBR 10 (10.0 Gbit/s per lane)
- UHBR 13.5 (13.5 Gbit/s per lane)
- UHBR 20 (20.0 Gbit/s per lane)

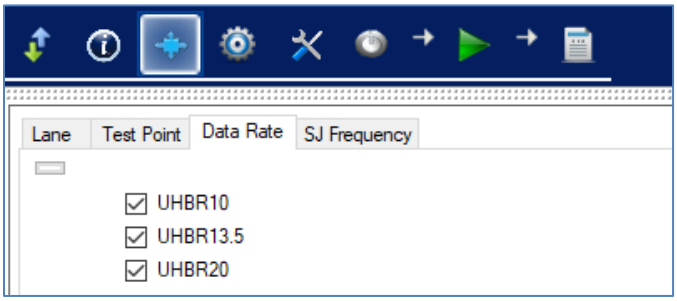


FIGURE 10. SELECT DATA RATES

d) **SJ Frequency** tab: Select the desired SJ frequencies for calibration or testing.

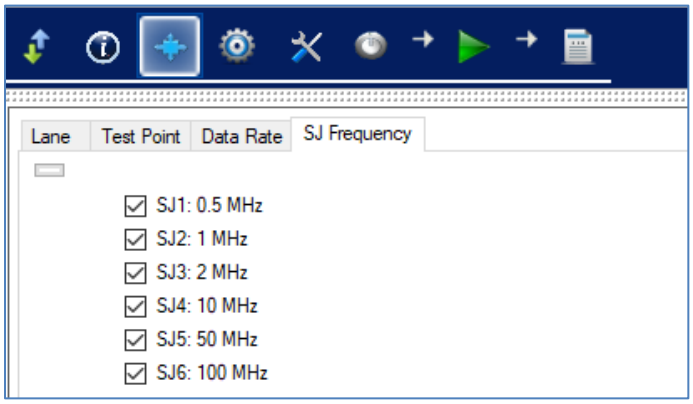


FIGURE 11. SELECT SJ FREQUENCIES

3.2.3 Set Up AUX Controller for DUT Test Automation

Select  from the menu to access the Setup Configuration page.

Select to use a supported AUX Controller in the DUT test setup or select 'None' if not using an AUX Controller. Then enter the COM port number of the connected AUX controller.

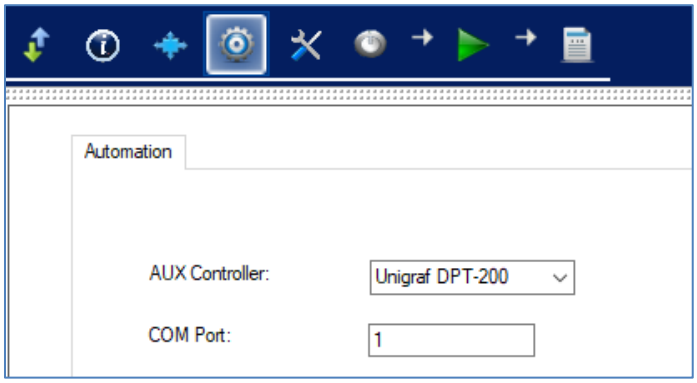


FIGURE 12. SELECT AUX CONTROLLER

3.3 Select Calibration/Test

Go to the **Select Tests** page on the left of the screen to select the available calibration or tests to be performed. Select the check box(s) of the desired calibration/test.

Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Sink Tests will show an error message.

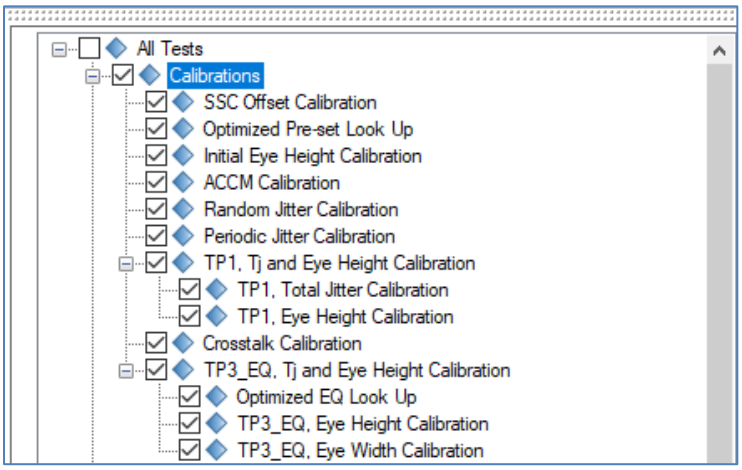


FIGURE 13. CALIBRATION SELECTION

Select the calibration groups to perform calibration for all DisplayPort Sink parameters. Note that while the user can select individual calibration parameters, it is possible that a particular calibration may require the previous calibration to be completed before it can proceed. Thus, it is advisable to complete all previous calibration before going on to the next calibration.

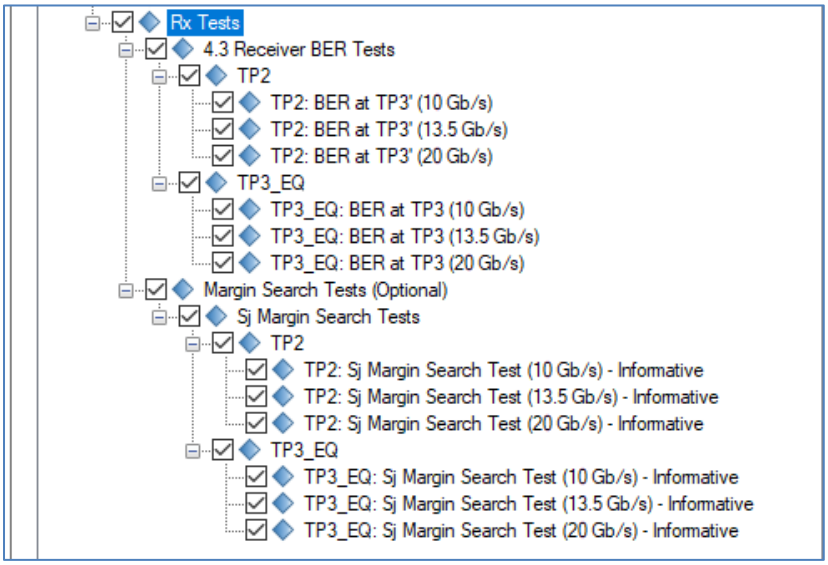


FIGURE 14. TESTS SELECTION

Select the test groups to perform DUT compliance tests for all DisplayPort Sink parameters.

3.4 Configure Calibration/Test Parameters

After selecting the desired calibration or test, select  from the menu to access the Configurations page. Set the required parameters for Sink calibration and testing as described in Table 4 below.

To return all parameters to their default values, select the 'Set Default' button.

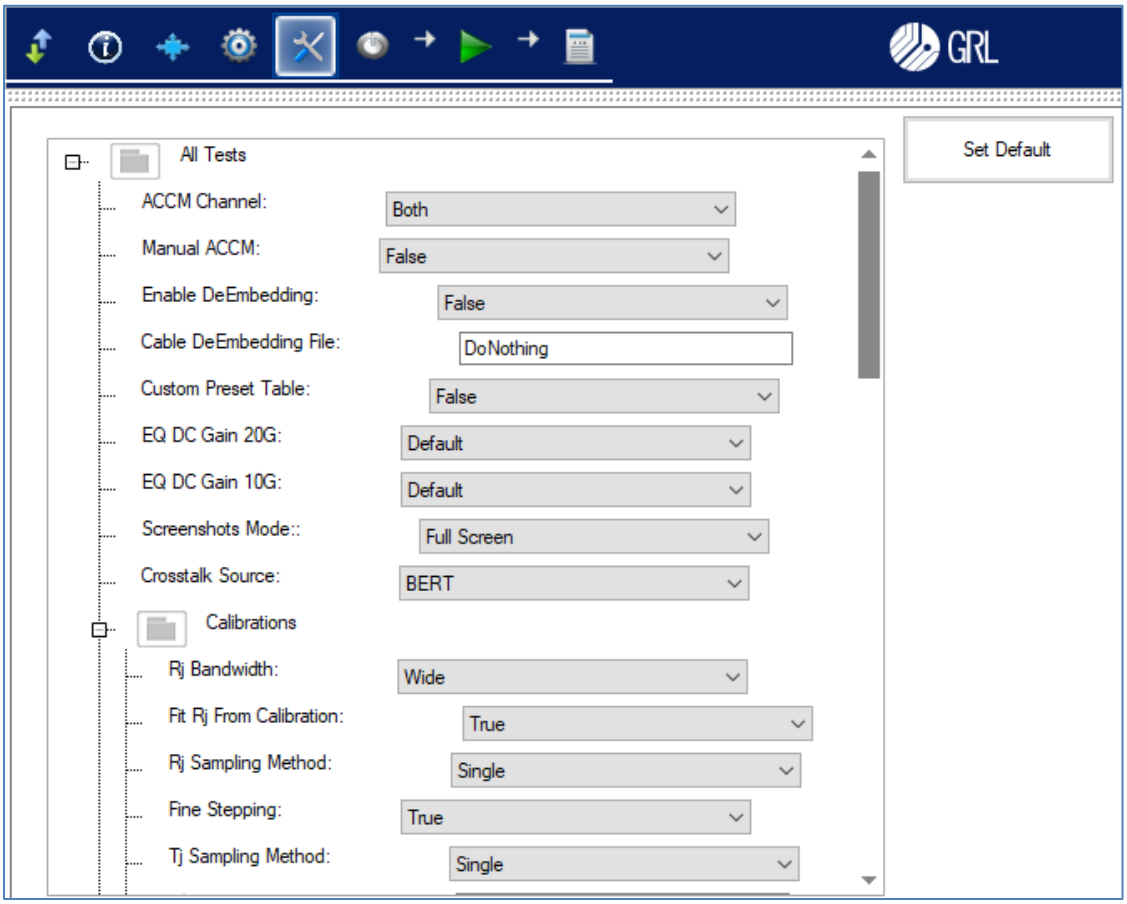


FIGURE 15. PARAMETERS CONFIGURATION PAGE

TABLE 4. CALIBRATION/TEST PARAMETERS DESCRIPTION

Parameter Name	Description
ACCM Channel	Select "Both" or single channel (splitter required) as the AC Common Mode (ACCM) source if used.
Manual ACCM	Set to "True" to manually set the ACCM source or "False" to apply calibrated values from ACCM calibration.
Enable DeEmbedding	Set to "True" to de-embed cable while calibrating.
Cable DeEmbedding File	Define the cable transfer function file. Applicable only when the "Enable DeEmbedding" field is set to "True".

Custom Preset Table	Set to “True” to use the list of user-defined measurement preset values for calibration.
EQ DC Gain (20G & 10G)	Select the DC Gain setting index for the 10G and 20G TP3_EQ systems.
Screenshots Mode	Select the type of screenshots to be captured when saving test results to a test report: • “Full Screen”: Image of the waveform along with the measurement area. • “Grid”: Image of only the waveform without showing the measurement area.
Crosstalk Source	Select whether to use the **MP1900A BERT** or an **External** source to generate crosstalk.
Rj Bandwidth	Select to use “Narrow” or “Wide” band for jitter decomposition algorithm to separate random jitter.
Fit Rj From Calibration	Set to “True” to fit random jitter value from calibration when running total jitter calibration.
Rj Sampling Method	Select the method to be used to perform random jitter sampling.
Fine Stepping	Set to “True” to enable fine stepping for the eye mask.
Tj Sampling Method	Select the method to be used to perform total jitter sampling.
10G & 20G Damping Factor	Define the 10G and 20G damping factor rates to use for calibration.
Tj Adjust Param	Select whether to use “Rj” or “Sj” for total jitter calibration for both <100 MHz and 100 MHz cases.
Eye Height Acquisition	Enter the number of measurements to acquire for Eye Height calibration.
Eye Mask Validation	Set to “True” to perform an eye mask validation test during calibration.
Eye Mask Max Violation Points	Define the maximum number of hits/violations that occur in the mask for eye mask validation.
EQ Eye Height Tolerance (mV)	Define the target tolerance value for equalization in mV during eye height validation.
Eye Width Tuning	Select “Retune” to repeat the tuning cycle or “Retry” to retry the current tuning procedure when measuring eye width.
Align Eye Mask Delay	Set to “True” to perform alignment for the delay in between validating the eye mask.
Maximum Retry	Enter the number of times to repeat calibration for pass/fail condition.
Save BERT Setup Only	“False” is usually the case. Set to “True” if you are sure that you only want to save the BERT test setup in the Rx test.
Prompt Before Link Training	“False” is usually the case. Set to “True” if you want to be prompted prior to start running link training.

Skip DUT Reset	"False" is usually the case. Set to "True" if you want to reset the DUT when performing tests.
PreEmphasis/Swing Loop Method	Select whether to use the **incremental** or DisplayPort Configuration Data (**DPCD**) register method for adjusting the Pre-emphasis and Swing voltage.
Initialize Training Lane Set	Set to "True" to reset HDCP register(0x102) before sending training pattern.
Reset Link Register	Set to "True" to perform link register reset during testing.
Ignore Error Count Mismatch	Set to "True" to ignore any differences in the error counts obtained during testing.
Always Initialize BERT	Set to "True" to bypass BERT initialization during testing.
Skip Link Training When SJ Changed	Set to "True" to skip the loopback link training sequence when there is a change in the SJ frequency.
Interval Time Factor	Specify the factor value for bit errors to be counted over a specified time interval.
10G & 20G Compliance Test Duration	Set how long it would take (in seconds) to test the DUT for 10G or 20G compliance.
Margin Step Size (%)	Set the step size for stepping through SJ or amplitude margins when running the optional margin search tests.
Maximum Margin Test Error	Define the maximum error count for error checking during margin search tests.
Maximum Steps	Define the maximum number of steps to step through margins.
20G/13.5G/10G Margin Test Minimum Bits (E9)	Set the minimum number of bits to run margin search tests for the 20 Gb/s, 13.5 Gb/s and 10 Gb/s data rates.
Margin Start (%)	Set the start point for the margin search test.
Prompt to Reset DUT	"False" is usually the case. Set to "True" if you want to be prompted to reset the DUT when performing tests.

3.5 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for certain calibration. To do this, select  from the menu to access the Calibration Target page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the 'Use Default Value' checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

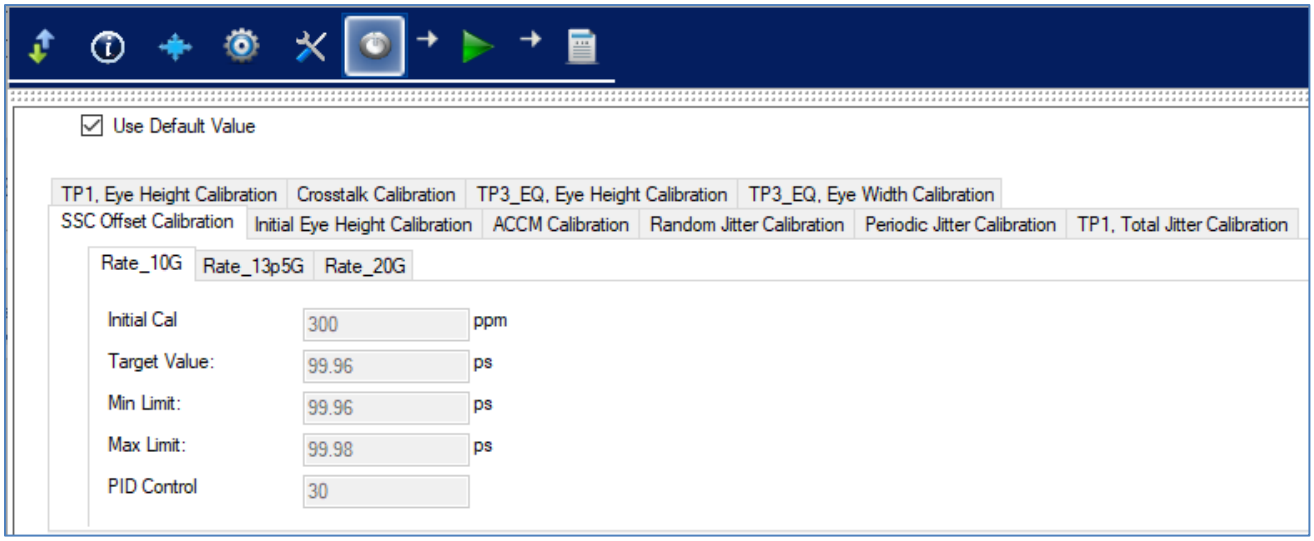


FIGURE 16. CALIBRATION OVERWRITE

3.6 Run Calibration/Tests

Select  from the menu to access the Run Tests page. The GRL software automatically runs the selected calibration or tests when initiated.

Before running the calibration or tests, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration/tests exist, the software will *skip* those calibration/tests.
- **Replace if Result Exists** – If results from previous calibration/tests exist, the software will *replace* those calibration/tests with new results.

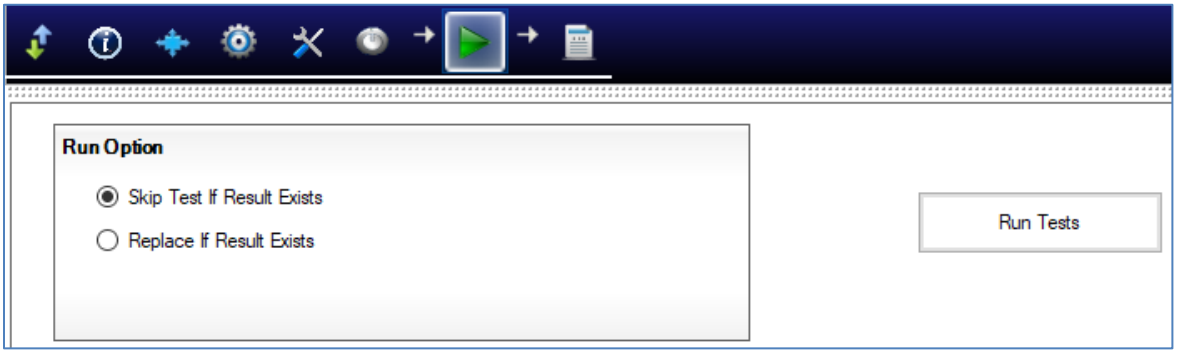


FIGURE 17. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration or tests. The connection diagram for the calibration or test being run will initially appear to allow the user to make sure

that the calibration/test environment has been properly set up before calibration/test can proceed.

If you need to re-run only certain calibration or tests on certain conditions, please delete the calibration or tests from the Report page and Run with **Skip Test if Result Exists**. The GRL software will keep track of the missing calibration or tests in the report and perform those calibration or tests only. See Section 6 for more information on Test Reports.

4 Sink Calibration Connection Setups

This section shows the typical connection setups to perform automated Sink Test Calibration.

4.1 Pre-Calibration/Test Procedures

Prior to running any calibration or test, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for the Oscilloscope and MP1900A BERT.
2. Run the Scope's SPC calibration routine. It is necessary to remove all probes from the Scope before running SPC.
3. Make sure you use a torque wrench with the proper torque specification to make all SMA connections.

4.2 Connection Setup for Anritsu MP1900A BERT Generator Set

Figure 18 shows the connection setup between each module of the Anritsu MP1900A BERT Generator Set.

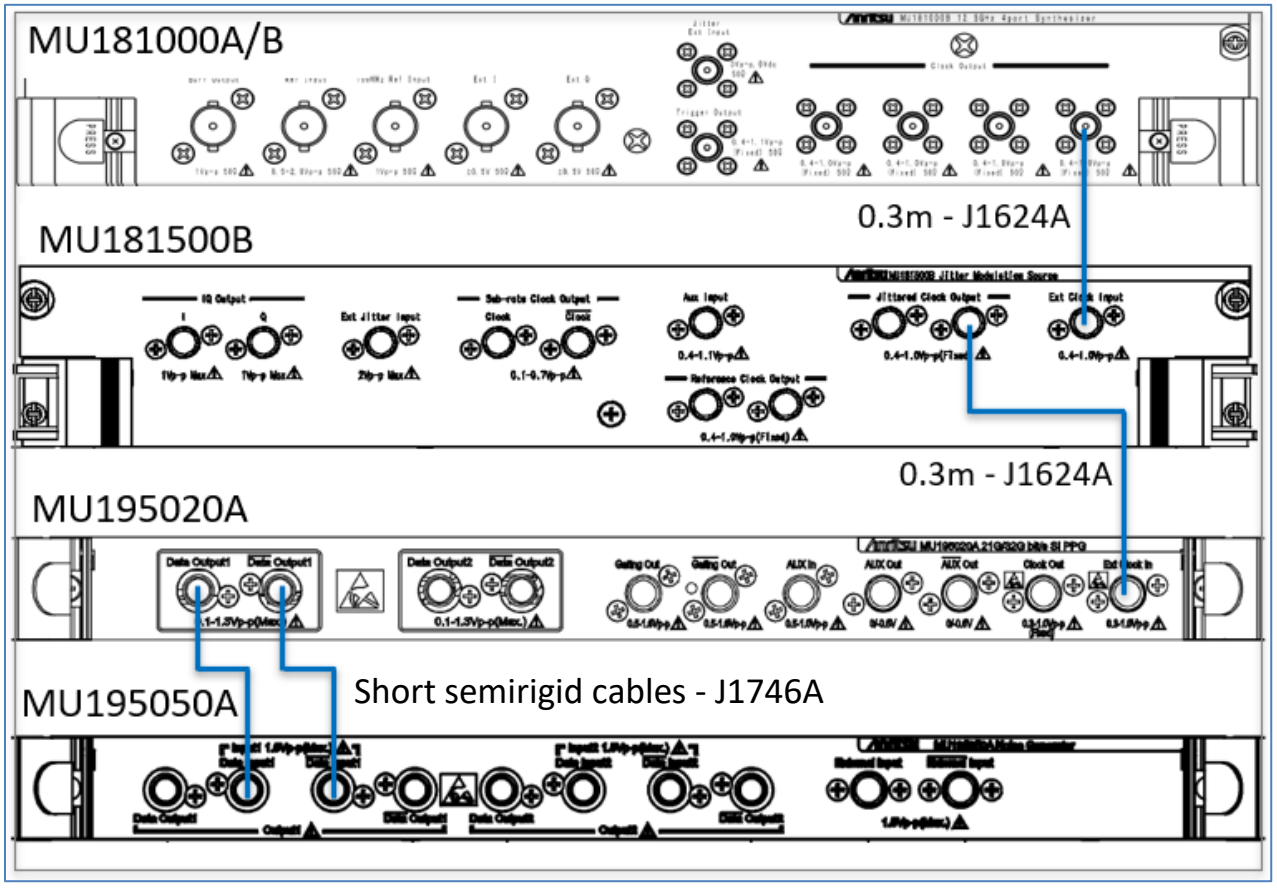


FIGURE 18. CONNECTION SETUP FOR MP1900A BERT GENERATOR SET MODULES

Connection Steps:

1. Using the J1624A SMA-SMA (0.3m) cable, connect the Clock Output of the MU181000A/B Synthesizer to the Ext Clock Input of the MU181500B Jitter Modulator.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU195020A Pulse Pattern Generator.
3. Using the J1746A K-K skew matched pair short semirigid cable, connect the MU195020A Data Outputs to the MU195050A Data Inputs.

4.3 DisplayPort USB Type-C Fixture Connector Pin Assignments

Figure 19 shows the pin assignments/ID for each connector pin of the DisplayPort USB Type-C Receptacle Fixture.

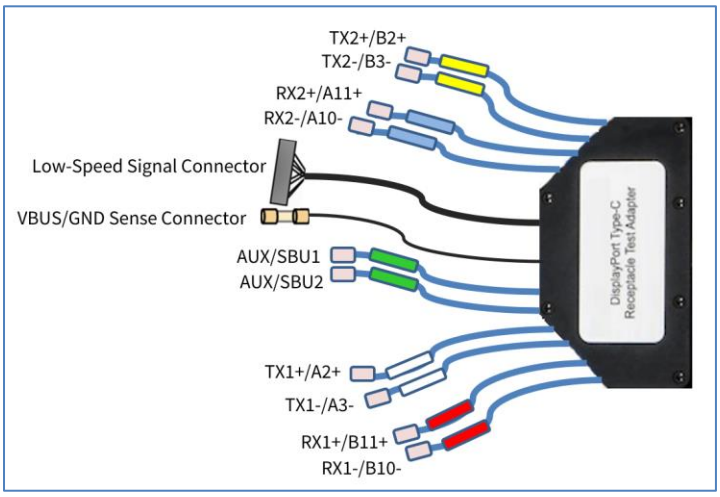


FIGURE 19. DISPLAYPORT USB TYPE-C RECEPTACLE FIXTURE CONNECTOR PIN ASSIGNMENTS

Figure 20 shows the pin assignments/ID for each connector pin of the DisplayPort USB Type-C Plug Fixture.

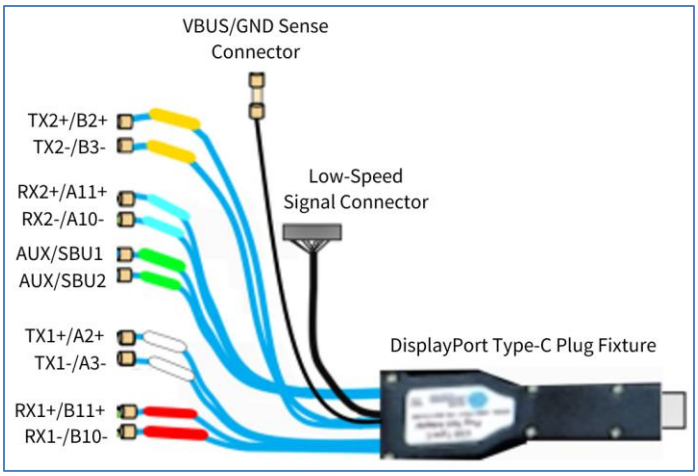


FIGURE 20. DISPLAYPORT USB TYPE-C PLUG FIXTURE CONNECTOR PIN ASSIGNMENTS

4.4 Standard/Mini DisplayPort Fixture Connector Pin Assignments

Figure 21 shows the pin assignments/ID for each connector pin of the Standard/Mini DisplayPort Receptacle Fixture.

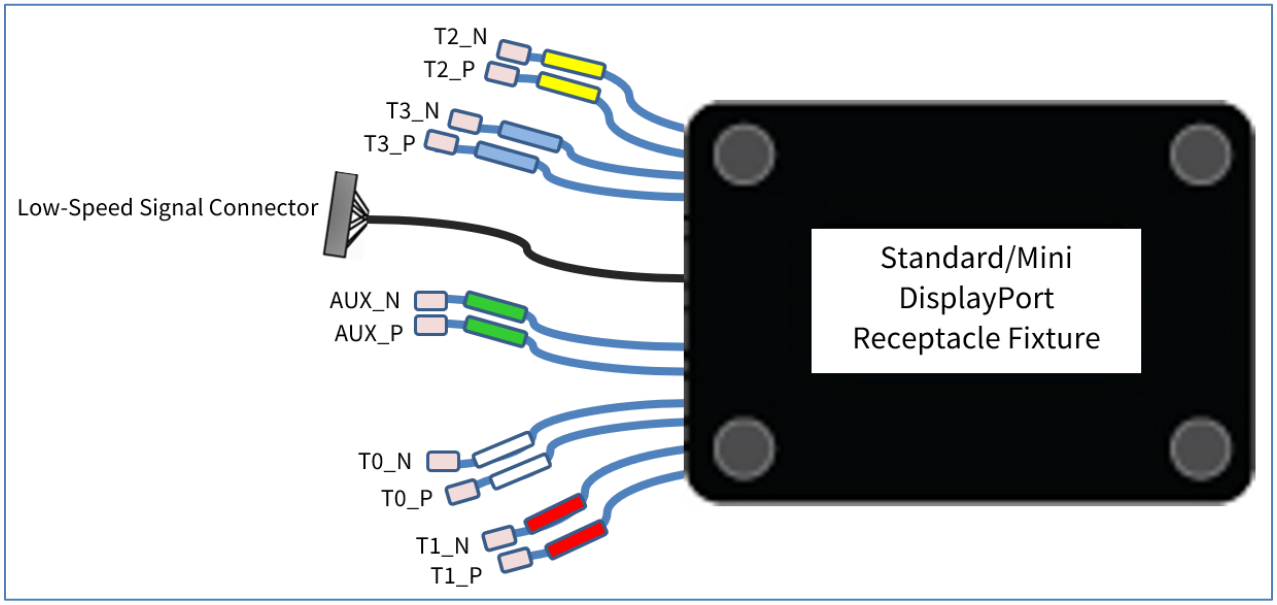


FIGURE 21. STANDARD/MINI DISPLAYPORT RECEPTACLE FIXTURE CONNECTOR PIN ASSIGNMENTS

Figure 22 shows the pin assignments/ID for each connector pin of the Standard/Mini DisplayPort Plug Fixture.

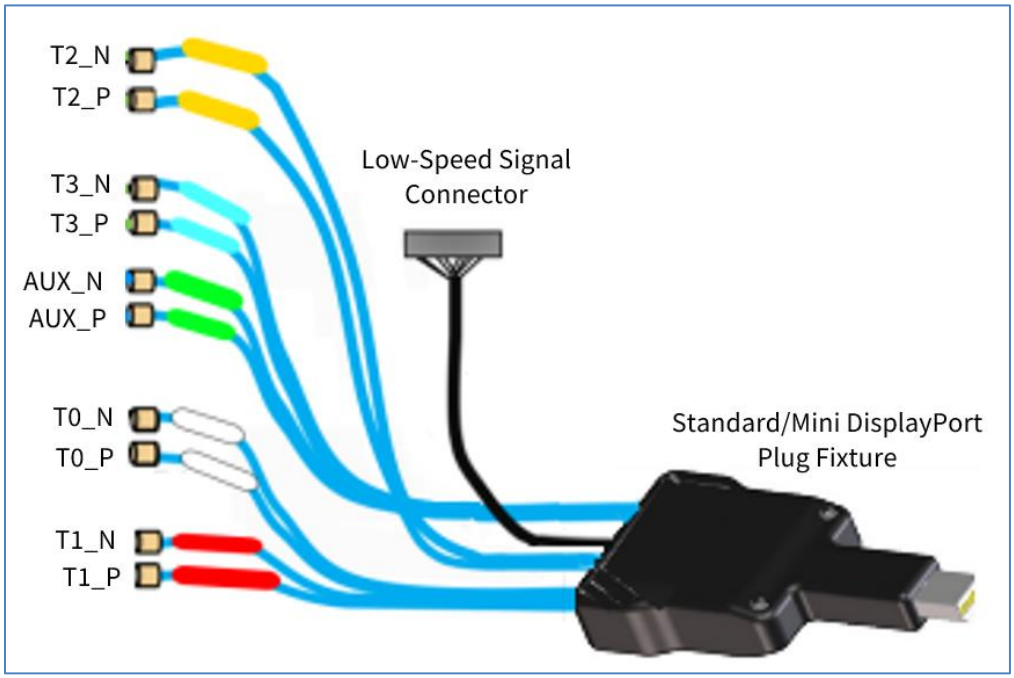


FIGURE 22. STANDARD/MINI DISPLAYPORT PLUG FIXTURE CONNECTOR PIN ASSIGNMENTS

4.5 Calibration Connection Setups

4.5.1 Calibration Setup at TP1

Figure 23 below shows the typical setup for Sink signal calibration at Test Point 1.

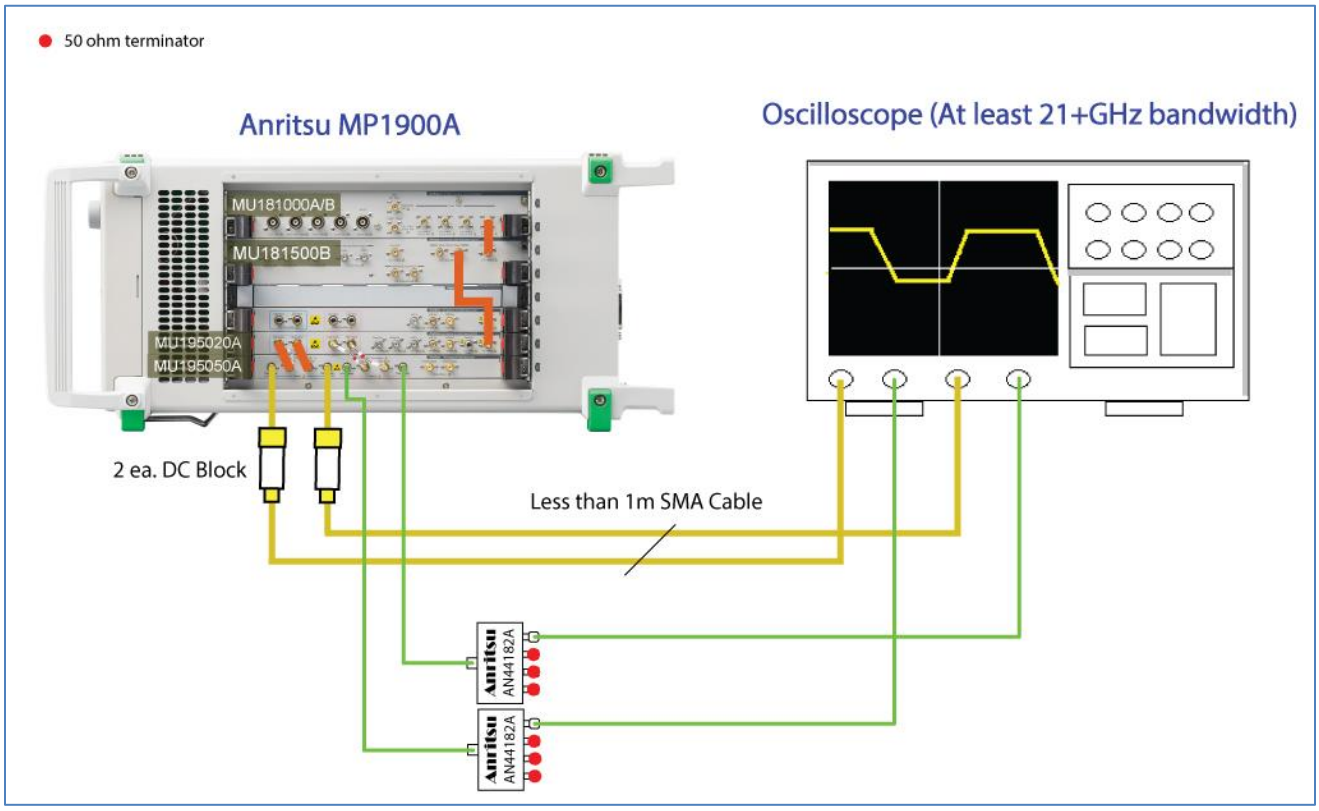


FIGURE 23. TYPICAL TP1 SINK CALIBRATION SETUP

Connection Steps:

1. Using the MP1900A BERT setup connections (Section 4.2), connect the MU195050A first data outputs through DC blocks to Channels 1 and 3 on the Scope using phase matched K-K coaxial cables.
2. Connect the MU195050A second data outputs through the AN44182A Power Dividers to Channels 2 and 4 on the Scope using phase matched K-K coaxial cables to inject crosstalk.
   Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.

4.5.2 Calibration Setup at TP3_EQ for DisplayPort USB Type-C Mode

Figure 24, Figure 25 and Figure 26 below show the DisplayPort USB Type-C mode typical setup for Sink signal calibration at Test Point 3 with Equalizer applied. TP3_EQ is a physical test point that will affect the eye opening due to the sum of a fixed channel length (representing the fixed ISI on the transmitter side of a host or device) and a physical USB Type-C Cable.

- For the UHBR 10 (10 Gb/s) data rate, the total Insertion Loss is -18.5 dB at 5 GHz, which uses a 2M USB Type-C cable.
- For the UHBR 13.5 (13.5 Gb/s) data rate, the total Insertion Loss is -17.5 dB at 6.75 GHz, which uses a 0.8M USB Type-C cable.
- For the UHBR 20 (20 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 10 GHz, which uses a 0.8M USB Type-C cable.

The cable's downstream plug connector is connected to a DisplayPort 2.1 receptacle adapter fixture to measure the signal with the scope. The scope uses software equalization to open the eye for calibration.

Note: Cables connecting the signal to the Scope should be de-embedded and ≤ 1m.

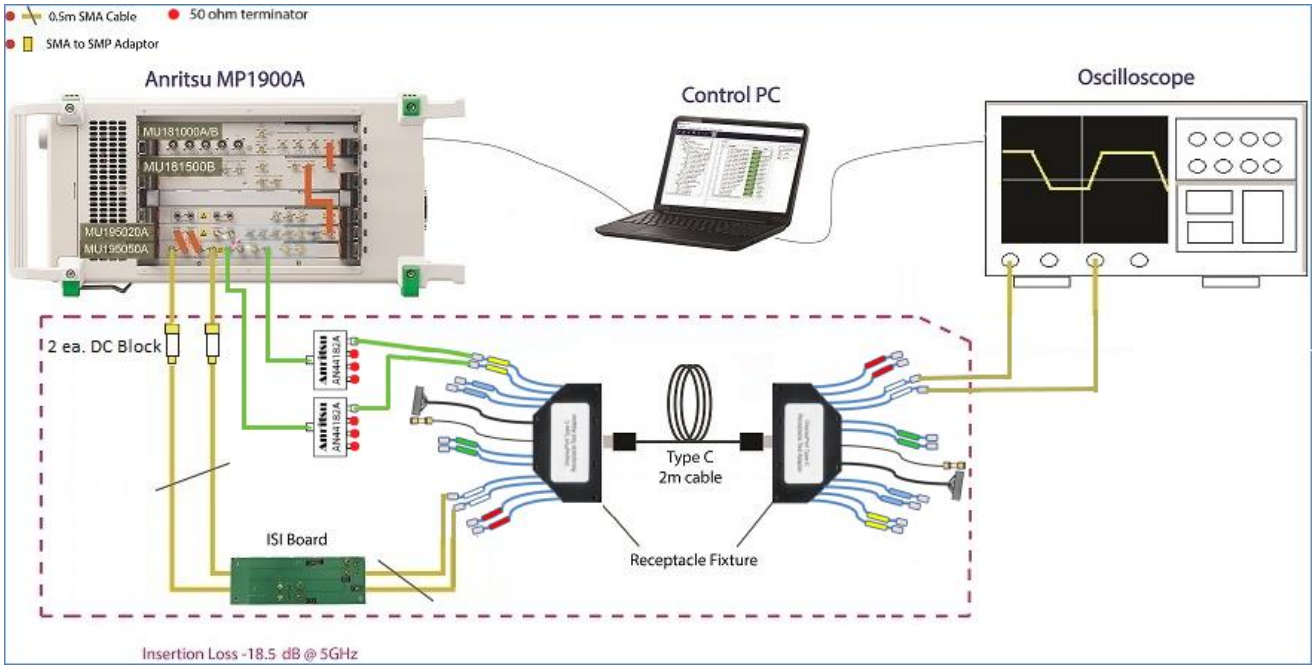


FIGURE 24. SETUP FOR TP3_EQ CALIBRATION AT 10G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.

2. Connect the MU195050A first data outputs through DC blocks to ISI channels (for 10 Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 2M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

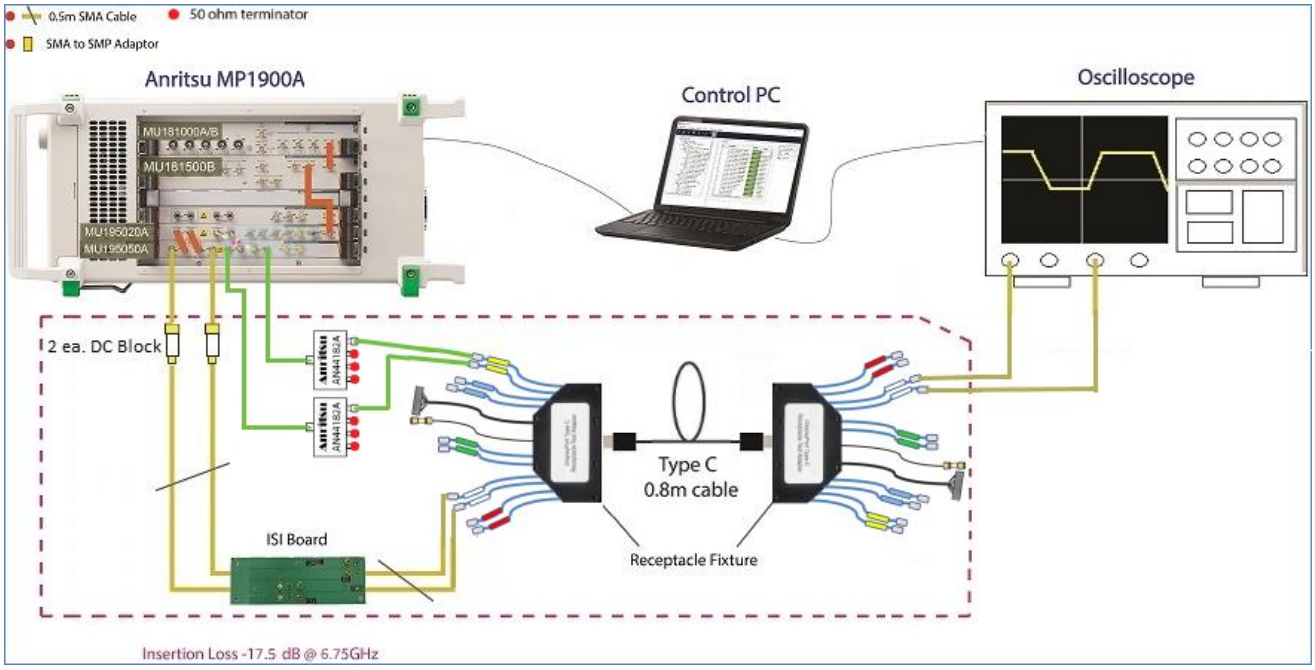


FIGURE 25. SETUP FOR TP3_EQ CALIBRATION AT 13.5G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 13.5Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 0.8M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

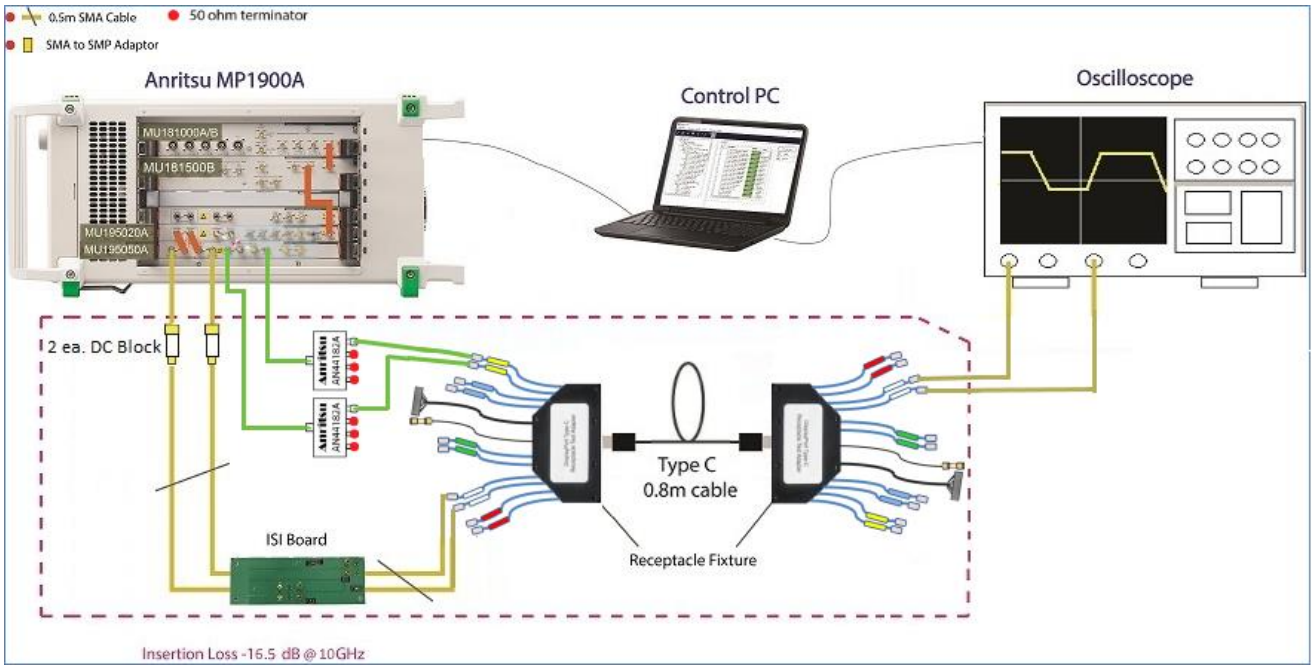


FIGURE 26. SETUP FOR TP3_EQ CALIBRATION AT 20G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 20Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 0.8M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

4.5.3 Calibration Setup at TP3_EQ for Standard/Mini DisplayPort Mode

Figure 27, Figure 28 and Figure 29 below show the Standard/Mini DisplayPort mode typical setup for Sink signal calibration at Test Point 3 with Equalizer applied. TP3_EQ is a physical test point that will affect the eye opening due to the sum of a fixed channel length (representing the fixed ISI on the transmitter side of a host or device) and a physical USB Type-C Cable.

- For the UHBR 10 (10 Gb/s) data rate, the total Insertion Loss is -19 dB at 5 GHz, which uses a 2M Standard/Mini DisplayPort cable.
- For the UHBR 13.5 (13.5 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 6.75 GHz, which uses a 0.8M Standard/Mini DisplayPort cable.
- For the UHBR 20 (20 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 10 GHz, which uses a 0.8M Standard/Mini DisplayPort cable.

The cable's downstream plug connector is connected to a Standard/Mini DisplayPort receptacle adapter fixture to measure the signal with the scope. The scope uses software equalization to open the eye for calibration.

Note: Cables connecting the signal to the Scope should be de-embedded and ≤ 1m.

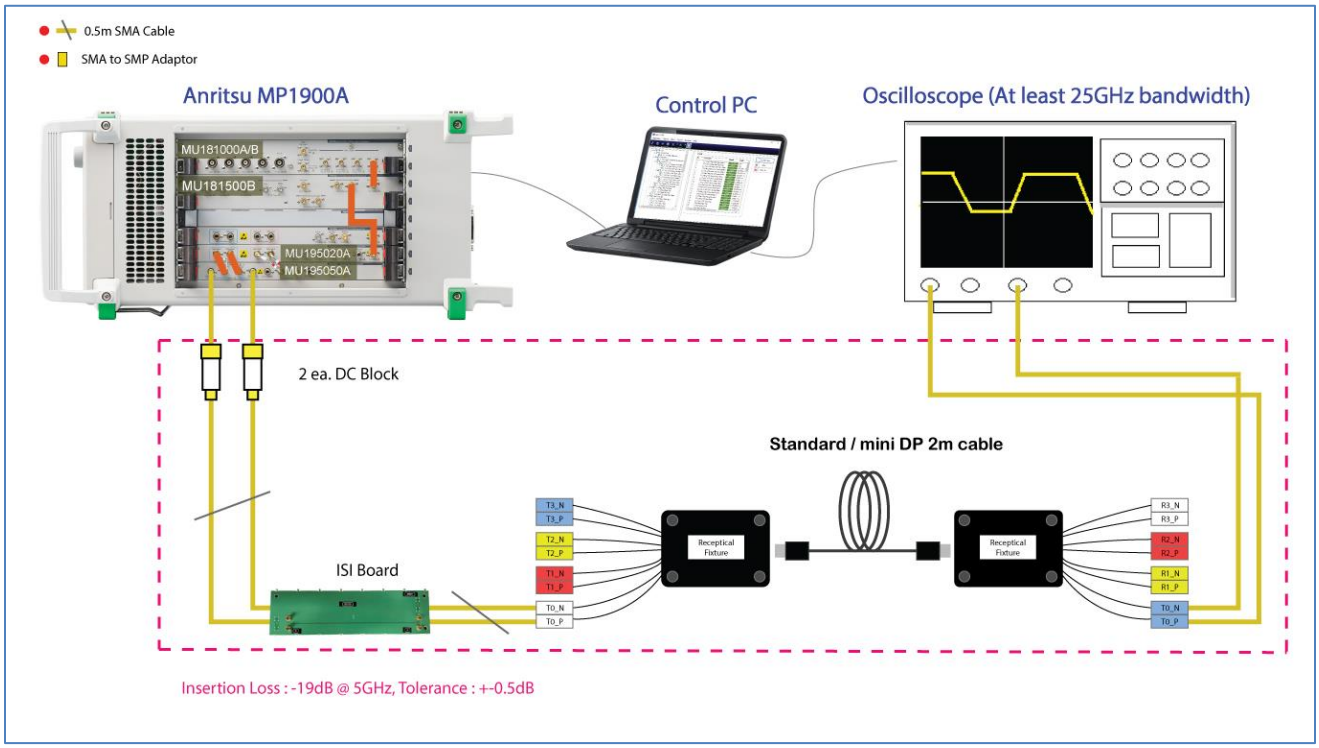


FIGURE 27. SETUP FOR TP3_EQ CALIBRATION AT 10G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.

2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 10 Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 2M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

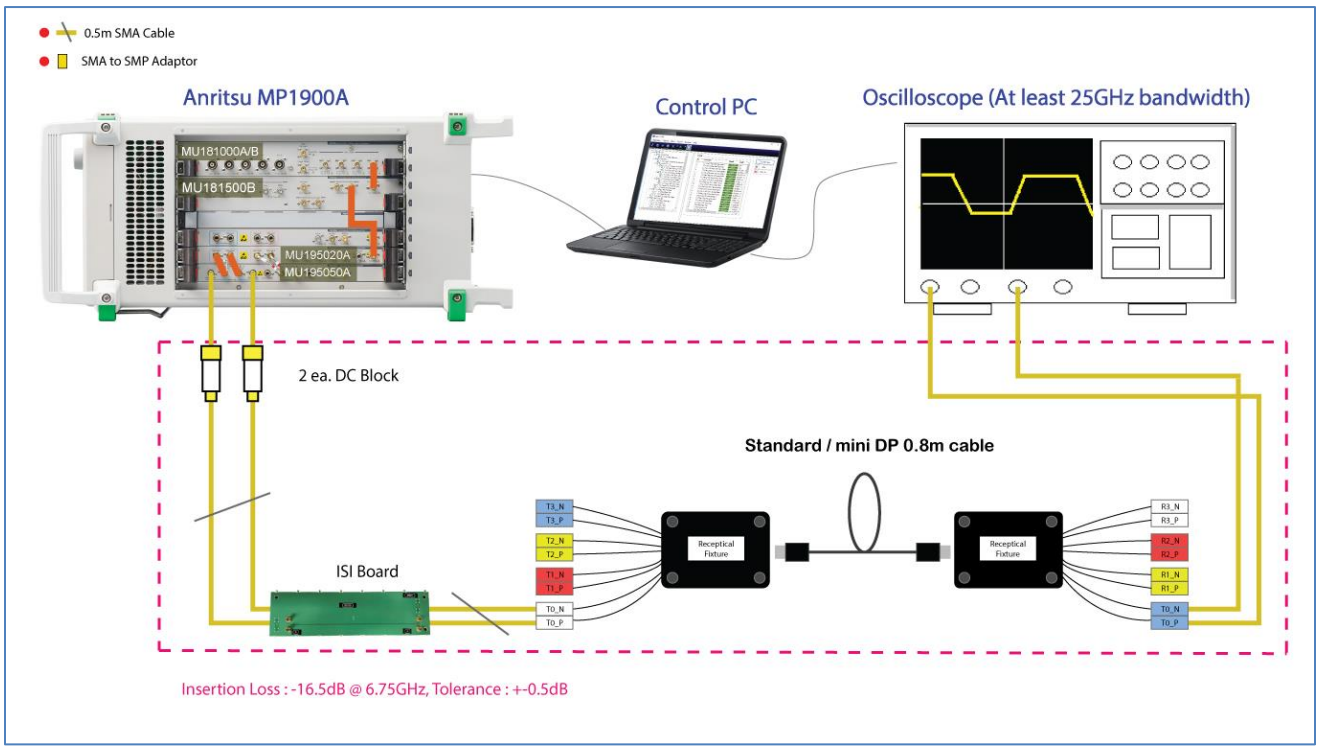


FIGURE 28. SETUP FOR TP3_EQ CALIBRATION AT 13.5G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 13.5Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 0.8M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

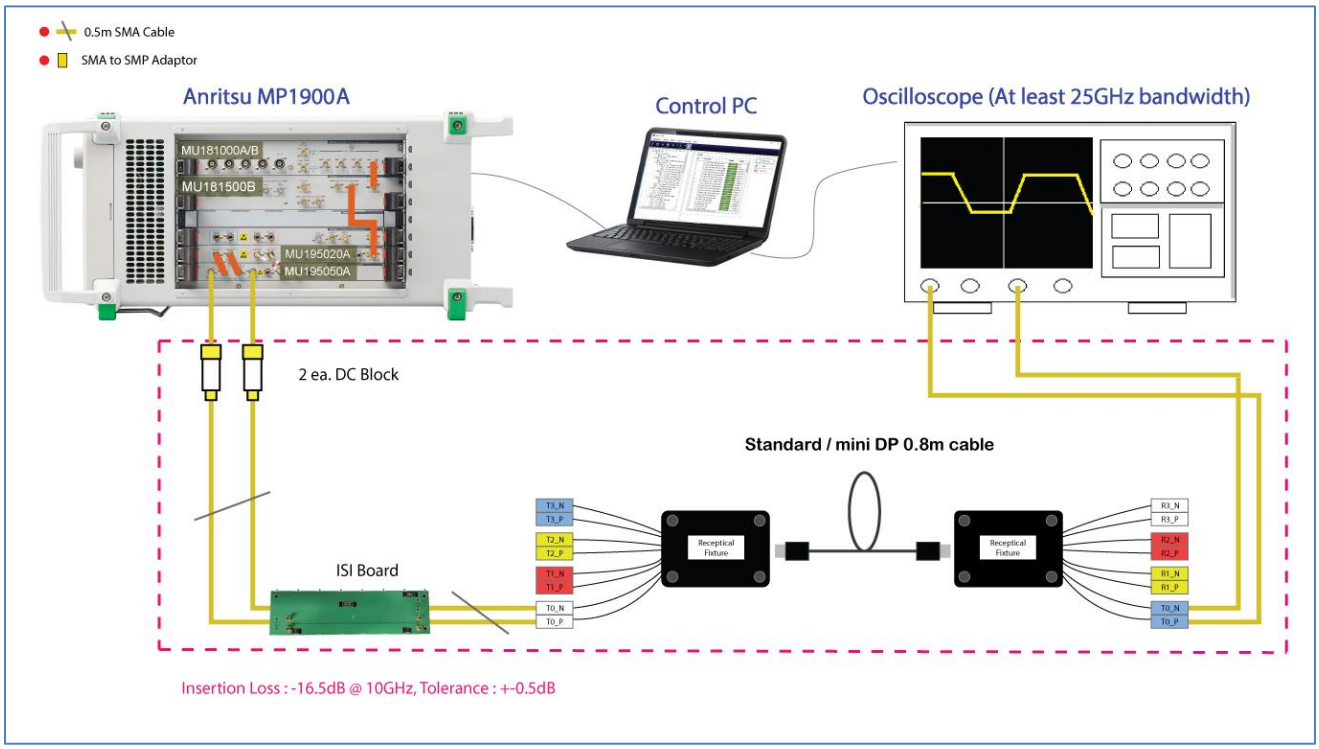


FIGURE 29. SETUP FOR TP3_EQ CALIBRATION AT 20G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 20Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 0.8M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

5 Sink DUT Compliance Test Setups

After calibration has completed, testing the DisplayPort Sink DUT for CTS compliance can be performed. The GRL-DP21-SINK-AN application supports automated testing of a DisplayPort Sink device if the device supports standard DPCD through the AUX channel or a compatible AUX controller is connected.

5.1 Test Connection Setups

5.1.1 DUT BER Compliance Test Setup at TP1 for DisplayPort USB Type-C Mode

Figure 30 below shows the DisplayPort USB Type-C mode physical setup for the DisplayPort Sink DUT BER test at Test Point 1. The calibrated stressed signal is attached to a DisplayPort 2.1 USB Type-C plug fixture and crosstalk is added to the fixture from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts.

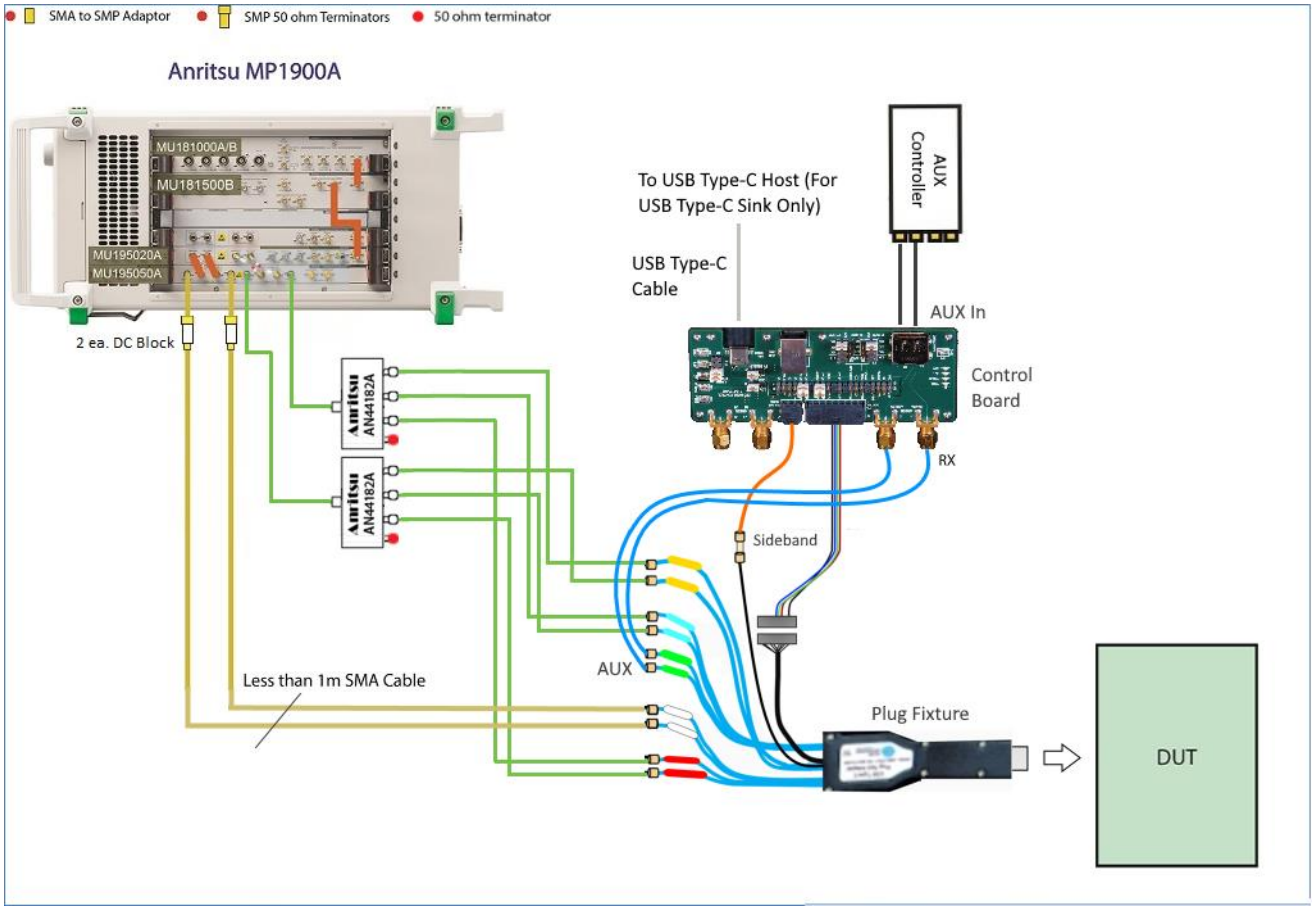


FIGURE 30. BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP1 FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Attach the USB Type-C connector of the DisplayPort 2.1 plug fixture to the DUT's USB Type-C receptacle connector.

2. Using the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
3. Connect the MU195050A first data outputs through DC blocks to Rx Lane0/Lane1 of the DUT through the DisplayPort 2.1 plug fixture (at TX1+/A2+ and TX1-/A3- pins).
4. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the DUT that are not under test through the plug fixture (for example, at TX2+/B2+ & TX2-/B3- pins, RX2+/A11+ & RX2-/A10- pins, and RX1+/B11+ & RX1-/B10- pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*
5. Connect the green AUX cable pair of the plug fixture to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the sideband cables of the plug fixture to their allocated slots on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

5.1.2 DUT BER Compliance Test Setup at TP1 for Standard/Mini DisplayPort Mode

Figure 31 below shows the Standard/Mini DisplayPort mode physical setup for the DisplayPort Sink DUT BER test at Test Point 1. The calibrated stressed signal is attached to a Standard/Mini DisplayPort plug fixture and crosstalk is added to the fixture from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts.

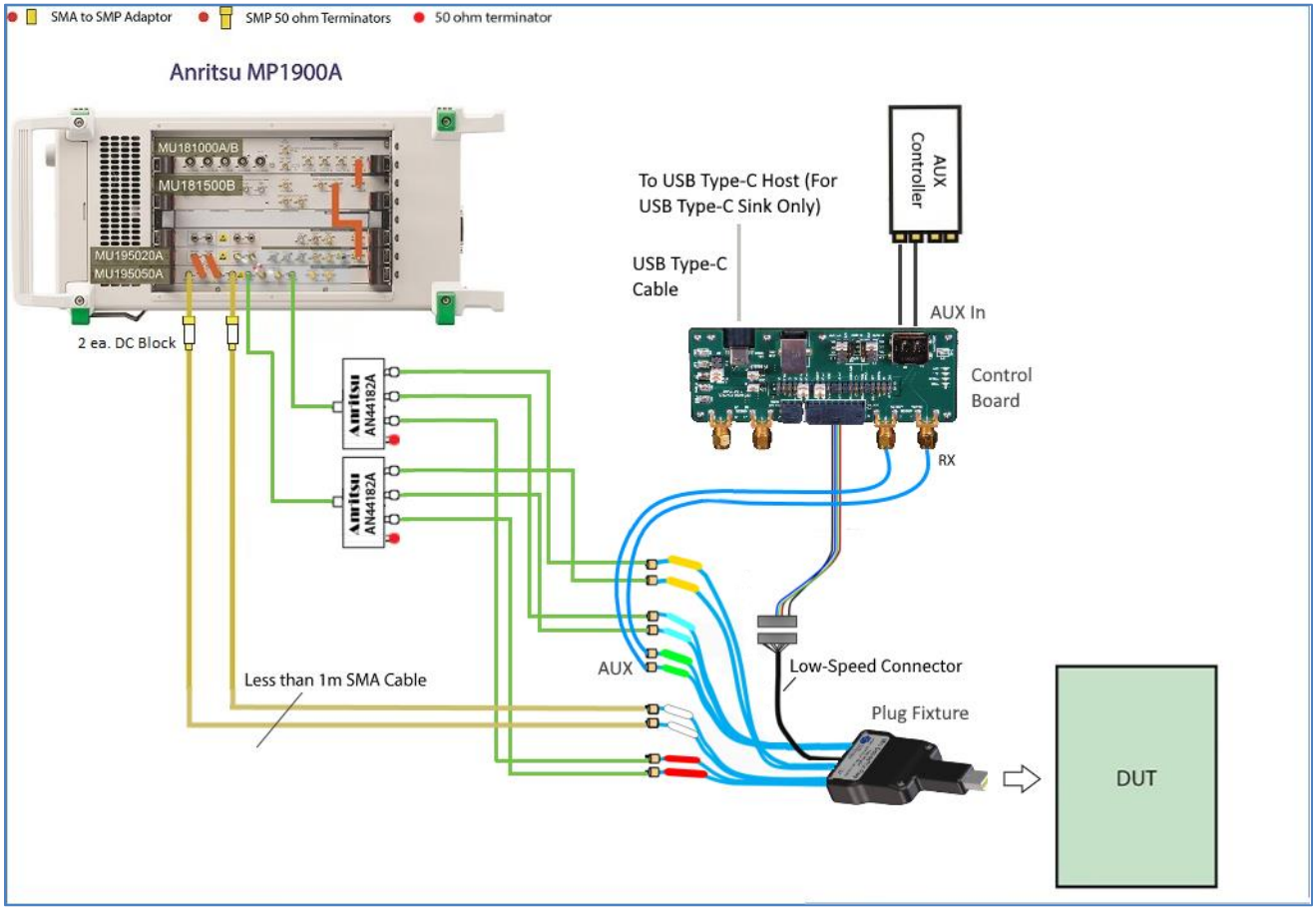


FIGURE 31. BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP1 FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Attach the Standard/Mini DisplayPort connector of the DisplayPort plug fixture to the DUT's Standard/Mini DisplayPort receptacle connector.
2. Using the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
3. Connect the MU195050A first data outputs through DC blocks to Rx Lane0/Lane1 of the DUT through the DisplayPort 2.1 plug fixture (at T0_P and T0_N pins).
4. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the DUT that are not under test through the plug fixture (for example, at T2_P & T2_N

pins, T3_P & T3_N pins, and T1_P & T1_N pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

5. Connect the green AUX cable pair of the plug fixture to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the low-speed connector cable of the receptacle adapter to the allocated slot on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

5.1.3 DUT BER Compliance Test Setup at TP3_EQ for DisplayPort USB Type-C Mode

Figure 32 and Figure 33 show the DisplayPort USB Type-C Mode physical setups for the DisplayPort Sink DUT BER test at Test Point 3 with Equalizer applied.

The calibrated stressed signal (with ISI) is attached to a DisplayPort 2.1 USB Type-C receptacle adapter and crosstalk is added to the adapter from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts. A USB Type-C cable is connected between the DisplayPort 2.1 receptacle adapter and the DUT's USB Type-C receptacle connector as follows:

- For the UHBR 10 (10 Gb/s) data rate, the setup uses a 2M USB Type-C cable.
- For the UHBR 13.5 (13.5 Gb/s) and UHBR 20 (20 Gb/s) data rates, the setup uses a 0.8M USB Type-C cable.

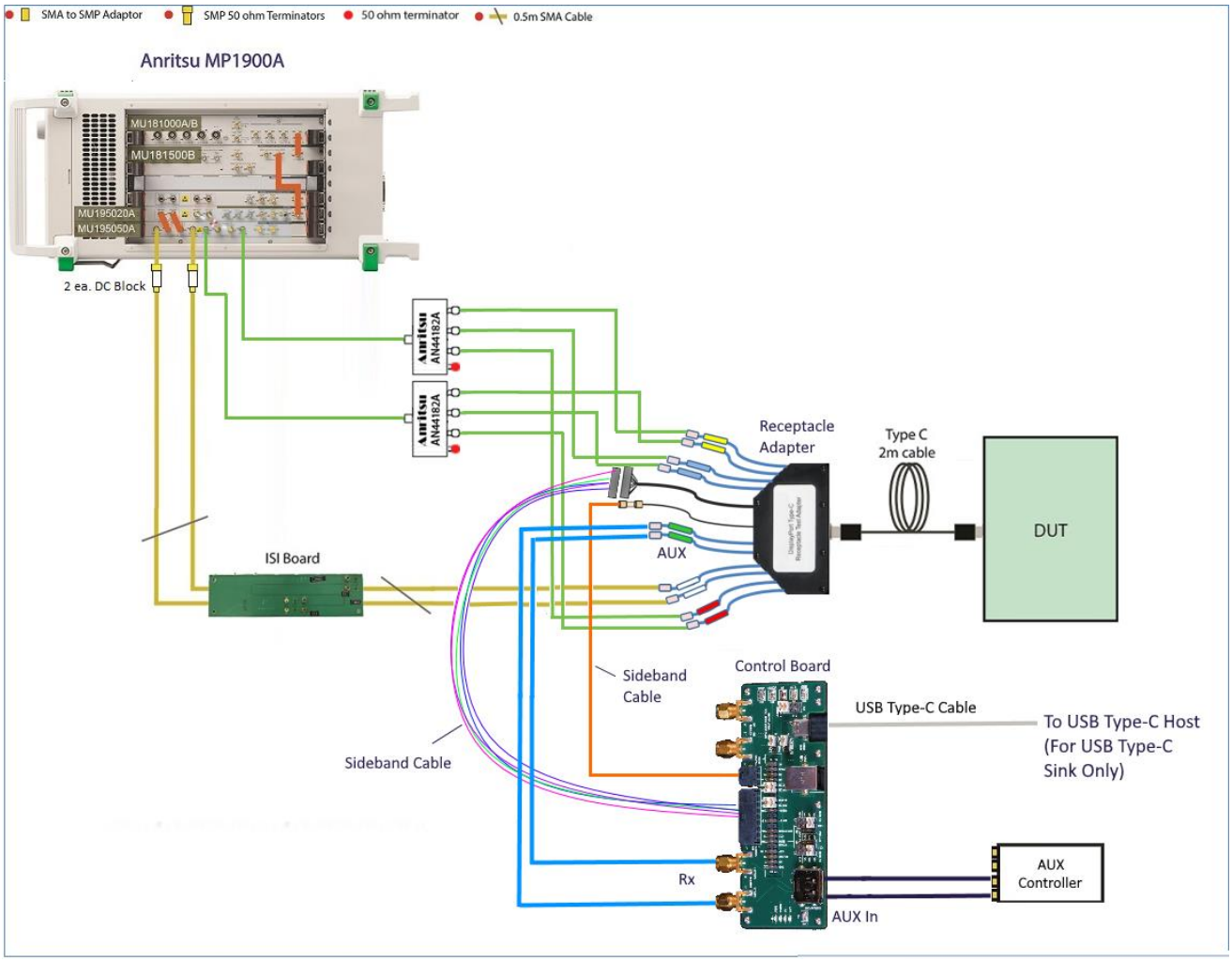


FIGURE 32. DISPLAYPORT USB TYPE-C MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 10G

Connection Steps:

1. Using the MP1900A BERT TP3_EQ calibration setup (Section 4.5.2), disconnect the DisplayPort 2.1 receptacle adapter fixture that connects to the scope.
2. Attach the 2M USB Type-C cable to the DUT's USB Type-C receptacle connector.
3. Connect the ISI channels to Rx Lane0/Lane1 of the DisplayPort 2.1 receptacle adapter (at TX1+/A2+ and TX1-/A3- pins).
4. Connect the AN44182A Power Dividers to the Rx lanes of the receptacle adapter that are not under test (for example, at TX2+/B2+ & TX2-/B3- pins, RX2+/A11+ & RX2-/A10- pins, and RX1+/B11+ & RX1-/B10- pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*
5. Connect the green AUX cable pair of the receptacle adapter to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the sideband cables of the receptacle adapter to their allocated slots on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

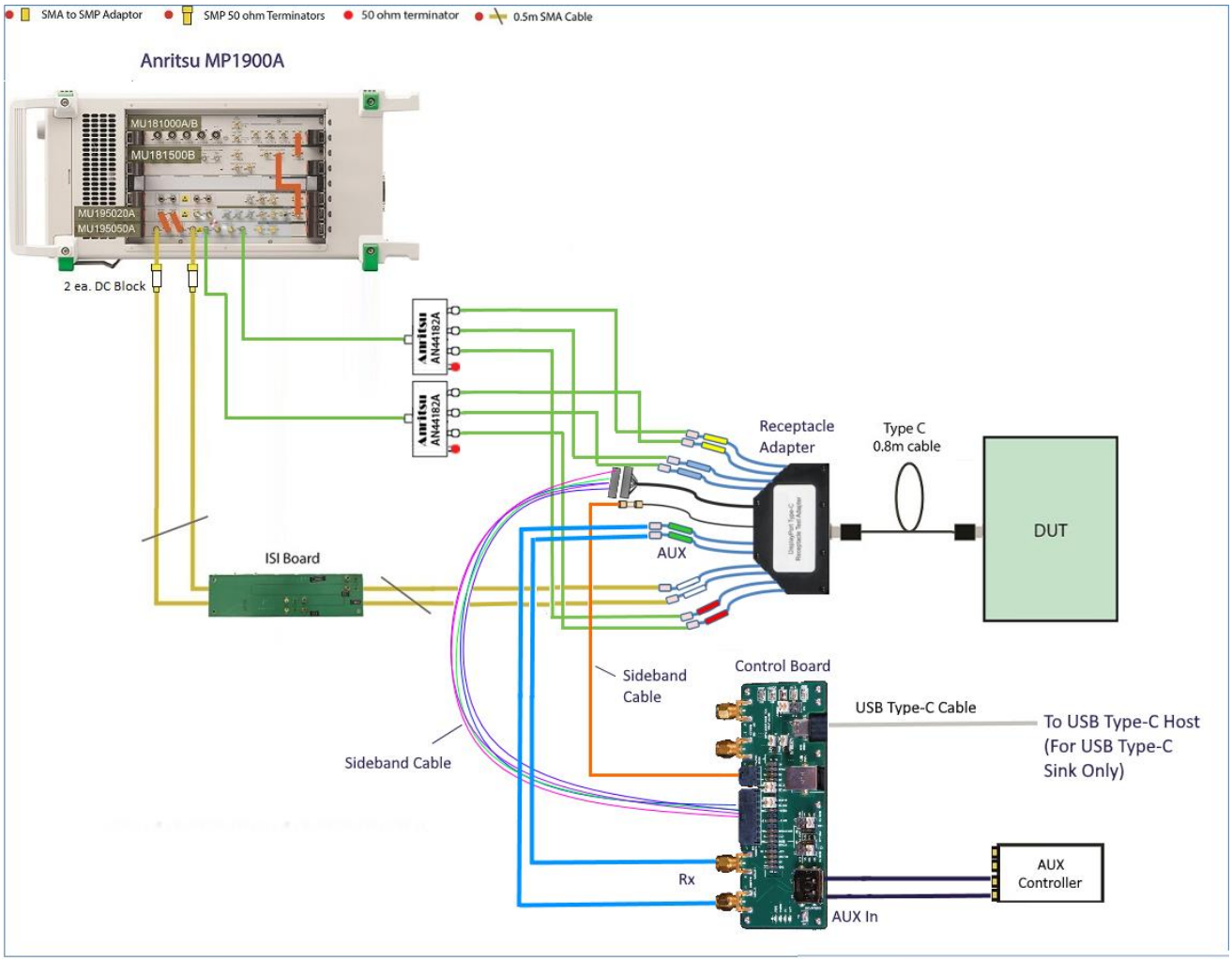


FIGURE 33. DISPLAYPORT USB TYPE-C MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 13.5G AND 20G

Connection Step:

Using the same setup for TP3_EQ at 10G in Figure 32, replace the 2M USB Type-C cable with the 0.8M USB Type-C cable to the DUT's USB Type-C receptacle connector.

5.1.4 DUT BER Compliance Test Setup at TP3_EQ for Standard/Mini DisplayPort Mode

Figure 34 and Figure 35 show the Standard/Mini DisplayPort Mode physical setups for the DisplayPort Sink DUT BER test at Test Point 3 with Equalizer applied.

The calibrated stressed signal (with ISI) is attached to a Standard/Mini DisplayPort receptacle adapter and crosstalk is added to the adapter from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts. A Standard/Mini DisplayPort cable is connected between the Standard/Mini DisplayPort receptacle adapter and the DUT's Standard/Mini DisplayPort receptacle connector as follows:

- For the UHBR 10 (10 Gb/s) data rate, the setup uses a 2M USB Type-C cable.
- For the UHBR 13.5 (13.5 Gb/s) and UHBR 20 (20 Gb/s) data rates, the setup uses a 0.8M USB Type-C cable.

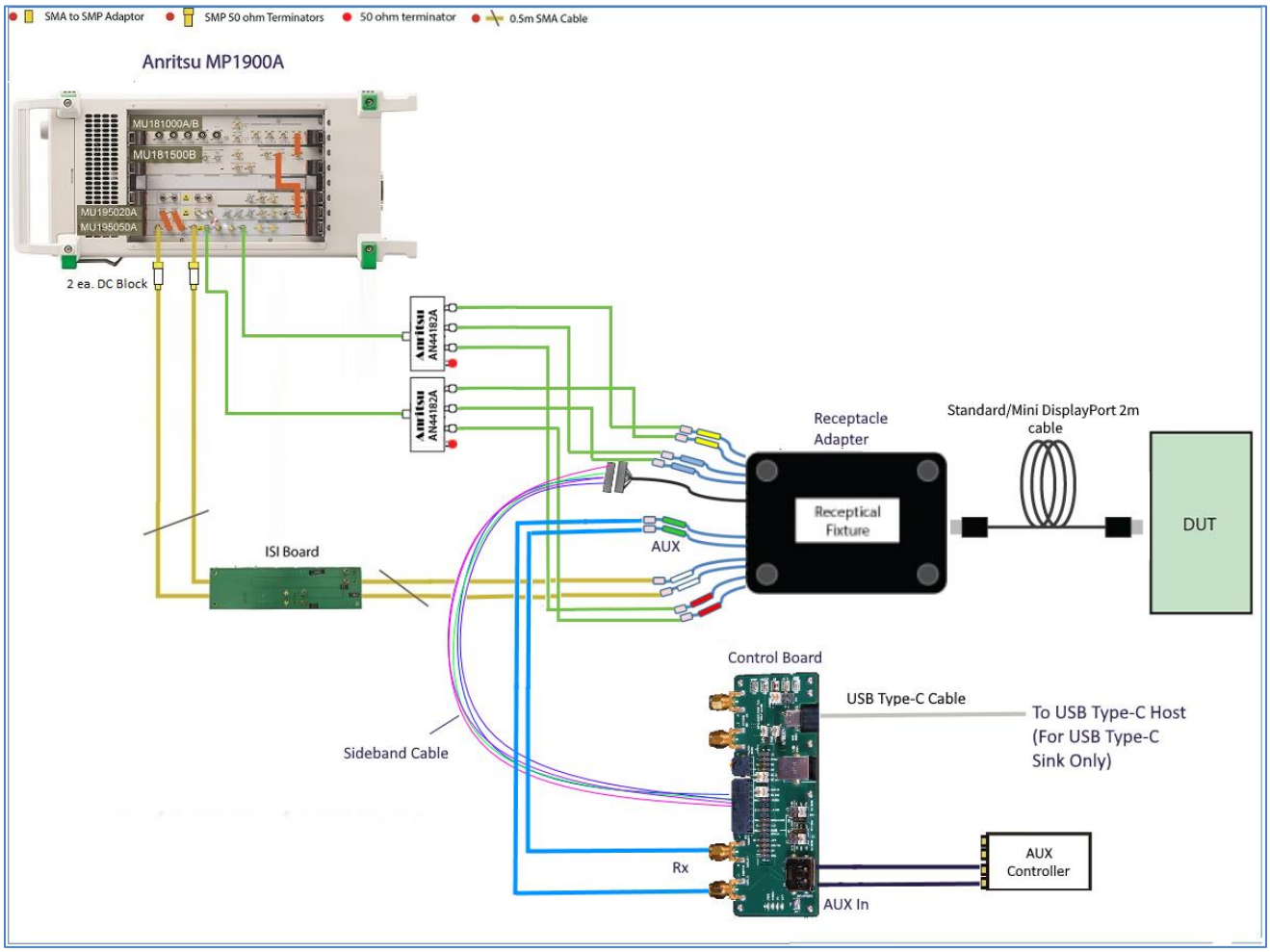


FIGURE 34. STANDARD/MINI DISPLAYPORT MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 10G

Connection Steps:

1. Using the MP1900A BERT TP3_EQ calibration setup (Section 4.5.3), disconnect the DisplayPort receptacle adapter fixture that connects to the scope.
2. Connect the MU195050A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at T2_P & T2_N pins, T3_P & T3_N pins, and T1_P & T1_N pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*
3. Attach the 2M Standard/Mini DisplayPort cable to the DUT's receptacle connector.
4. Connect the ISI channels to Rx Lane0/Lane1 of the Standard/Mini DisplayPort receptacle adapter (at T0_P and T0_N pins).
5. Connect the green AUX cable pair of the receptacle adapter to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the low-speed connector cable of the receptacle adapter to the allocated slot on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

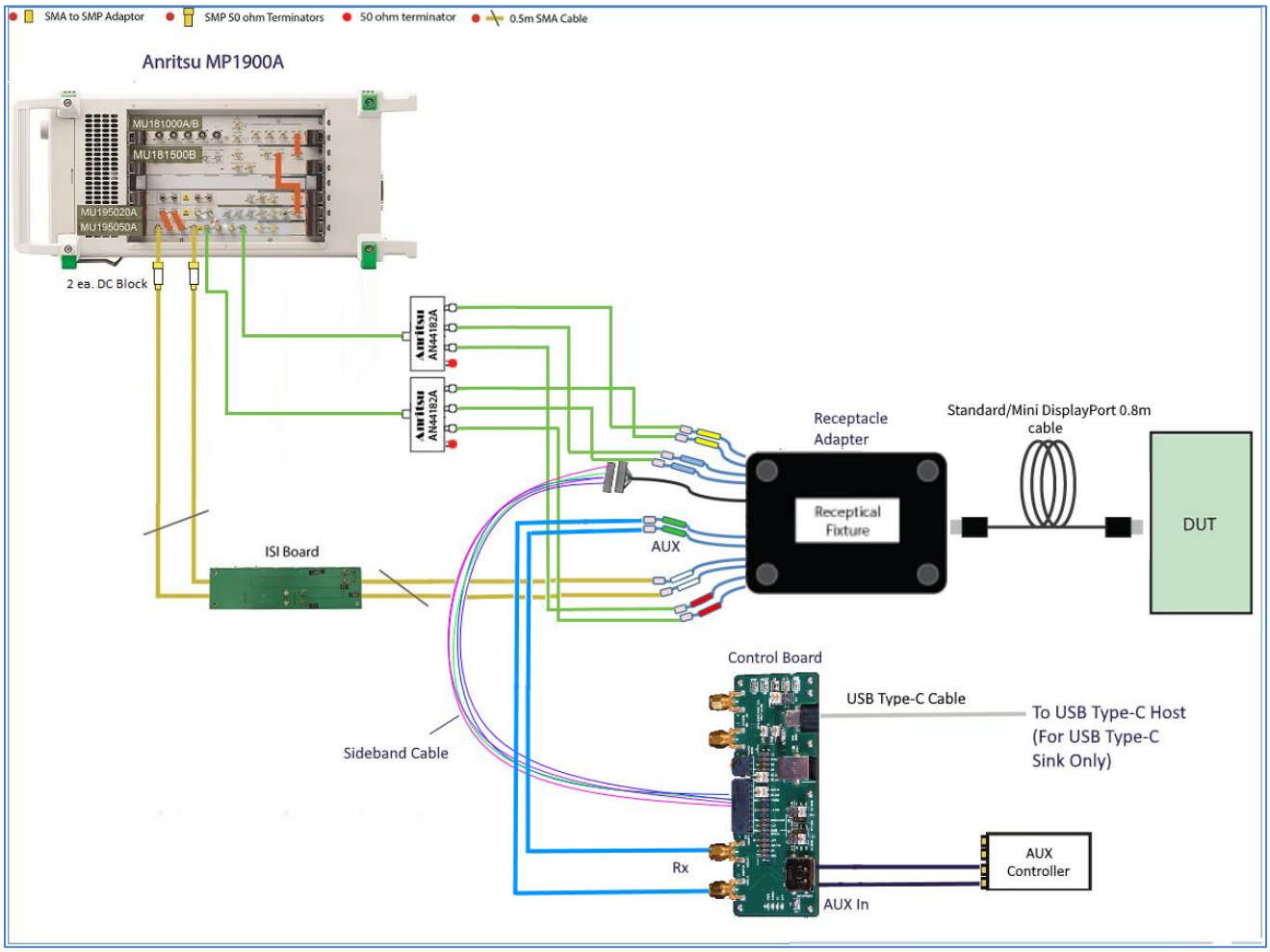


FIGURE 35. STANDARD/MINI DISPLAYPORT MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 13.5G AND 20G

Connection Step:

Using the same setup for TP3_EQ at 10G in Figure 34, replace the 2M Standard/Mini DisplayPort cable with the 0.8M Standard/Mini DisplayPort cable to the DUT's receptacle connector.

5.1.5 Margin Testing

While it is sufficient to perform the BER Compliance Test for each test condition to meet compliance specifications, it is also useful to determine how much Margin your design contains.

The Margin for each test condition can be verified as follows:

a) In the Configurations page, set up the following margin test parameters. Refer to Section 3.4 for the description of each parameter.

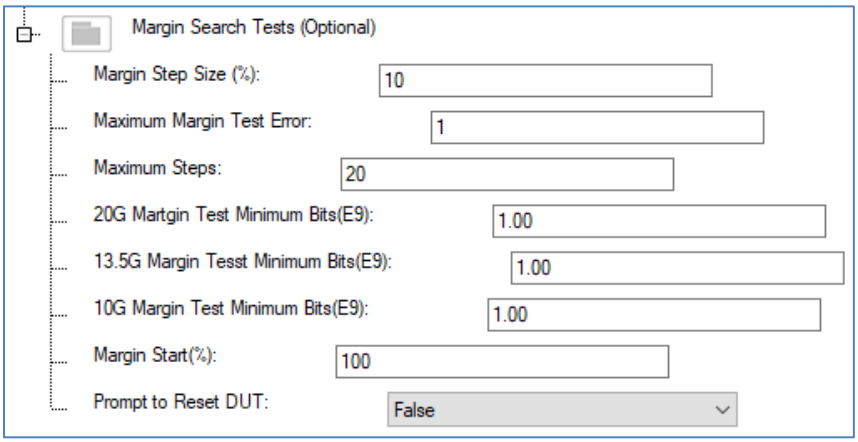


FIGURE 36. MARGIN TEST CONFIGURATION

b) Once configured, select and run the "Sink Margin Test" for the test point(s) and data rate(s) as required.

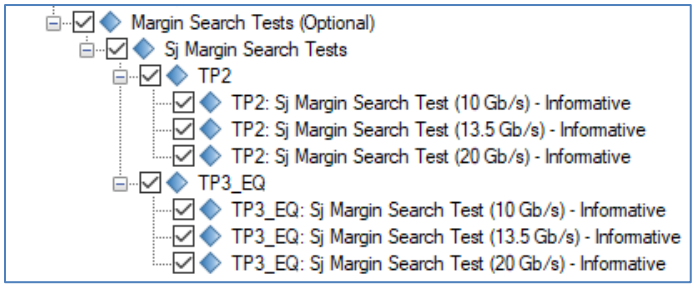


FIGURE 37. SINK MARGIN TEST SELECTION

6 Test Results and Reports Using GRL-DP21-SINK-AN

The **Report** page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

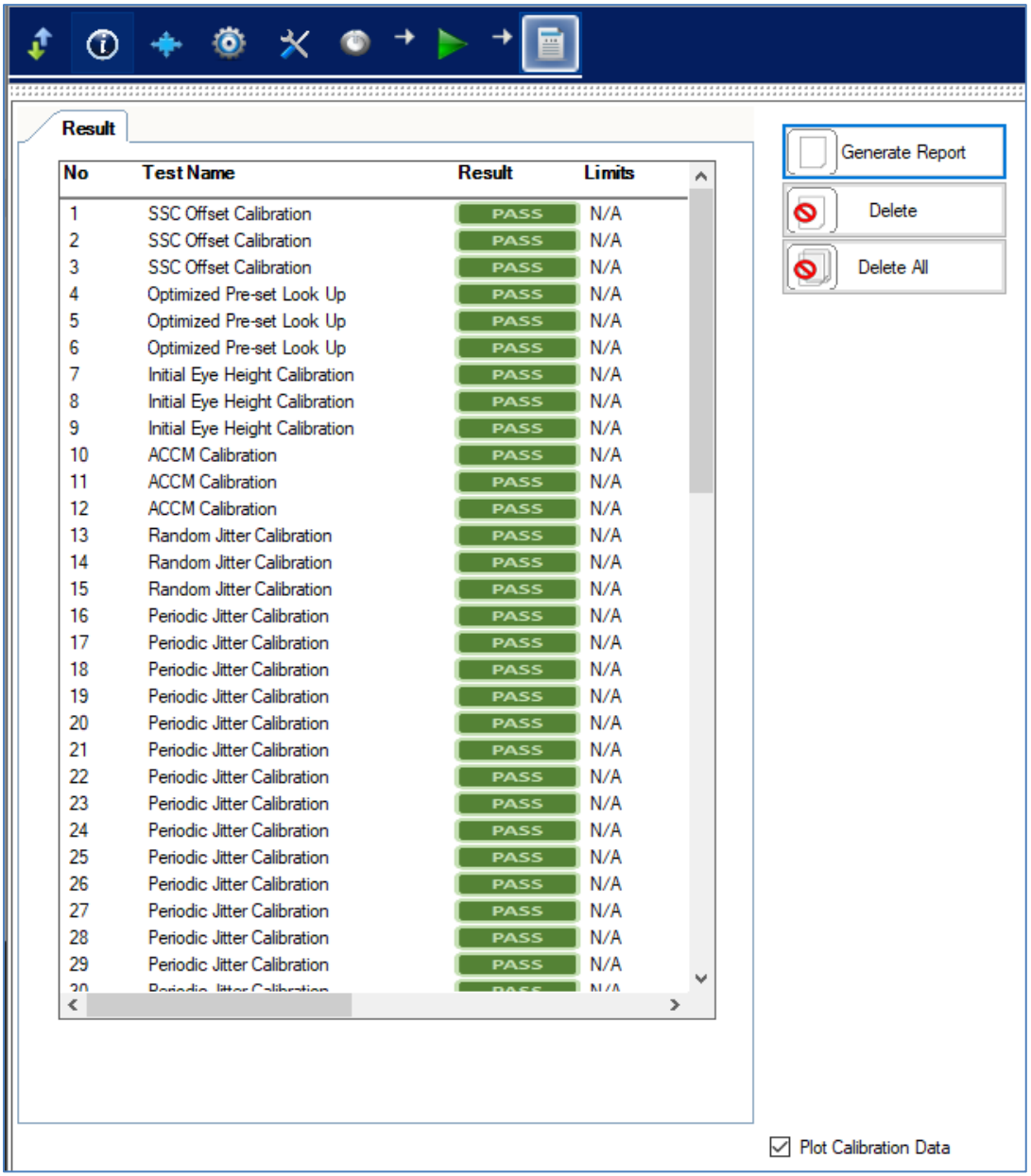
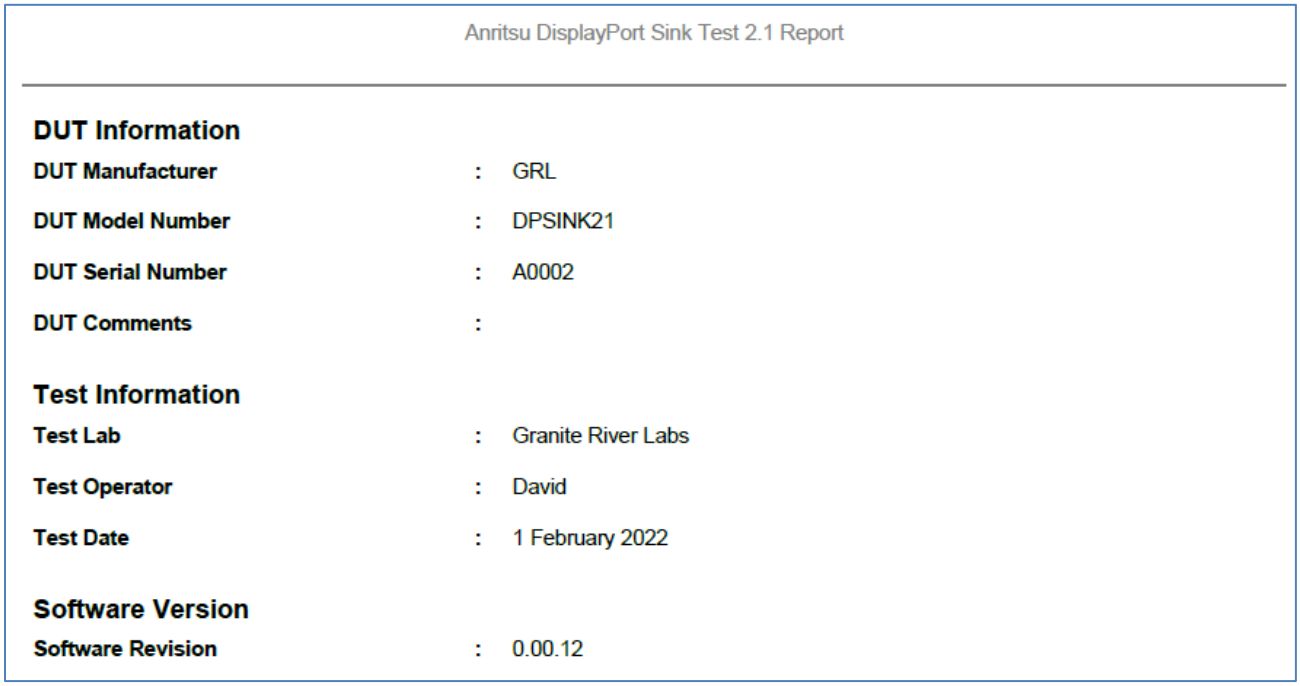


FIGURE 38. REPORT RESULTS PAGE

6.1.1 DUT Information

This portion is populated from the information in the DUT tab on the **Session Info** page.


Anritsu DisplayPort Sink Test 2.1 Report

DUT Information

DUT Manufacturer	:	GRL
DUT Model Number	:	DPSINK21
DUT Serial Number	:	A0002
DUT Comments	:	

Test Information

Test Lab	:	Granite River Labs
Test Operator	:	David
Test Date	:	1 February 2022

Software Version

Software Revision	:	0.00.12

FIGURE 39. DUT INFORMATION

6.1.2 Results Summary Table

This portion is populated from the calibration and tests performed with their respective results. This gives an overall view of all the results and test conditions.

No	TestName	Limits	Value	Results	Lane	Test Point	Data Rate	SJ Frequency
1	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
2	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
3	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
4	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
5	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
6	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
7	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
8	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
9	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
10	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
11	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
12	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
13	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
14	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
15	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
16	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ1
17	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ2
18	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ3
19	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ4
20	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ5
21	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ6
22	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ1
23	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ2
24	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ3
25	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ4
26	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ5
27	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ6
28	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ1
29	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ2
30	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ3
31	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ4
32	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ5
33	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ6
34	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ1
35	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ2

No	TestName	Limits	Value	Results	Lane	Test Point	Data Rate	SJ Frequency
36	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ3
37	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ4
38	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ5
39	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ6
40	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ1
41	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ2
42	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ3
43	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ4
44	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ5
45	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ6
46	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ1
47	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ2
48	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ3
49	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ4
50	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ5
51	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ6
52	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ1
53	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ2
54	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ3
55	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ4
56	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ5
57	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ6
58	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ1
59	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ2
60	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ3
61	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ4
62	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ5
63	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ6
64	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ1
65	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ2
66	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ3
67	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ4
68	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ5
69	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ6
70	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate_10G	N/A
71	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate_13p5G	N/A
72	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate_20G	N/A
73	Optimized EQ Look Up	N/A	N/A	Pass	N/A	TP3	Rate_13p5G	N/A
74	TP3, EQ, Eye Height Calibration	N/A	N/A	Pass	N/A	TP3	Rate_13p5G	SJ5

FIGURE 40. RESULTS SUMMARY TABLE EXAMPLE

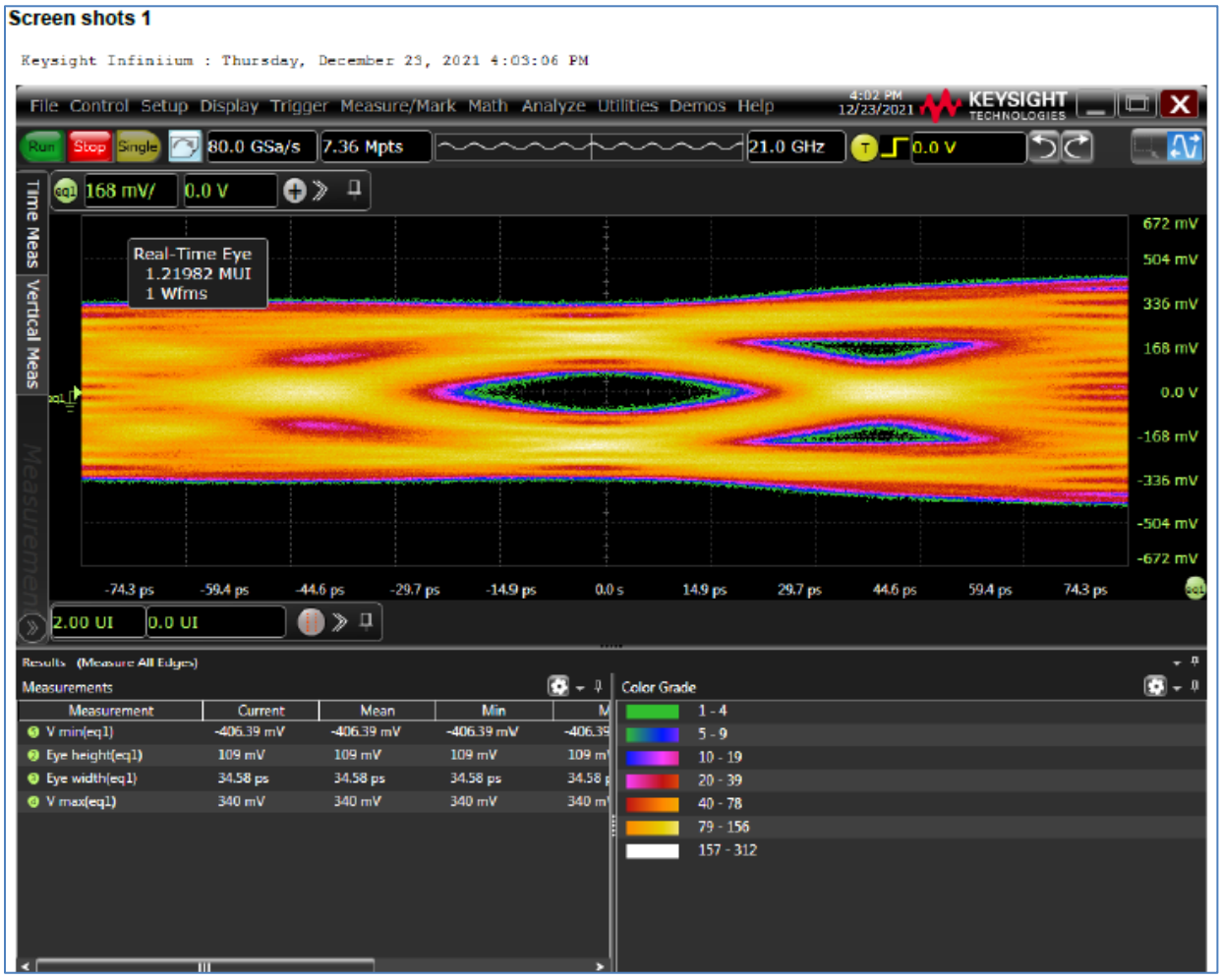
6.1.3 Calibration & Test Result Details

This portion is populated with results from each of the calibration and test runs. Here the results are explained in depth with supporting data points and screenshots. If the Plot Calibration Data checkbox is selected, then the plots are also displayed.

74. TP3_EQ, Eye Height Calibration [TP3_EQ,Rate_13p5G,SJ5]

Pass/Fail Stats	:	Pass
Cal Parameter	:	Final Eye Height_Rate_13p5G__TP3__SJ5
Settings Parameter	:	Eye Amplitude
Settings	:	1060.0000 mV
Measured Parameter	:	Eye Height
Measured Value	:	106.0000 mV
Sj Frequency	:	50.0000 MHz
Test completed time	:	23 December 2021 16:03:11 PM

Screen shots 1



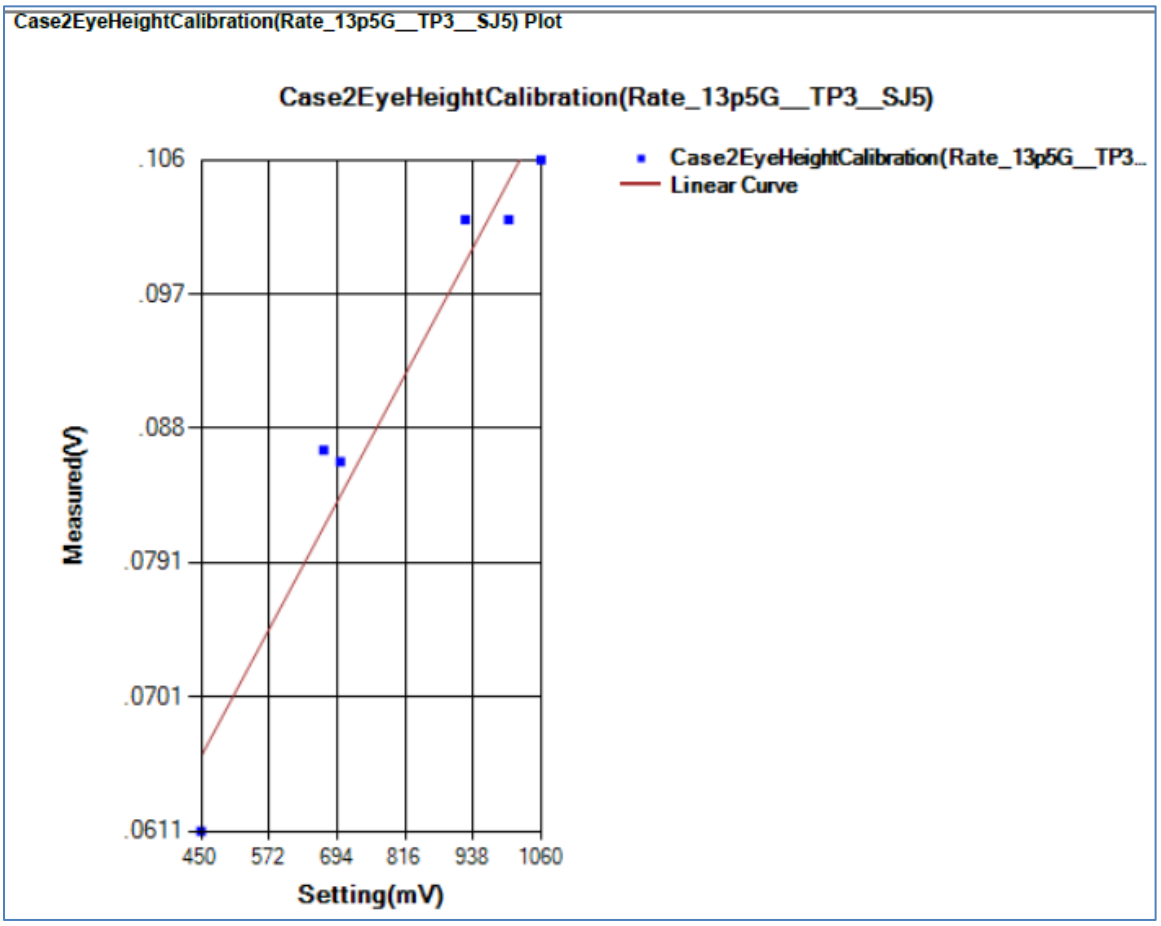


FIGURE 41. CALIBRATION/TEST RESULT DETAILS EXAMPLE

6.2 Delete Test Results

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

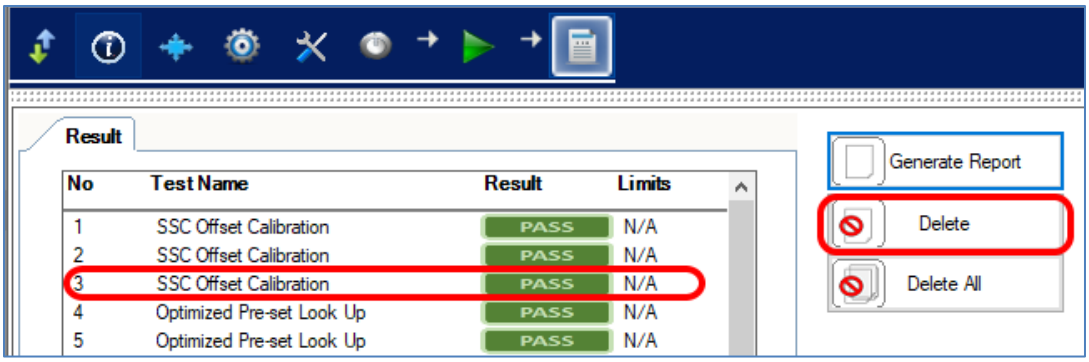


FIGURE 42. DELETE INDIVIDUAL CALIBRATION/TEST RESULTS EXAMPLE

To remove all results, select the **Delete All** button.

7 Saving and Loading Test Sessions

The GRL-DP21-SINK-AN software enables Calibration and Test Results to be created and maintained as a 'Live Session' in the application. This allows you to quit the application and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To save a session, with all of the parameter information, the test results, and any waveforms, use the "Options" command on the menu bar, then the "Save Session" command.

To load a session back into the software, including the saved parameter settings, use the "Options" command on the menu bar, then the "Load Session" command.

To create a New session and return the application back to a default configuration, use "Options" command on the menu bar, then the "New Session" command.

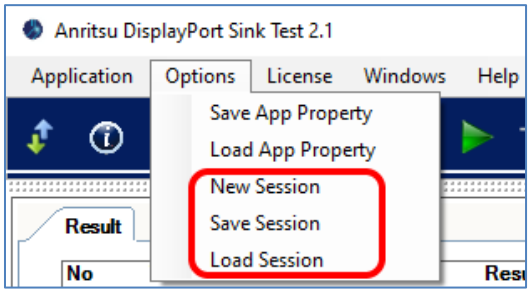


FIGURE 43. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

8 Appendix A: Manual CTS Sink Calibration and Test Procedure

The DisplayPort PHY CTS outlines the requirements for manual DisplayPort Sink Calibration and Testing in this section.

Note: See Section 2, Resource Requirements for equipment required in the following setups.

8.1 Calibrate Receiver Stressed Eye for UHBR 10 (10.0 Gbit/s) at TP1

1. Set up the physical equipment connections without the ISI channel, as per Figure 23.
2. Set up the MP1900A BERT as follows:

    a) Go to Menu Bar → File → Initialize.
    b) Go to Jitter tab and set Clock Source to “Unit1:Slot2:MU181000B”. See Figure 44.
    c) Go to PPG → Misc2.
    d) Set Clock Source to “Unit1:Slot4:MU181500B”. See Figure 45.
    e) Set Bit Rate to 10Gbit/s. See Figure 45.
    f) Set Offset (ppm) to 300ppm for 10G. See Figure 45.
    g) Set Output Clock Rate to “Fullrate”. See Figure 45.
    h) Set Test Pattern on PPG to “PRBS” and Length to “2^15-1” bits. See Figure 46.
    i) Turn on PPG Data Output.
    j) Go to PPG → Emphasis tab and turn on “Manual Setting”. See Figure 47.
    k) Turn on “SSC”, with settings of 33kHz (for 10G) with 5300ppm (for 10G) triangle down spread. (SSC will remain ON for all of the following steps.) See Figure 48.
    l) Set DATA+ amplitude to 620mV. A differential amplitude just over the 700mV EH should show as an initial value. (See the lower left in Figure 49.)
    m) Set initial CM frequency to 400MHz. See Figure 50.
    n) Turn the CM output to “Off” until the CM Calibration Step.

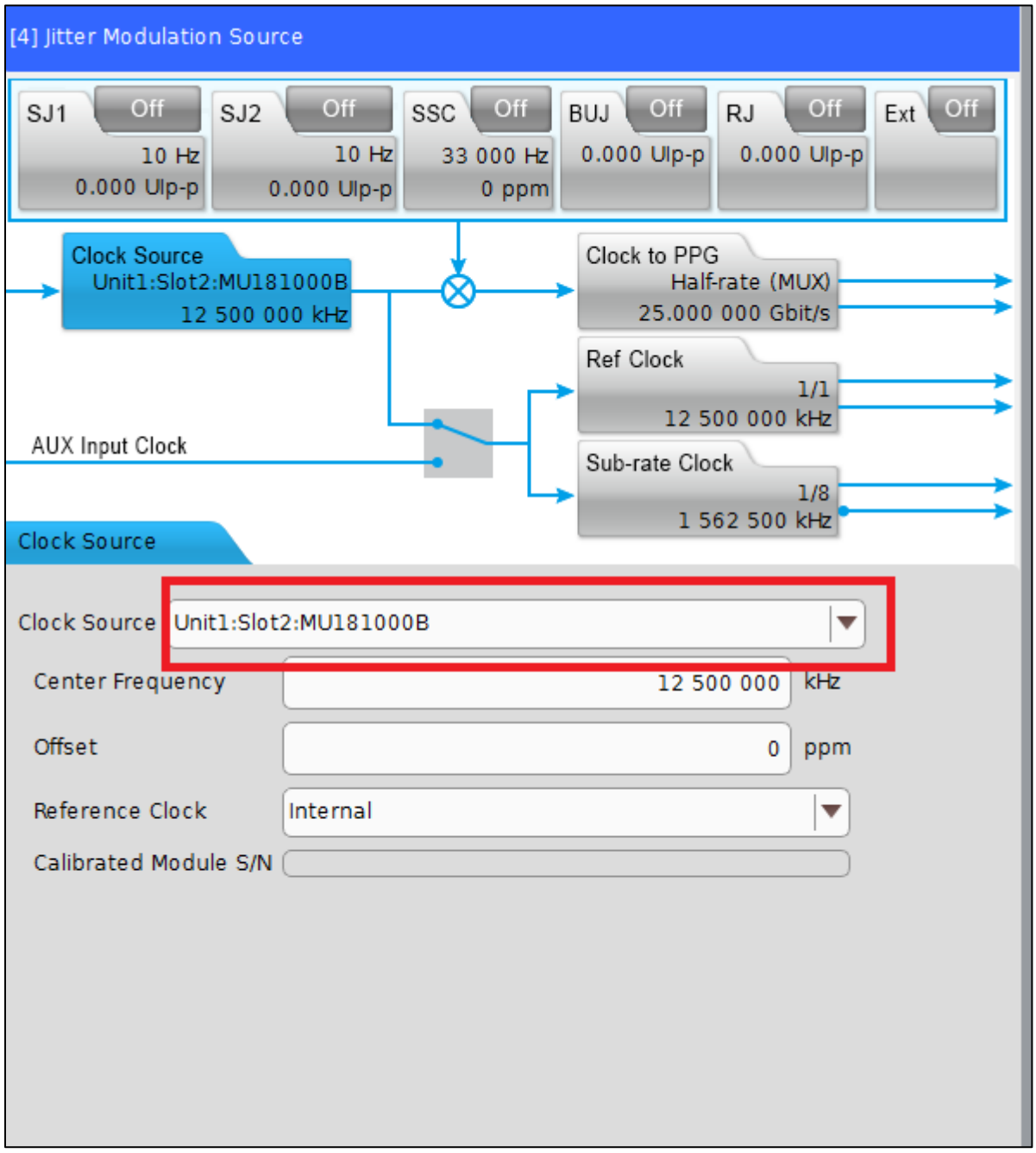


FIGURE 44. JITTER CLOCK SOURCE SETTING

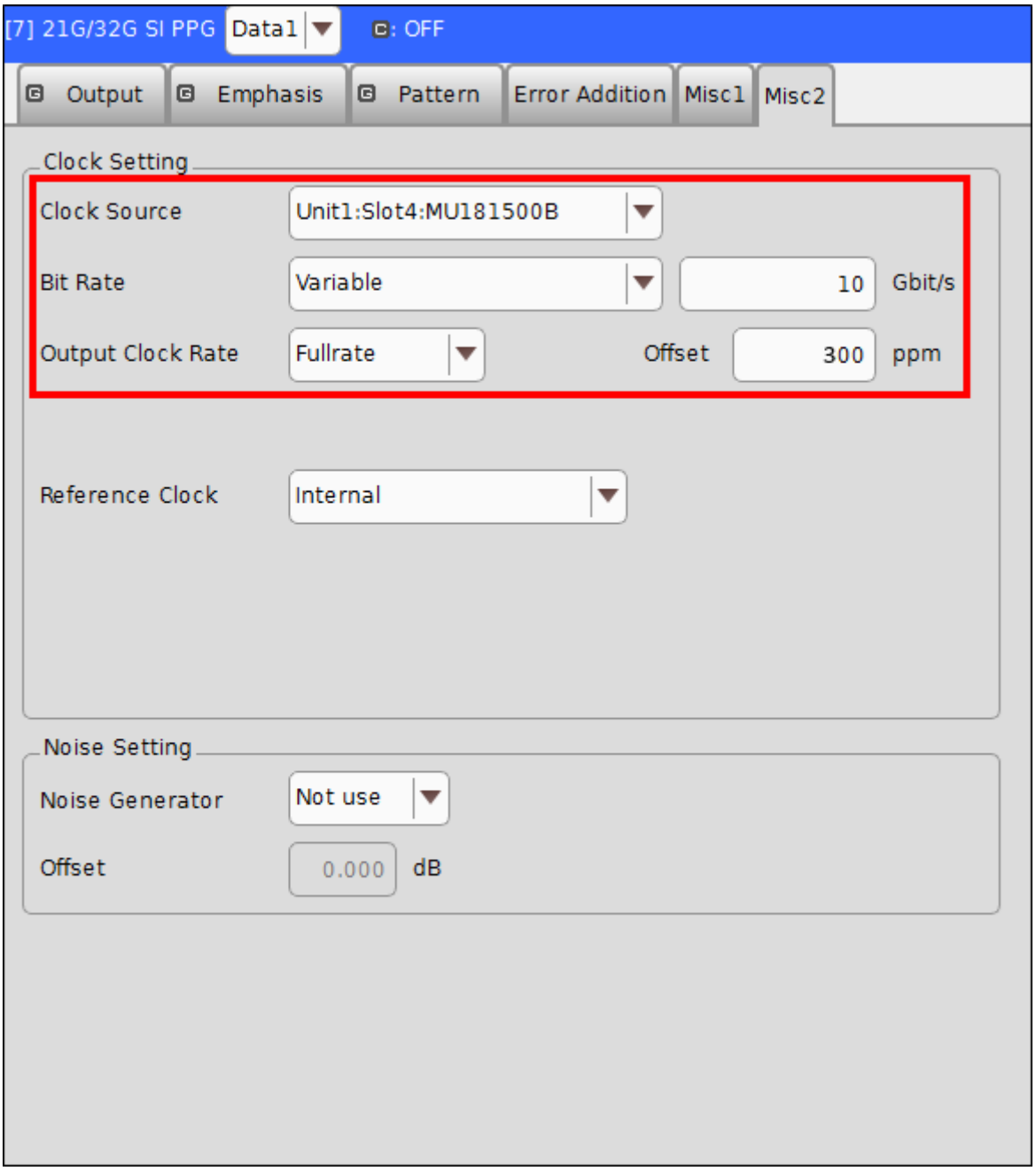


FIGURE 45. PPG MISC2 SETTINGS

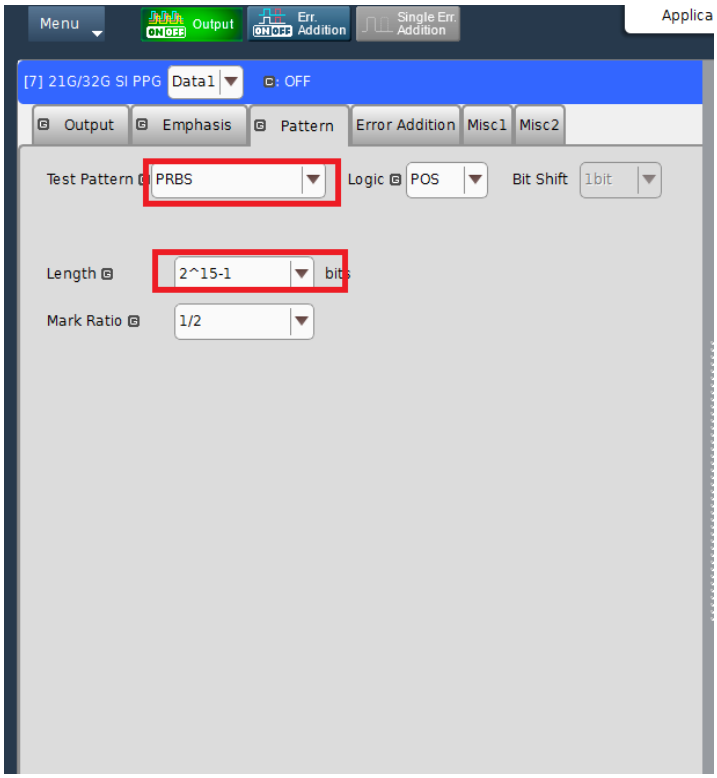


FIGURE 46. PATTERN SETTING

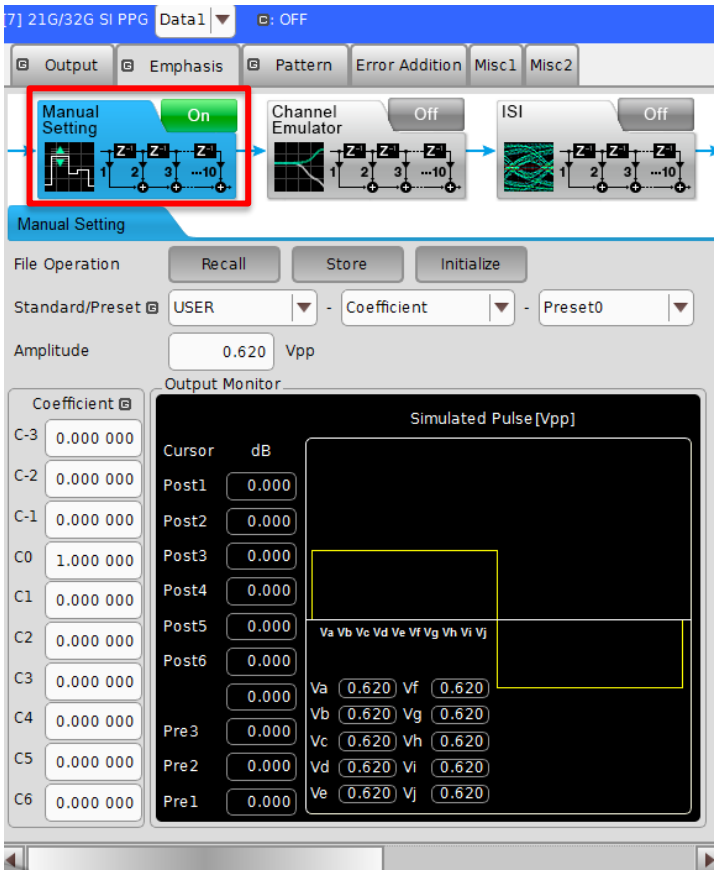


FIGURE 47. PPG EMPHASIS SETTING

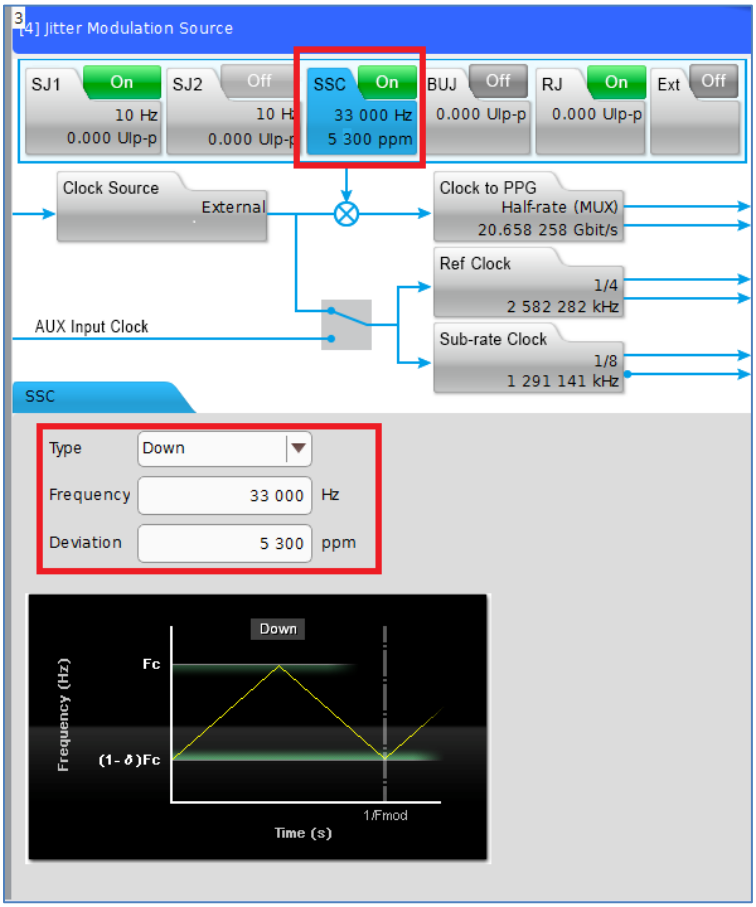


FIGURE 48. SSC SETUP

FIGURE 49. DATA+ AMPLITUDE SETTING

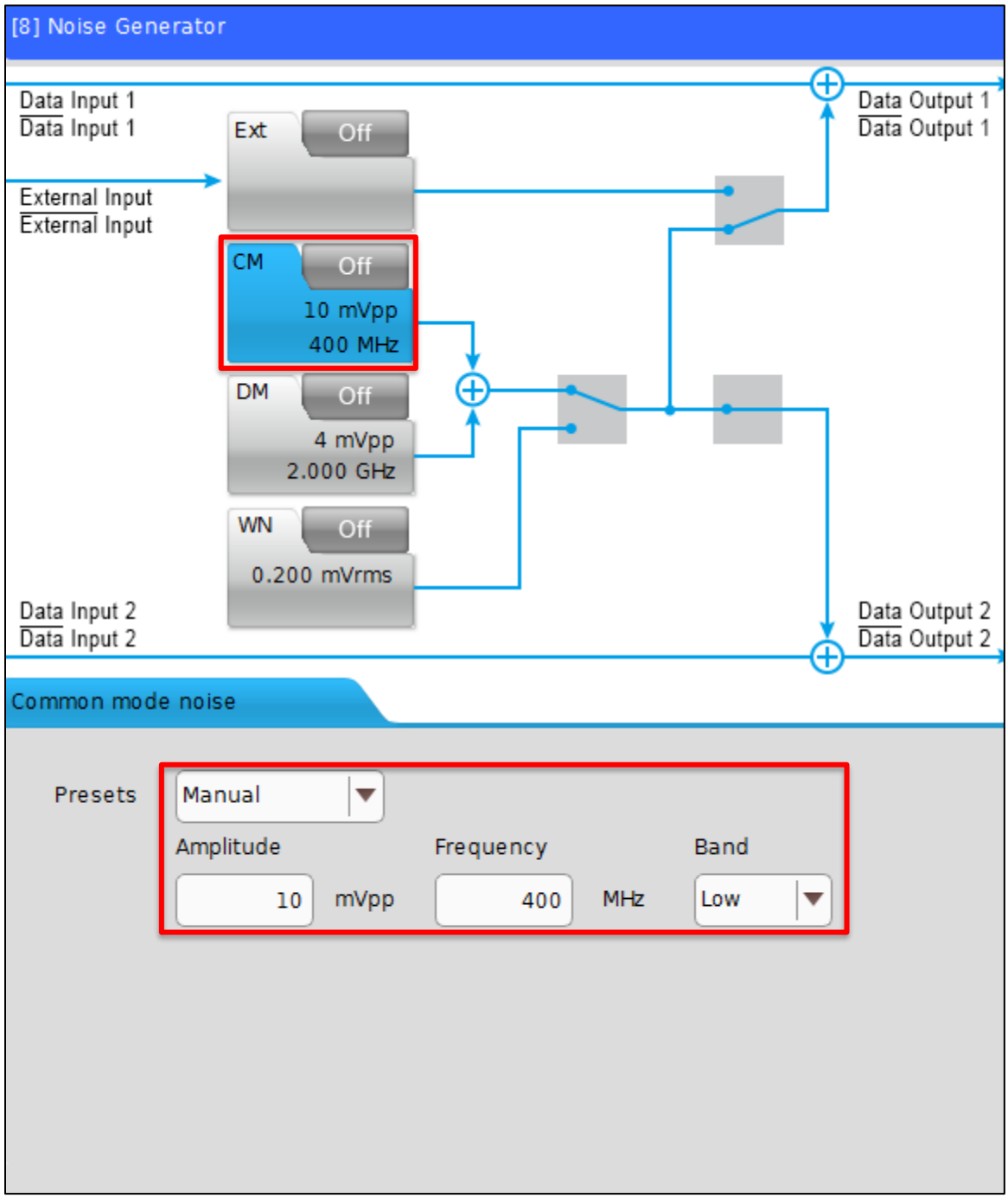


FIGURE 50. CM SETTING

8.1.1 Set Up Oscilloscope

8.1.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 5.

TABLE 5. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Record Length	40M in a single acquisition
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	16GHz
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF

FIGURE 51. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

8.1.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 6.

TABLE 6. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	10Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000MHz Damping factor: 0.94

FIGURE 52. OSCILLOSCOPE CLOCK RECOVERY SETUP

8.1.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 7.

TABLE 7. OSCILLOSCOPE ACCM SETUP

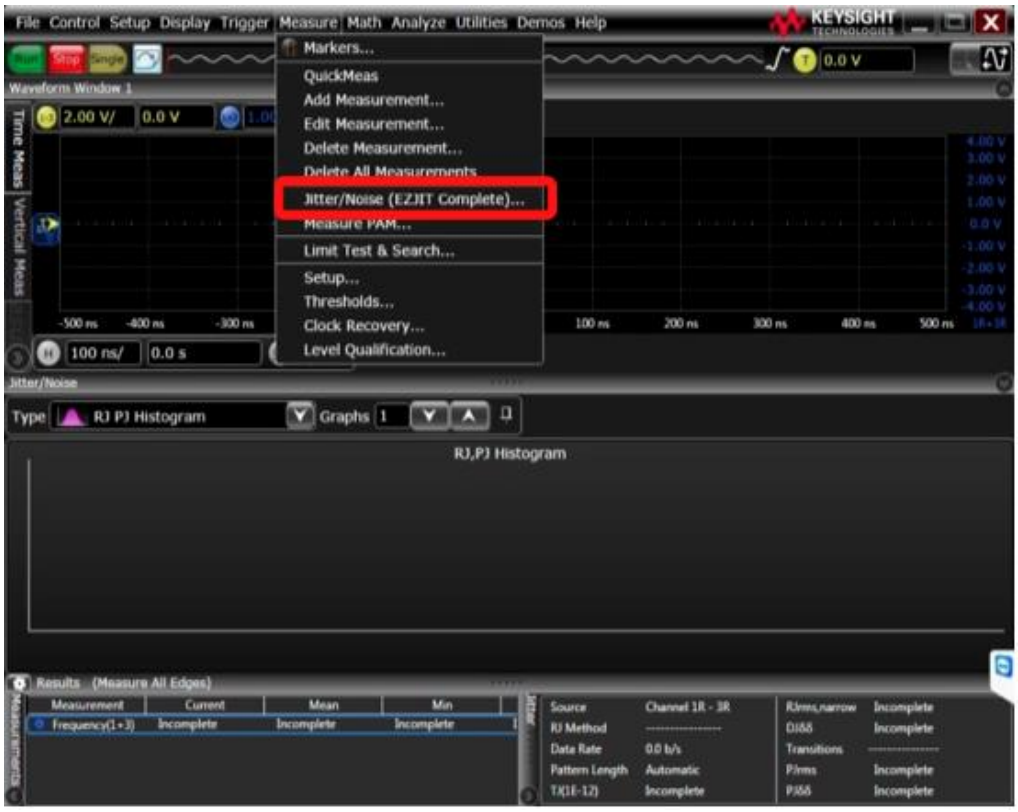
Setting	Setup
Sample Rate	≥ 80Gs/s
Record Length	40Mpts per channel
Bandwidth	16GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.1.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 8.

TABLE 8. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-9
Pattern	Periodic, Repeating Pattern (2^{15}-1 = 32,767 bits)



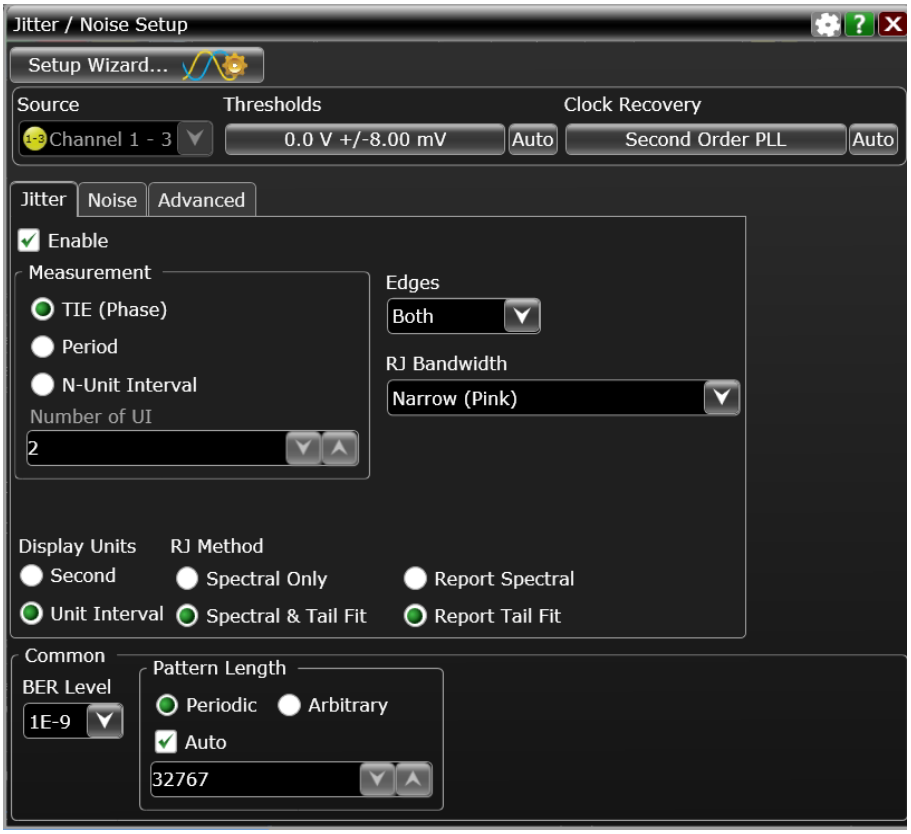


FIGURE 53. OSCILLOSCOPE JITTER SETUP

8.1.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 9.

TABLE 9. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	92 mV (for final Eye Height Calibration)
Eye Mask Width	513 mUI

8.1.2 Record ISI Measurements

1. Step through Pre-set coefficients 0 to 14 and use a Preset which gives minimum DDJ Measurement. Although these are not calibrated values, record ISI measurement as part of the measurement table.

√Table 3-53: Preset FFE Coefficients [a] [b]

Preset #	Pre-shoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C-1	Co	C+~
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	~~3.8~~ 3.6	~~-3.8~~ 0	~~-0.13~~ -0.17	~~0.74~~ 0.83	~~-0.13~~ 0
15	1.7	-1.7	-0.05	0.55	-0.05

FIGURE 54. ISI MEASUREMENT PRESET TABLE

2. In 4Tap Emphasis Ch1 Menu, create 15 Presets with coefficients which match the Table in the DisplayPort 2.1 Specification. See Figure 55 below.

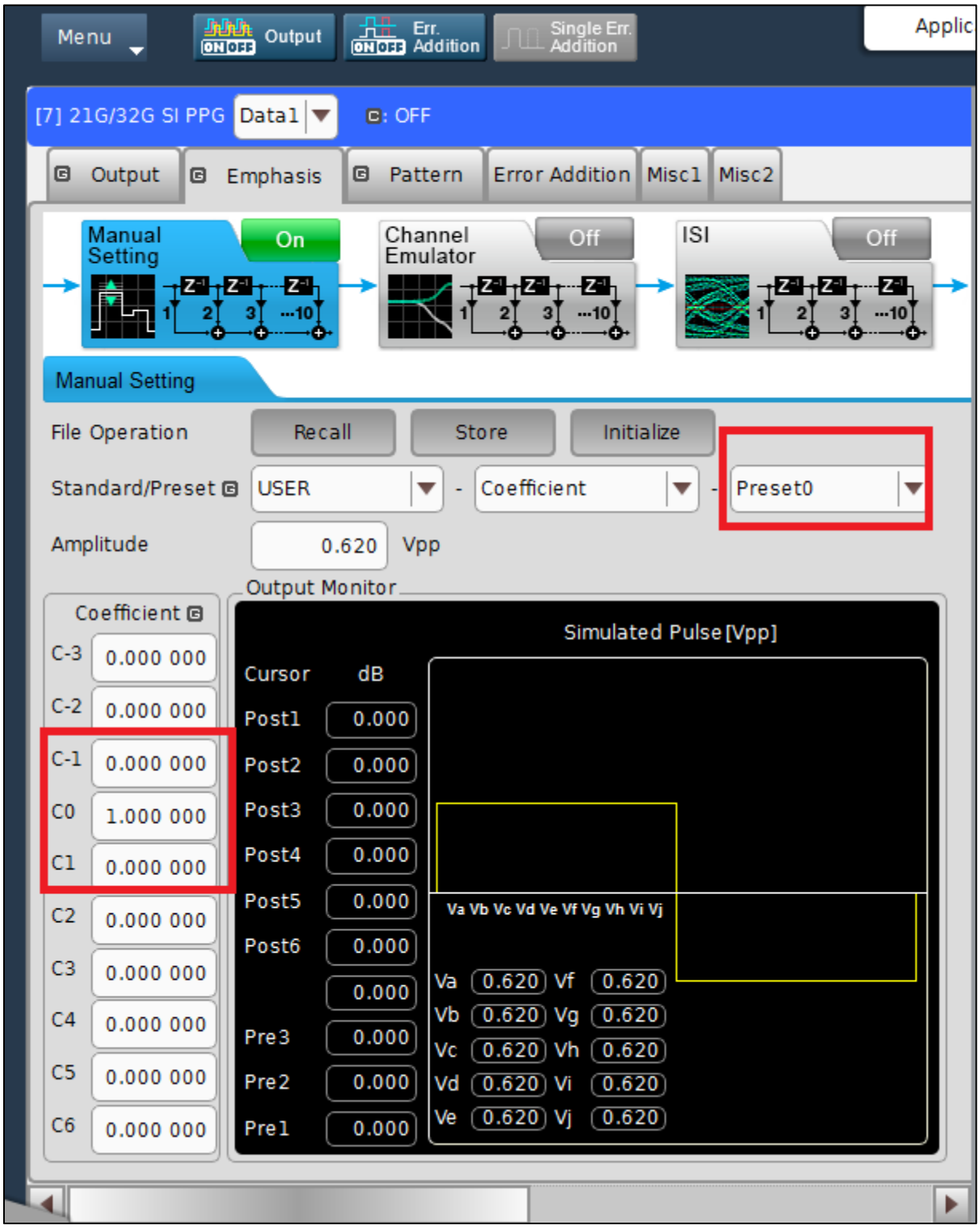


FIGURE 55. 4TAP EMPHASIS CH1 INTERFACE

3. Step through all 15 Presets. The Preset with the minimum DDJpp measurement is the optimized preset.

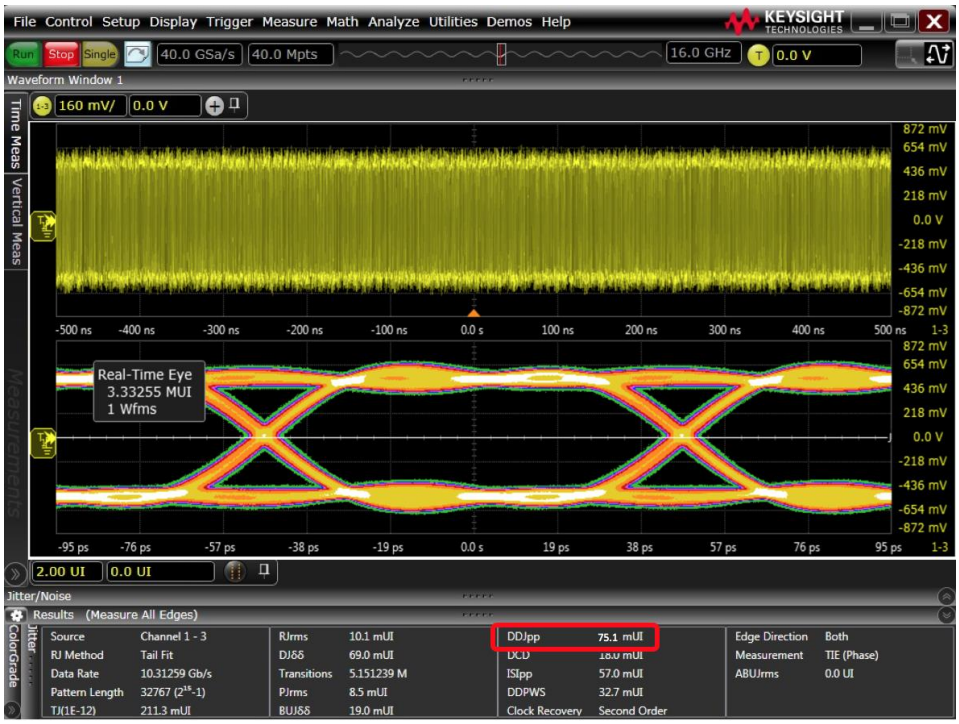


FIGURE 56. OPTIMIZED PRESET (MINIMUM DDJPP) MEASUREMENT ON KEYSIGHT SCOPE

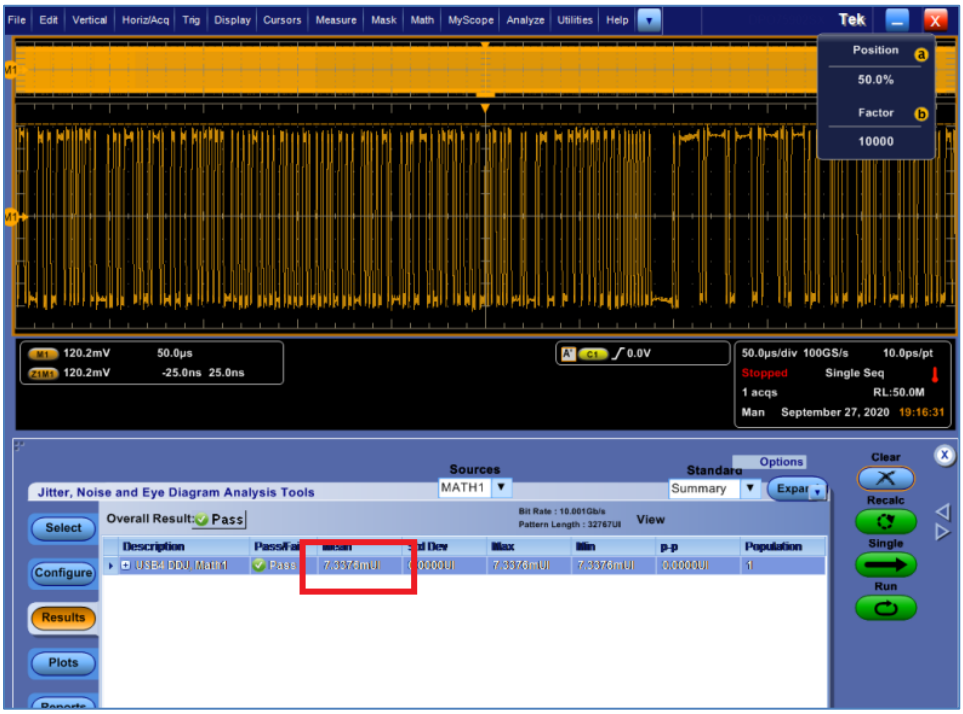


FIGURE 57. OPTIMIZED PRESET (MINIMUM DDJPP) MEASUREMENT ON TEKTRONIX SCOPE

4. Set up the Scope so that Channel 1 and Channel 3 scale to 80% of screen.
5. Turn on Function1 of Scope to perform subtraction of Channel 1 and Channel 3.
6. Measure VPP on Function1.

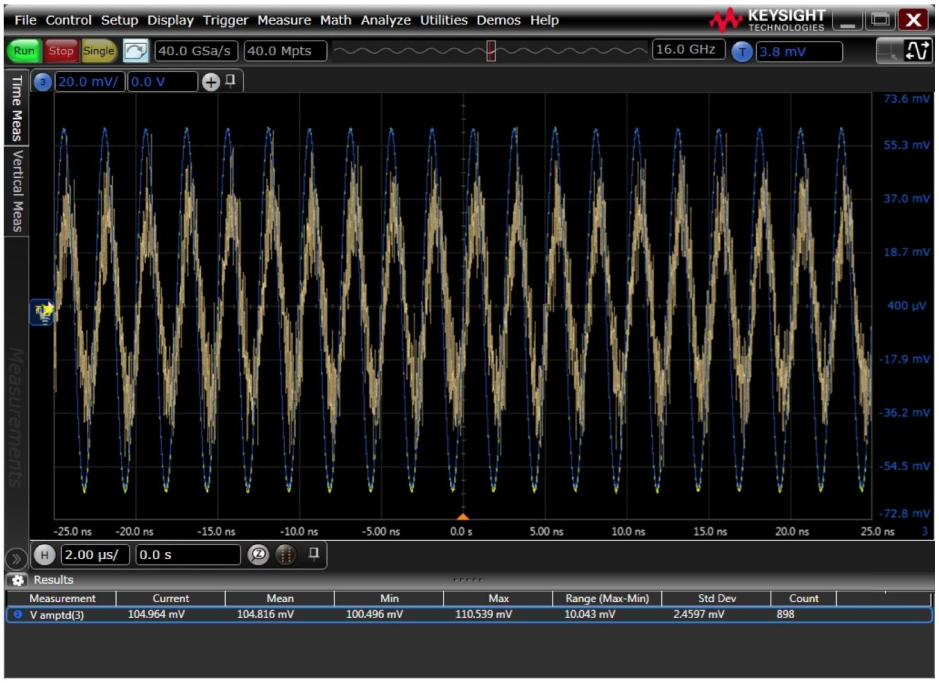


FIGURE 58. CALIBRATION TO PHASE MATCH ON KEYSIGHT SCOPE

FIGURE 59. CALIBRATION TO PHASE MATCH ON TEKTRONIX SCOPE

7. Calibrate ACCM to be 100mVpp at 400MHz Clock, using ACCM Scope Setup. Then return CM Amplitude to zero.

   a) Turn On SSC and turn Off all jitter components on the MP1900A Generator. Change the test pattern to PRBS31 and transmit the PRBS31 pattern from the MP1900A.

   b) Set the frequency to 400MHz on the MP1900A CM Generator.

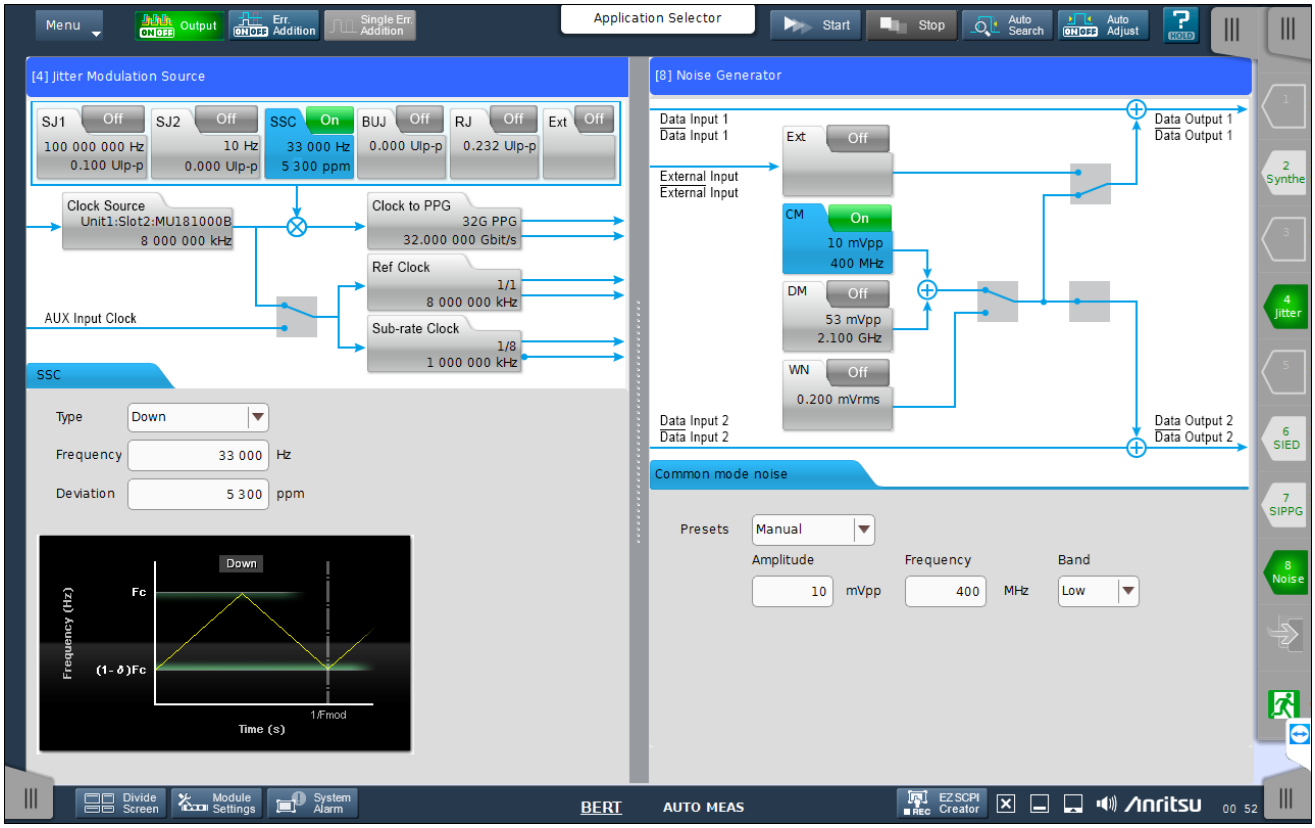


FIGURE 60. CALIBRATE ACCM

   c) Measure Ch1 and Ch3 Signals on the scope to have an amplitude of a Mean Peak-to-Peak measurement of 100mVpp.

   $V_{AC\text{-}CM} = (V_{TX\text{-}P} + V_{TX\text{-}N})/2$

   d) Turn Off the CM output.

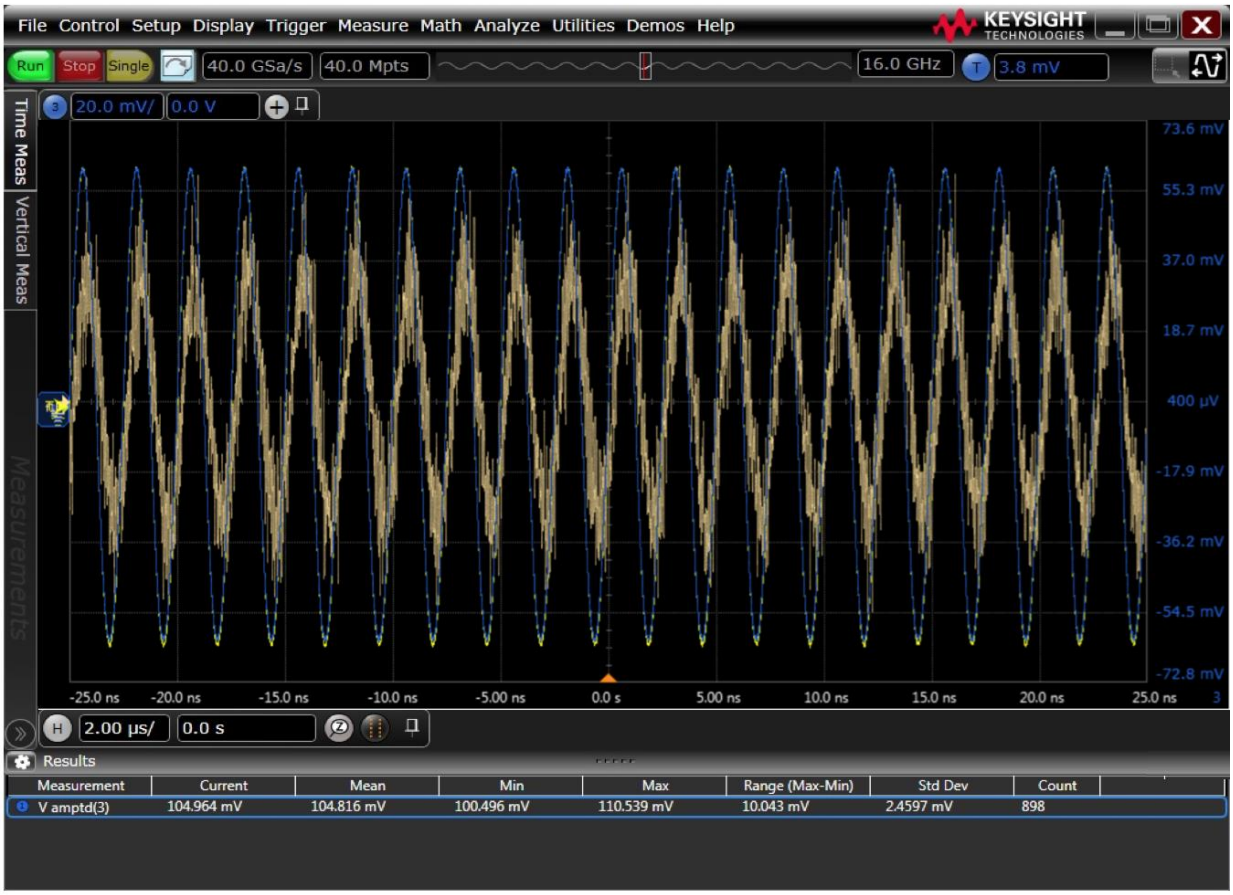


FIGURE 61. CALIBRATE ACCM PEAK-TO-PEAK AMPLITUDE

8. Turn on all remaining Jitter terms (RJ-Filtered (User); HPF (10MHz); SJ@100MHz); and set all jitter amplitudes to zero.

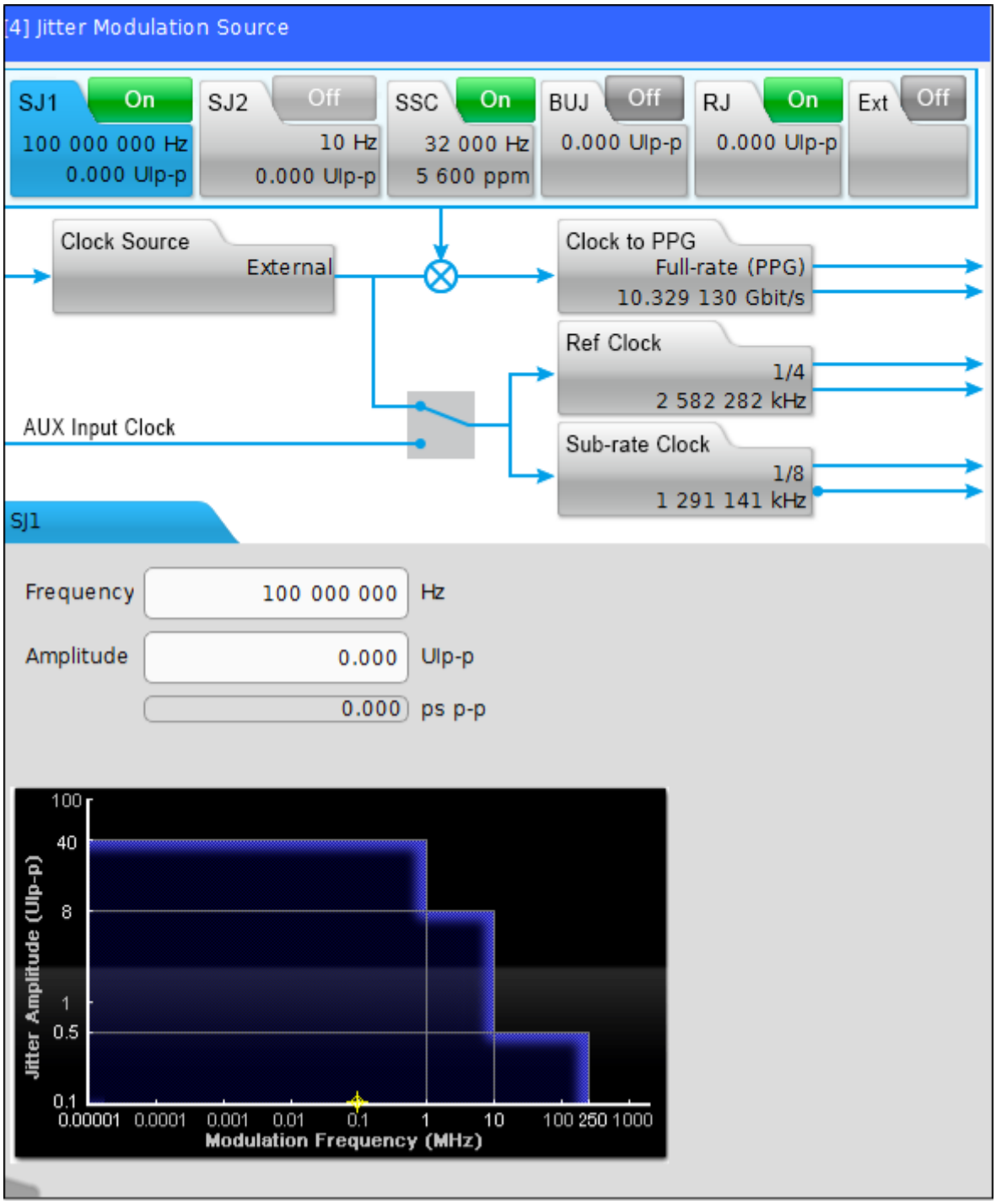


FIGURE 62. JITTER AMPLITUDES

9. Return the Scope setup to the jitter setup.
10. Set the PRBS15 pattern on the MP1900A.
11. Calibrate RJ amplitude to 115mUI peak-to-peak or 9.58mUI RMS.
12. Return amplitude to zero.

13. Capture a screen shot.

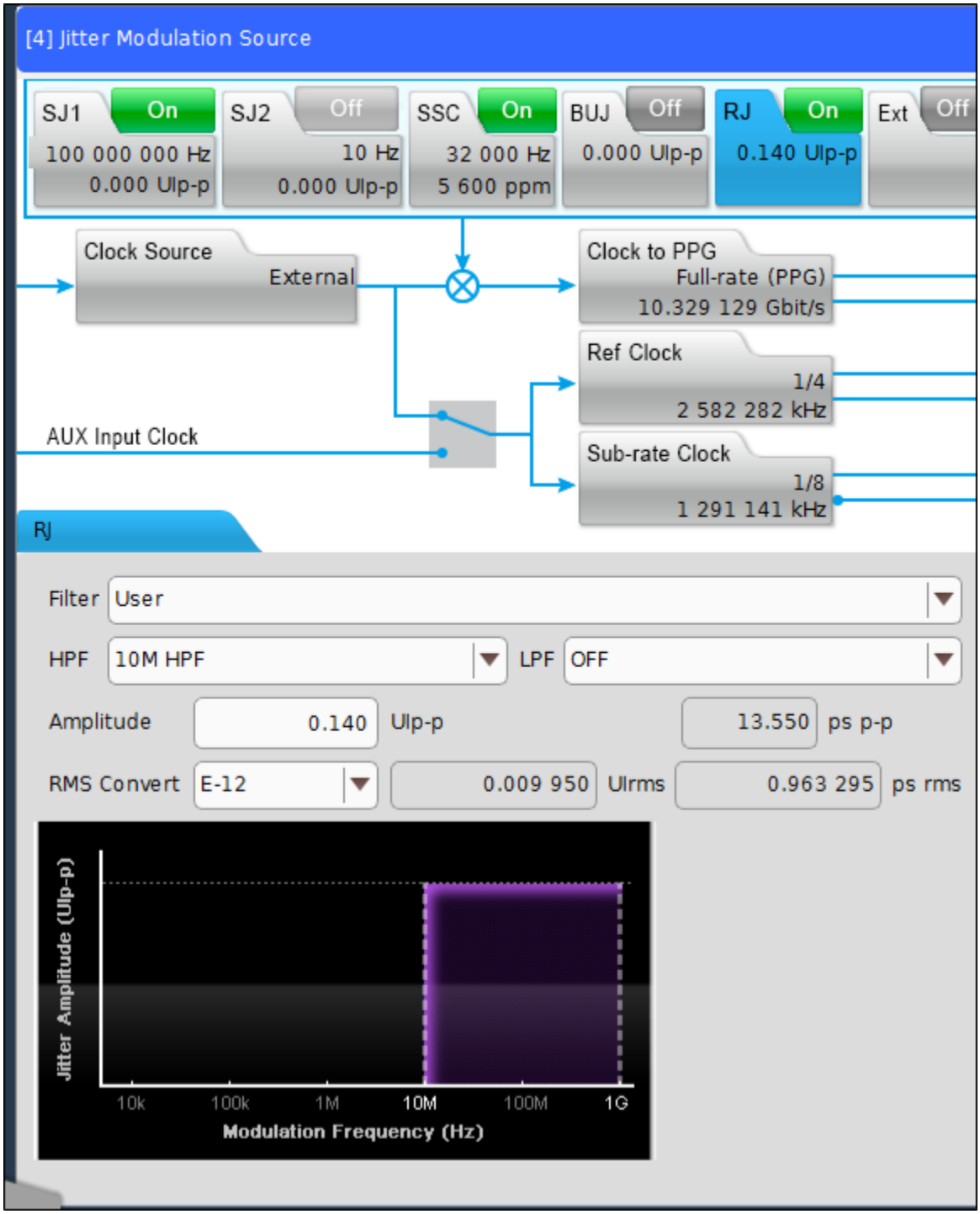


FIGURE 63. CALIBRATE RJ AMPLITUDE #1

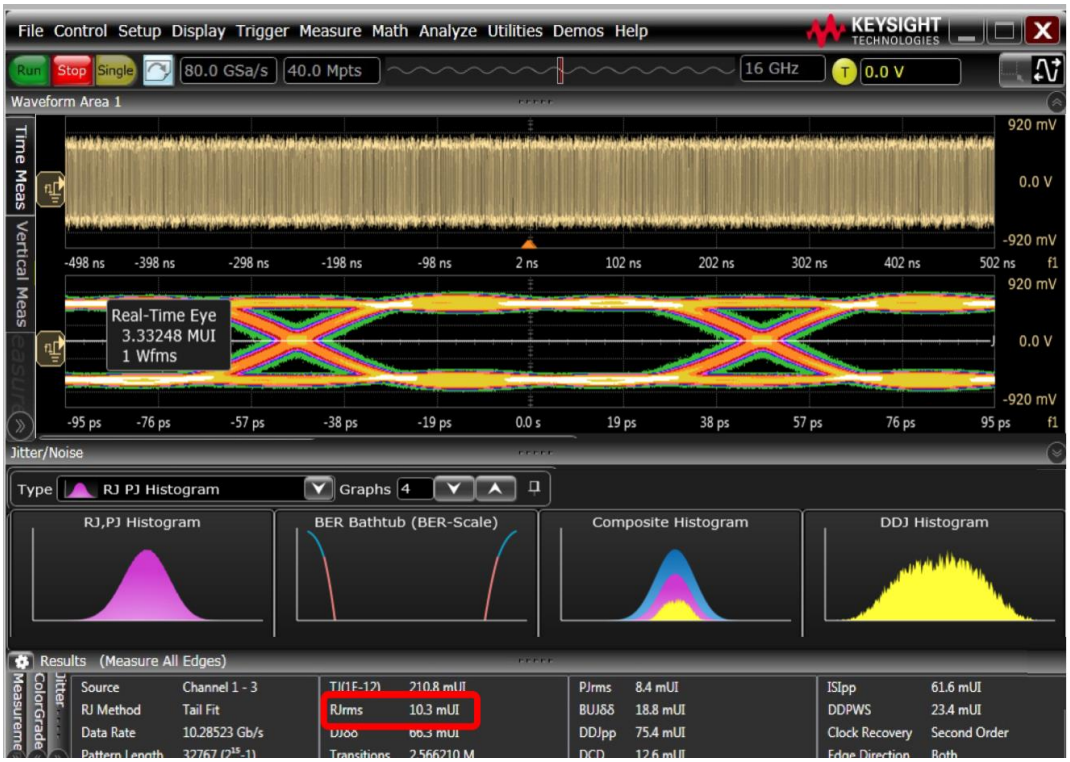


FIGURE 64. CALIBRATE RJ AMPLITUDE #2 ON KEYSIGHT SCOPE

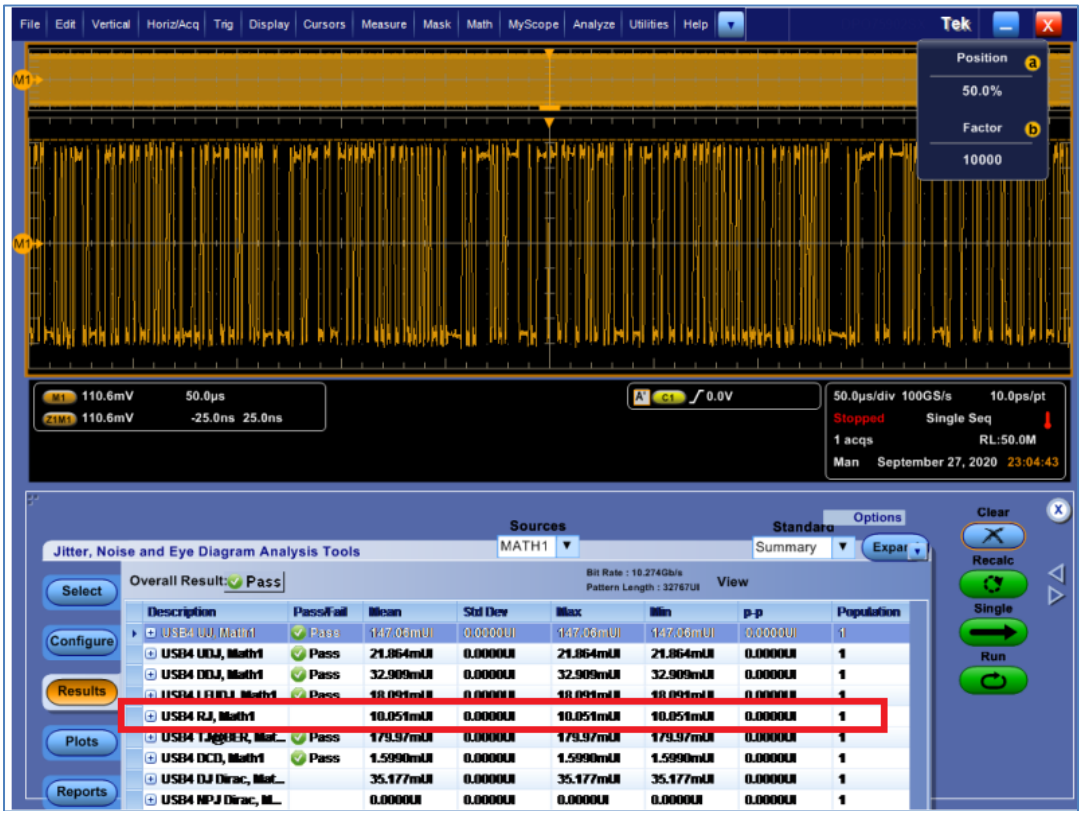


FIGURE 65. CALIBRATE RJ AMPLITUDE #2 ON TEKTRONIX SCOPE

14. Calibrate SJ amplitude to 170mUI peak-to-peak at 100MHz, where “peak-to-peak” is 170mUI.

15. Capture screen shot.

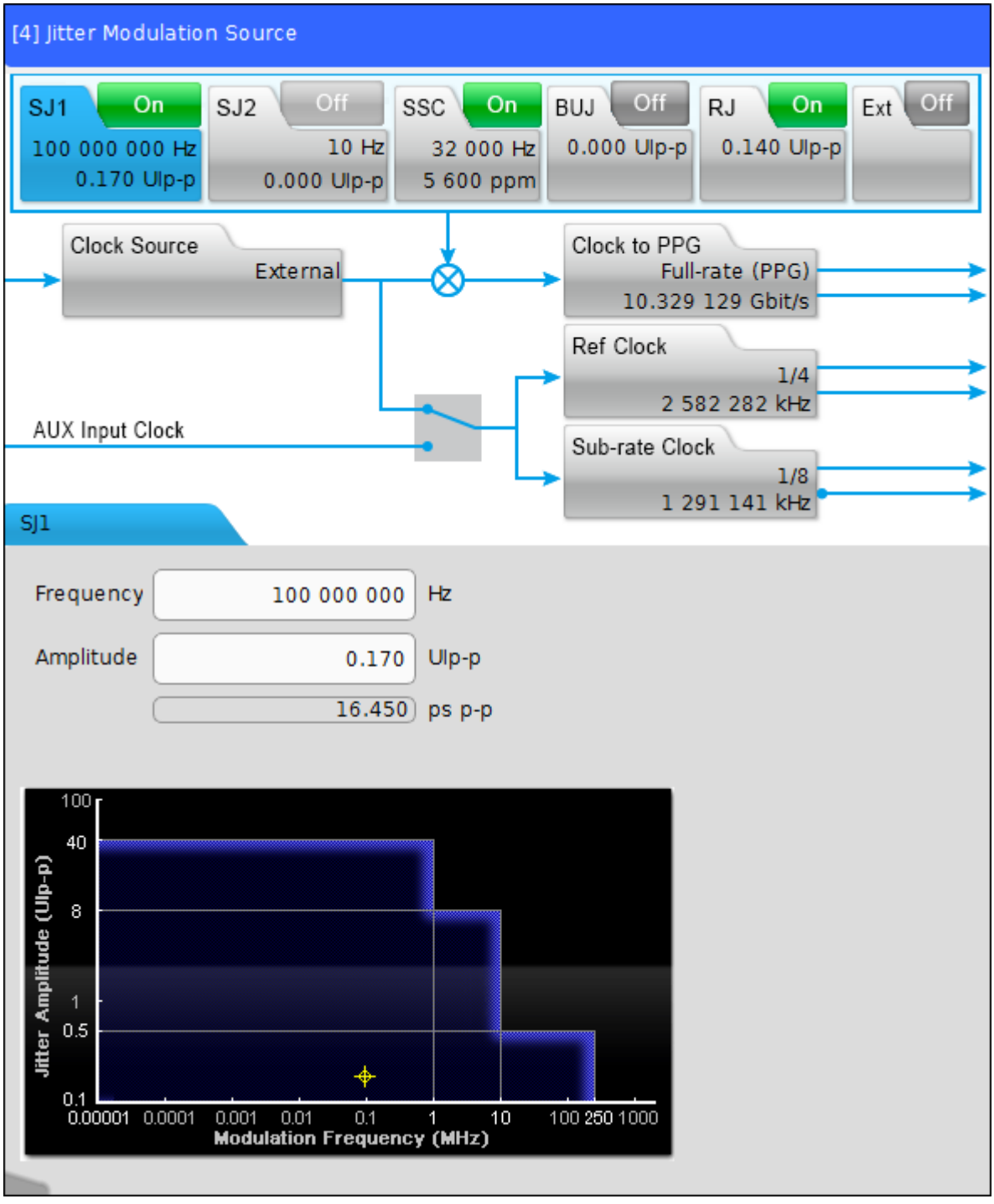


FIGURE 66. CALIBRATE SJ AMPLITUDE #1

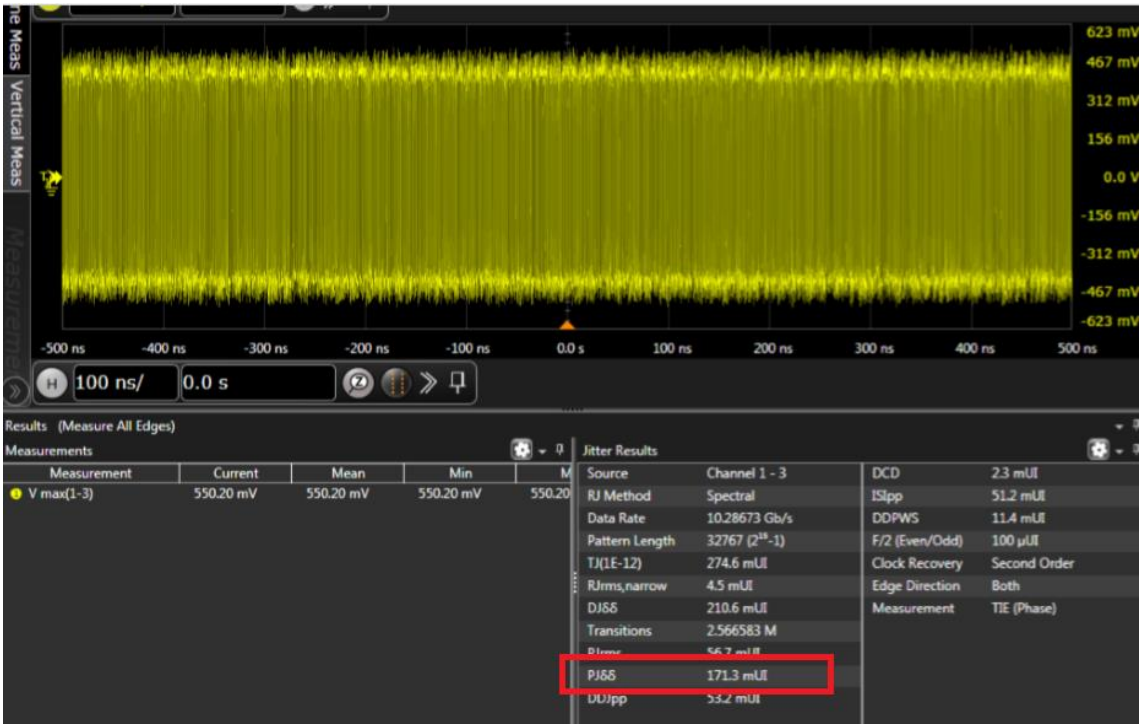


FIGURE 67. CALIBRATE SJ AMPLITUDE #2 ON KEYSIGHT SCOPE

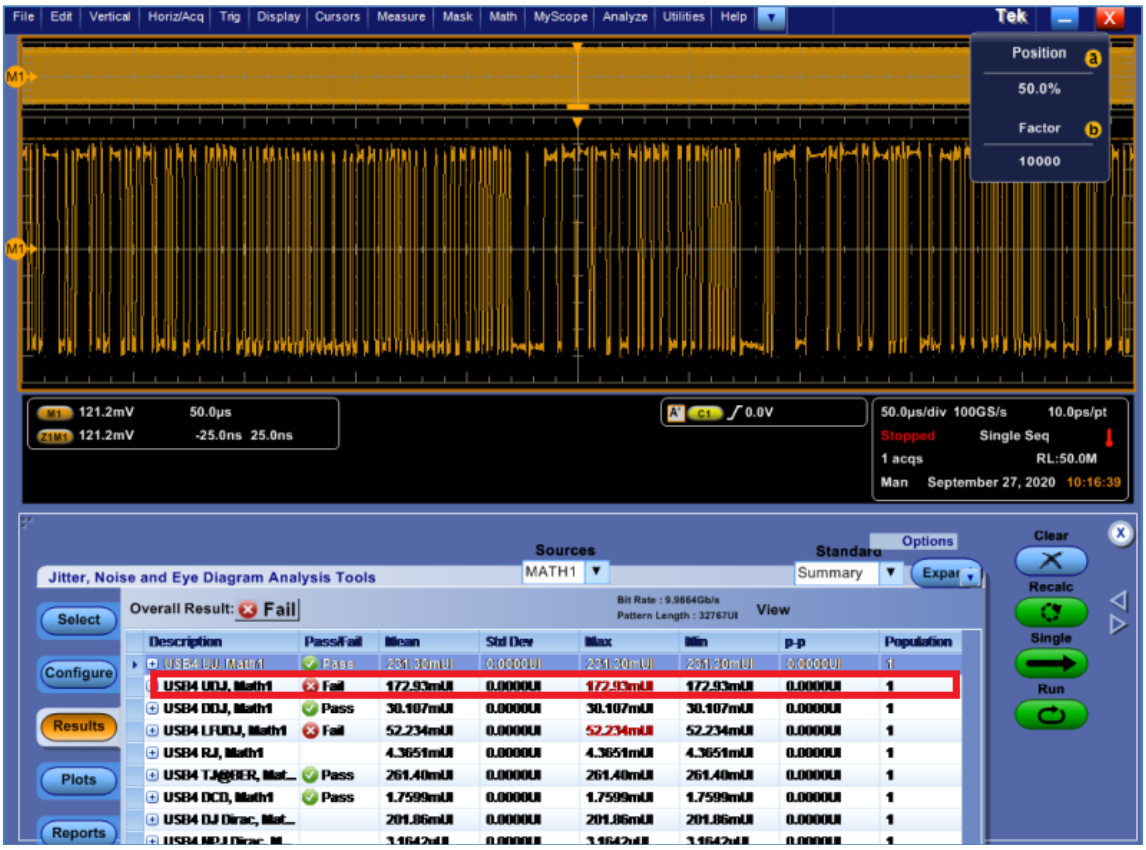


FIGURE 68. CALIBRATE SJ AMPLITUDE #2 ON TEKTRONIX SCOPE

16. Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.
17. Calibrate the TJ measurement to 330mUI ± 12.5mUI, using the SJ Amplitude control (for SJ frequency of 100MHz) and RJ Amplitude control (for SJ frequencies of less than 100MHz) as an adjustment on the BERT.
18. Capture screen shot.

FIGURE 69. TJ MEASUREMENT ON KEYSIGHT SCOPE

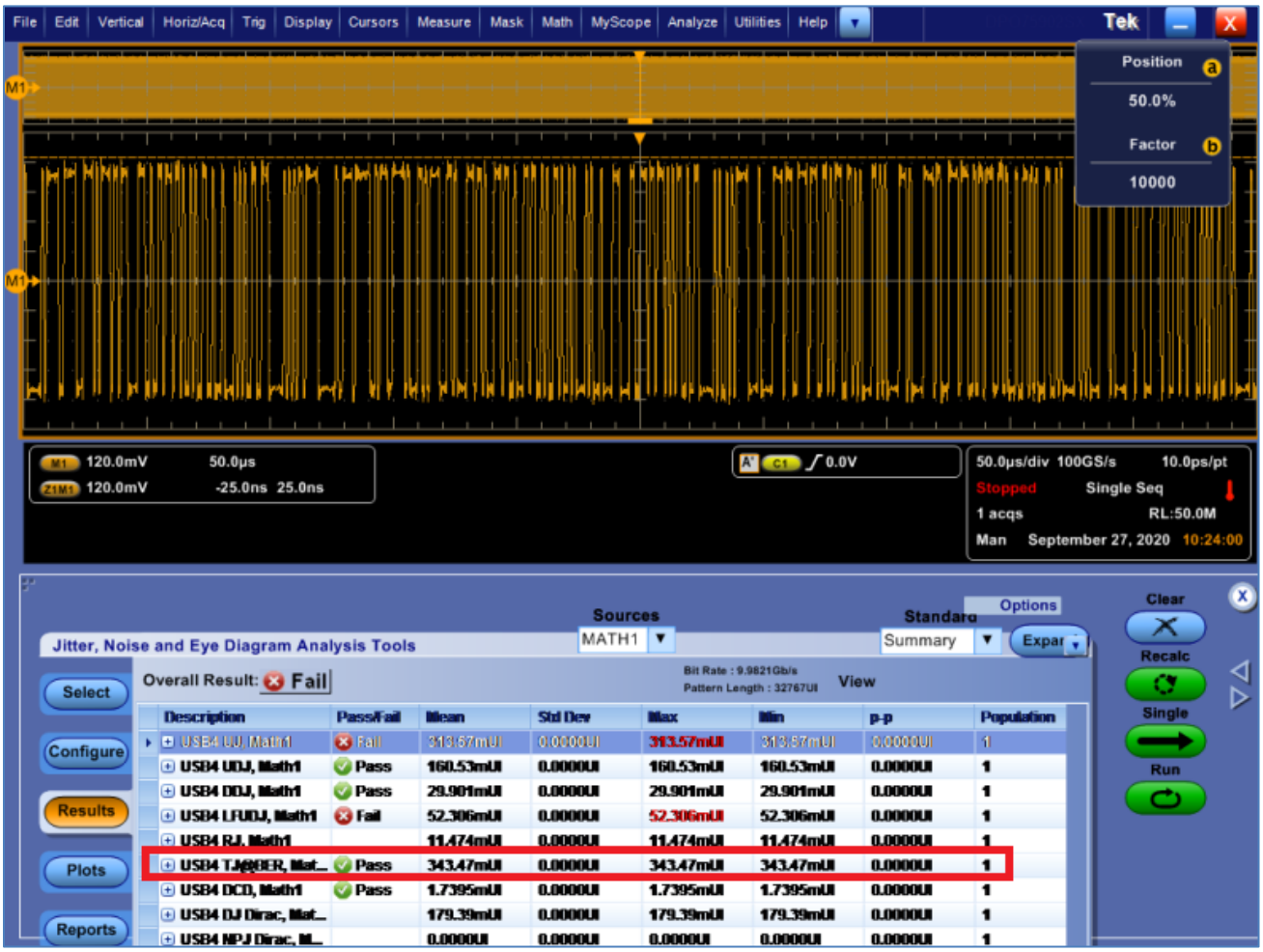


FIGURE 70. TJ MEASUREMENT ON TEKTRONIX SCOPE

19. Adjust the memory depth to capture 1,000,000 (1E6) bits.
20. Change the Pattern on the MP1900A BERT to PRBS31.
21. Calibrate Inner Eye Height to 700mV (top and bottom of the triangle eye mask are V:700mV, H:650mUI).
22. Capture screen shot.

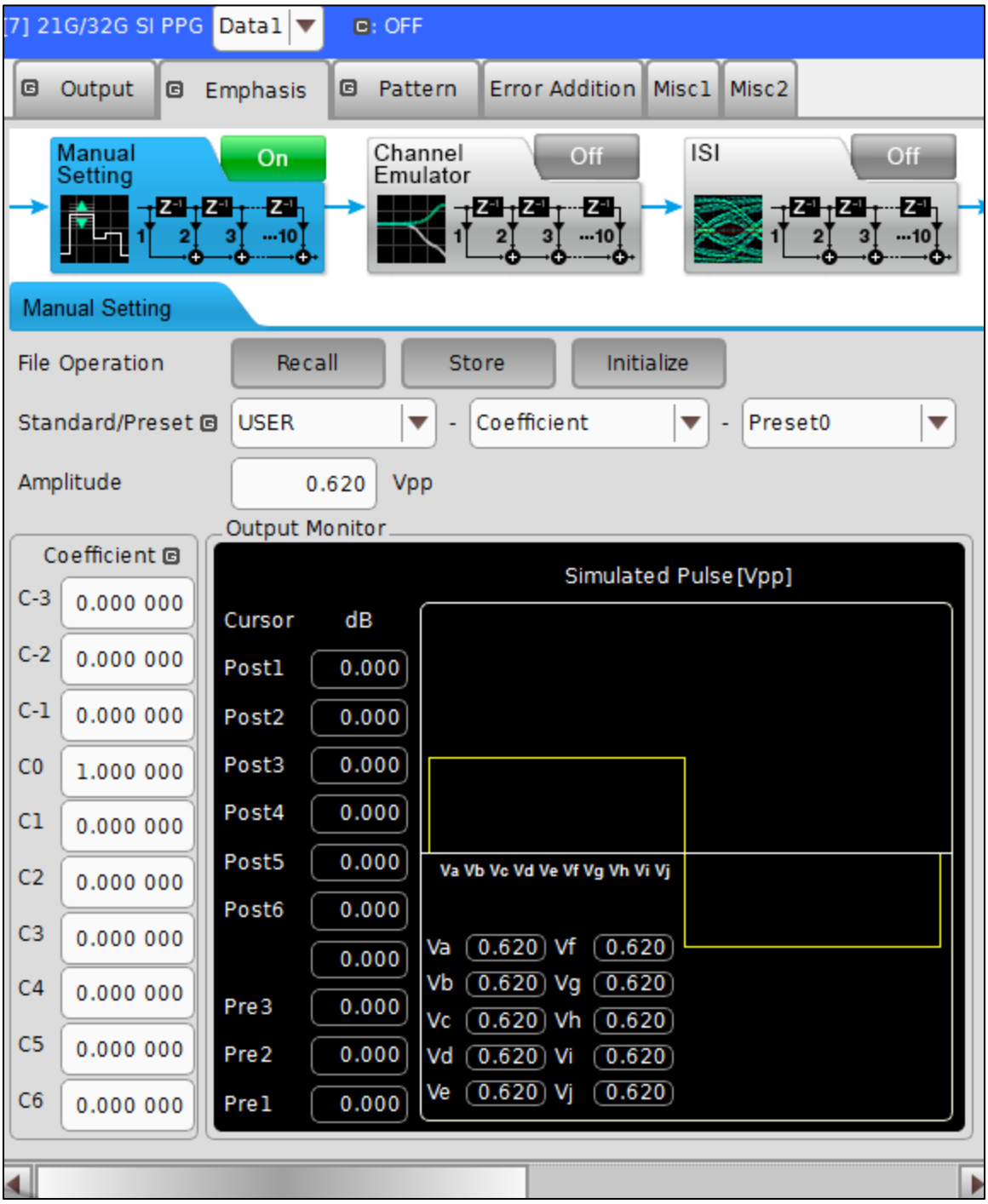


FIGURE 71. EYE AMPLITUDE

FIGURE 72. EYE MASK ON KEYSIGHT SCOPE

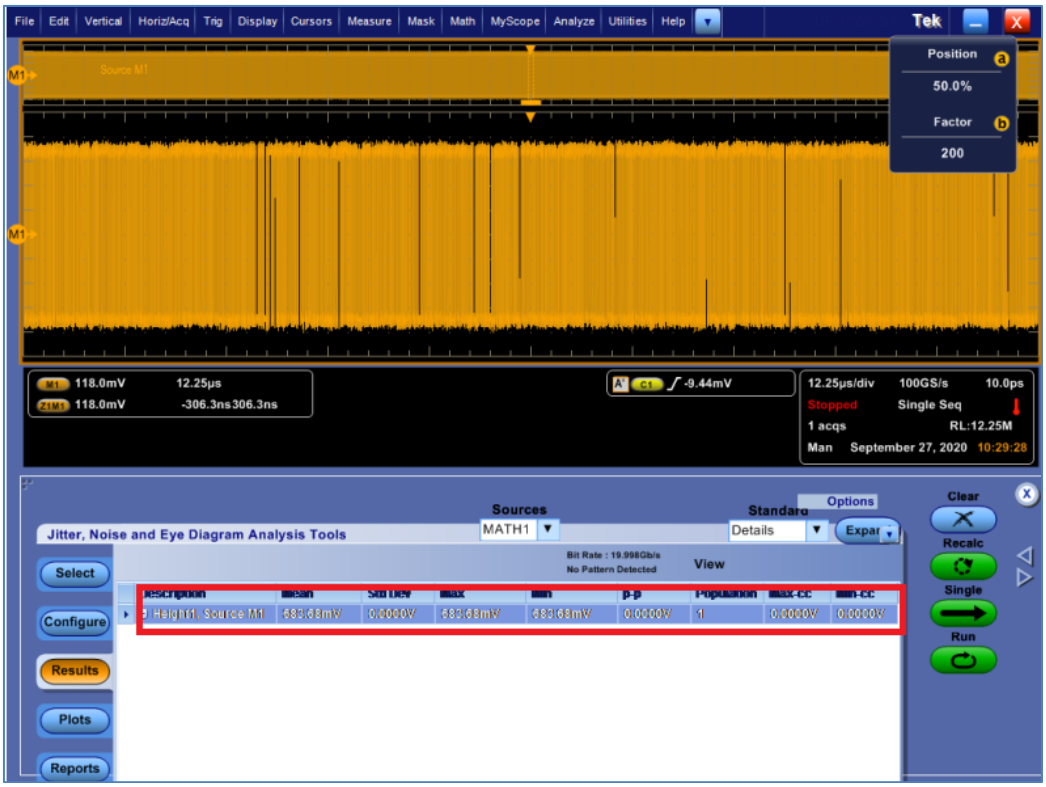


FIGURE 73. EYE MASK ON TEKTRONIX SCOPE

23. Save the BERT setup to “10G_TC1_100MHz”.
24. Return CM, RJ and PJ sources to zero amplitude.
25. Repeat step 8-21 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving the setups after each frequency as “10G_TC1_1MHz”, “10G_TC1_2MHz”, “10G_TC1_10MHz” and “10G_TC1_50MHz” respectively.

8.2 Calibrate and Save for UHBR 10 (10.0 Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -18.5dB @ 5GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 10G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 24.
3. Search for the optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.

   a) Set up the Scope as follows for CTLE:

      i) Number of Poles set to “2 Poles, AC Gain”
      ii) DC Gain set to 1.00
      iii) AC Gain set to 1.41
      iv) Pole #1 Frequency set to 1.50 GHz
      v) Pole #2 Frequency set to 5.00 GHz

   b) Use the DC Gain Setting in Table 10 which yields the largest Eye Height.

TABLE 10. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

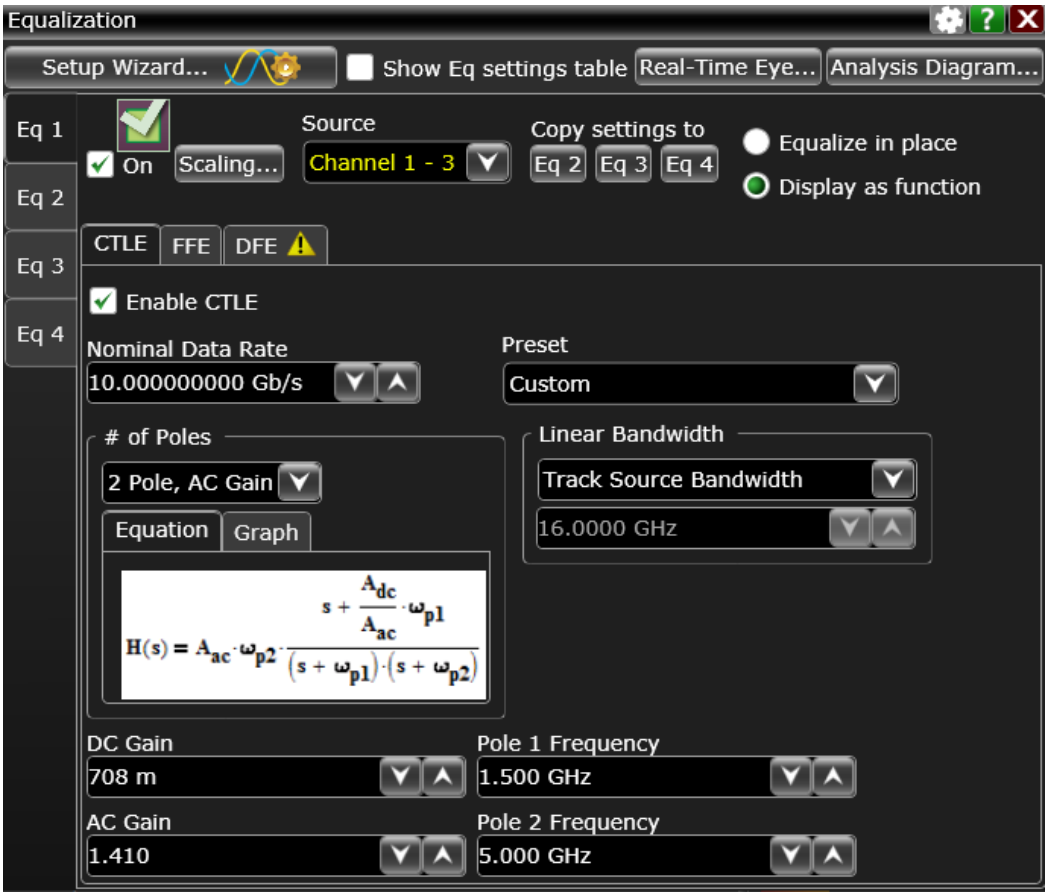


FIGURE 74. DC GAIN SETTING

c) Set up the DFE:

i) Set Max Tap to 50mV.
ii) Run Auto DFE.

FIGURE 75. DFE SETTING

d) Change the BERT Data pattern to PRBS31.
e) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UIs per Acquisition).
f) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via *Eye Width * Eye Height*.
g) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest eye area is used for the following measurements.

11. By adjusting data amplitude, calibrate the Inner Eye Height to 92 ± 10mV diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

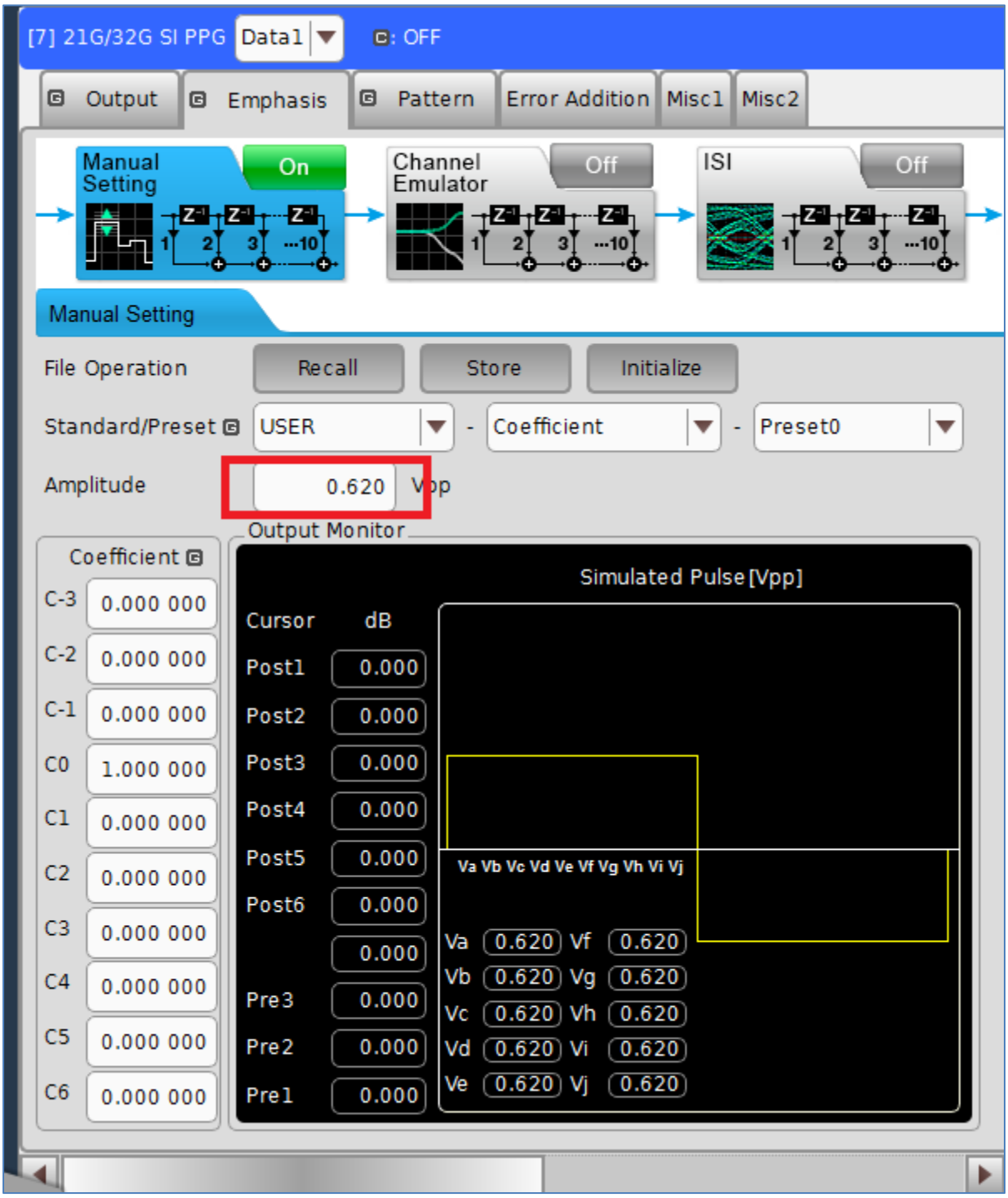
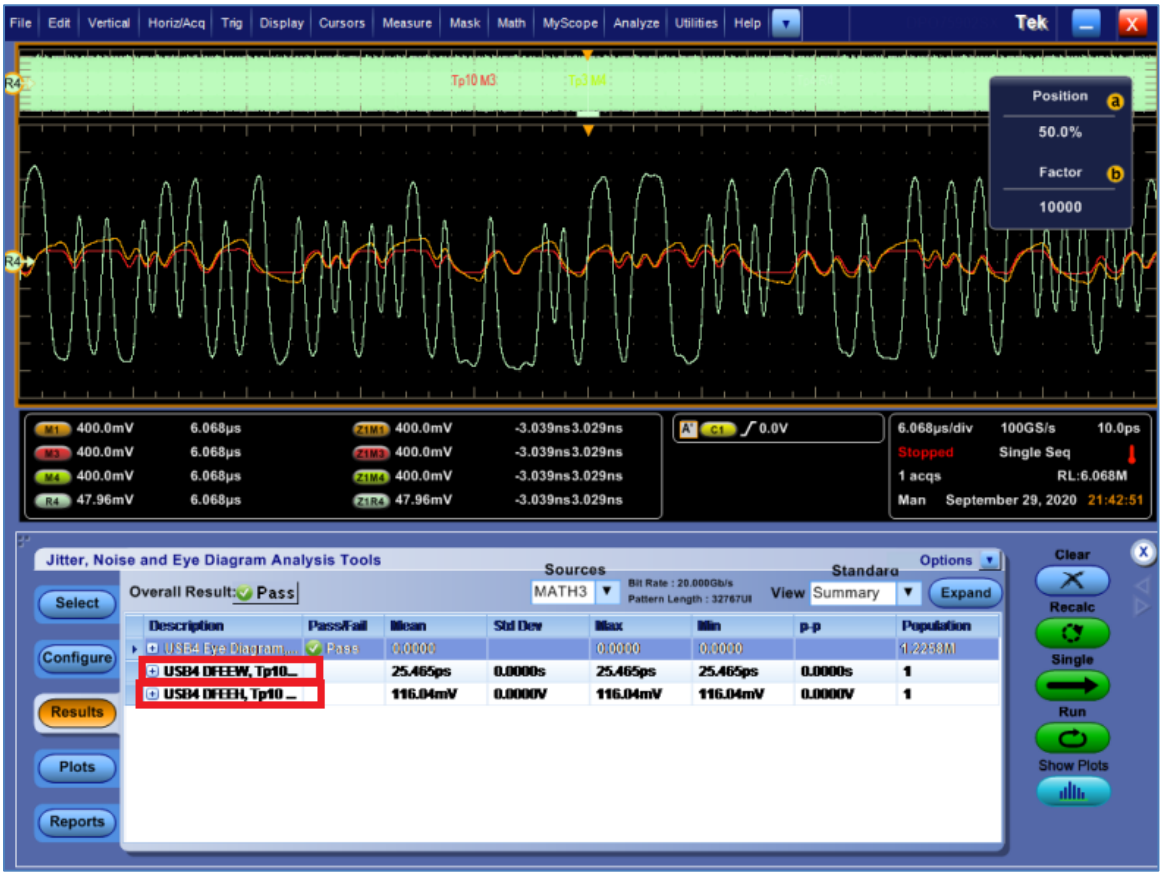


FIGURE 76. EYE AMPLITUDE


File Control Setup Display Trigger Measure/Mark Math Analyze Utilities Demos Help
KEYSIGHT TECHNOLOGIES
Run Stop Single
80.0 GSa/s
9.85 Mpts
16.0 GHz
0.0 V
52.0 mV/
0.0 V
Real-Time Eye
1.21799 MUI
1 Wfms
208 mV
156 mV
104 mV
52.0 mV
0.0 V
-52.0 mV
-104 mV
-156 mV
-208 mV
-100 ps
-80.2 ps
-60.2 ps
-40.1 ps
-20.1 ps
0.0 s
20.1 ps
40.1 ps
60.2 ps
80.2 ps
100 ps
2.00 UI
0.0 UI
Results (Measure All Edges)
Measurements
Measurement
Current
Mean
V max(eq1)
114.9 mV
114.9 mV
Eye width(eq1)
60.16 ps
60.16 ps
V min(eq1)
-113.3 mV
-113.3 mV
Eye height(eq1)
84.9 mV
84.9 mV
Histogram
Y scale
917 hits/
Y offset
0 hits
Hist mean
68.26777 ps
Hist std dev
16.1647 ps
Hist μ±1σ
60.8%
Hist μ±2σ
99.6%
Hist μ±3σ
100%
Hist μ-3σ
19.77 ps
Hist μ+3σ
116.76 ps
Hist p-p
73.48 ps
Hist FWHM
47.82 ps
Hist min
26.48 ps
Color Grade
1 - 36
37 - 73
74 - 147
148 - 295
296 - 591
592 - 1183
1184 - 2366


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
Tp10 M3
Tp3 M4
Position
50.0%
Factor
10000
M1 400.0mV 6.068µs
M3 400.0mV 6.068µs
M4 400.0mV 6.068µs
R4 47.96mV 6.068µs
Z1M1 400.0mV -3.039ns 3.029ns
Z1M3 400.0mV -3.039ns 3.029ns
Z1M4 400.0mV -3.039ns 3.029ns
Z1R4 47.96mV -3.039ns 3.029ns
C1 0.0V
6.068µs/div 100GS/s 10.0ps
Stopped Single Seq
1 acqs RL:6.068M
Man September 29, 2020 21:42:51
Jitter, Noise and Eye Diagram Analysis Tools
Sources
MATH3
Bit Rate : 20.000Gb/s
Pattern Length : 32767UI
Standard
View Summary
Options
Expand
Overall Result: Pass
Select
Configure
Results
Plots
Reports
Description
Pass/Fail
Mean
Std Dev
Max
Min
p-p
Population
USB4 Eye Diagram...
Pass
0.0000
0.0000
0.0000
1.2288M
USB4 DFEEW, Tp10...
25.465ps
0.0000s
25.465ps
25.465ps
0.0000s
1
USB4 DFEEH, Tp10 ...
116.04mV
0.0000V
116.04mV
116.04mV
0.0000V
1
Clear
Recalc
Single
Run
Show Plots

12. Measure the Eye Width at ±2.5mV from 0mV. If the Eye width is not within the 513 ± 25mUI p-p specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the eye width is within specification.
13. Save the BERT Setup to "10G_TC2_100MHz".
14. Repeat steps #1 to #10 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each setup as 10G_TC2_1MHz, 10G_TC2_2MHz, 10G_TC2_10MHz and 10G_TC2_50MHz respectively.

8.3 Calibrate and Save for UHBR 13.5 (13.5 Gbit/s) Receiver at TP1

The initial setups for the BERT and Scope are the same as defined for the 10Gb/s section above, except for the settings highlighted in **bold** below:

1. Set up the physical equipment connections without the ISI channel, as per Figure 23.
2. Set up the BERT as follows:
   a) Set the Data Rate to **13.5Gb/s**.
   b) Set the Pattern to PRBS15.
   c) Turn on "SSC", with settings of 33kHz (for 13.5G) with 5300ppm (for 13.5G) triangle down spread. (SSC will remain ON for all of the following steps.)
   d) Set DATA+/DATA- Launch Amplitude to 750mV. This should set the differential amplitude just above the 700mV Eye Height target value as an initial value.
   e) Set the initial CM interference amplitude to 0mV.

8.3.1 Set Up Oscilloscope

8.3.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 17.

TABLE 11. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Horizontal	20Gb/s
Record Length	40M
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	21GHz (The Calibration Bandwidth is limited to the Bit Rate of the signal, which is 2 * 1st harmonic. This is done intentionally to be on the order of a Thunderbolt Receiver's Bandwidth. This is essentially acting as an "Electrical Reference

	Receiver", used for calibration. It reduces the noise measured by the Scope which a real Receiver will never perceive.)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF

8.3.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 18.

TABLE 12. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	13.5Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000 MHz Damping factor: 0.94

8.3.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 19.

TABLE 13. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	≥ 80Gs/s
Record Length	27Mpts per channel
Bandwidth	21GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.3.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 20.

TABLE 14. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-9
Pattern	Periodic, Repeating Pattern (2^{15}-1 = 32,767 bits)

8.3.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 21.

TABLE 15. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	112 mV (for final Eye Height Calibration)
Eye Mask Width	540 mUI

8.3.2 Record ISI Measurements

1. Step through the Preset Coefficients 0-15 and use the Preset which yields the minimum DDJ Measurement. Although this is not a Calibrated value, record this ISI Measurement as part of the measurements table.
2. Change the pattern on the BERT to PRBS31. Calibrate ACCM to be 100mVpp at 400MHz Clock, using the ACCM Scope Setup.
3. Return CM Amplitude to zero.
4. Turn on all remaining Jitter terms (RJ-Filtered [10MHz HPF] and SJ at 100MHz).
5. Set all jitter amplitudes to zero.
6. Return the Scope setup to the setup in Section 8.3.1.
7. Change the pattern on the BERT to PRBS15.
8. Calibrate RJ Amplitude to 115mUI peak-to-peak (9.58mUI RMS).
9. Return amplitude to zero.
10. Capture screen shot.

11. Calibrate SJ Amplitude to 170mUI peak-to-peak at 100MHz.
12. Capture screen shot.
13. Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.
14. Calibrate the TJ measurement to 360mUI ± 17mUI using SJ Amplitude control (for SJ Frequency of 100MHz) and RJ Amplitude control (for SJ Frequencies of less than 100 MHz) as an adjustment on the BERT.
15. Capture screen shot.
16. Change the pattern on the BERT to PRBS31.
17. Calibrate Inner Eye Height to 700mV (top and bottom of triangle eye mask, with V:700mV; H:620mUI).
18. Capture screen shot.
19. Save BERT Setup to “135G_TC1_100MHz”.
20. Repeat steps #1 to #18 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each BERT Setup as 135G_TC1_1MHz, 135G_TC1_2MHz, 135G_TC1_10MHz and 135G_TC1_50MHz.

8.4 Calibrate and Save for UHBR 13.5 (13.5Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -16.5dB@10GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 135G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 25.
3. Search for Optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.
   a) Set up the Scope as follows for CTLE:
      i) Number of Poles set to “2 Poles, AC Gain”
      ii) DC Gain set to 1.00
      iii) AC Gain set to 1.41
      iv) Pole #1 Frequency set to 3.375 GHz
      v) Pole #2 Frequency set to 6.75 GHz
   b) Use the DC Gain Setting in Table 22 which yields the largest Eye Height.

TABLE 16. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

   c) Set up the DFE:
      i) Set Max Tap to 50mV.
      ii) Run Auto DFE.

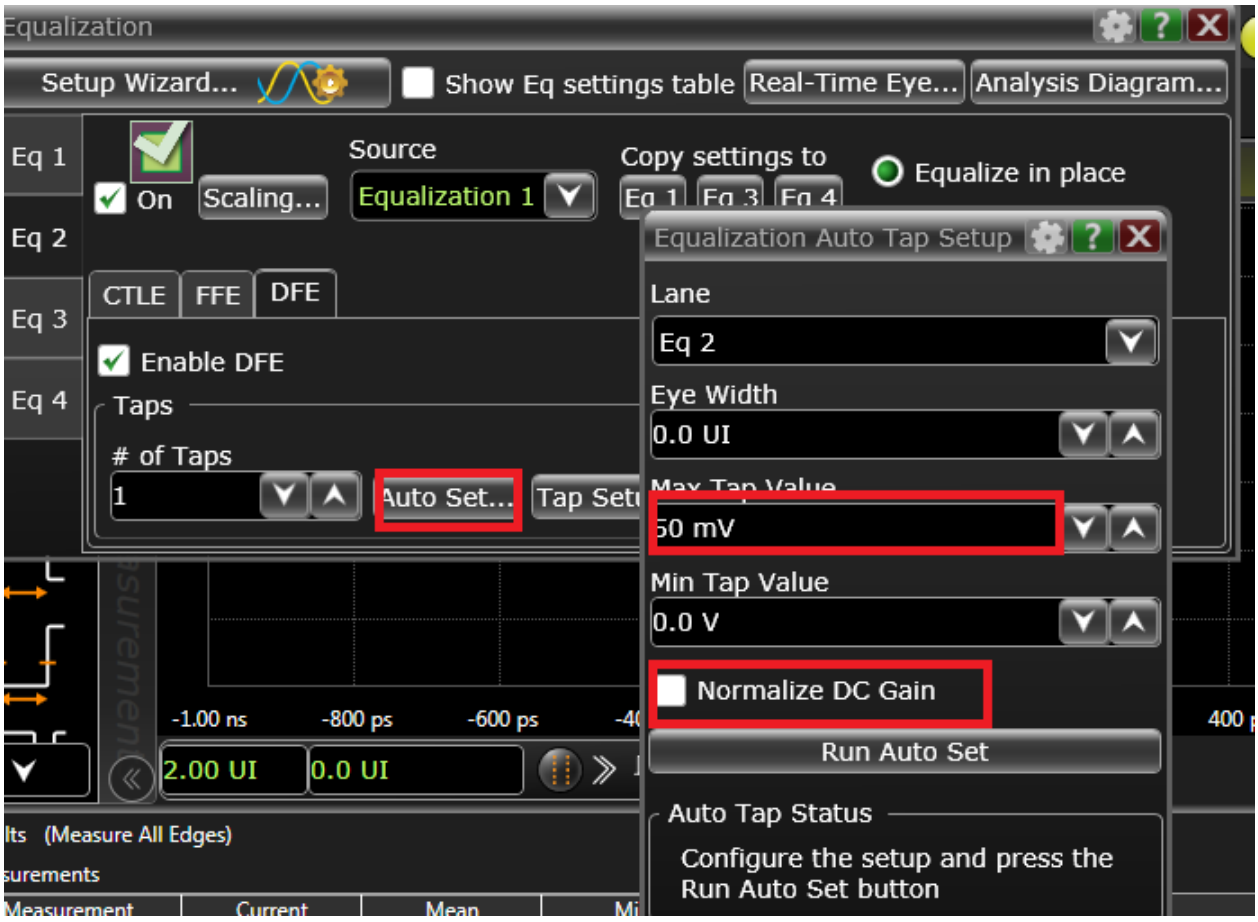

Equalization
Setup Wizard...
Show Eq settings table
Real-Time Eye...
Analysis Diagram...
Eq 1
Eq 2
Eq 3
Eq 4
On
Scaling...
Source
Equalization 1
Copy settings to
Eq 1
Eq 3
Eq 4
Equalize in place
CTLE
FFE
DFE
Enable DFE
Taps
# of Taps
1
Auto Set...
Tap Setu
Equalization Auto Tap Setup
Lane
Eq 2
Eye Width
0.0 UI
Max Tap Value
50 mV
Min Tap Value
0.0 V
Normalize DC Gain
Run Auto Set
Auto Tap Status
Configure the setup and press the Run Auto Set button
-1.00 ns
-800 ps
-600 ps
2.00 UI
0.0 UI
lts (Measure All Edges)
surements
Measurement
Current
Mean

FIGURE 77. DFE SETTING

d) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UI's per Acquisition).
e) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via *Eye Width * Eye Height*.
f) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest Eye area is used for the following measurements.

15. Calibrate the Inner Eye Height to 112 ± 10mV diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

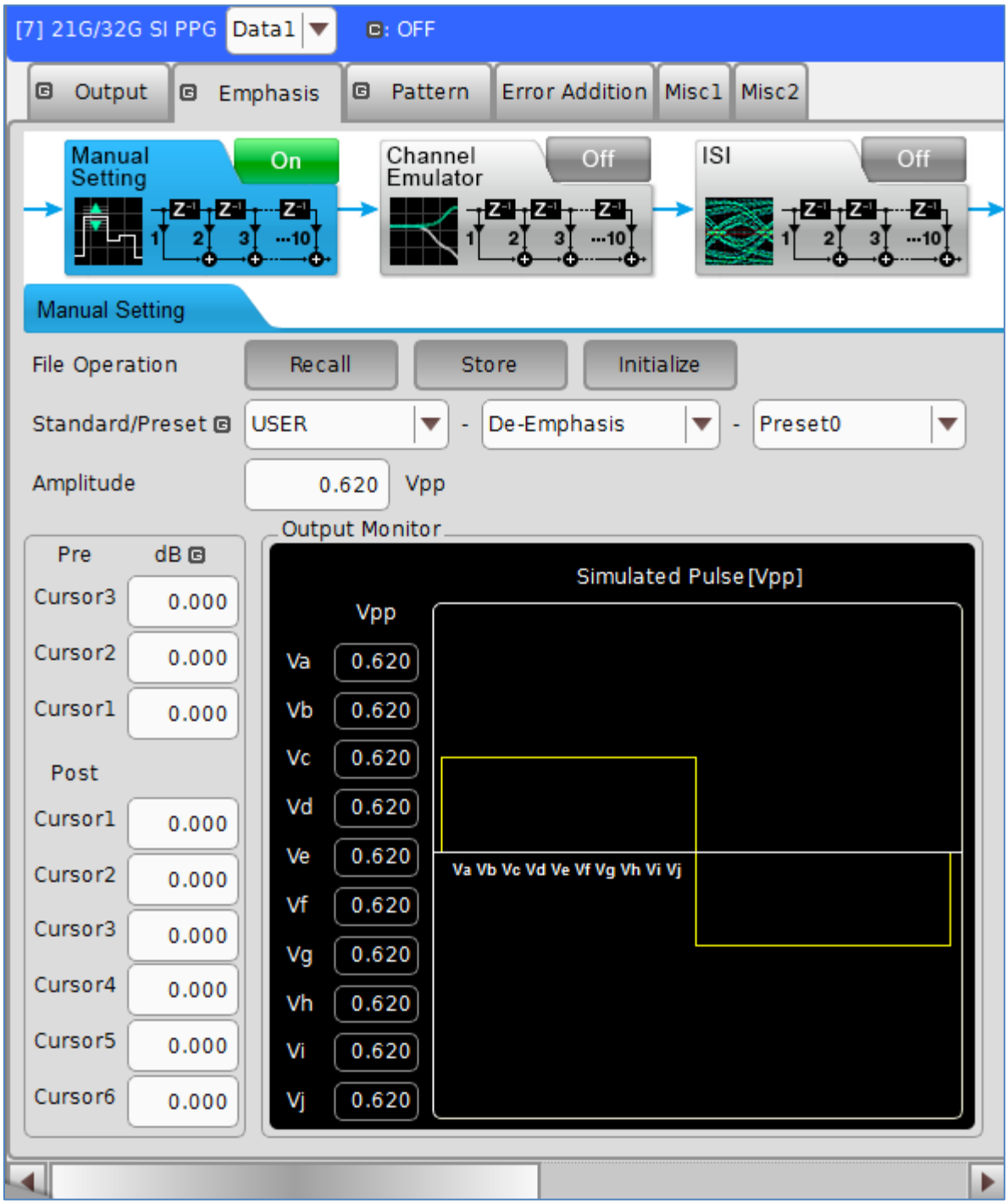


FIGURE 78. EYE AMPLITUDE

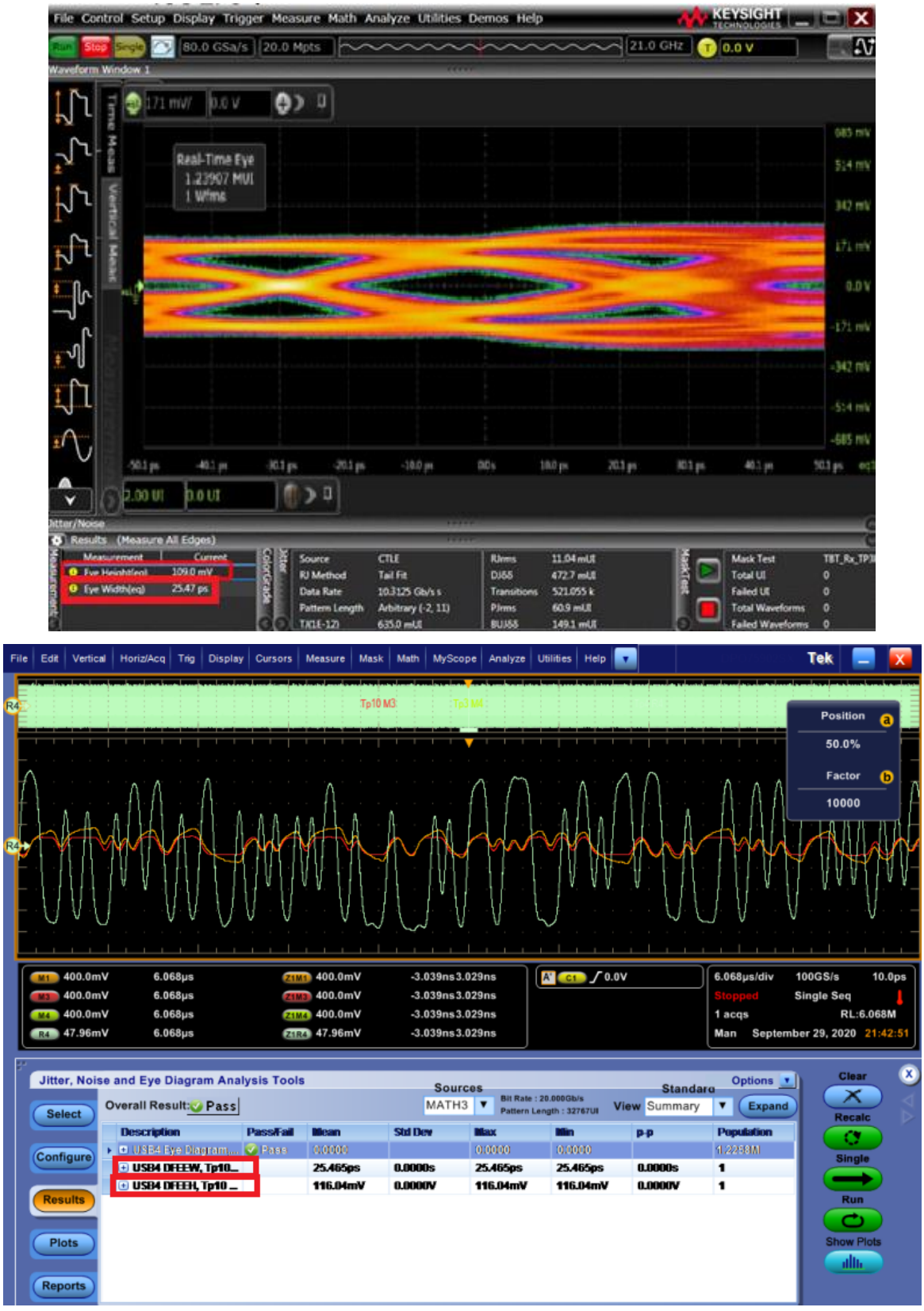


FIGURE 79. EYE AMPLITUDE MEASUREMENTS

16. Measure the Eye Width at ±2.5mV. If the Eye Width is not within the 540 ± 50mUI p-p specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the Eye Width is within specification.
17. Capture screen shot.
18. Save BERT Setup to "135G_TC2_100MHz".
19. Repeat steps #1 to #11 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each setup as 135G_TC2_1MHz, 135G_TC2_2MHz, 135G_TC2_10MHz and 135G_TC2_50MHz respectively.

8.5 Calibrate and Save for UHBR 20 (20.0 Gbit/s) Receiver at TP1

The initial setups for the BERT and Scope are the same as defined for the 10Gb/s section above, except for the settings highlighted in **bold** below.

1. Set up the physical equipment connections without the ISI channel, as per Figure 23.
2. Set up the BERT as follows:

   a) Set the Data Rate to **20Gb/s**.
   b) Set the Pattern to PRBS15.
   c) Turn on "SSC", with settings of 32kHz (for 20G) with 5600ppm (for 20G) triangle down spread. (SSC will remain ON for all of the following steps.)
   d) Set DATA+/DATA- Launch Amplitude to 750mV. This should set the differential amplitude just above the 700mV Eye Height target value as an initial value.
   e) Set the initial CM interference amplitude to 0mV.

8.5.1 Set Up Oscilloscope

8.5.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 17.

TABLE 17. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Horizontal	20Gb/s
Record Length	40M
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	21GHz (The Calibration Bandwidth is limited to the Bit Rate of the signal, which is 2 * 1st harmonic. This is done intentionally to be on the order of a Thunderbolt

	Receiver's Bandwidth. This is essentially acting as an "Electrical Reference Receiver", used for calibration. It reduces the noise measured by the Scope which a real Receiver will never perceive.)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF

8.5.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 18.

TABLE 18. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	20Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000 MHz Damping factor: 0.94

8.5.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 19.

TABLE 19. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	≥ 80Gs/s
Record Length	27Mpts per channel
Bandwidth	21GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.5.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 20.

TABLE 20. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-12
Pattern	Periodic, Repeating Pattern (2^{15}-1 = 32,767 bits)

8.5.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 21.

TABLE 21. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	96 mV (for final Eye Height Calibration)
Eye Mask Width	520 mUI

8.5.2 Record ISI Measurements

1. Step through the Preset Coefficients 0-15 and use the Preset which yields the minimum DDJ Measurement. Although this is not a Calibrated value, record this ISI Measurement as part of the measurements table.
2. Change the pattern on the BERT to PRBS31. Calibrate ACCM to be 100mVpp at 400MHz Clock, using the ACCM Scope Setup.
3. Return CM Amplitude to zero.
4. Turn on all remaining Jitter terms (RJ-Filtered [10MHz HPF] and SJ at 100MHz).
5. Set all jitter amplitudes to zero.
6. Return the Scope setup to the setup in Section 8.5.1.
7. Change the pattern on the BERT to PRBS15.
8. Calibrate RJ Amplitude to 115mUI peak-to-peak (9.58mUI RMS).
9. Return amplitude to zero.
10. Capture screen shot.

11. Calibrate SJ Amplitude to 170mUI peak-to-peak at 100MHz.
12. Capture screen shot.
13. Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.
14. Calibrate the TJ measurement to 360mUI ± 25mUI using SJ Amplitude control (for SJ Frequency of 100MHz) and RJ Amplitude control (for SJ Frequencies of less than 100 MHz) as an adjustment on the BERT.
15. Capture screen shot.
16. Change the pattern on the BERT to PRBS31.
17. Calibrate Inner Eye Height to 700mV (top and bottom of triangle eye mask, with V:700mV; H:620mUI).
18. Capture screen shot.
19. Save BERT Setup to “20G_TC1_100MHz”.
20. Repeat steps #1 to #18 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each BERT Setup as 20G_TC1_1MHz, 20G_TC1_2MHz, 20G_TC1_10MHz and 20G_TC1_50MHz.

8.6 Calibrate and Save for UHBR 20 (20.0 Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -16.5dB@10GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 20G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 26.
3. Search for Optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.
   a) Set up the Scope as follows for CTLE:
      i) Number of Poles set to “2 Poles, AC Gain”
      ii) DC Gain set to 1.00
      iii) AC Gain set to 1.41
      iv) Pole #1 Frequency set to 5 GHz
      v) Pole #2 Frequency set to 10 GHz
   b) Use the DC Gain Setting in Table 22 which yields the largest Eye Height.

TABLE 22. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

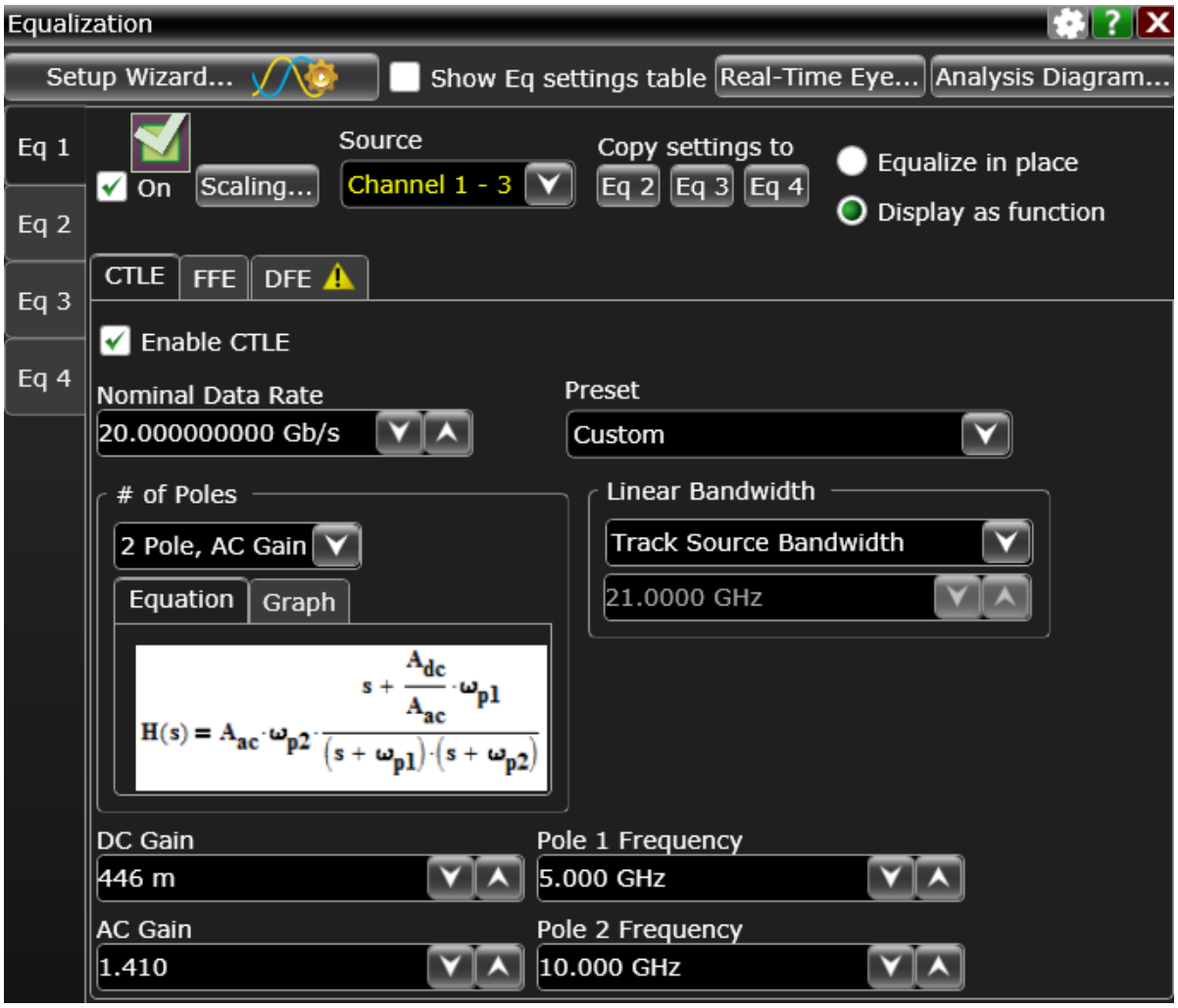


FIGURE 80. DC GAIN SETTING

c) Set up the DFE:

i) Set Max Tap to 50mV.
ii) Run Auto DFE.

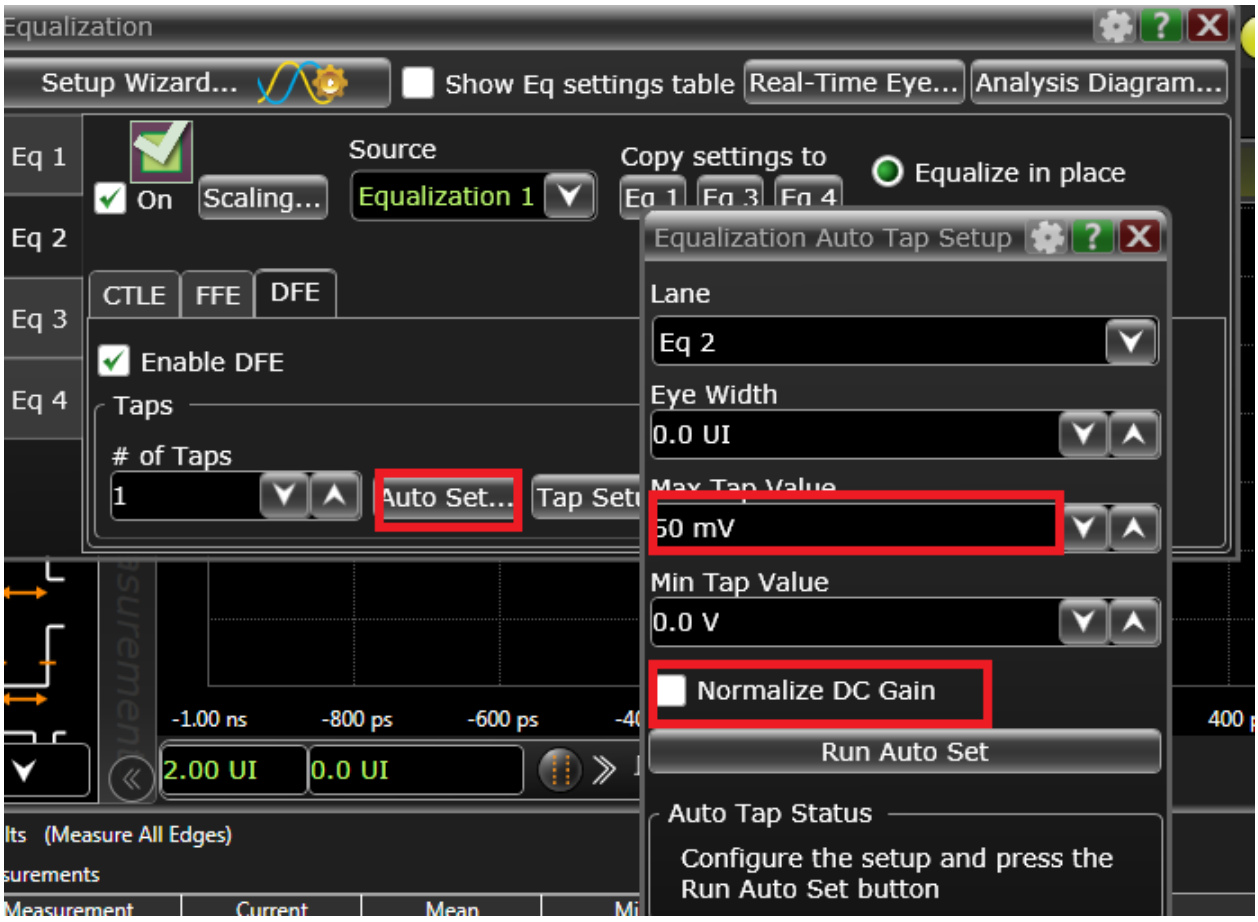


FIGURE 81. DFE SETTING

d) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UI's per Acquisition).
e) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via *Eye Width * Eye Height*.
f) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest Eye area is used for the following measurements.

20. Calibrate the Inner Eye Height to 96 ± 10mV diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

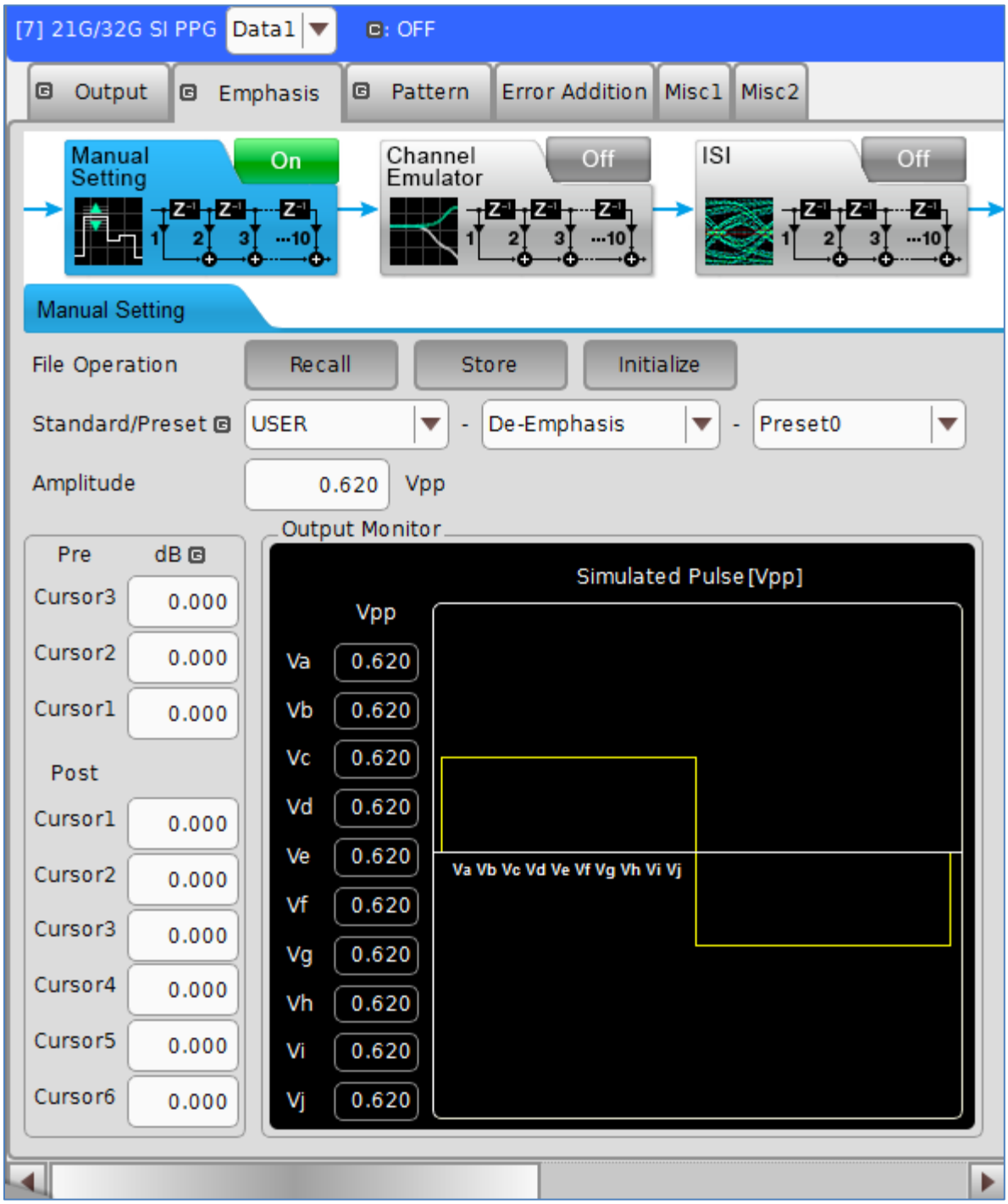


FIGURE 82. EYE AMPLITUDE

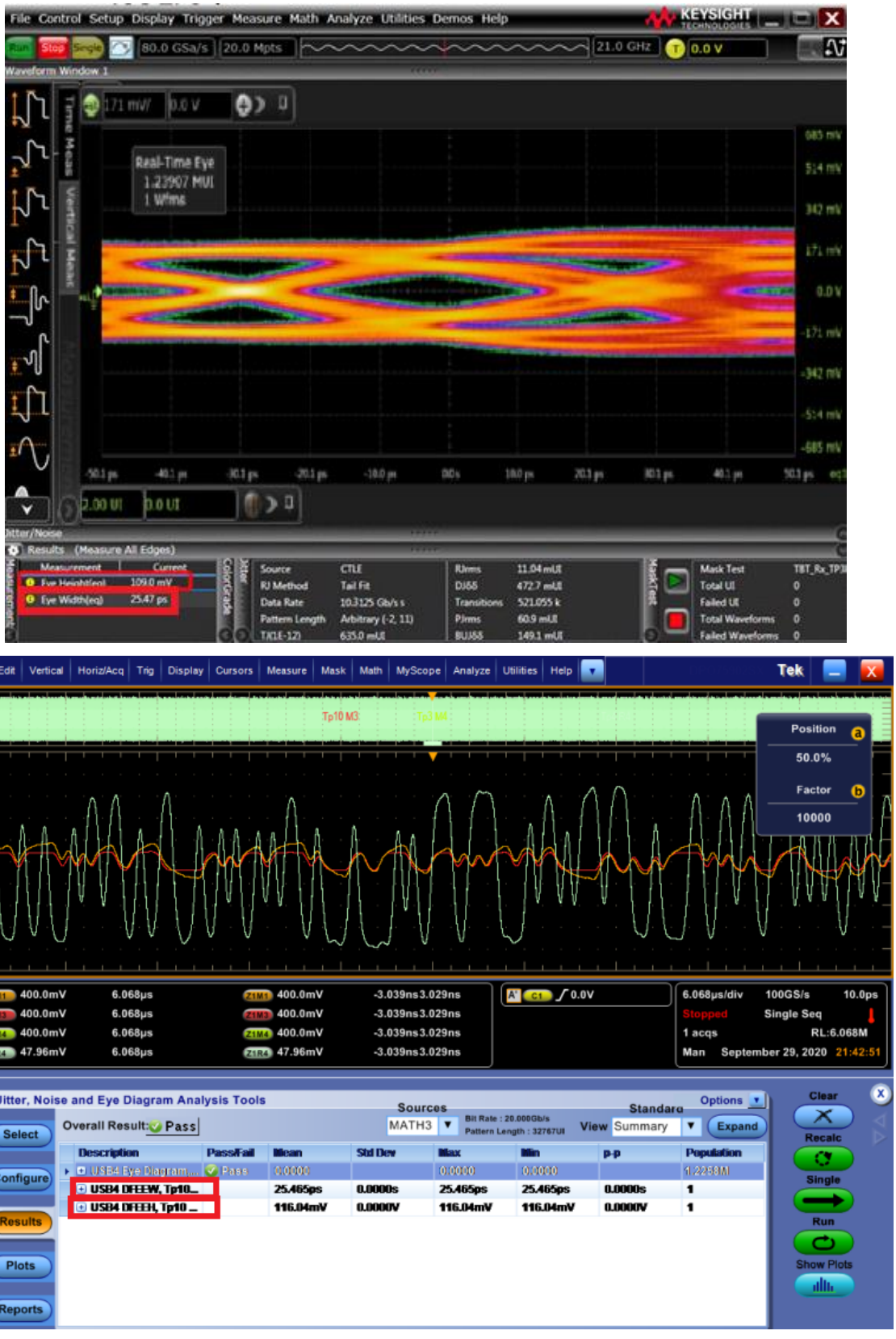


FIGURE 83. EYE AMPLITUDE MEASUREMENTS

21. Measure the Eye Width at ±2.5mV from 0mV. If the Eye Width is not within the 520 ± 50mUI p-p specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the Eye Width is within specification.
22. Capture screen shot.
23. Save BERT Setup to “20G_TC2_100MHz”.
24. Repeat steps #1 to #11 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each setup as 20G_TC2_1MHz, 20G_TC2_2MHz, 20G_TC2_10MHz and 20G_TC2_50MHz respectively.

9 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a controller PC. The Keysight Scope can be connected to the controller PC through GPIB, USB or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the controller PC.
2. When installed successfully, the IO icon ( ) will appear in the taskbar notification area of the controller PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

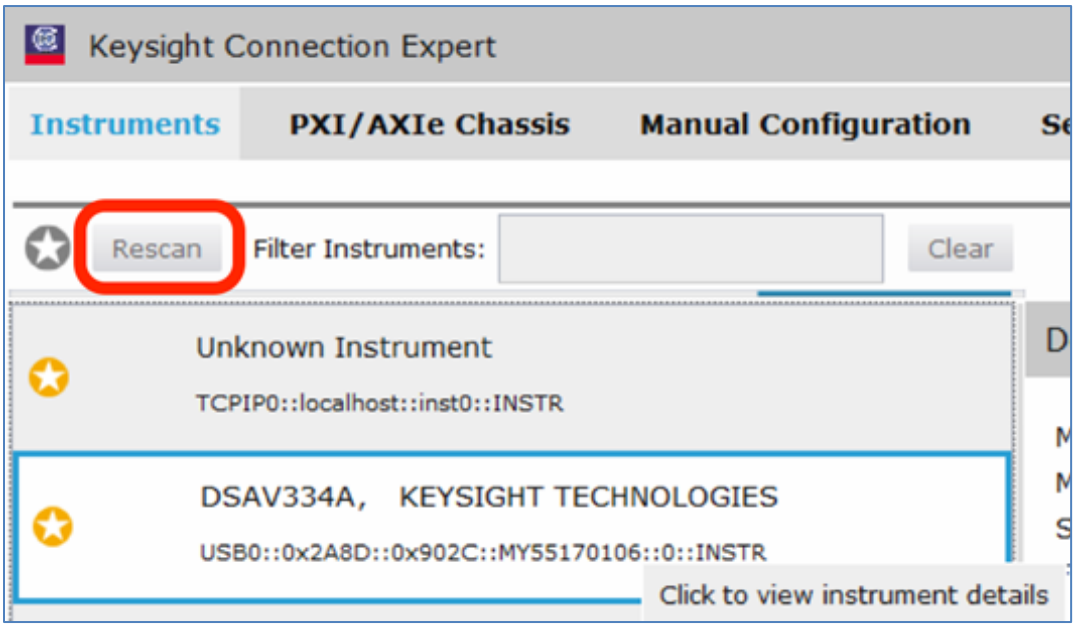


FIGURE 84. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

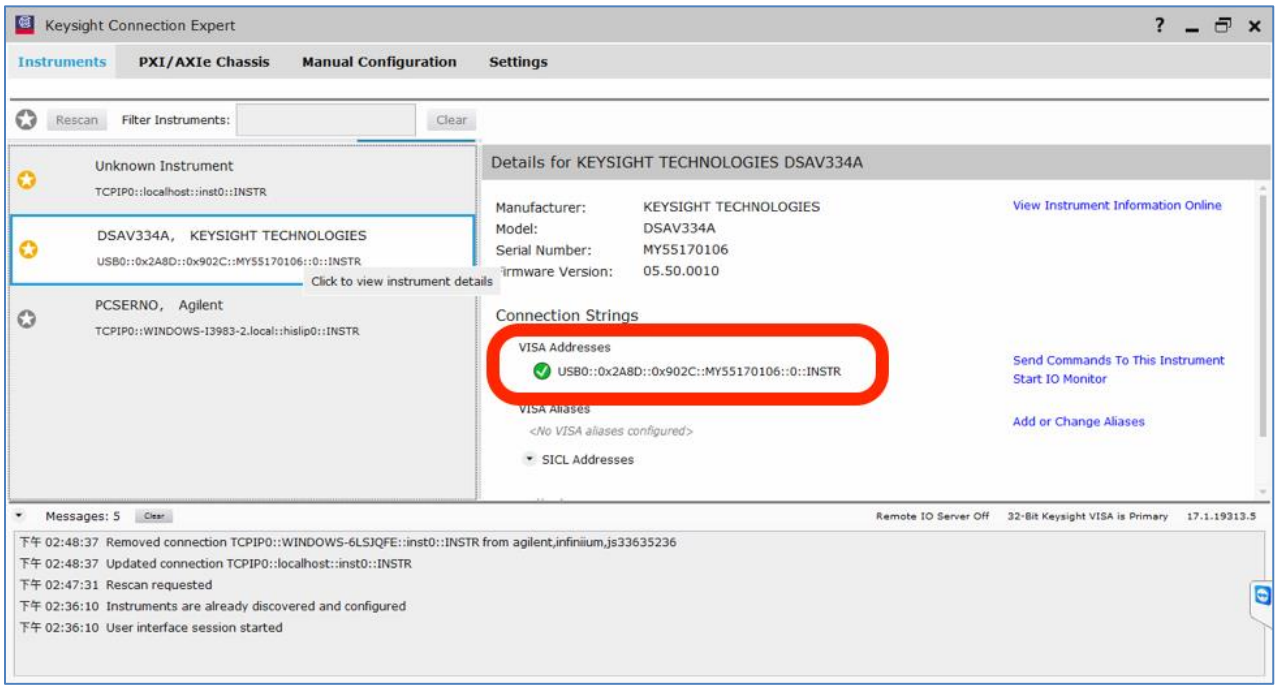


FIGURE 85. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL-Anritsu DisplayPort Sink 2.1 Test Application. If the GRL-Anritsu DisplayPort Sink 2.1 Test Application is installed on the Keysight Scope, type in the Scope IP address, for example "TCPIP0::127.0.0.1::inst0::INSTR". If the GRL software is installed on the controller PC to control the Scope via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.100::inst0::INSTR". Note to ***omit*** the Port number from the address.

   If there is error in connection, type in the Scope IP address as "TCPIP0:: 192.168.0.100::5025::SOCKET".

10 Appendix C: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

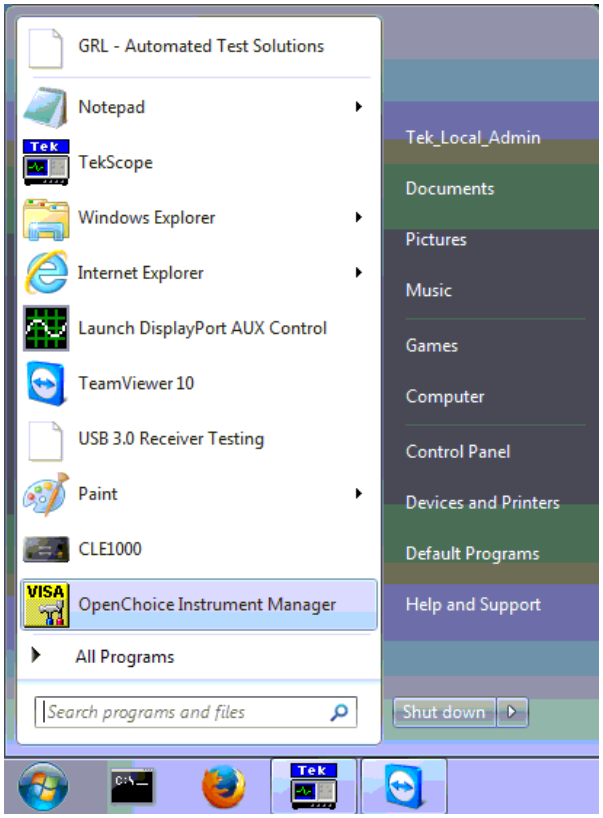


FIGURE 86. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
   a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
   b) “Search Criteria”: Select to configure the instrument search function.
   c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
   d) “Properties”: Select to display and view the selected instrument properties.

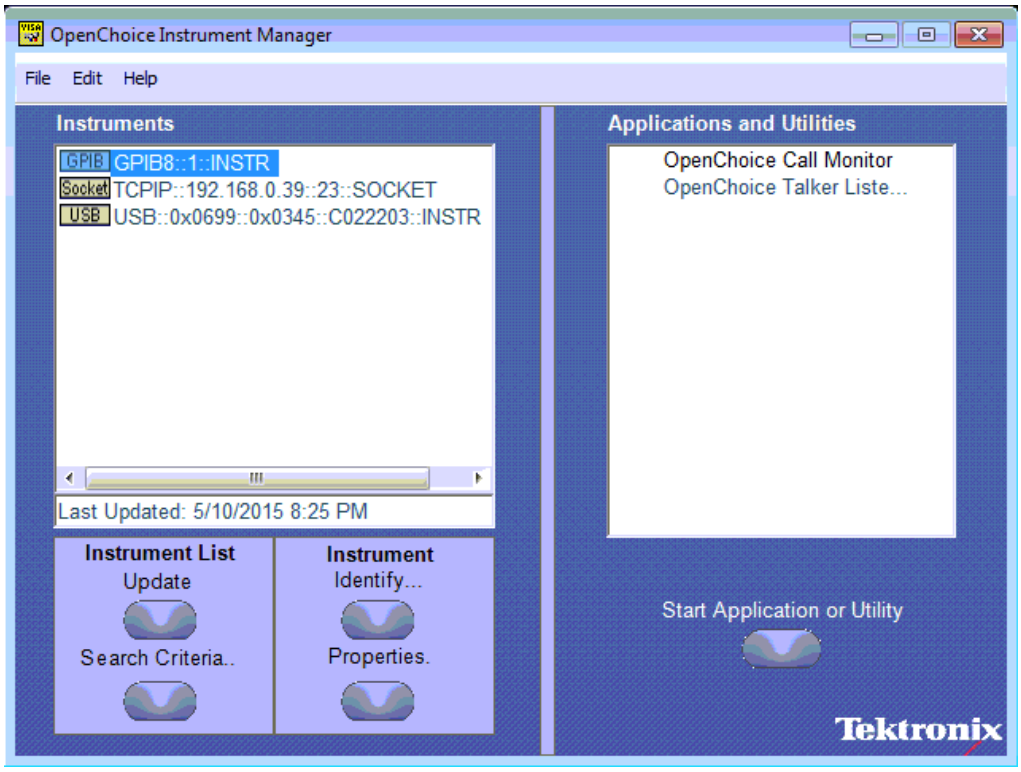


FIGURE 87. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the "Search Criteria" function to ensure that USB connection is enabled, and then select the "Instrument List Update" function. When the Scope appears on the "Instruments" panel, select it and then go to the "Instrument Identify" function. This will display the model and serial number of the Scope once detected. Select the "Properties" function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the "Search Criteria" function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by "Search". The Scope should then appear on the "Instruments" panel. Select it and access the "Instrument Identify" function to view the Scope model and serial number as well as the "Properties" function to view the Scope address.
6. On the Equipment Setup page of the GRL DisplayPort Sink 2.1 Test Application, type in the Scope address into the 'Address' field. If the GRL DisplayPort Sink 2.1 Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR". If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to ***omit*** the Port number from the address.

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