

Granite River Labs

DisplayPort™ PHY 1.4 Sink Calibration and Test User Guide & Method of Implementation (MOI)

Using

Anritsu MP1900A BERT and Keysight DSO V Series Real-Time Oscilloscope / Tektronix DPO/MSO70000 Series Real-Time Oscilloscope

with

GRL-DP14-SINKAN or GRL-DP-SINK DisplayPort 1.4 Sink Calibration and Test Automation Software



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1 Introduction

This User Guide & MOI describes the step-by-step calibration and procedures to perform DisplayPort 1.4 Sink tests of the VESA DisplayPort Logo Compliance Program using the Anritsu MP1900A BERT and Keysight DSO V Series Real-Time Oscilloscopes or Tektronix DPO/MSO70000 Series Real-Time Oscilloscopes in conformance with the DisplayPort PHY 1.4 Compliance Test Specification (CTS). Sink tests are required to qualify a Sink product or silicon building block for Logo certification and listing on the DP Integrators List.

This User Guide & MOI also explains how to set up and use the GRL-DP14-SINKAN software to automate receiver calibration and compliance testing for DisplayPort 1.4 Sink conformance. The GRL-DP14-SINKAN software is used with the Anritsu MP1900A BERT for testing DisplayPort Sink receivers per the Jitter Tolerance requirements of the DisplayPort PHY CTS version 1.4 and DisplayPort over USB Type-C CTS Rev 1.2a respectively.

The GRL-DP14-SINKAN software automates stressed signal calibration and jitter tolerance testing at the following DisplayPort data rates– RBR (1.62 Gb/s), HBR (2.7 Gb/s), HBR2 (5.4 Gb/s), HBR3 (8.1 Gb/s) and supports USB Type-C and standard DisplayPort sink device-under-tests (DUT's). The GRL software also supports variable ISI generation through the Artek CLE1000-A2 which enables calibration to be performed with minimum reconfiguration of the setup, allowing measurements to be more fully automated. For link training, compliance, and margin testing through DPCD registers, the software provides automation control using the Tektronix DP-AUX or Unigraf DPT-200 AUX controller for standard DisplayPort connectors and the GRL-USB-PD-C2 USB Type-C Power Delivery Tester for USB Type-C connectors.

The following are the main topics covered by this User Guide & MOI:

1. Equipment required for calibration and testing.
2. GRL-DP14-SINKAN software setup for calibration and test automation.
3. Manual DisplayPort PHY CTS Sink calibration and test methodology.

The MOI reduces the CTS test description to practice using the specified test equipment and procedures in an effort to standardize testing across ATC's and equipment manufacturers who perform their own certification measurements.

2 Reference Documents

[1] VESA DisplayPort 1.4a PHY Layer Compliance Test Specification (PHY CTS), Version 1.4, Revision 1.0, 27 July 2018

[2] VESA DisplayPort (DP) Standard v1.4 Specifications

[3] VESA DisplayPort over USB Type-C CTS Rev. 1.2a

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3 Resource Requirements

3.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description	Key Specification Requirement
GRL-DP14-SINKAN	1	Granite River Labs DisplayPort 1.4 Sink Compliance Calibration & Test Automation Software for the Anritsu MP1900A BERT – www.graniteriverlabs.com *– with Node Locked License to single Oscilloscope/PC OS*	
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 21G/32G bit/s SI Pulse Pattern Generator • MU195050A Noise Generator	• Option STR for stress generation • Proper test patterns [a]
Real-time Oscilloscope [b]	1	Keysight (InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization) Oscilloscope Or Tektronix DPO/MSO70000DX or 70000SX Series Oscilloscope with DPOJET (Jitter and Eye Analysis) software	• ≥ 13 GHz bandwidth (for HBR2 and below) • > 16 GHz (for HBR3)
ISI Generator	1	Artek CLE1000-A2 [c]	For variable ISI generation
VISA (Virtual Instrument Software Architecture) API Software	1	VISA Software is required to be installed on the host PC running GRL-DP14-SINKAN software. GRL's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com (Search on IO Libraries) 3. Tektronix TekVISA: www.tek.com (Downloads > Software > TekVisa)	
AUX Controller [d]	1	Unigraf DPT-200	For link training and error detection
Computer	1	Laptop or desktop PC	For external automation control

[a] MP1900A DisplayPort patterns are distributed with GRL-DP14-SINKAN software and are installed during installation process.

[b] Infiniium / DPOJET setup files and SDLA filters are distributed with the GRL-DP14-SINKAN software and are installed during installation process.

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[c] If using the ARTEK CLE1000-A2 as the ISI generator, its USB driver software must be installed on the PC being used for testing and the ARTEK CLE1000-A2 must be connected to the PC via USB. The driver is available from the manufacturer. Refer to Appendix for the driver installation procedure.

[d] The USB driver software for the AUX Controller being used must be installed on the PC being used for testing, and the AUX controller must be connected to the PC via USB. The driver for the AUX controller is available from the AUX controller manufacturer. Refer to Appendix for driver installation information for Unigraf AUX controllers.

TABLE 2. EQUIPMENT REQUIREMENTS – ACCESSORIES

Accessory	Qty.	Description	Key Specification Requirement
VESA-Approved DisplayPort Mated Adapter Fixture Pair	1	Standard DP, mDP, or USB Type-C plug-receptacle mated pair adapter (Wilder-Tech, LS-ICT) – *DUT connector type dependent*	Meets DP1.4 CTS electrical requirements
SMA Torque Wrench	1	8 in-lb SMA	
DC Block	2	Anritsu K261 Precision DC Block or Weinchel Aeroflex Model 7006-1 20 GHz DC Block or equivalent	
TTC (Transition Time Converter)	2	For Data signals (TTC): HYPERLABS Model # HL9452-60 or equivalent	60 ps rise time, 5.83 GHz (10-90%)
	2	For Crosstalk signals: HYPERLABS Model # HL9452-150 or equivalent	150 ps rise time, 2.33 GHz (10-90%)
÷4 RF Splitter or ÷3 RF Splitter	2	Anritsu AN44182A 4-Way Power Divider or JFW Model 50PD-292 or equivalent	
SMA-Female to SMA-Female Adapter	4		
LAN Switch	1	Optional [a]	
LAN Cable	1 or 3	For Oscilloscope and MP1900A BERT [a]	
300 MHz Vector Signal Generator	1	As external SJ Fixed source (Rigol DSG815 recommended)	
6 dB Attenuator	1	For Vector Signal Generator to protect External Jitter Input (Anritsu 41KB-6 recommended if connector type is SMA)	Max 2 V
SMA-to-SMA Cable	1	Anritsu J1625A or equivalent	
Skew Matched Pair Cable	6 pairs	Anritsu J1550A 80 cm skew matched pair cable or equivalent	
N-SMA Adapter	1	Anritsu J1398A or equivalent	

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Accessory	Qty.	Description	Key Specification Requirement
50 Ohm SMA Terminator	15		

[a] If the Scope OS is used for automation, one LAN cable can be connected directly from the Scope to the MP1900A BERT. If an external PC is used, two LAN cables will be required to connect to the network. (These cables are not shown in the connection diagrams in this document.)

4 GRL-DP14-SINKAN Software Setup

4.1 Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL-DP14-SINKAN automation software. It also helps you familiarize yourself with the basic operation of the application.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

4.1.1 Download GRL-DP14-SINKAN Software

Download and install the GRL-DP14-SINKAN software on a PC or an oscilloscope (where GRL-DP14-SINKAN software is referred to as 'Controller PC' or 'Scope' respectively in this User Guide & MOI):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-DP14-SINKAN is to be used (see Section 3.1).
2. Download the **DPSinkTest14VX.XX.XX.zip** package from Granite River Labs support site.
3. The ZIP file contains:
   a) **DPSink14PatternFilesInstallation00xxxxxxxSetup.exe** – Run this on the MP1900A BERT to install the DisplayPort 1.4 test pattern setup files. This will place the DisplayPort Configuration and Pattern files on the MP1900A BERT in the *'C:\Configurations\Anritsu DisplayPort Sink Test 1.4'* directory hierarchy.
   b) **DPSinkTest14Application14xxxxxxxxxSetup.exe** – Run this on the Controller PC or Oscilloscope to install the GRL-DP14-SINKAN application. This application will create the *'C:\GRL\Rx Test Solution\Applications\DPSinkTest14_AN'* directory hierarchy.
   c) **DPSinkTest14ScopeSetupFilesInstallation00xxxxxxxSetup.exe** – Run this on the Oscilloscope to install the Infiniium setup files. This will place the DisplayPort Setup and Filter folders in the *'C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4'* of the Keysight Scope or *C:\TekApplications\DPOJET* of the Tektronix Scope directory hierarchy.

4.1.2 Launch and Set Up GRL-DP14-SINKAN Software

4.1.2.1 On the MP1900A BERT

1. Launch the Signal Quality Analyzer-R Control Software.
2. Select the "Expert BERT" button to turn on the Miscellaneous System. This will allow you to remotely control the MP1900A BERT.

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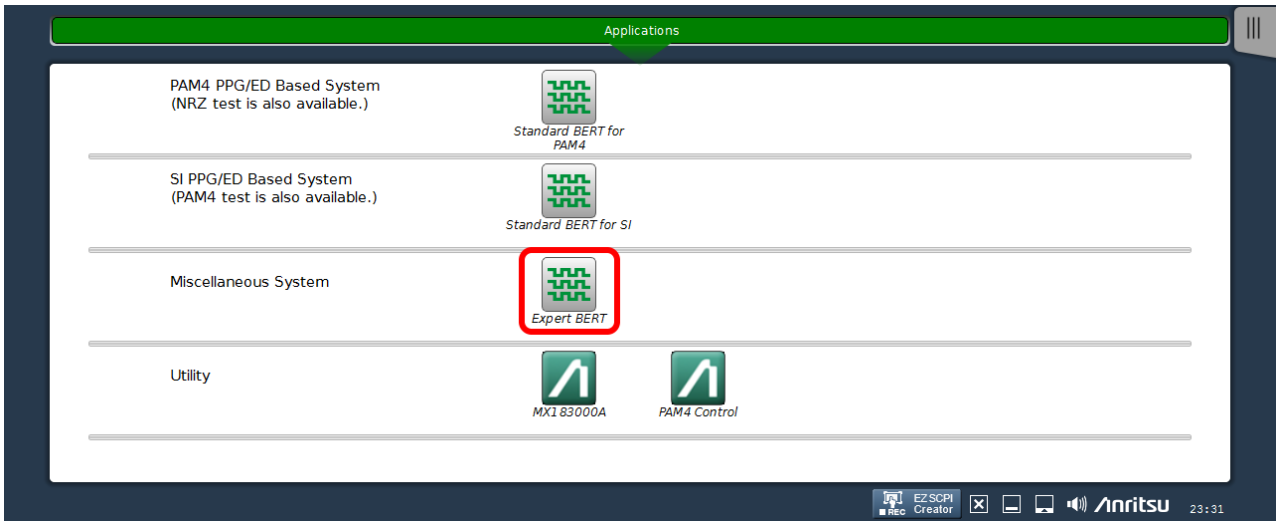


FIGURE 1. TURN ON MISCELLANEOUS SYSTEM

3. Note the IP Address as it will be used to connect the MP1900A BERT with the GRL-DP14-SINKAN software.

4.1.2.2 On the PC Used for GRL Framework Installation

1. Open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL software framework.

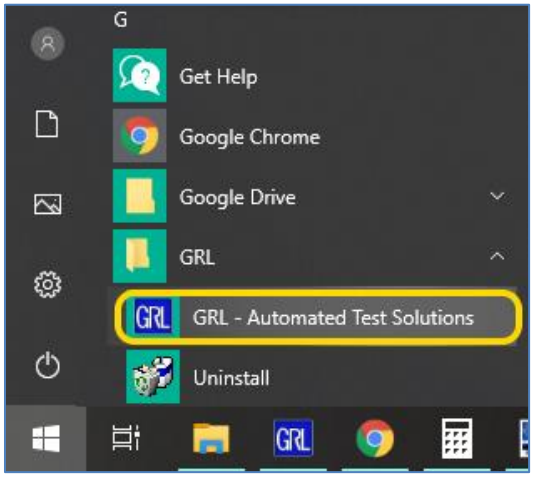


FIGURE 2. SELECT AND LAUNCH GRL FRAMEWORK

2. From the Application→Rx Test Solution drop-down menu, select 'Anritsu DisplayPort Sink Test 1.4' to start the application. If the selection is grayed out, it means that your license has expired.

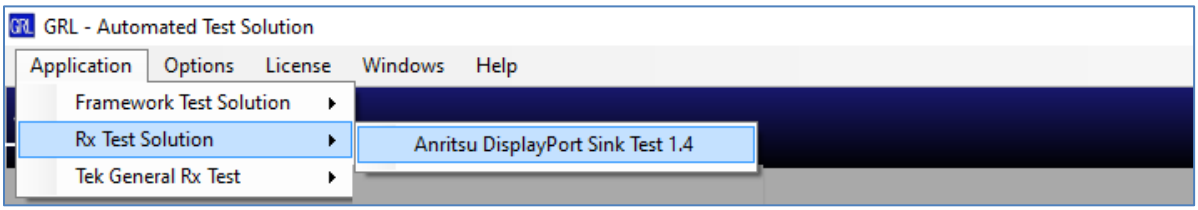


FIGURE 3. START DISPLAYPORT SINK TEST 1.4 APPLICATION

3. To enable license, go to License→License Details.

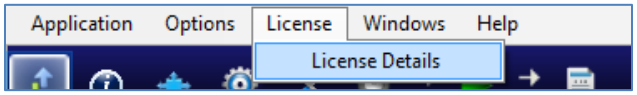


FIGURE 4. SEE LICENSE DETAILS

a) Check the license status for the installed application.

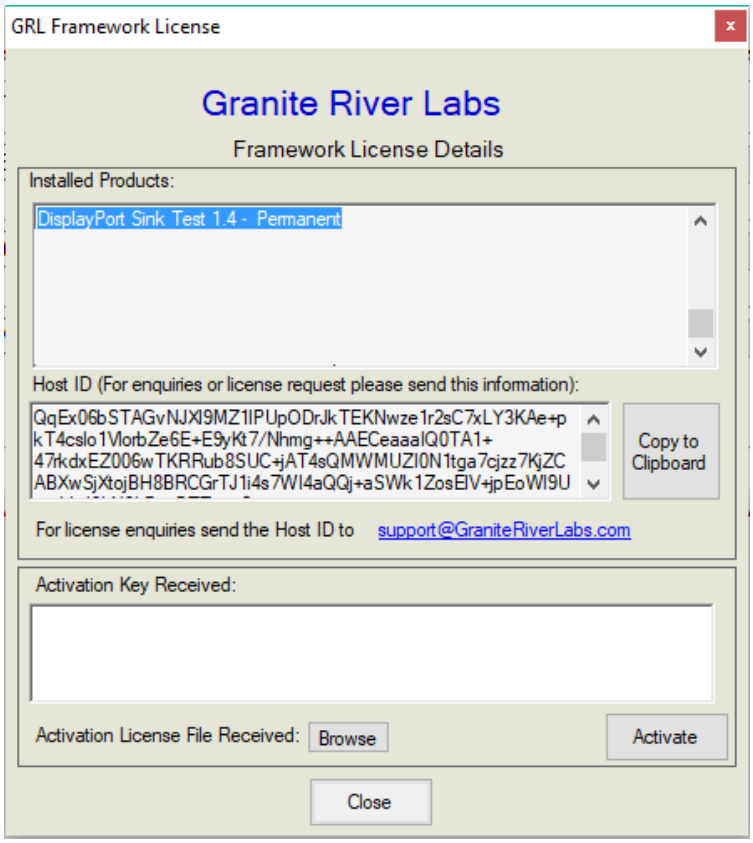


FIGURE 5. CHECK LICENSE FOR INSTALLED APPLICATIONS

4. Activate License:

a) If you have an Activation Key, please enter in the box provided and select **Activate**.
b) If you do not have an Activation Key, select **Close** to use a demo version of the software over a free 10-day trial period.

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Note: *Once the 10-day trial period ends, you will need to request an Activation Key to continue using the software on the same computer or oscilloscope. The demo software is also limited in its capability, in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request an Activation Key by contacting support@graniteriverlabs.com.*

5. Select the Equipment Setup icon on the DisplayPort Sink Test 1.4 Application menu.
4. Connect the Anritsu MP1900A BERT via LAN to the GRL automation control enabled Scope or PC. Enter the MP1900A IP address and Port number to match what is shown in the MP1900A *Remote Client* window in Section 4.1.2.1. For example, the BERT can be connected using a connection string in the following format: "TCPIP0::192.168.0.14::5001::SOCKET" or "192.168.0.14:5001". Note the IP address listed is only example and should be changed according to the actual network connection being used.
6. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL automation software.

   (Note: The Scope IP address can be obtained, if not known, by typing CMD → IPCONFIG on the Scope and observe the IP address listed. If the GRL software is installed on the ***Tektronix Scope****, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR".) If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to* ***omit*** *the Port number from the address.)*
7. Enter the COM address of the ISI Generator to be used.
8. Then select the "lightning" button ( ) for each connected instrument.

   The "lightning" button should turn green ( ) once the GRL software has successfully established connection with each instrument.

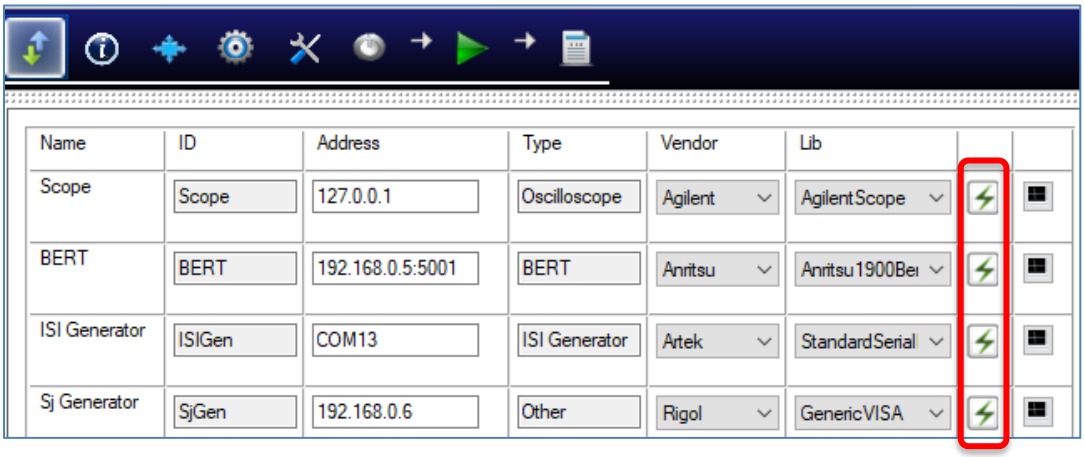


FIGURE 6. CONNECT INSTRUMENTS WITH GRL SOFTWARE

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Additional notes:

- *Further information for connecting the Keysight and Tektronix oscilloscopes to the PC is provided in the Appendix of this document.*
- *The USB driver software for the Artek ISI Generator must be installed on the PC being used for testing, and the ISI generator must be connected to the PC via USB. The driver for the ISI generator is available from the ISI generator manufacturer. Refer to Appendix for the driver installation information.*

4.2 Configuring the Software Before Calibration and Testing

4.2.1 Session Info

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

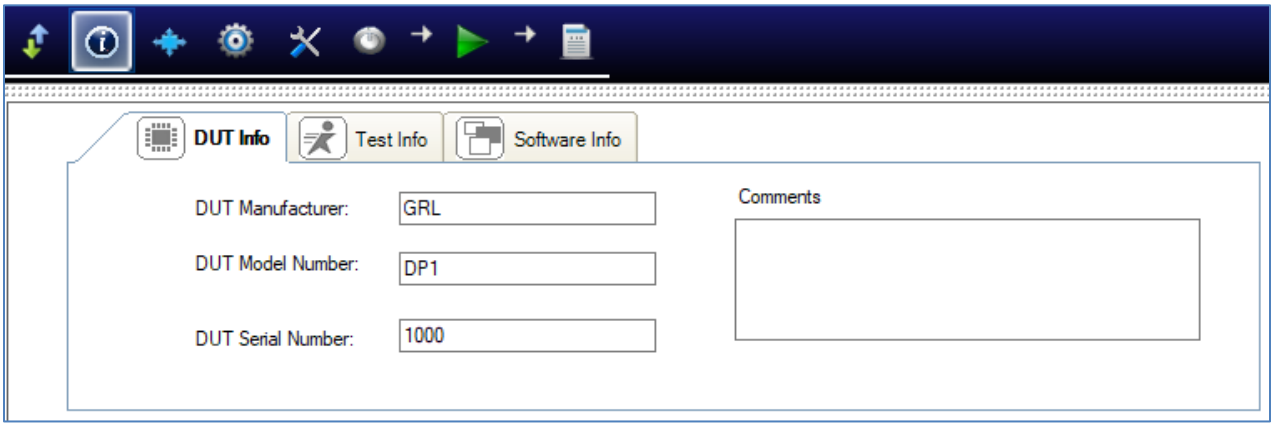


FIGURE 7. SESSION INFO PAGE

4.2.2 Conditions for Testing and Calibration

Select  from the menu to access the **Conditions** page to set the conditions for calibration and testing.

When calibrating, the application will calibrate for the selected Lanes, Test Points, Data Rates and Frequencies. The application will perform testing at these selected Lanes, Test Points, SSC Capabilities, Data Rates and Frequencies.

Recommended procedure:

- *Step 1*: When calibrating, select the desired conditions and perform the calibration tests.

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- *Step 2*: When ready for testing, re-select the desired test conditions. For example, if required to test only one Lane at one Frequency for the RBR Data Rate, then select the appropriate conditions for testing.

a) **Lane tab**: Select the desired Lanes for calibration or testing.

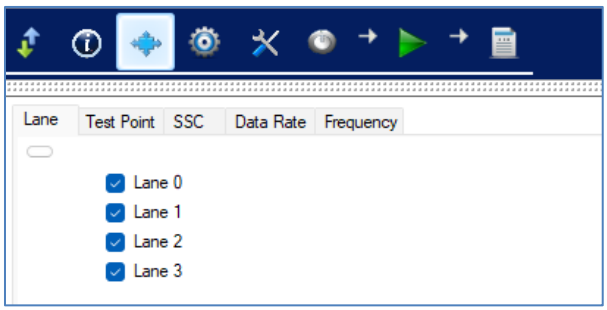


FIGURE 8. SELECT LANE UNDER TESTS

b) **Test Point tab**: Select the test points for calibration and testing.

Note:

- *'TP2 CTLE Long' and 'TP2 CTLE Short' represent the TP2_CTLE test points for Long and Short Channel measurements of the HBR3 Tethered cable respectively.*
- *For the DP Sink Device, select only the TP3 test point for the RBR, HBR and HBR2 data rates. For the HBR3 data rate, select the TP3, TP2 and TP2 CTLE Short test points.*
- *For the Tethered Device, select the TP2, TP2 CTLE Long and TP2 CTLE Short test points.*

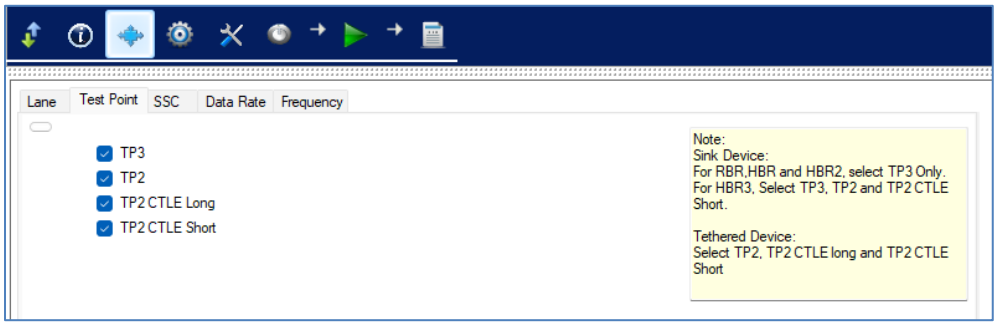


FIGURE 9. SELECT TEST POINTS

c) **SSC tab**: Select to enable or disable SSC Capability supported by the DUT for testing.

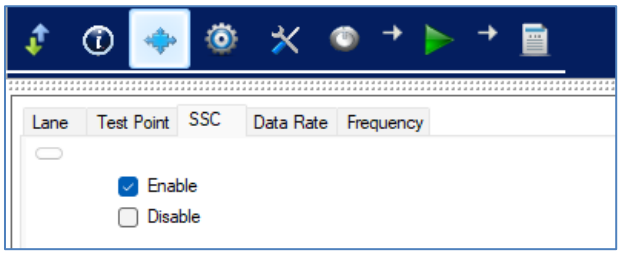


FIGURE 10. SELECT SSC CONDITION

d) **Data Rate tab**: Select the desired data rates for calibration or testing.

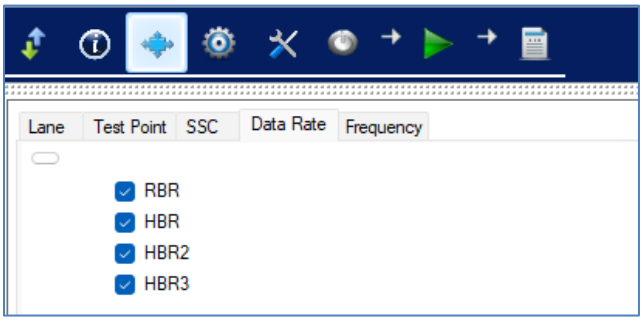


FIGURE 11. SELECT DATA RATES

e) **Frequency** tab: Select the desired SJ frequencies for calibration or testing.

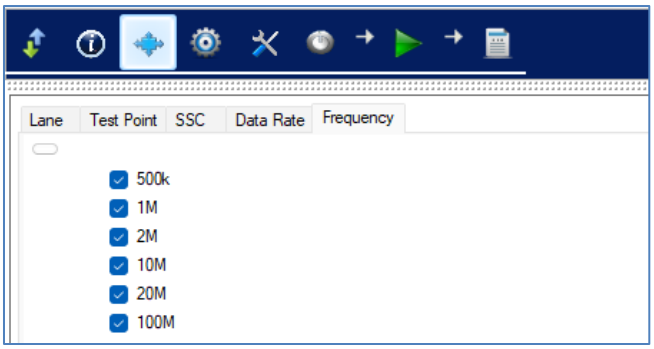


FIGURE 12. SELECT SJ FREQUENCIES

4.2.3 Setup Configuration for Testing and Calibration

Select  from the menu to access the Setup Configuration page to configure the necessary settings prior to running tests or calibration.

4.2.3.1 Test Mode Tab

Select to apply the Standard DisplayPort or 2+2 Alternate Mode test mode for calibration or testing.

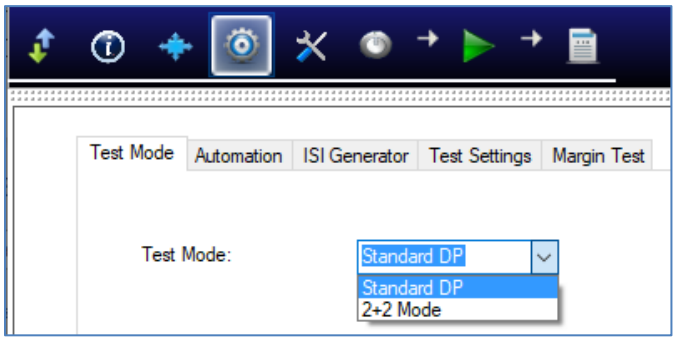


FIGURE 13. SELECT TEST MODE

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4.2.3.2 Automation Tab

Select to use the Tektronix DP Aux Controller or Unigraf DPT-200 Aux Controller in the calibration or test setup. Select 'None' if not using an Aux Controller. Then enter the COM port number of the connected Aux controller.

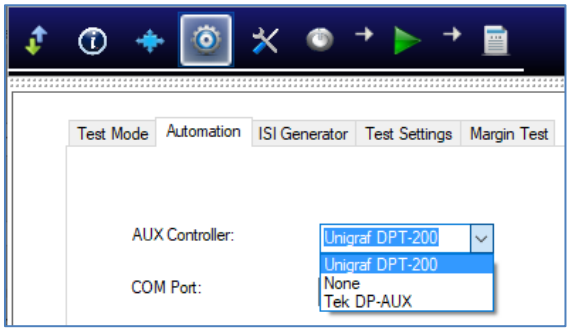


FIGURE 14. SELECT AUX CONTROLLER

4.2.3.3 ISI Generator Tab

Select the ISI Generator to be used in calibration or testing.

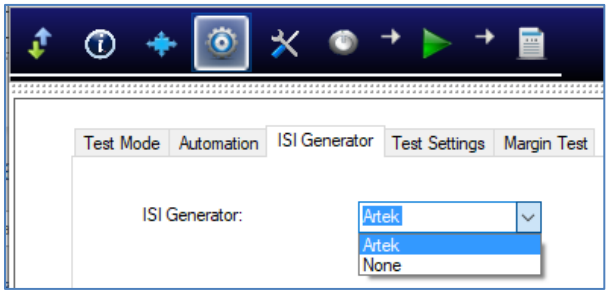


FIGURE 15. SELECT ISI GENERATOR

4.2.3.4 Test Settings Tab

Select the Symbol Lock Pattern. *(Note: It is suggested to start with TPS2.)* Also select the HBR2 Compliance Pattern and choose the option to enable the ESI Register.

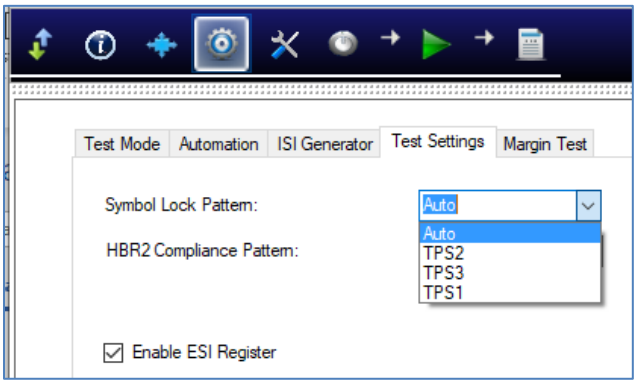


FIGURE 16. CONFIGURE TEST SETTINGS

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4.2.3.5 Margin Test Tab

Configure the Search Mode Jitter Tolerance parameters for marginal testing. Also select the option to use binary search and/or receive prompts to reset the DUT as required during testing.

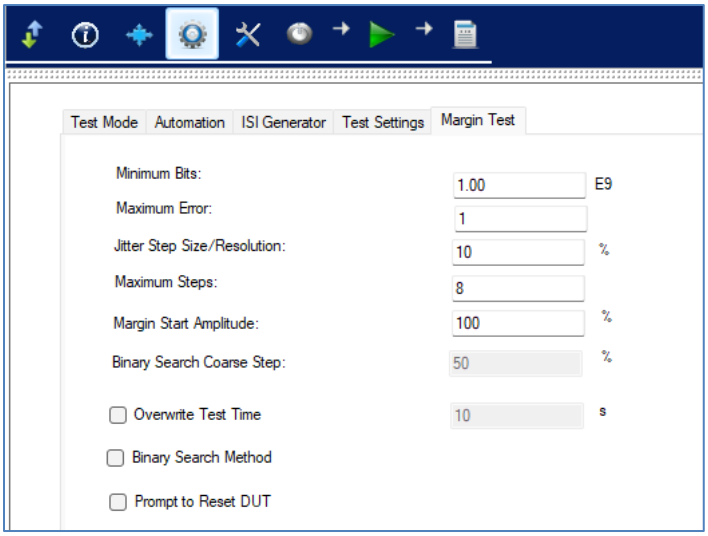


FIGURE 17. CONFIGURE MARGIN TEST PARAMETERS

4.3 Calibration/Test Selection Page

Go to the **Select Tests** page on the left of the screen to select the available calibration or tests to be performed. Select the check box(s) of the desired calibration/test.

Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Sink Tests will show an error message.

Note: For calibration/testing, it is recommended to use a Variable ISI channel as it allows the channel to be more easily adjusted to meet the required specification. The application supports automated control of the ARTEK CLE1000-A2 variable ISI generator.

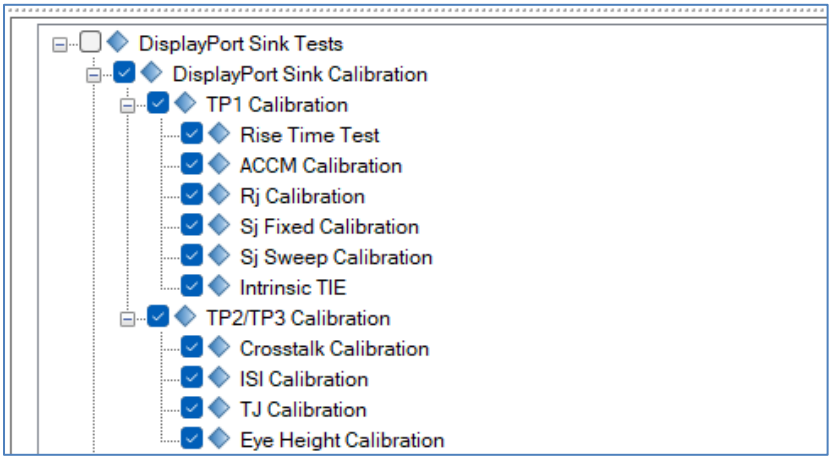


FIGURE 18. CALIBRATION SELECTION

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Select the calibration groups to perform calibration for all DisplayPort Sink parameters. Note that while user can select individual calibration parameters, it is possible that a particular calibration may require the previous calibration to be completed before it can proceed. Thus, it is advisable to complete all previous calibration before going on to the next calibration.

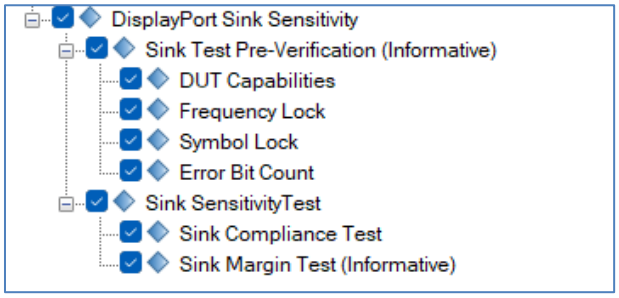


FIGURE 19. TESTS SELECTION

Select the test groups to perform DUT compliance tests for all DisplayPort Sink parameters.

Note: The Sink Test Pre-Verification group is optional which when selected, performs "pre-test" link training before running the actual tests. These pre-verification tests are carried out mainly for debugging purposes and will not include any jitter tolerance testing.

4.4 Calibration/Test Parameters Configuration Page

Select  from the menu to access the Configurations page. Set the required parameters for Sink calibration and testing as described in Table 3 below.

To return all parameters to their default values, select the 'Set Default' button.

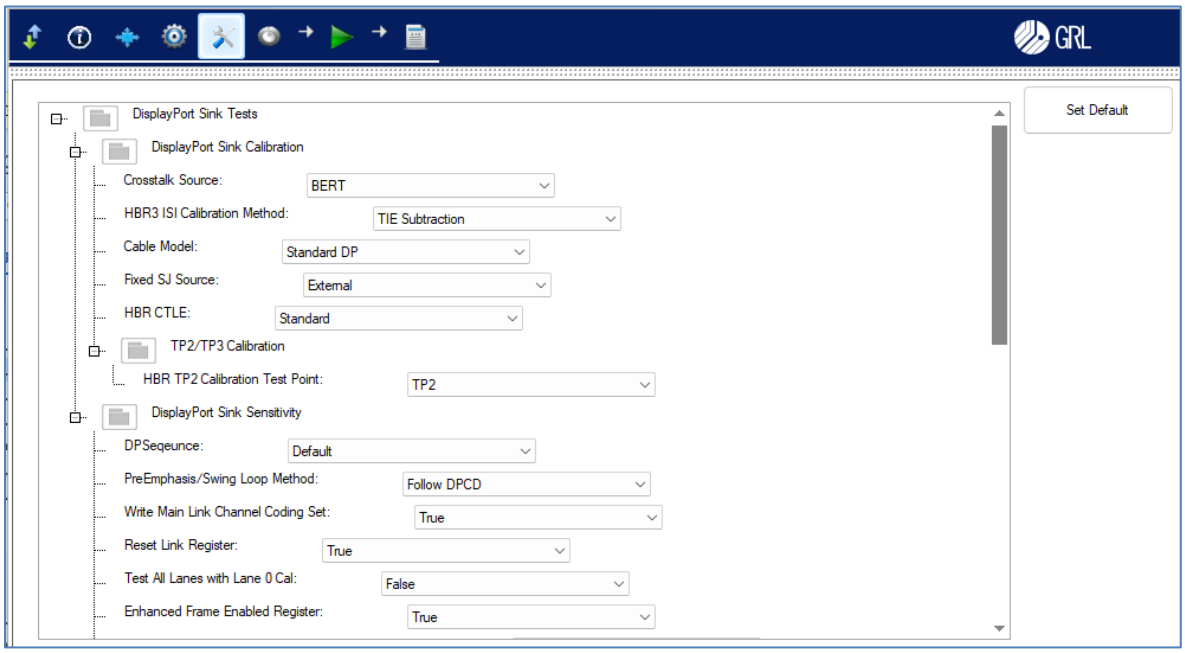
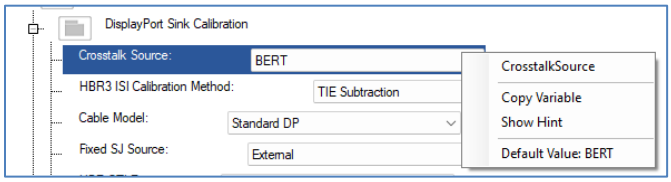


FIGURE 20. PARAMETERS CONFIGURATION PAGE

Note that the user can right-click on each parameter value to:

- display and copy the property variable,
- display the Hint property which will show contextual help about forms, controls and other screen objects,
- copy and paste the value (only applicable for the text input field), or
- set the value to default.

Examples as shown below:



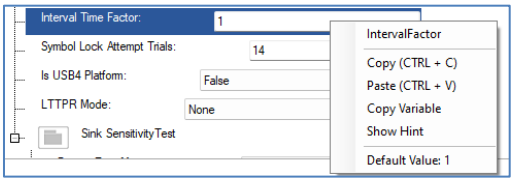


TABLE 3. CALIBRATION/TEST PARAMETERS DESCRIPTION

Parameter Name	Description
Crosstalk Source	The **MP1900A BERT** will be used to generate crosstalk.
HBR3 ISI Calibration Method	Select whether to use the **TIE Subtraction** or **DDJ** method to calibrate ISI for HBR3 data rate.
Cable Model	Select whether to use a **Standard** DisplayPort cable or a **Type-C** cable type for calibration.
Fixed SJ Source	Select whether to use **Internal** Fixed SJ source or **External** source or **Manual** inject jitter source for calibration.
HBR CTLE	Select whether to use the **Standard** HBR Reference EQ or **Enhanced** HBR CTLE EQ.
HBR TP2 Calibration Test Point	Select whether to use **TP2** or **TP3_EQ** test point for calibrating for the HBR data rate.
DP Sequence	Select the DisplayPort version to be used.
PreEmphasis/Swing Loop Method	Select whether to use the **Incremental** or DisplayPort Configuration Data (**DPCD**) register method for adjusting the Pre-emphasis and Swing voltage.
Write Main Link Channel Coding Set	Set to **True** or **False** to write the signal coding of the main link lane channel configuration.
Reset Link Register	Set to **True** or **False** to perform link register reset during testing.
Test All Lanes with Lane 0 Cal	Set to **True** or **False** to use the calibrated Lane 0 values to test for all lanes under test.

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Enhanced Frame Enabled Register	Set to **True** or **False** to enable the Enhanced Frame bit in the DPCD register.
TPS1/TPS2/TPS3/PRBS/CPAT Scrambling Disable	Set to **True** or **False** to disable data symbol scrambling of the TPS1/TPS2/TPS3/PRBS/CPAT training pattern for D10.2, RBR, HBR and HBR2 devices.
TPS4 Scrambling Disable	Set to **True** or **False** to disable data symbol scrambling of the TPS4 training pattern for HBR3 devices.
Freq/Symbol Lock Training Pattern Register	Write the training pattern value to **TRAINING_PATTERN_SET** or **LINK_QUAL_PATTERN_SET** or write both addresses.
Training Pattern Select	Select the **default** or a **specific training pattern type** to be applied when testing a specific data rate.
Initialize Training Lane Set	Set to **True** or **False** to reset HDCP register(0x102) before sending a training pattern.
Ignore Error Count Mismatch	Set to **True** or **False** to ignore any differences in the error counts obtained during testing.
RBR/HBR Test Pattern	Select the test pattern **PRBS7**, **TPS2** or **TPS3** for testing with RBR and HBR data rate.
Invert PRBS7	Set to **True** or **False** to invert the PRBS7 test pattern.
Reset Training Pattern on Fail Error Count	Set to **True** or **False** to reset the training pattern when the “Error Count” of the Sink is determined to have failed the test.
Always Initialize BERT	Set to **True** or **False** to bypass BERT initialization during testing.
Skip Link Training When SJ Frequency Changed	Set to **True** or **False** to skip the loopback link training sequence when there is a change in the SJ frequency.
Skip Link Training When SJ Amplitude Changed	Set to **True** or **False** to skip the loopback link training sequence when there is a change in the SJ amplitude.
Interval Time Factor	Specify the factor value for bit errors to be counted over a specified time interval.
Symbol Lock Attempt Trials	Set the number of attempts to execute the symbol lock phase.
Is USB4 Platform	Set to **True** or **False** if the Sink DUT runs on a USB4 based platform.
LTTPR Mode	Select the Link-Training Tunable PHY Repeater (LTTPR) operating mode (**Transparent** or **Non-Transparent**) if supported by the Sink DUT.
Prompt Error Message	Set to **True** or **False** to enable or disable the GRL-DP14-SINKAN

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	software to show error messages for failed or incomplete tests respectively.

4.5 Calibration Target Configuration Page

For debugging purposes ONLY, the default calibration target values can be changed for certain calibration. To do this, select  from the menu to access the Calibration Target page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the 'Use Default Value' checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

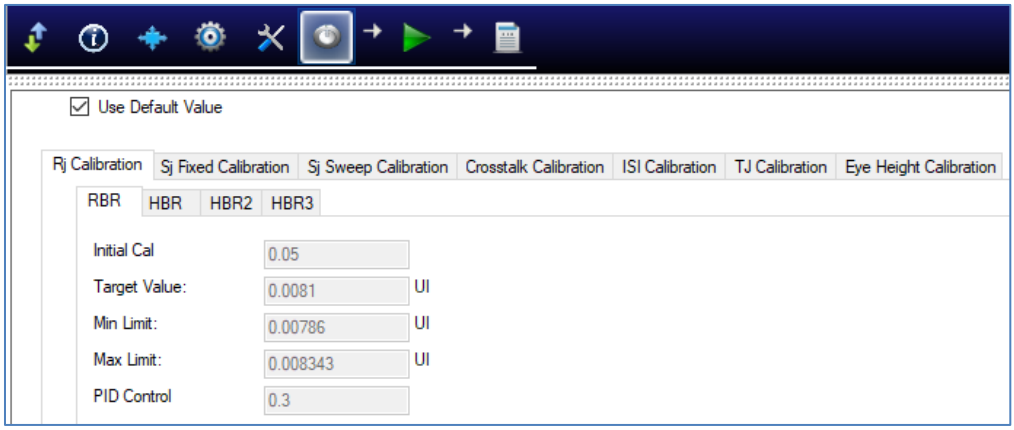


FIGURE 21. CALIBRATION OVERWRITE

4.6 Running Calibration/Tests

Select  from the menu to access the Run Tests page. The GRL software automatically runs the selected calibration or tests when initiated.

Before running the calibration or tests, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration/tests exist, the software will *skip* those calibration/tests.
- **Replace if Result Exists** – If results from previous calibration/tests exist, the software will *replace* those calibration/tests with new results.

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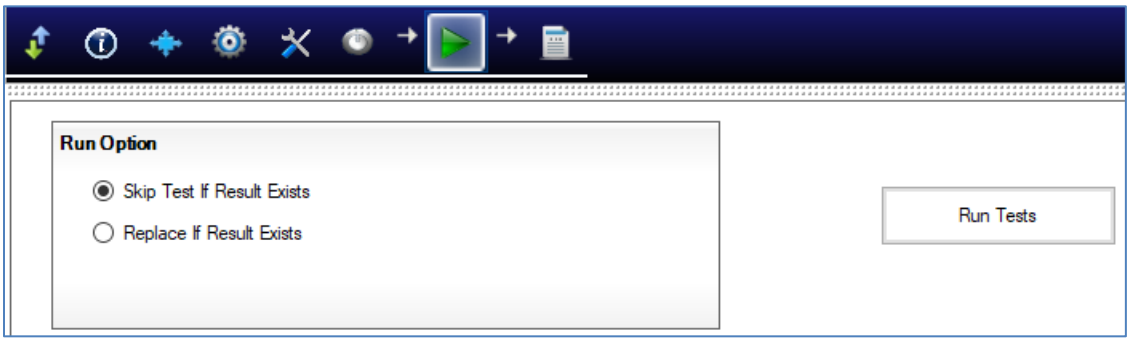


FIGURE 22. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration or tests. The connection diagram for the calibration or test being run will initially appear to allow the user to make sure that the calibration/test environment has been properly set up before calibration/test can proceed.

If you need to re-run only certain calibration or tests on certain conditions, please delete the calibration or tests from the Report page and Run with **Skip Test if Result Exists**. The GRL software will keep track of the missing calibration or tests in the report and perform those calibration or tests only. See Section 7 for more information on Test Reports.

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5 Sink Calibration Setups

This section shows the typical connection setups to perform automated Sink Test Calibration.

5.1 Pre-Calibration/Test Procedures

Prior to running any calibration or test, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for the Oscilloscope and MP1900A BERT.
2. Run the Scope's SPC calibration routine. It is necessary to remove all probes from the Scope before running SPC.
3. Make sure you use a torque wrench with the proper torque specification to make all SMA connections.

5.2 Calibration Connection Setups

Note: Using a Variable ISI Generator enables calibration to be performed with minimum reconfiguration of the test setup, which allows testing to be more fully automated.

5.2.1 Calibration Setup at TP1

Figure 23 below shows the typical setup for Sink signal calibration at Test Point 1.

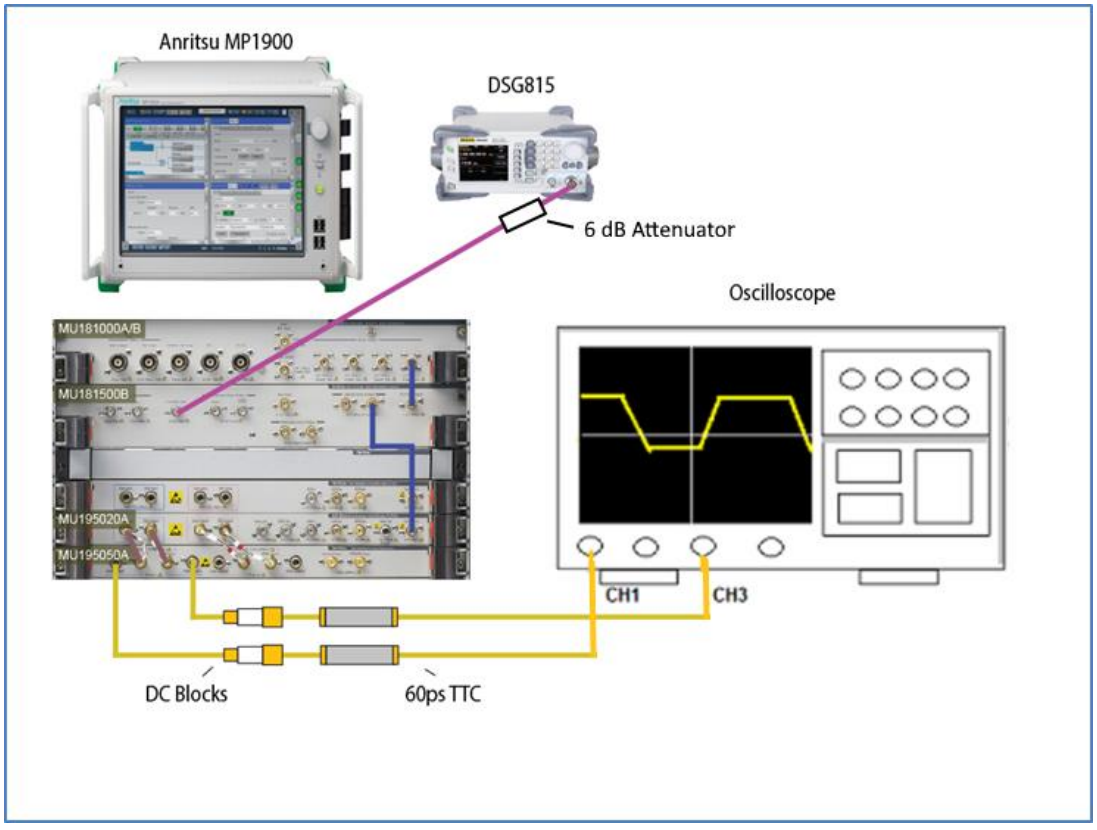


FIGURE 23. TYPICAL TP1 SINK CALIBRATION SETUP

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Set up the equipment as shown in the above diagram. Connect the DATA Outputs of the MP1900A BERT to Channels 1 and 3 of the Oscilloscope.

5.2.2 Calibration Steps at TP1

The following table summarizes the DP1.4 PHY CTS steps and calibration target values for each data rate at TP1.

Calibration Step	Unit	HBR3	HBR2	HBR	RBR
Rise Time (20-80) [a]	ps	40	NA	NA	NA
TTC Value (10-90)	ps	60	60	60	60
Pattern		256 Bit Clock	NA	NA	NA
ACCM Calibration (pk-pk)	mV	100	NA	NA	NA
ACCM Pattern		Sine	NA	NA	NA
Frequency	MHz	400	NA	NA	NA
RJ Calibration (Amplitude RMS)	mUI	13	16.7	13.5	8.1
RJ Pattern		D24.3	D24.3	D24.3	D24.3
SJ Fixed Calibration (Amplitude pk-pk)	mUI	130	80	NA	NA
SJ Fixed Pattern		D24.3	D24.3	NA	NA
SJ Fixed Frequency	MHz	297	297	NA	NA
SJ Sweep Calibration					
SJ Sweep Pattern		D24.3	D24.3	D24.3	D24.3
0.5 MHz SJ (Amplitude pk-pk)	mUI	NA	NA	6951	13000
1 MHz SJ (Amplitude pk-pk)	mUI	NA	NA	1722	3751
2 MHz SJ (Amplitude pk-pk)	mUI	1013	505	904	981
10 MHz SJ (Amplitude pk-pk)	mUI	137	116	225	111
20 MHz SJ (Amplitude pk-pk)	mUI	109	104	182	80
100 MHz SJ (Amplitude pk-pk)	mUI	100	100	168	NA
SJ Sweep Calibration					
Intrinsic ISI Pattern		TPS4	NA	NA	NA
TP1 TJ Calibration	mUI	430	NA	NA	NA
TP1 Eye Height Calibration	mV	280	NA	NA	NA

[a] *If testing only bit rates HBR2 and lower, Rise/Fall time is not calibrated and 60 ps (10-90) TTC's are not required.*

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5.2.3 Calibration Setup at TP2/TP3

Figure 24 below shows the typical setup for Sink signal calibration at Test Point 2 or 3 using the MP1900A BERT as the crosstalk source.

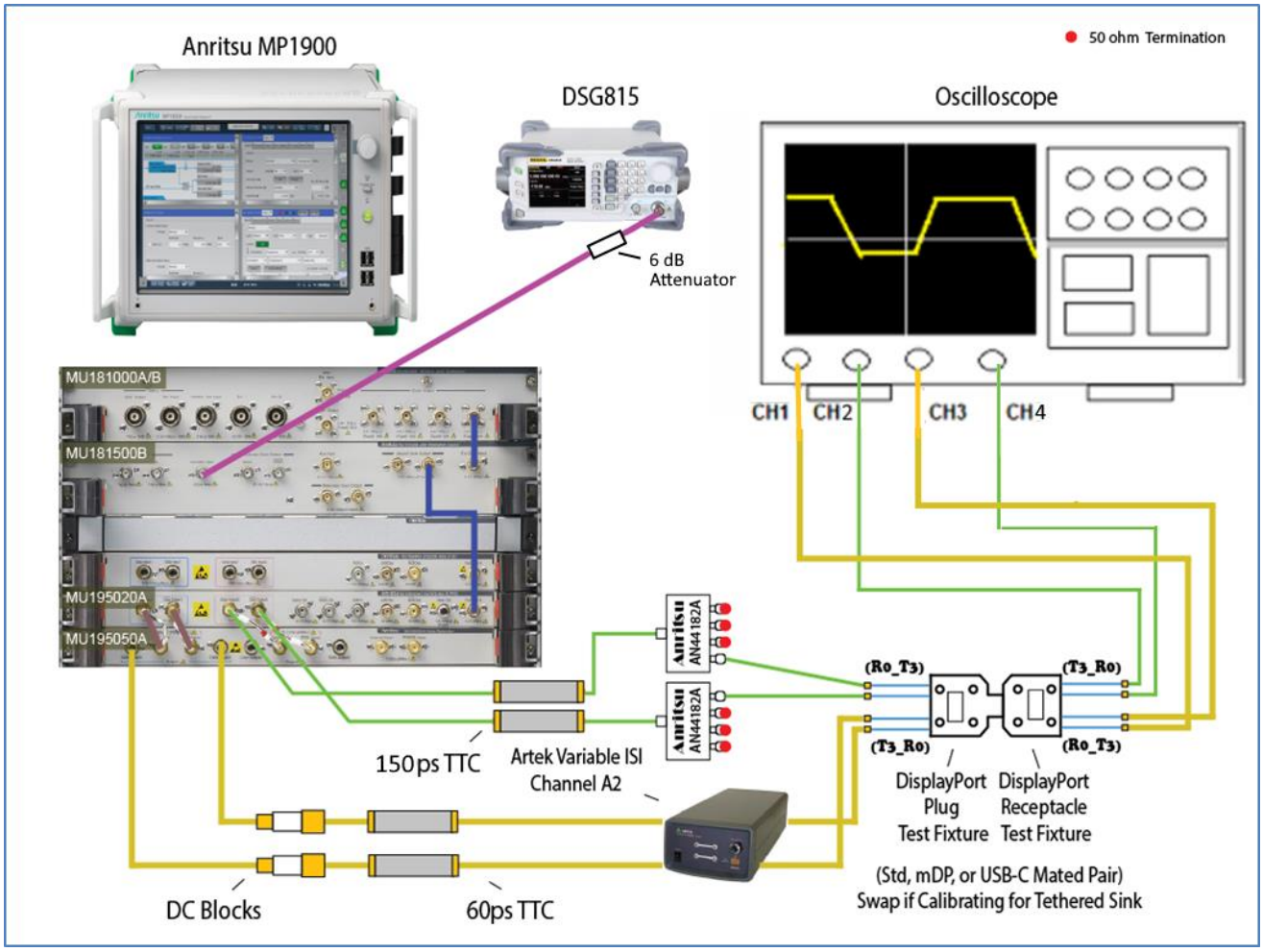


FIGURE 24. TYPICAL TP2/TP3 SINK CALIBRATION SETUP

Set up the equipment as shown in the above diagram. Connect the Clock Outputs of the MP1900A BERT to the DisplayPort fixture and Scope. Connect the ISI Output to the selected Lane of the DisplayPort fixture and Scope.

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5.2.4 Calibration Steps at TP1, TP2 and TP3

The following table summarizes the DP1.4 PHY CTS steps and calibration target values for each data rate at TP1, TP2 and TP3.

Calibration Step	Unit	HBR3	HBR2	HBR	RBR
Crosstalk	mV	300	300	450	138
Pattern	-	D24.3	D24.3	D24.3	D24.3
TTC Value (10-90)	ps	150	150	150	150
ISI & TJ Data Pattern	-	TPS4	CP2520	PRBS7	PRBS7_X2
TP3 & TP3_EQ ISI Calibration	mUI	240	220	161	570
Specified Test Point [a]	-	TP3_CTLE	TP3_EQ	TP3_EQ	TP3
TP3_CTLE and TP3_EQ TJ Calibration [b]	mUI	600 [c]	600	471	NA
TP3_CTLE, TP3_EQ, and TP3 Eye Height Calibration	mV	50 [c]	100	150	56
TP2 ISI Calibration	mUI	120	NA	144	60
Specified Test Point [d]	-	TP2_CTLE	TP2	TP2	TP2
TP2_CTLE TJ Calibration	mUI	480	NA	NA	NA
TP2_CTLE Eye Height Calibration	mV	170 [c]	NA	NA	NA
TP2_CTLE Short Channel [e]	mVpp	250	NA	NA	NA
TP2_CTLE Long Channel [e]	mVpp	170	NA	NA	NA

[a] Notes about TP3 ISI Calibration:

- *RBR ISI is measured directly without equalizer function applied.*
- *HBR and HBR2 are measured at TP3 with equalizer function in the scope for single TP3_EQ function in the spec.*
- *HBR3: TP3_CTLE calibration shall be done using CTLE curve with -8 dB Adc. Physical measurement of the end-to-end ISI should be made to verify that it is within 22 to 24 dB insertion loss, including all cables, fixtures, and DC blocks.*

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[b] *HBR3: SJ_{FIXED} is adjusted during calibration to achieve target TJ. TJ measurement for HBR2, HBR, or RBR is not performed directly. It is achieved by summation of measured jitter components.*

[c] *Eye Height Calibration target of 50 mV @TP3_CTLE or 250 mV @TP2_CTLE is achieved without crosstalk applied and will be reduced to approximately 40mV or 240mV respectively with crosstalk applied. HBR3 TJ is measured at TP3_CTLE after the PLL transfer function over 10^{-6} BER.*

[d] *Notes about TP2 ISI Calibration:*

- *RBR and HBR ISI are measured directly at TP2 without equalizer function applied.*
- *HB2 is measured with embedded S-parameter of HBR2 WC cable in place of HW ISI. This results in proper ISI being calibrated at TP2 when calibration fixture is removed.*
- *HBR3: TP2_CTLE calibration shall be done using CTLE curve with -4dB Adc.*

[e] *Notes about TP2_CTLE Short/Long Channel Eye Height Calibration:*

- *Only applicable for the HBR3 Tethered cable DP Sink Device to be measured at TP2_CTLE.*
- *Below shows the CTS illustrated typical test setups for both Long and Short Channels.*
- *The Long Channel receiver for a tethered DP Sink device is tested to determine if the receiver can operate correctly with reduced amplitude signals due to a lossy source channel.*
- *The Short Channel receiver for a tethered DP Sink device is tested to determine if the receiver can operate correctly with a larger amplitude signal presented to the system connector.*

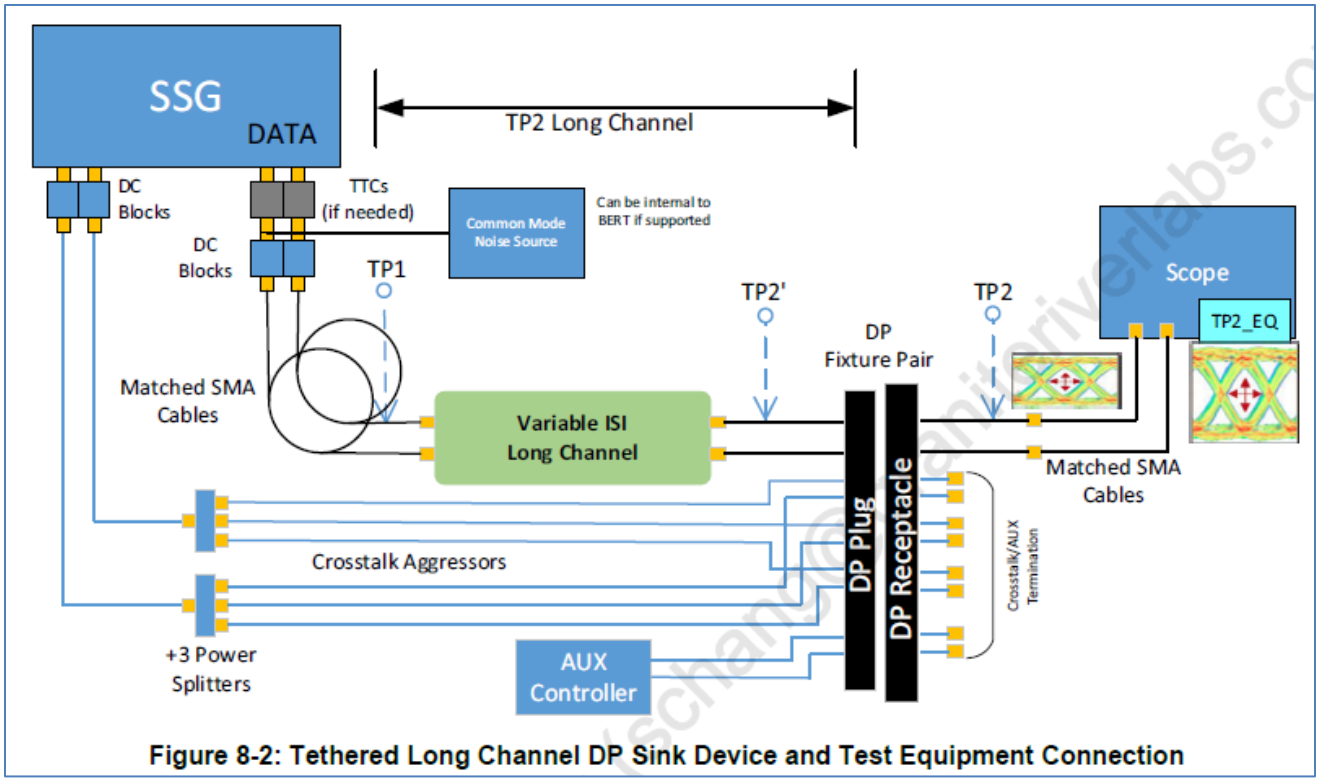


Figure 8-2: Tethered Long Channel DP Sink Device and Test Equipment Connection

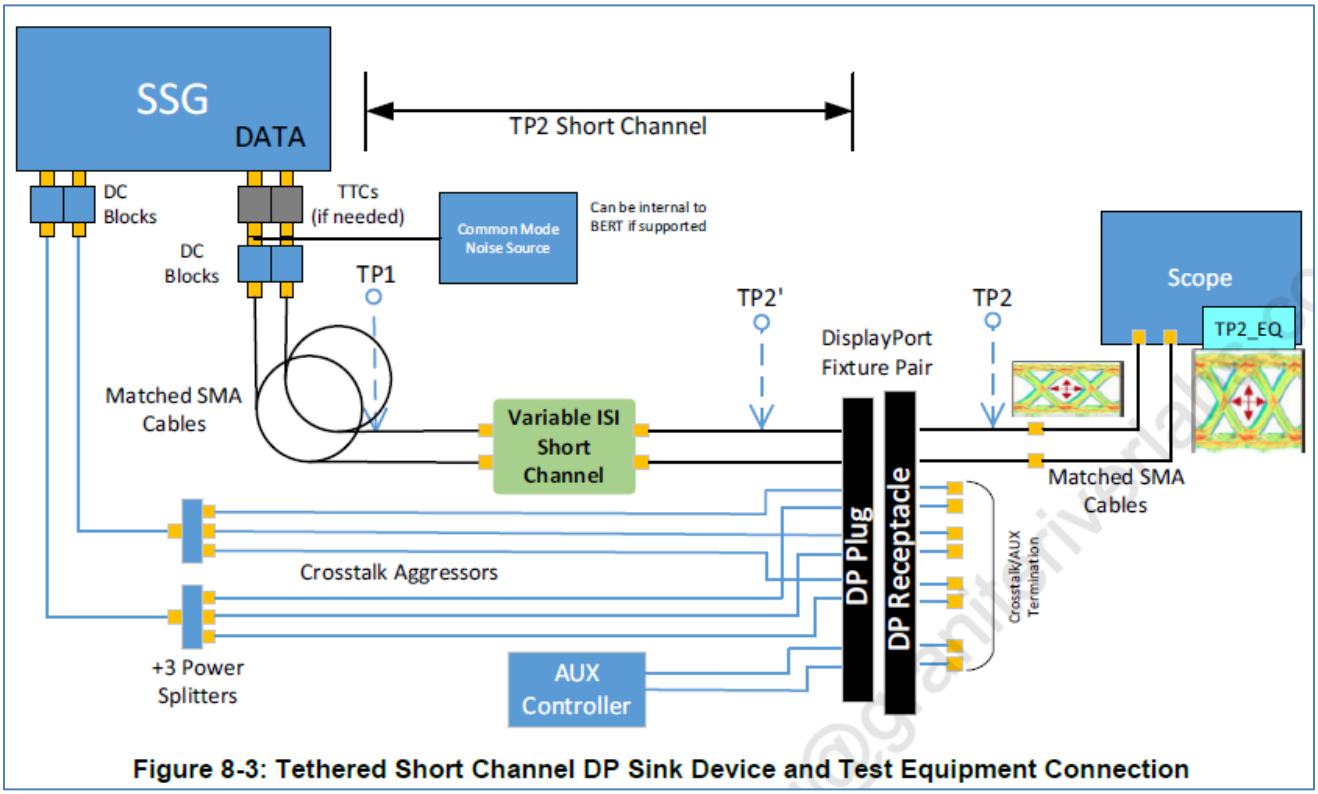


Figure 8-3: Tethered Short Channel DP Sink Device and Test Equipment Connection

5.3 Saving Calibrated Signals

The application will save calibration files of calibrated stressed signals when running the calibration sequence. For example, on the MP1900A BERT, the application will save the final configuration for LANE0-HBR2 to a file called *EYEHEIGHTCALIBRATION_LANE0__HBR3.CND*.

This is the basic calibration file that will be recalled during testing.

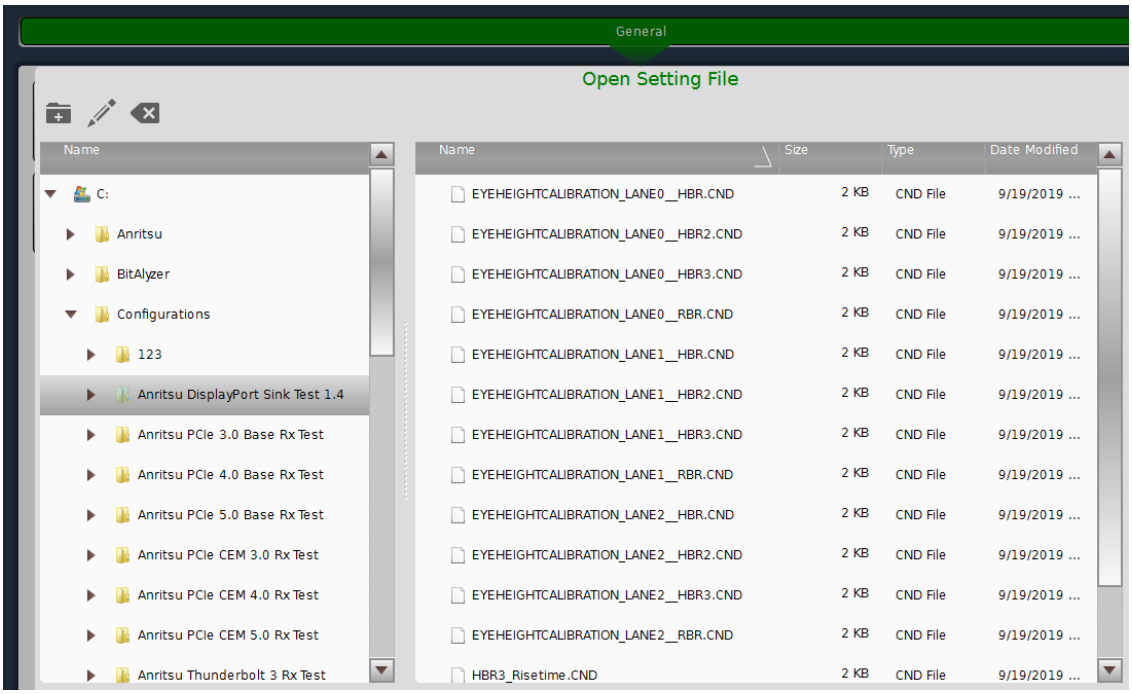


FIGURE 25. SAVED CALIBRATION FILE EXAMPLE

On the PC or Scope running the GRL application, a *calibration.cal* file will be created that contains the stored calibration values for each frequency that was calibrated.

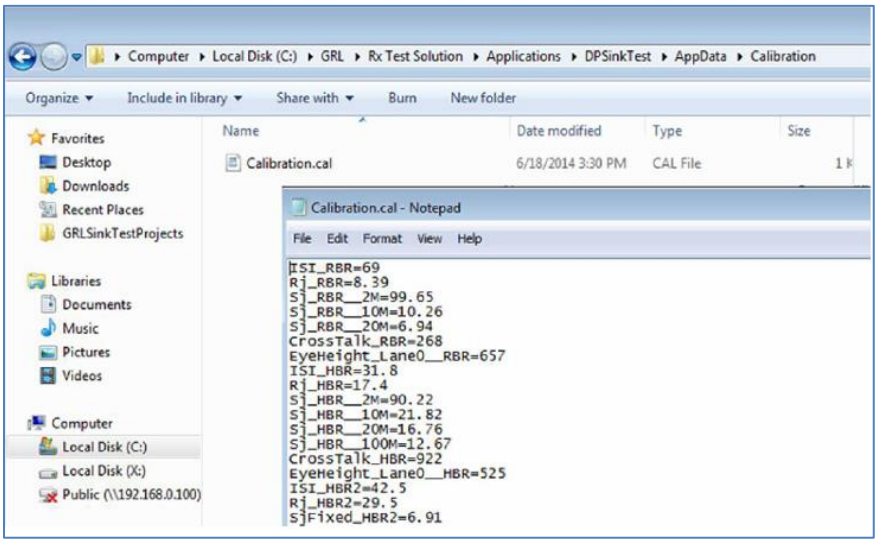


FIGURE 26. CALIBRATION.CAL FILE EXAMPLE

6 Sink DUT Compliance Test Setups

After calibration has completed, then testing the DisplayPort Sink DUT for CTS compliance can be performed. The GRL application supports automated testing of a DisplayPort Sink device if the device supports standard DPCD through the AUX channel. *Note: The Aux controller is required for testing.*

6.1 Test Connection Setups

6.1.1 DUT Jitter Tolerance Compliance Test Setup

Figure 27 below shows the physical setup for the DisplayPort Sink DUT jitter tolerance test using the MP1900A BERT as the crosstalk source.

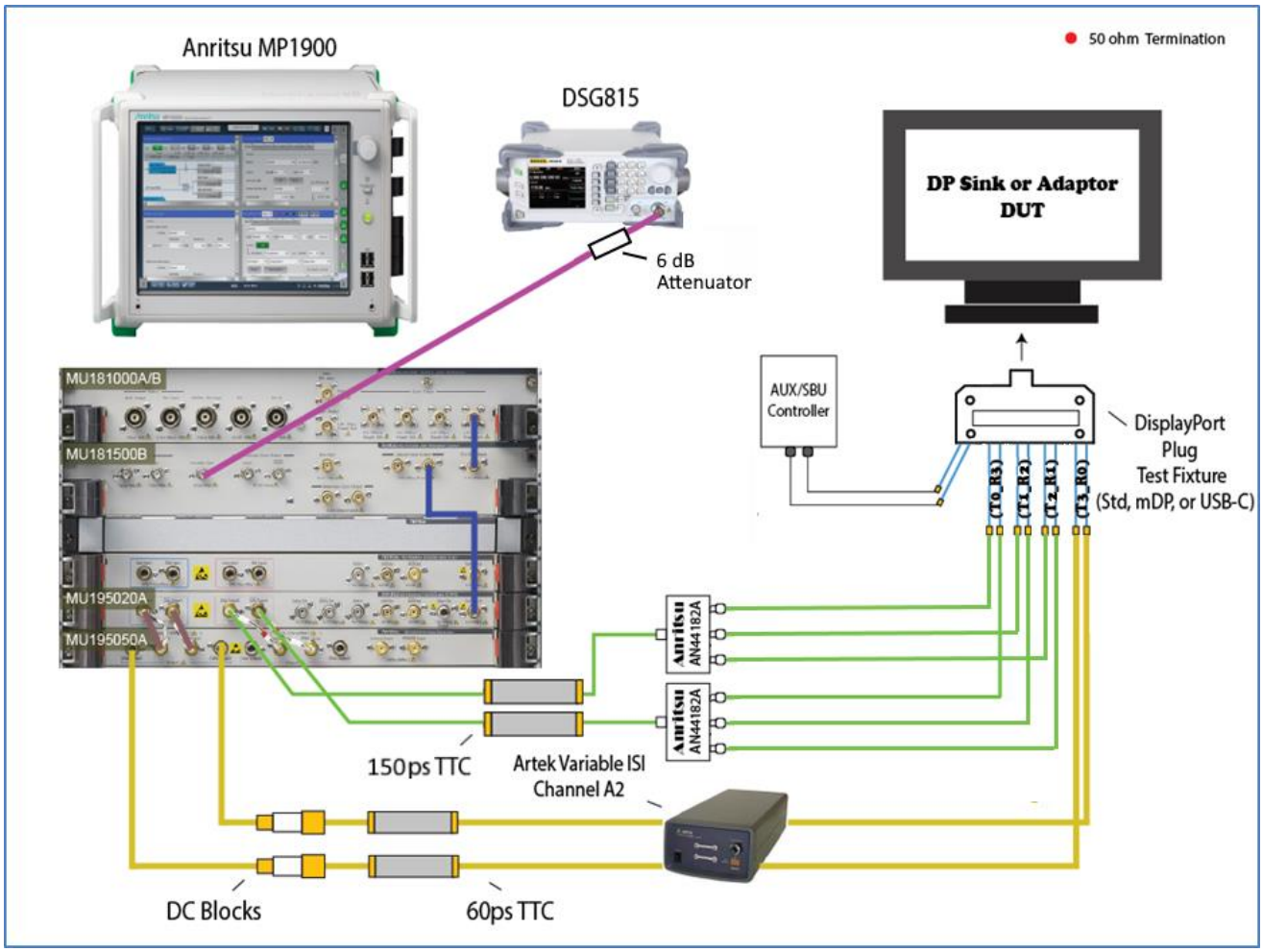


FIGURE 27. COMPLIANCE TEST SETUP FOR DP SINK DUT JITTER TOLERANCE

Set up the equipment as shown in the above diagram. Disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing. Change the connection from the ISI Output to the selected Lane under test of the DisplayPort fixture.

Note: If the Unigraf DPT-200 Aux controller is used, an additional DP-Cable to AUX-SMA adapter is required. The Tektronix DP-AUX is connected directly to the DUT via SMAs. Both Aux control solutions have USB connection and drivers that need to be loaded on the Computer being used for the testing.

General procedure to perform testing using the application:

a) Select the "Sink Test Pre-Verification" test group to perform pre-test link training on the DUT. The tests under this group will train the DUT into test mode for receiver testing. This is mainly performed for debugging purposes. *Note: Any individual test from the group is also allowed to be selected as desired.*

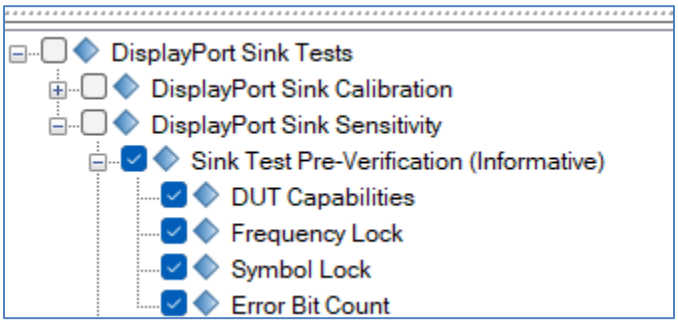


FIGURE 28. SINK TEST PRE-VERIFICATION SELECTION

DUT Capabilities	Lists the DUT capabilities in the Results window under the Report page.
Frequency Lock	Loads the Frequency Lock pattern on the MP1900A BERT and verifies the Frequency Lock.
Symbol Lock	Loads the Symbol Lock pattern on the MP1900A BERT and verifies the Symbol Lock.
Error Bit Count	Sends a random number of errors (1 to 5) from the MP1900A BERT to the DUT, which then checks the DUT's error count registers and confirms that the error counter is working correctly.

b) Select the "Sink Compliance Test". The GRL application will perform link training followed by running the jitter tolerance compliance test at selected frequencies.

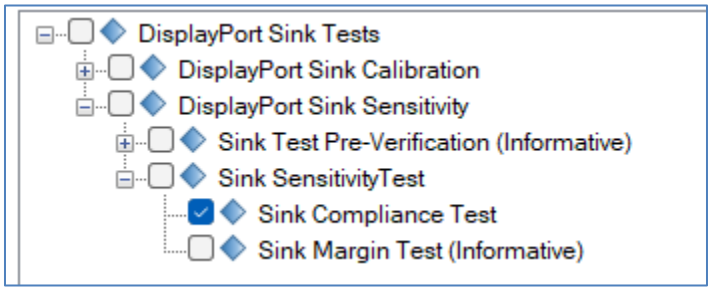


FIGURE 29. SINK COMPLIANCE TEST SELECTION

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Note: If running only a specific test, select only that test, e.g., Sink Compliance Test. If other tests/calibration that come before the desired test are selected, the application will complete those tests first following the sequence before running the desired test.

c) Below shows the required test parameters for BER measurement from the CTS.

Table 4-3: BER Measurement Test Parameters

Jitter Frequency (MHz)	Number of Bits	Maximum Number of Allowable Bit Errors	Bit Rate	Observation Time (Seconds)[a]	Data Rate Offset
2	10^{12}	1000	HBR3	123	0
			HBR2	185	
			HBR	370	
			RBR	620	
10	10^{11}	100	HBR3	13	+350ppm
			HBR2	19	
			HBR	37	
			RBR	62	
20	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	
			RBR	62	
100	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	

a. To evaluate, the number of bits shall be multiplied by the unit interval (UI) in picoseconds (e.g., for HBR, 10^{11} bits at HBR = 370ps/UI × 10^{11}UI = 37 seconds).

FIGURE 30. TEST PARAMETERS FOR BER MEASUREMENT

d) Once testing is completed, repeat the test for each Lane supported by the DUT.

Note: The link width and highest supported Link Frequency are determined by selecting "DUT Capabilities" under Sink Test Pre-Verification and then running the test.

Note: As DUTs may behave differently during testing, it is recommended to always reset the DUT before each test sequence.

6.1.2 Margin Testing

While it is sufficient to perform the Compliance Test for each test condition to meet compliance specifications, it is also useful to determine how much Margin your design contains.

The Margin for each test condition can be verified as follows:

a) Under the Setup Configuration page, select the **Margin Test** tab.

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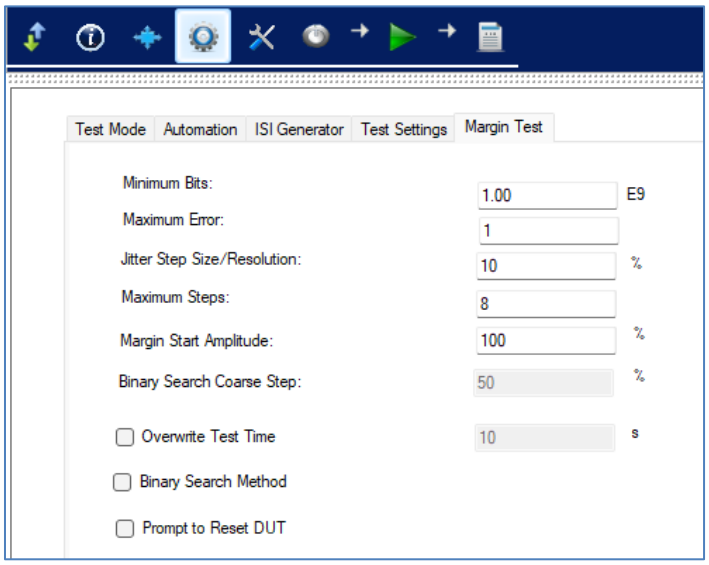


FIGURE 31. MARGIN TEST CONFIGURATION

b) For the desired Link Rate and Frequency pair, configure the following parameters:

- **Minimum Bits**: Minimum number of bits tested at each SJ amplitude.
- **Maximum Error**: Maximum number of errors allowed at each swept-SJ amplitude.
- **Jitter Step Size/Resolution**: The swept-SJ amplitude will increase by the selected amplitude during testing. For example, if the initial swept-SJ is 100mUI, then the test points would be 100mUI, 120mUI, 140mUI, 160mUI, etc.
- **Maximum Steps**: Maximum number of steps to be implemented for margin testing.
- **Margin Start Amplitude**: Start amplitude for margin testing.
- **Binary Search Coarse Step**: Select the "Binary Search Method" checkbox to set the coarse step value for binary search.

c) Once configured, select and run the "Sink Margin Test" for the selected Link Rate/Frequency pair.

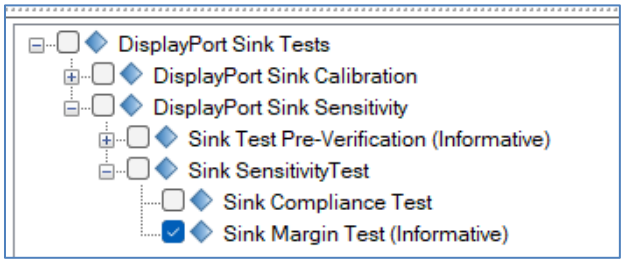


FIGURE 32. SINK MARGIN TEST SELECTION

Note: If running only a specific test, select only that test, e.g., Sink Margin Test. If other tests/calibration that come before the desired test are selected, the application will complete those tests first following the sequence before running the desired test.

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7 Test Results and Reports Using GRL-DP14-SINKAN

When all calibration and test runs have completed from the previous section, the GRL-DP14-SINKAN software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

7.1 Test Report Generation

Click the **Generate report** button for the detailed calibration and tests report.

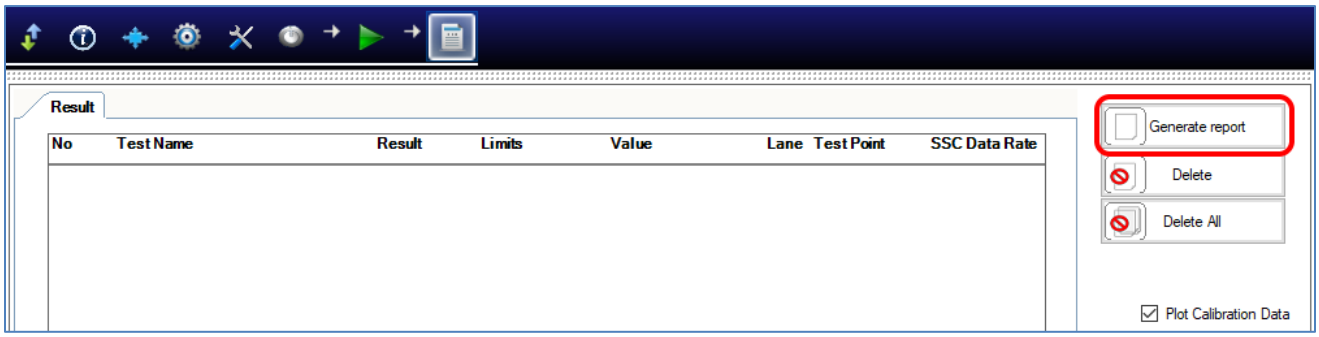


FIGURE 33. GENERATE REPORT PAGE

7.1.1 DUT Information

This portion is populated from the information in the DUT tab on the **Session Info** page.

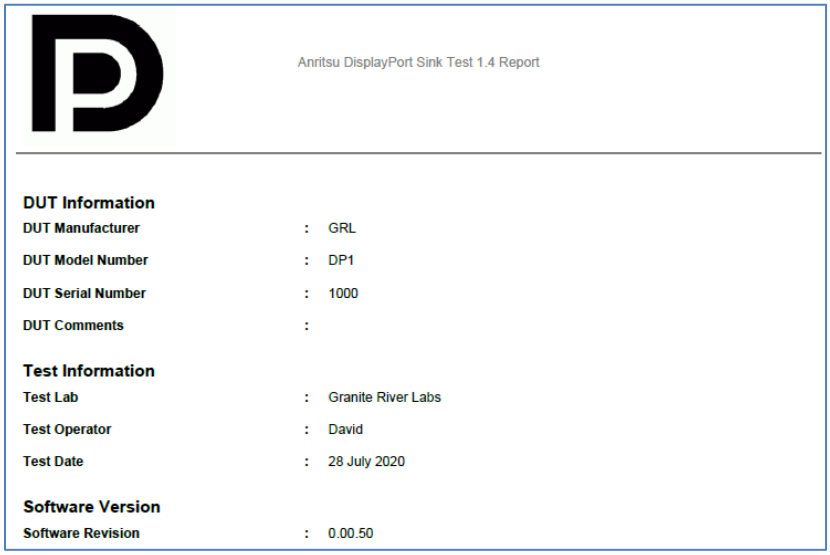


FIGURE 34. DUT INFORMATION

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7.1.2 Summary Table

This portion is populated from the calibration and tests performed, which gives an overall view of all the results and test conditions.

No	TestName	Limits	Value	Results	Lane	Test Point	SSC	Data Rate	Frequency
1	Rise Time Test	True/False	True	Pass	Lane0	TP1		HBR2	2M
2	ACCM Calibration	True/False	True	Pass	Lane1	TP1		HBR3	2M
3	Rj Calibration	True/False	True	Pass	Lane0	TP1	SSC_ON	HBR2	10M
4	Sj Fixed Calibration	True/False	True	Pass	Lane0	TP1	SSC_ON	HBR3	100M

FIGURE 35. SUMMARY TABLE

7.1.3 Test Results

This portion is populated from each of the test results. Here the results are explained in depth with supporting data points and screenshots.

7.1.3.1 Compliance Test

This portion is populated from the results of all compliance tests performed.

Compliance Test(TP2,Enable,HBR2)

Sj Frequency	2M	10M	20M	100M
Lane0	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane1	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane2	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane3	PASS(0)	PASS(0)	PASS(0)	PASS(0)

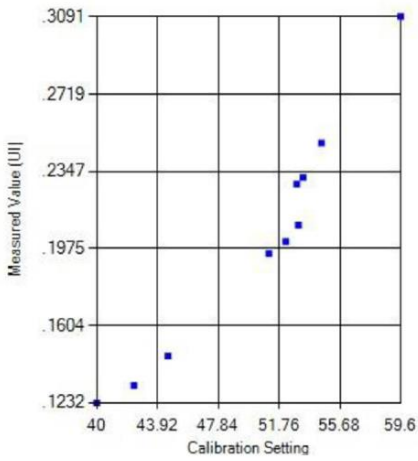
Compliance Test(TP2,Enable,HBR3)

Sj Frequency	2M	10M	20M	100M
Lane0	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane1	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane2	PASS(0)	PASS(0)	PASS(0)	PASS(0)
Lane3	PASS(0)	PASS(0)	PASS(0)	PASS(0)

FIGURE 36. COMPLIANCE TEST RESULTS PAGE

7.1.4 Calibration Data Plots

This portion is populated from each of the calibration steps. Below is an example of an ISI calibration plot showing the calibration points using the ARTEK CLE1000-A2.



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FIGURE 37. CALIBRATION RESULTS PAGE

7.1.5 Margin Test Plots

This portion is populated from the Margin Tests. Below is an example of a margin test plot showing pass results.

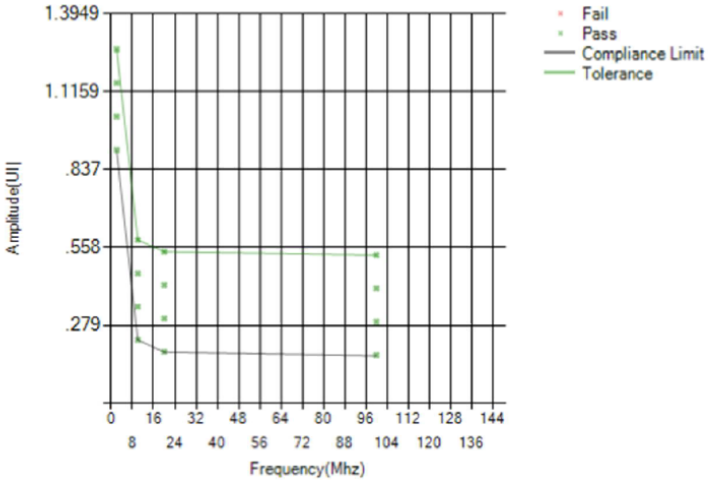


FIGURE 38. MARGIN TEST RESULTS PAGE

7.2 Deleting Test Reports

Click the **Delete** button to delete individual test results or **Delete All** to delete the entire test report.

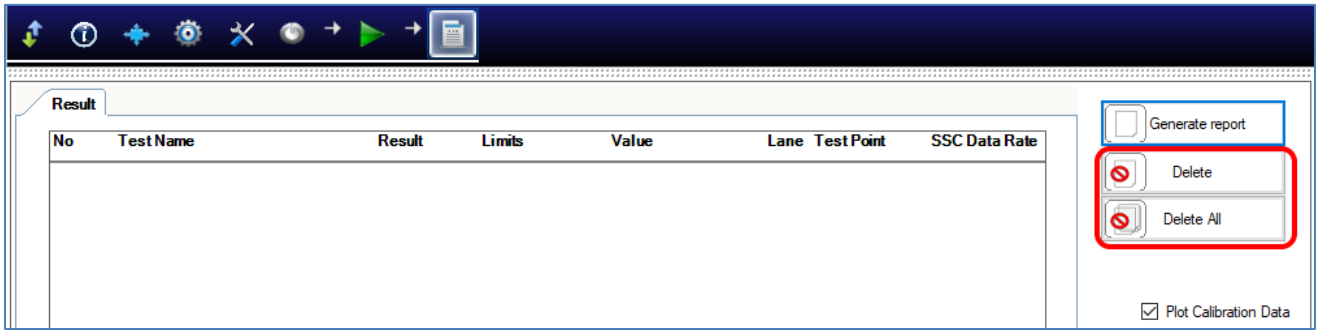


FIGURE 39. TEST REPORT DELETED

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8 Saving and Loading Test Sessions

The usage model for the GRL-DP14-SINKAN software is that Calibration and Test Results are created and maintained as a 'Live Session' in the software. This allows you to Quit the software and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To Save a session, with all of the parameter information, test results, and any waveforms, select **Options** on the menu bar and select **Save Session**.

To Load a session back into the software, including the saved parameter settings, select **Options** on the menu bar and select **Load Session**.

To create a New session and return the software to the default configuration, select **Options** on the menu bar and select **New Session**.

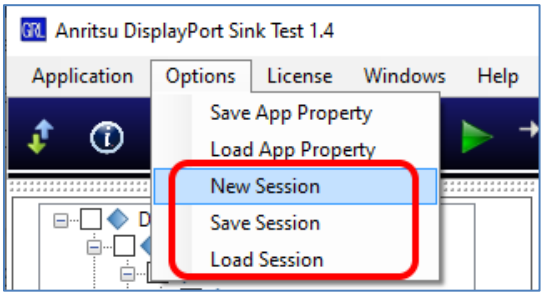


FIGURE 40. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

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9 Appendix A: Manual CTS Sink Calibration and Test Procedure

The DisplayPort PHY CTS outlines the requirements for manual DisplayPort Sink Calibration and Testing in this section.

Note: See Section 3, Resource Requirements for equipment required in the following setups.

9.1 HBR3 Sink Calibration/Test Setup

The following methodology provides a typical example on how to calibrate and test the stressed impairments for HBR3 per the DP CTS. This method will be performed using the Anritsu MP1900A BERT as SSG (Stressed Signal Generator) and the Keysight or Tektronix high performance Oscilloscope (≥ 16GHz) as JMD (Jitter Measurement Device).

Note: This is an early market MOI that may change as the DP1.4 CTS becomes final, however, it will be used to Certify early market DP Sinks per the DP1.4 Best Effort Test Program.

9.1.1 Calibration Setup and Procedure (at TP1)

Calibration for HBR3 will be performed at test points TP1, TP2, and TP3. The following figure shows the conceptual calibration setup at TP1.

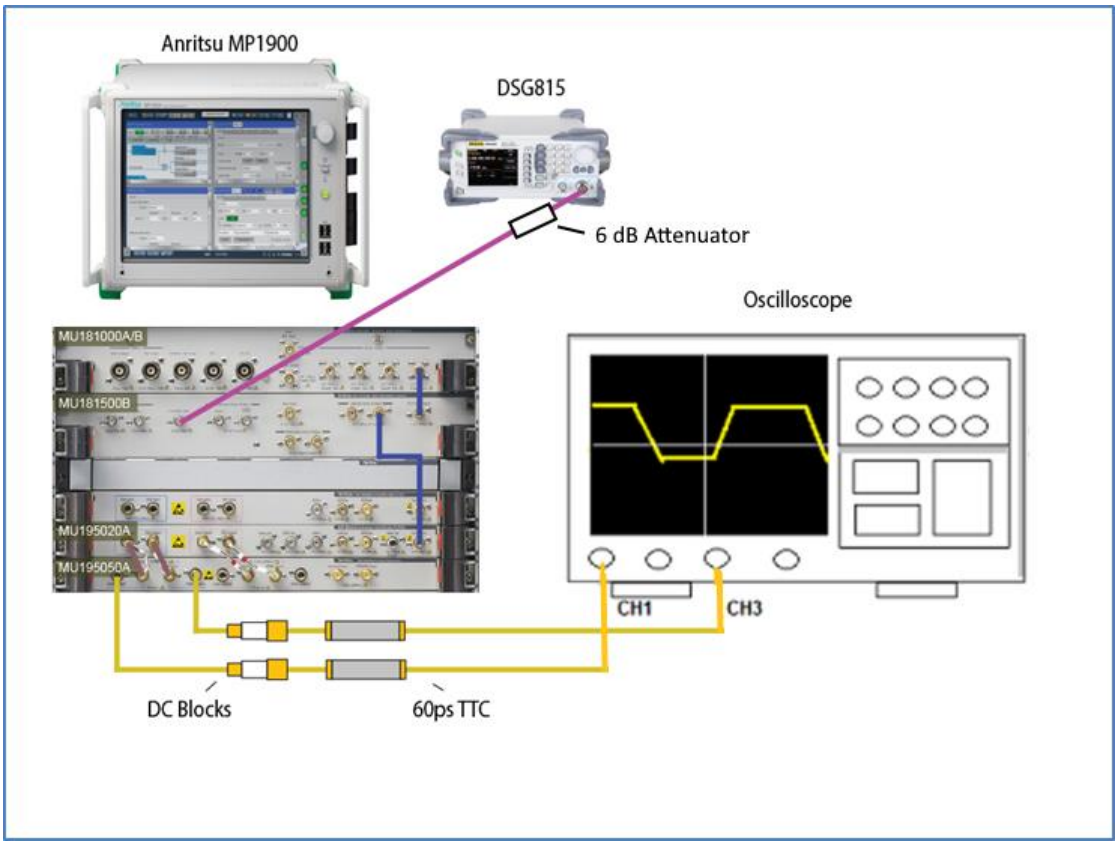


FIGURE 41. HBR3 CONCEPTUAL SETUP FOR TP1 CALIBRATION

1. Connect the equipment as shown in the above setup diagram.
2. Turn on Output of the MP1900A BERT.
3. Set up the MP1900A BERT to recall *HBR3_Risetime.CND* as follows:

   - Bitrate: 8.1Gb/s
   - Launch Amplitude: 1.4V Differential (700mV with divider) to provide a voltage that is found to be close to the final value when calibration is complete.
   - Pattern: Clock/256
   - Jitter Terms enabled and set to zero

   Note: The HBR3_Risetime.CND MP1900A setup uses the Clock/256 pattern to provide a long run length in order to produce accurate rise time measurement when averaged.

4. Set up the Oscilloscope to recall *Risetime.set* as follows:

   - Data: Ch1 – Ch3
   - Crosstalk: Ch2 – Ch4 BW = 16GHz
   - SR: 100GS/s (Ch1 – Ch3 or Ch2 – Ch4)
   - 60mV/div Differential Math
   - 20-80 Rise Time Measurement enabled
   - Averaged to 16 acquisitions as set in the Acquisition Menu of the oscilloscope.

   Note: The Risetime.set oscilloscope setup provides the Differential math signal which is optimized for swing of the MP1900A signal and averaged for accurate 20-80 rise time measurement.

5. On the MP1900A BERT, verify that the 20-80 rise time is between **40-60ps** (measured at the above BW).
6. Calibrate the AC Common Mode (**ACCM**) to **100mV pk-pk +/- 5% at 400MHz** as follows:

   a) On the Scope, recall *CM.set*:

      - Math1: (Ch1 + Ch3)/2
      - Averaged to 16 acquisitions
      - Measure Pk-Pk (Math1)

   b) On the MP1900A BERT:

      - CM Control: On
      - CM Frequency: 400MHz
      - pk-pk Amplitude: 100mV

   c) Calibrate the CM Amplitude to 100mV pk-pk +/- 5%.
   d) Return the CM Amplitude to 0V, but leave the CM Source Enabled.

7. Calibrate **RJ** to **13mUI +/- 5% RMS (160mUI pk-pk)** and then return to zero as follows:

   a) On the MP1900A BERT, adjust RANDOM JITTER(RJ) (10MHz to 1GHz).

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b) On the MP1900A BERT, recall *HBR3_RjPj.CND* using Pattern = D24.3 and 1100 Quarter Rate Clock.
Note: The Quarter Rate Clock is used to maintain 50% Edge Density.
c) On the Scope, recall *HBR3_RjPj.set* as follows:
- EZJIT or DPOJET settings:
  - Clock Recovery: Mean
  - Pattern Length: 4UI

d) Calibrate to RJ = 13mUI +/- 5% RMS (160mUI pk-pk), measurement = RJ-DD.
e) Return the RJ Amplitude to zero on the MP1900A BERT, but leave it Enabled.

8. Calibrate **SJ_Fixed** to **130mUI pk-pk at 297MHz +/- 5%** as follows:

a) Connect the DSG815 "RF output" to the MP1900A "Ext SJ" input, and turn on Ext SJ on the MP1900A BERT.
Warning: Do not output signal amplitude over 2Vp-p from the DSG815. It will damage the MP1900A "External Jitter Input".
b) Adjust the output level on the DSG815.
c) Calibrate to SJ = 130mUI pk-pk, measurement = PJ1.
d) Return the output level to -110dBm, but leave the Ext SJ Enabled.

9. Calibrate **SJ_Sweep** to **100mUI pk-pk at 100MHz +/- 5%** as follows:

a) On the MP1900A BERT, adjust SINE JITTER.
b) Calibrate to SJ = 100mUI +/- 5% pk-pk, measurement = PJ1.
c) Repeat steps (a) and (b) above for:
- 1013mUI pk-pk at 2MHz +/- 5%
- 137mUI pk-pk at 10MHz +/- 5%
- 109mUI pk-pk at 20MHz +/- 5%

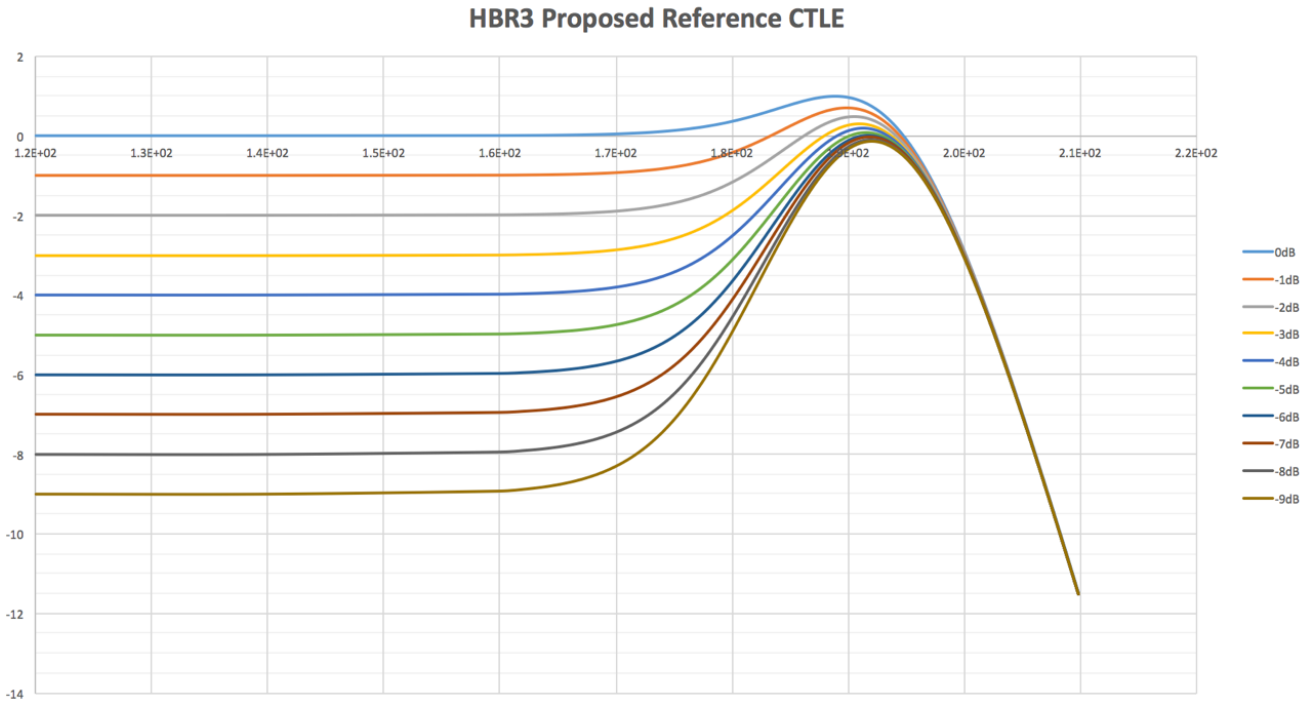
d) Return the SJ Sweep Amplitude to zero, but leave the SINE JITTER Enabled.

10. Measure **DATA TIE Reference** for ISI Measurement at TP1 as follows:

a) On the Scope, change the EZJIT or DPOJET settings to:

- Clock Recovery: 15MHz, Damping Factor = 1
- Fixed Data Rate: 8.1GHz
- Pattern Length: 4
- Apply CTLE (fz = 806MHz, fp1 = 3.03GHz, fp2 = 5.6GHz) *(Note: This comes from worst case CTLE used in Tx testing — the -8dB curve from the below family of CTLEs.)*

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Measurement = DATA $TIE_{Pk\text{-}Pk}$(TP1)

Note: Instead of using the DDJ measurement on the Scope for ISI measurement, a relative TIE (pk-pk) measurement from TP1 to TP3_EQ is made. The reason is that if there is some non-zero ISI intrinsic from the Scope measurement, it will be calibrated out of the measurement. Here the same clock recovery and JTF is applied at TP3_EQ before adding the channel, and then the DATA TIE (pk-pk) is measured with a clock pattern applied. This is a baseline intrinsic value to subtract from the TIE (pk-pk) value, which will give a true ISI value after applying the channel.

9.1.2 Calibration Setup and Procedure (at TP3)

Figure 42 shows the conceptual calibration setup at TP3. This setup uses the Artek CLE1000-A2 as the variable ISI source and the MP1900A BERT as the crosstalk source.

Note: Using variable ISI generation enables calibration for all data rates to be performed using the same test setup. This only requires minimum reconfiguration of the test setup, which allows testing to be more fully automated.

Note: The following diagram shows an example of an equipment setup that provides adequate ISI. The actual ISI calibration results may vary depending on cables and adapters used. Additional cables and adapters may be needed to achieve a calibration value that is within +/-5% of the target value. It is up to the user to ensure that the ISI values in the DP CTS for ISI are achieved and measured. You should make sure to capture the screenshot of the ISI you calibrate to and keep it with your test results for future reference.

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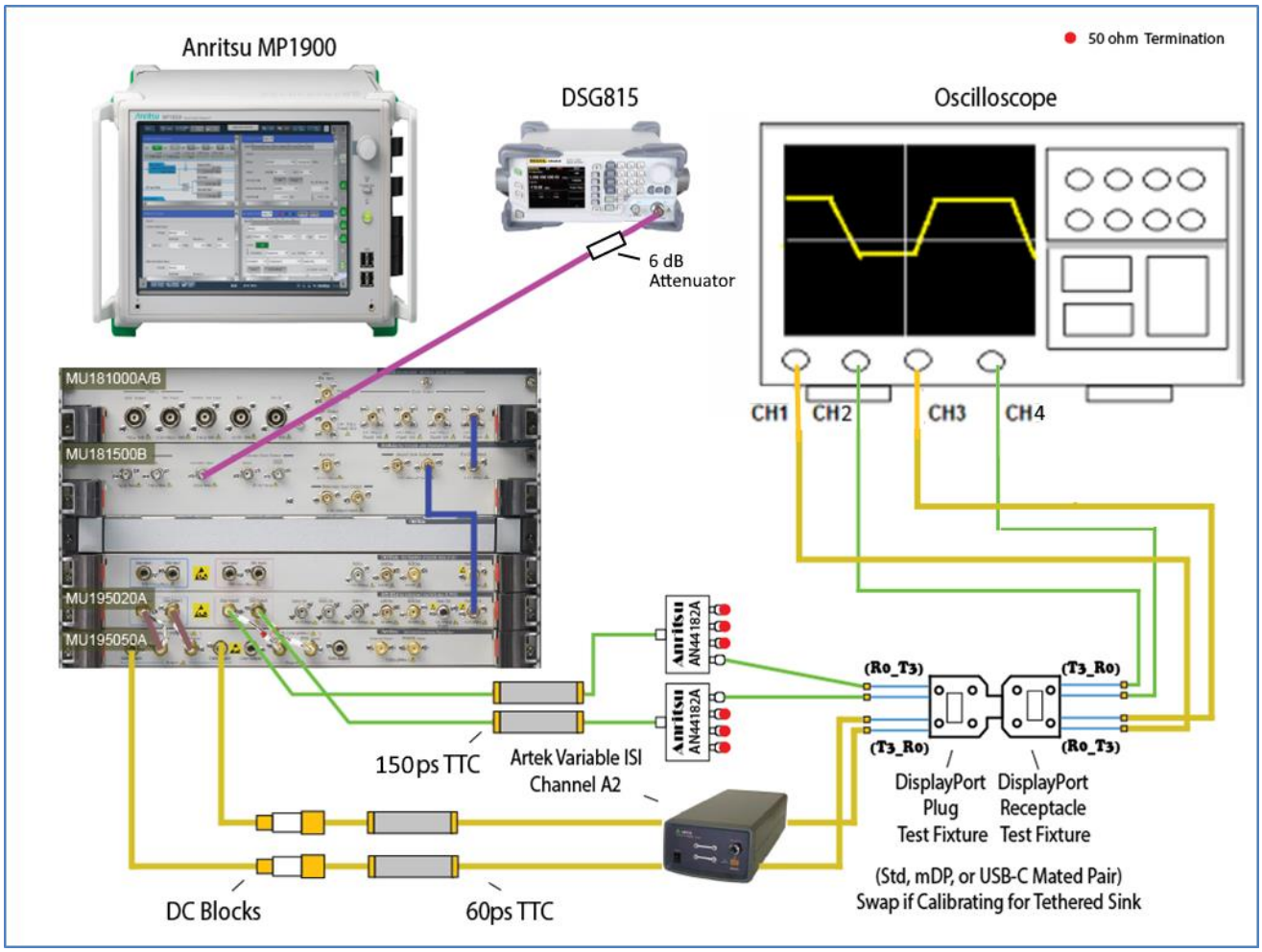


FIGURE 42. HBR3 CONCEPTUAL SETUP FOR TP3 CALIBRATION

1. Change the previous setup to the above setup.
2. Calibrate **ISI** = [DATA $TIE_{Pk\text{-}Pk}$(TP3_EQ) – DATA $TIE_{Pk\text{-}Pk}$(TP1)] to **240mUI +/- 5%** as follows:
   a) On the Scope, measure DATA $TIE_{Pk\text{-}Pk}$(TP3_EQ):
      - Set up the Scope to recall *HBR3_TP3_EQ_Eye.set* as follows:
        - Use the same Horizontal settings from the TP1 calibration.
        - Set the Vertical channels to 30mV/div.
        - Set up EZJIT or DPOJET as follows:
          - Clock Recovery: 15MHz, Damping Factor = 1
          - Fixed Data Rate: 8.1GHz
          - Pattern Length: 2520
          - Apply CTLE (fz = 806MHz, fp1 = 3.03GHz, fp2 = 5.6GHz)

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- Subtract the measurement in Step 2(a) from the measurement in Step 10(b) of the TP1 calibration.
- Adjust ISI on the CLE1000-A2 until [DATA TIE_{Pk-Pk}(TP3_EQ) – DATA TIE_{Pk-Pk}(TP1)] = 240mUI +/- 5%.

Note: A physical measurement of the ISI channel and attached cables should be made with a VNA to verify it fits within 22-24dB Insertion Loss including all cables, mated pair fixture and DC Block.

3. Calibrate **Complete Stressed Eye** at each SJ Frequency:
    - Return Amplitude of CM, RJ, SJ_Fixed, and SJ_Sweep to add to the calibrated ISI.
    - Turn on SSC on the MP1900A and set Deviation to 5000ppm.
    - Set SSC Frequency to 33kHz.
    - Set SSC Type to Down.
4. Calibrate **TJ** to **600mUI +/- 5%** using SJ_Fixed as Calibration Knob:
    - Measure TJ at TP3_EQ.
    - Use Fixed RJ as the TJ method by fixing the RJ in the EZJIT Preference menu to be RJ measured in Step 7 from TP1.
    - TJ = DJ + 12*RJ; where RJ is the fixed value measured in Step 7 from TP1. This can be done by using TJ measurement in the EZJIT with the Fixed RJ Preference setting selected.
5. Repeat Step 4 to achieve **600mUI +/- 5%** for 2MHz, 10MHz, and 20MHz.
6. Calibrate **Eye Height** to **50mV -0%, +5%** by adjusting the MP1900A Amplitude at each SJ_Sweep Frequency. Measure Eye Height.
7. Measure or calibrate **Crosstalk** using the MP1900A Quarter Rate Clock Method as the crosstalk source as follows:
    - Connect the crosstalk source (Channel 2) to the fixture and Scope as shown in Figure 42.
    - Select 1100 pattern (D24.3 HBR3 Pattern) from the MP1900A Channel 2 Output.
    - Calibrate the Amplitude of the crosstalk signal to 500mV pk-pk at TP3.
8. Save the MP1900A configuration file for each SJ_Sweep Stressed Eye.

9.1.3 DUT Test Setup and Procedure (at TP3)

The following figure shows the conceptual setup for testing the DUT at TP3 which follows up from the previous TP3 calibration setup.

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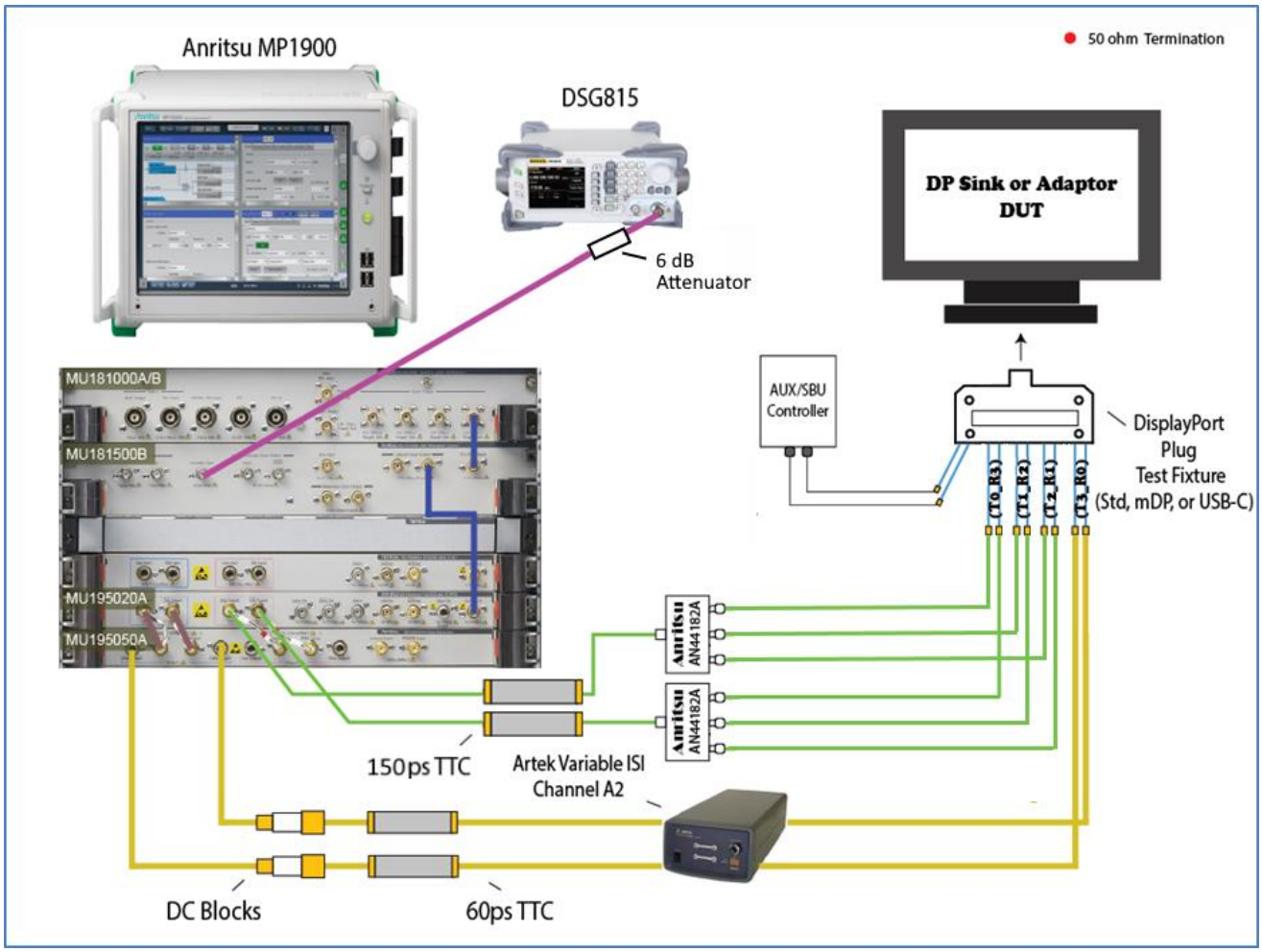


FIGURE 43. HBR3 CONCEPTUAL SETUP FOR TP3 DUT TEST

1. From the previous TP3 calibration setup, disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing.
2. Connect crosstalk lanes between the 'P' type adapter and crosstalk source.
3. Recall the MP1900A BERT setup for SJ_Sweep Stressed Eye at 100MHz.
4. Attach the Stressed Eye Signal to Lane 0 of the DUT.
5. If the DUT is a USB Type-C Sink, initiate the DP Alt Mode.
6. Test the DUT using the AUX/SBU Controller as follows:
   - Initiate the desired 'Alt Mode' if the DUT is a USB Type-C Sink.
   - Verify the Frequency Lock.
   - Verify the Symbol Lock.
   - Inject Errors and verify the correct amount of errors is being detected using the TPS4 Signal.
   - Test BER at the duration specified in the CTS.
7. Repeat Step 2 for 2MHz, 10MHz, and 20MHz SJ_Sweep Frequencies.
8. For a 4-Lane DUT, repeat Steps 3 to 6 for Lanes 1, 2, and 3.

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9.1.4 Calibration Procedure at TP2

If running calibration at TP2, perform the following steps:

1. Calibrate to the ISI target value (120mUI) at TP2 (with CTLE applied) as specified in the DP1.4 and DP Over Type-C CTS.
2. Calibrate to the target Eye Height (170mV) at TP2_CTLE in a similar way as described in the previous TP3 calibration.
3. Substitute the TP2_CTLE ISI value for TP3_EQ to obtain the final calibrated signal.
4. Capture the TP2 Eye Diagram to be included in the test report.

Notes:

- *The TP2 Eye Diagram is captured using the same CDR/JTF function as at TP3_EQ with CTLE applied.*
- *The final Eye Height at TP2 is established by TP34 Eye Height Calibration.*

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9.2 HBR2, HBR, and RBR Sink Calibration/Test Setup

The following methodology describes how to calibrate the stressed impairments for HBR2, HBR, and RBR per the PHY CTS using the DisplayPort standard configuration at TP1 and TP3/TP3_EQ. The detailed example shown is for HBR2.

RBR calibration is very similar to HBR/HBR2 calibration except that RBR calibration is done at TP3 instead of TP3_EQ.

9.2.1 Calibration Setup and Procedure

The following diagrams show the conceptual setup at TP1 and TP3/TP3_EQ as described in the CTS.

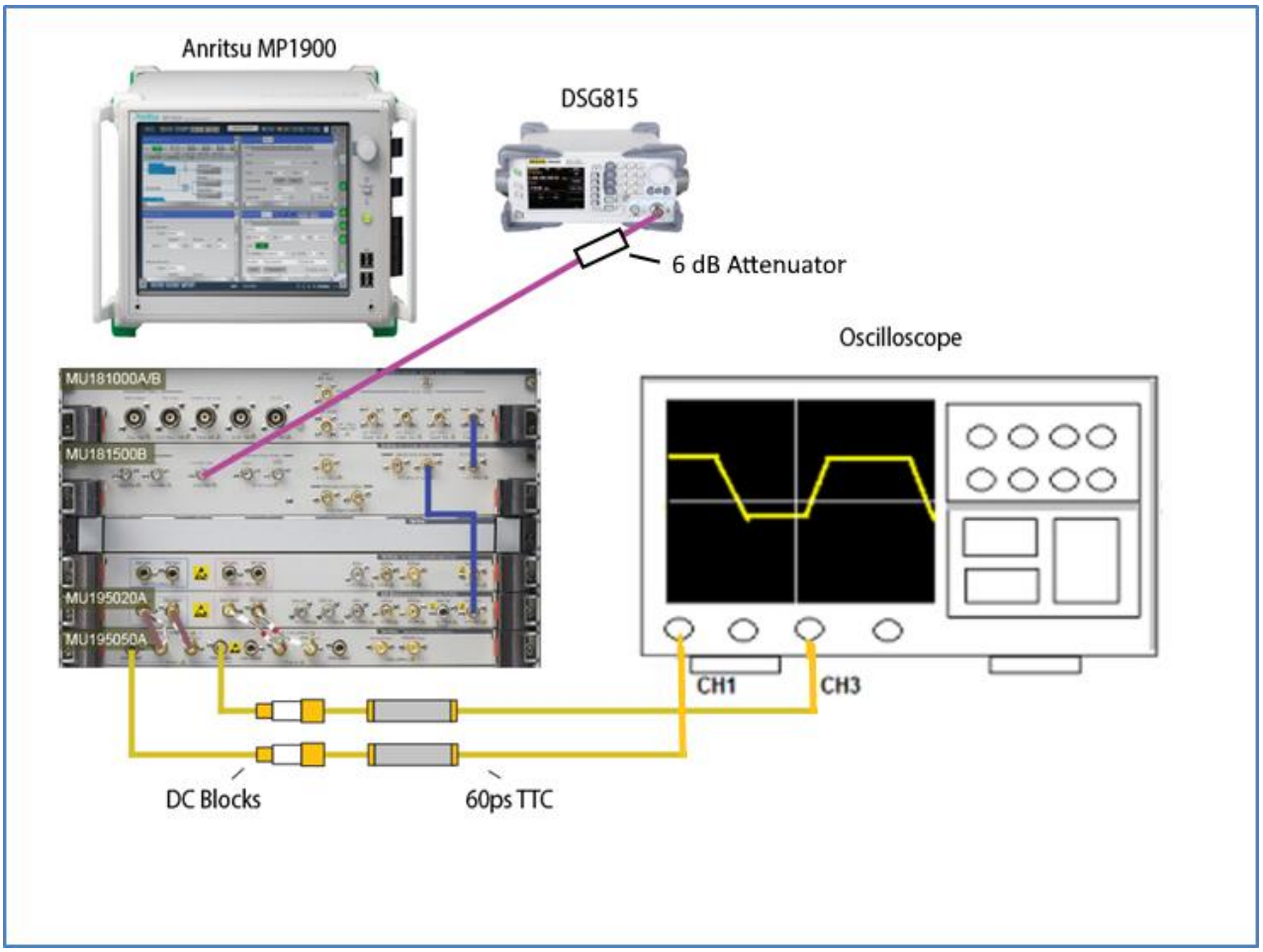


FIGURE 44. CONCEPTUAL CALIBRATION SETUP AT TP1

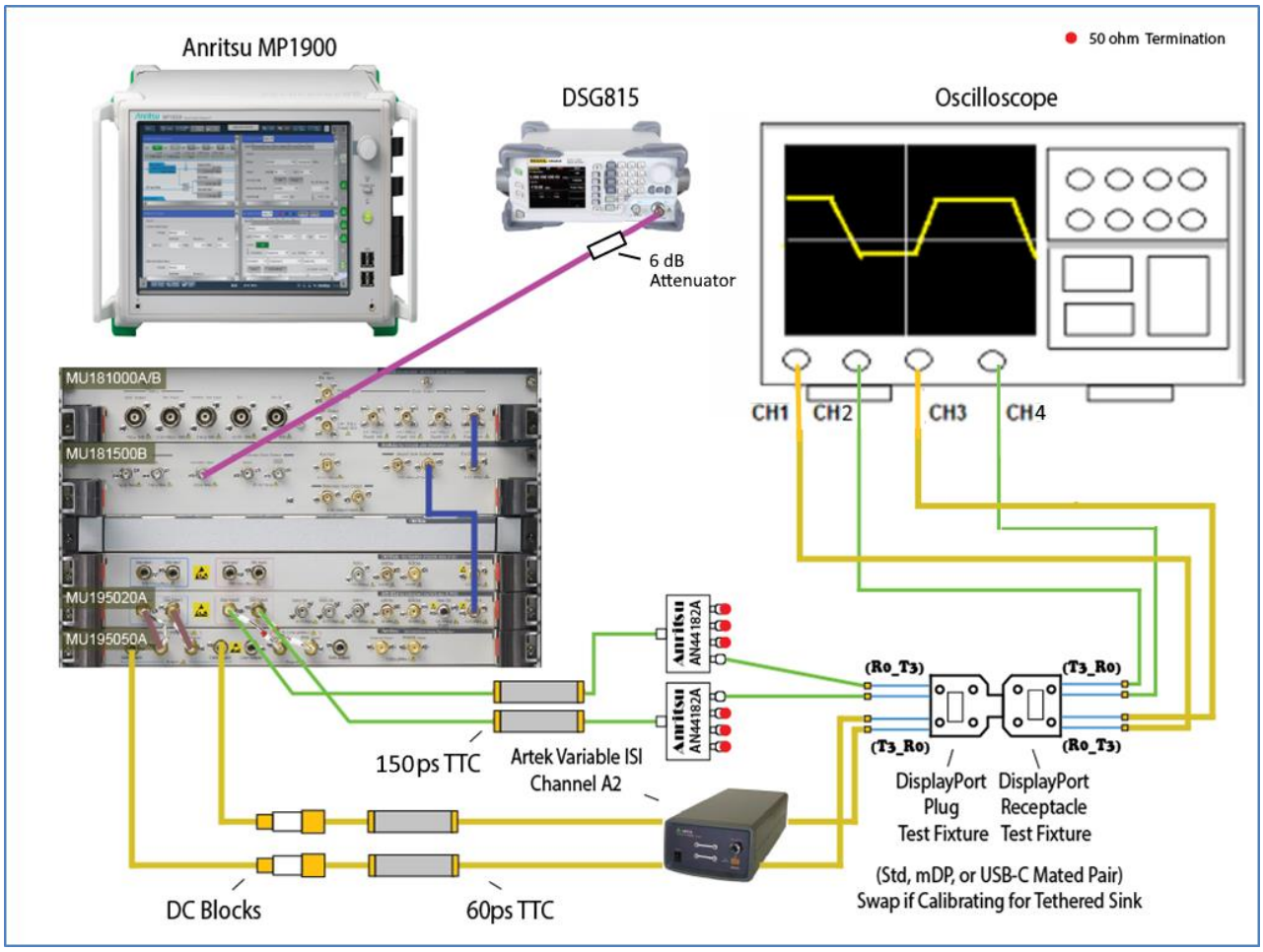


FIGURE 45. CONCEPTUAL CALIBRATION SETUP AT TP3/TP3_EQ (STANDARD CONNECTION)

1. Set up the equipment for TP1 calibration. Turn on the MP1900A BERT and apply Differential amplitude and AC coupling.
   - Ensure that pre-calibration/test procedure have been performed for the MP1900A BERT and Oscilloscope as described in Section 5.1.
   - On the MP1900A BERT, make sure the Outputs On/Off is set to Off while making connections.
   - Connect the DATA outputs of the MP1900A BERT directly to the Scope channels.
   - Set up the MP1900A BERT as follows:

RBR	HBR	HBR2	HBR3
MP1900A: SI PPG>Misc2: ▪ Data Rate: 3240.00MHz (1,620.00MHz Double Rate) ▪ Output: Ampl =	MP1900A: SI PPG>Misc2: ▪ Synthesizer: 2,700.00MHz ▪ DATA+: Ampl = 300mV (600mV Differential).	MP1900A: SI PPG>Misc2: ▪ Synthesizer: 5,400.00MHz ▪ DATA+: Ampl = 700mV (1.4V Differential).	MP1900A: SI PPG>Misc2: ▪ Synthesizer: 8,100.00MHz ▪ DATA+: Ampl = 700mV (1.4V Differential).

200mV (400mV Differential). ▪ Outputs On/Off: On	▪ Outputs On/Off: On	▪ Outputs On/Off: On	Outputs On/Off: On

2. Perform RJ(rms) calibration at TP1. Apply the D24.3 user pattern and set constant clock for JMD.

Initialization of MP1900A BERT for Jitter Composition:

a) On the MP1900A BERT, enable and set all jitter terms to zero before calibrating each term independently.

- For HBR3 and HBR2 only, turn on "Ext" as shown below:

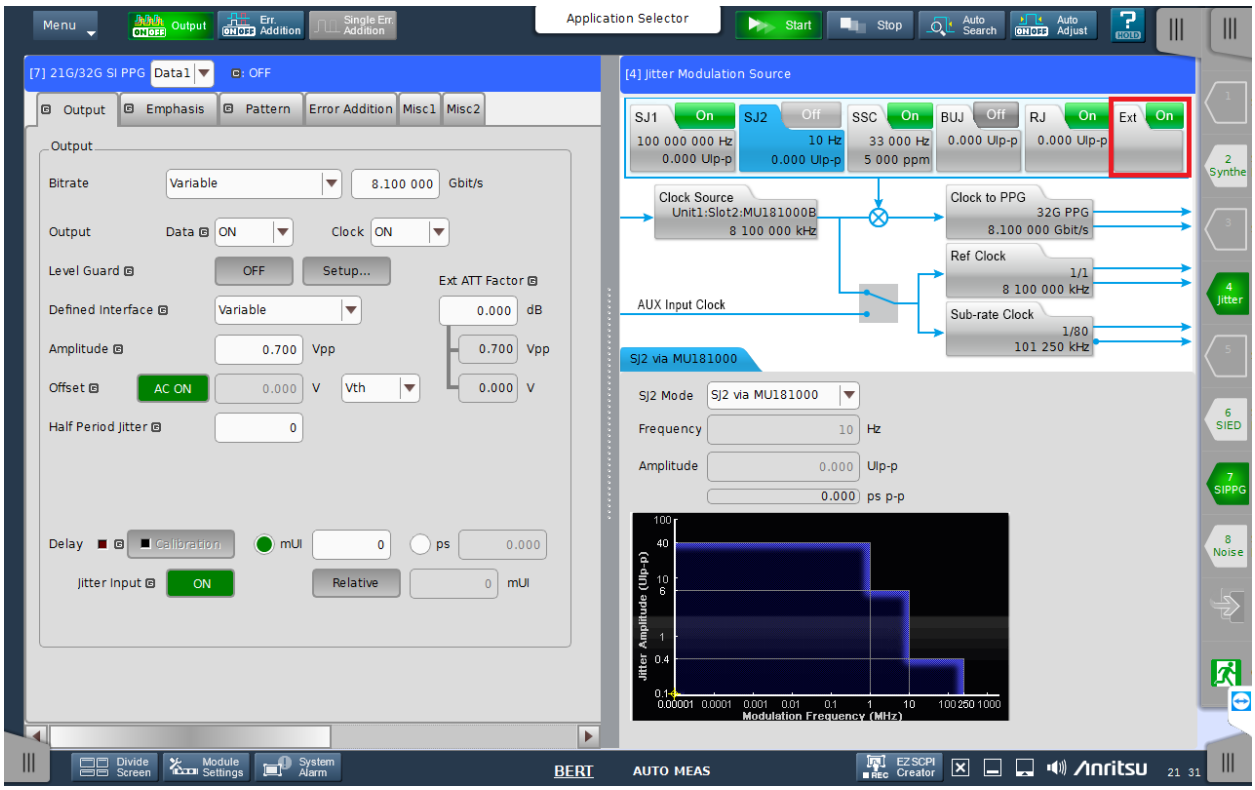


FIGURE 46. TURN ON EXTERNAL JITTER INPUT("EXT")

- Turn on SJ1 and set the frequency to 10MHz and amplitude to 0 UIp-p.
- Turn on RJ and set the amplitude to 0 UIp-p. *Note: It will default to Intrinsic Limit.*

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FIGURE 47. INITIAL JITTER SETUP

Random Jitter Calibration:

b) On the MP1900A BERT, select SI PPG > RJ >" Test Pattern" to "Data". Select the User Pattern and import the *1100.txt* pattern file.

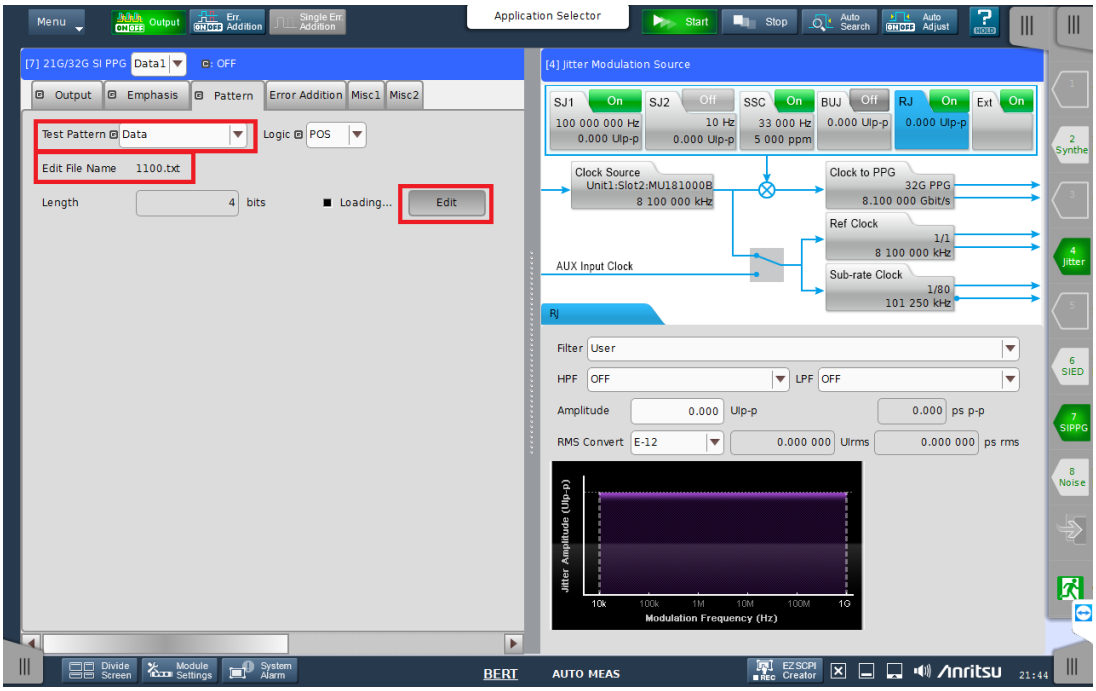


FIGURE 48. MP1900A 1100.TXT PATTERN

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c) On the MP1900A BERT, select Jitter Modulation Source > RJ.

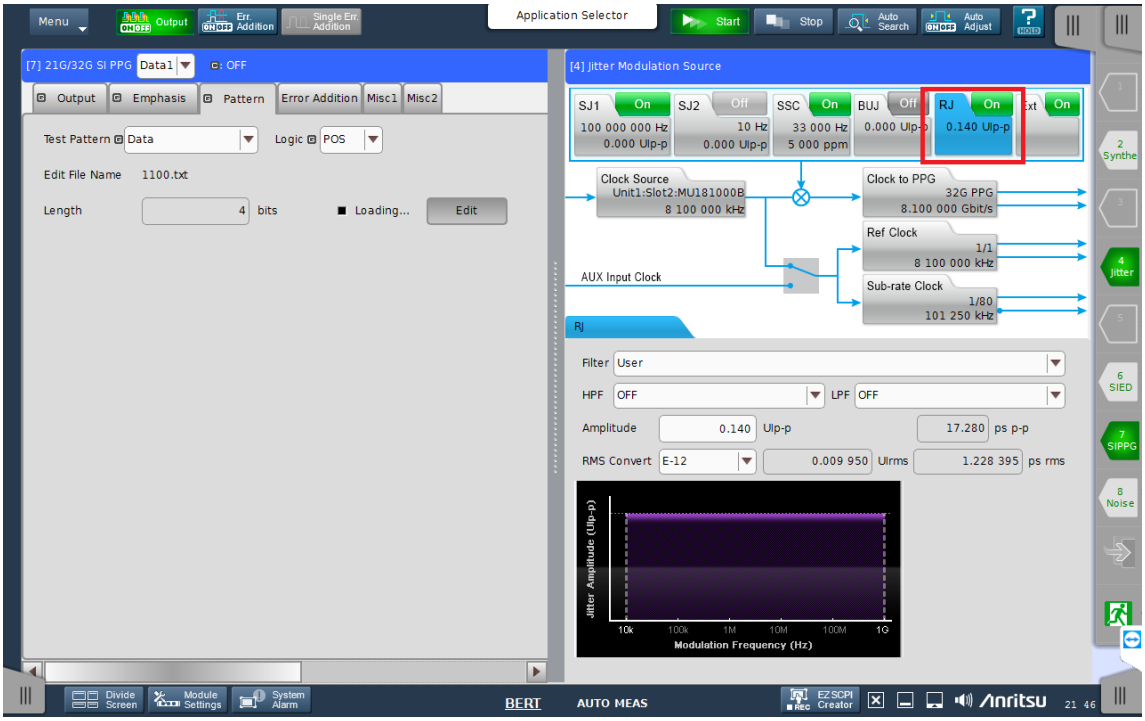


FIGURE 49. MP1900A RJ ADJUSTMENT

d) On the Keysight Scope EZJIT or Tektronix DPOJET (Jitter and Eye Tools SW), calibrate Random Jitter for the desired data rate using the following setup files:

Keysight Scope EZJIT:

C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR3_RjPj.set

C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR2_RjPj.set

C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR_RjPj.set

C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\RBR_RjPj.set

Tektronix Scope DPOJET (Jitter and Eye Tools SW):

C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2_RjPj.set

C:\TekApplications\DPOJET\Setups\DisplayPort\HBR_RjPj.set

C:\TekApplications\DPOJET\Setups\DisplayPort\RBR_RjPj.set

e) Adjust RJ on the MP1900A user interface while using the Single function on the EZJIT SW until RJ is calibrated to the following target values:

- RBR: **8.1mUI RMS**
- HBR: **13.5mUI RMS**
- HBR2: **16.7mUI RMS, 200mUI pk-pk (16.7 RMS x 12.0)**

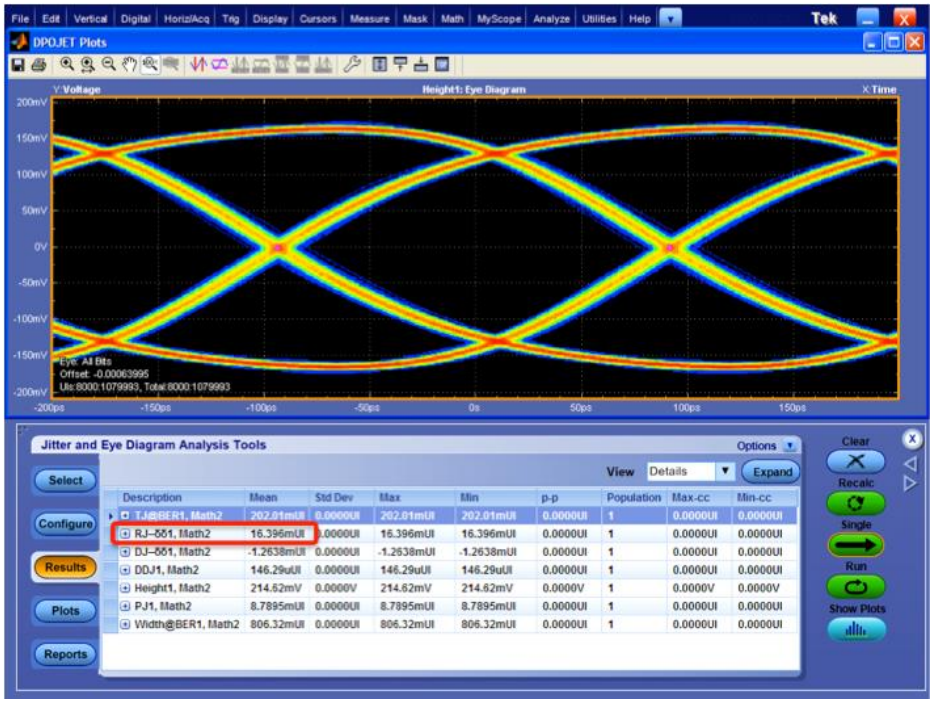
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- HBR3: **13mUI RMS, 123.5mUI pk-pk (13 RMS x 9.5)**



FIGURE 50. HBR3 RJ MEASUREMENT EXAMPLE ON KEYSIGHT SCOPE

Note: The RJ value in the above example is measured at 12.4mUI.



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FIGURE 51. HBR2 RJ MEASUREMENT EXAMPLE ON TEKTRONIX SCOPE

Note: The RJ value in the above example is measured at 16.4mUI.

f) Record the calibrated value for RJ.

g) Return the RJ value on the MP1900A BERT to zero *(Note: Intrinsic Jitter Limit will be displayed)*. The value will be returned to the above calibrated value in Step 7.

3. Perform calibration for SJ_{FIXED} at TP1 for HBR3 and HBR2 only. Apply the 1100.txt user pattern and set constant clock for JMD.

a) Turn on Ext on the MP1900A BERT.

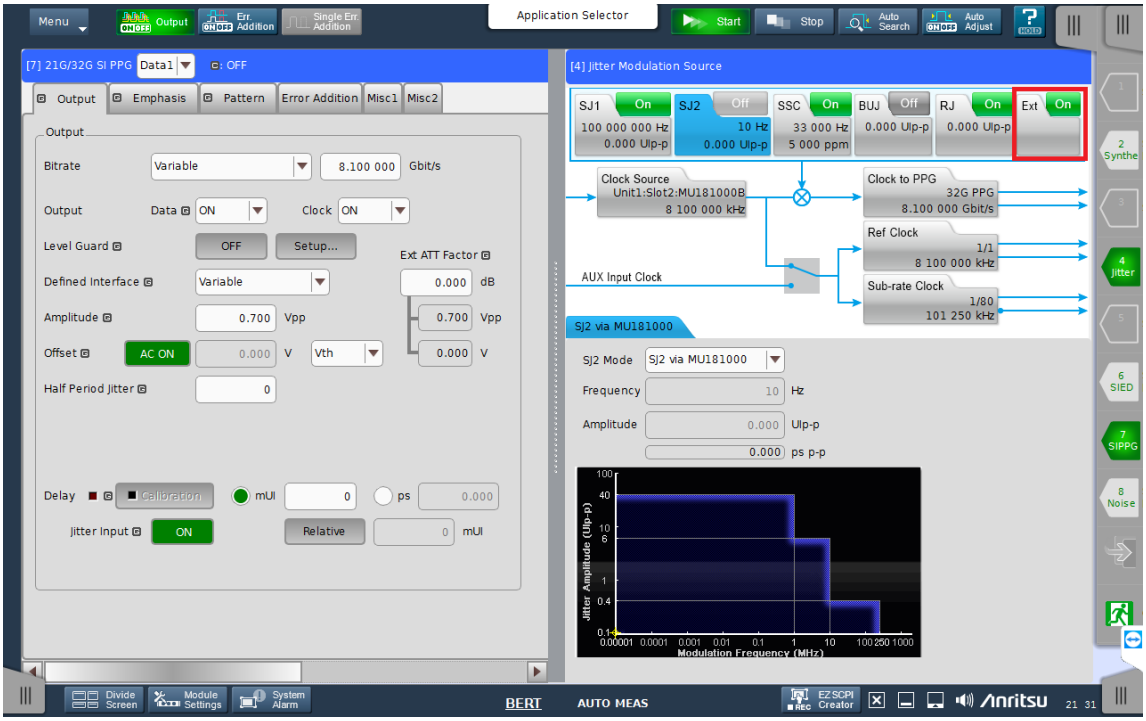


FIGURE 52. MP1900A SJ_{FIXED} SETTING FOR HBR3 AND HBR2

b) Set the DSG815 Frequency to 297 MHz and Level to -110 dBm (Minimum amplitude output)



FIGURE 53. DSG815 SJ_{FIXED} ADJUSTMENT EXAMPLE FOR HBR3 AND HBR2

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c) On the Scope, use the *HBR2_RjPj.set* configuration to calibrate the Sinusoidal Jitter.
d) Adjust the HIGH FREQ SINE JITTER amplitude on the MP1900A BERT while using the Single function on the Scope SW to calibrate Pj to the following target values:

- RBR: **NA**
- HBR: **NA**
- HBR2: **80mUI**
- HBR3: **130mUI**



FIGURE 54. HBR3 SJ_{FIXED} MEASUREMENT EXAMPLE ON KEYSIGHT SCOPE (NOT SHOWING TARGET 80MUI)

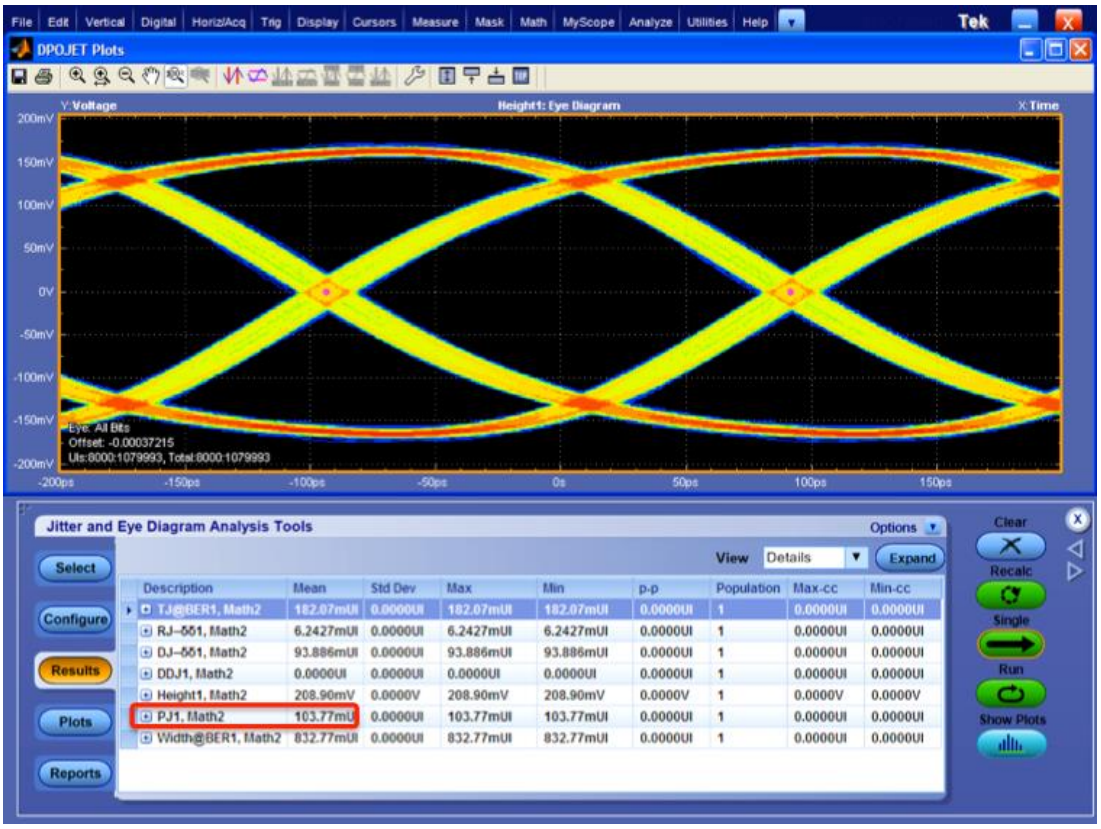


FIGURE 55. HBR2 SJ_{FIXED} MEASUREMENT EXAMPLE ON TEKTRONIX SCOPE (NOT SHOWING TARGET 80MUI)

e) Record the calibrated value for SJ_{FIXED}.
f) Return the Level value on the DSG815 to -110dBm. The value will be returned to the above calibrated value in Step 7.

4. Perform calibration for SJ_{SWEEP} for each frequency at TP1. Set constant clock for JMD.

Table 4-16: RBR TP3 Jitter Component Settings[a] [b]

Frequency (SJ) (MHz)	TJ (mUI)	ISI (mUI)	RJ_{rms} (mUI)	Approximate SJ (mUI)
2	1648	570	8.1	981
10	778			111
20	747			80

a. See DP 1.4a, Figure 3-31.
b. This table does not account for crosstalk-injected jitter.

Table 4-11: HBR TP3_EQ Jitter Component Settings[a]

Frequency (SJ) (MHz)	TJ (mUI)	ISI (mUI)	RJ_{rms} (mUI)	Approximate SJ_{SWEEP} (mUI)
2	1227	161	13.5	904
10	548			225
20	505			182
100	491			168

a. See DP 1.4a, Figure 3-30.

Table 4-9: HBR2 TP3_EQ Jitter Component Settings[a]

Frequency (SJ) (MHz)	TJ (mUI)	ISI (mUI)	RJ_{rms} (mUI)	Approximate SJ_{SWEEP} (mUI)	SJ_{FIXED} at 297MHz (mUI)	Crosstalk[b] (mUI)
2	1026	220	16.7	505	80	20
10	636			116		
20	624			104		
100	620			100		

a. See DP 1.4a, Figure 3-29.
b. Crosstalk jitter of 20mUI is assumed (not calibrated on the test fixture) to be generated from the fixed-amount aggressors.

Table 4-6: HBR3 TP3_CTLE Jitter Component Settings[a]

Frequency (SJ) (MHz)	TJ (mUI)	ISI[b] (mUI)	RJ_{rms} (mUI)	Approximate SJ_{SWEEP} (mUI)	SJ_{FIXED} at 297MHz[c] (mUI)	Crosstalk[d] (mUI)
2	620	240	13	1013	130	20
10				137		
20				109		
100				100		

FIGURE 56. JITTER COMPONENT SETTINGS FROM CTS

a) On the MP1900A BERT, turn on SINE JITTER.

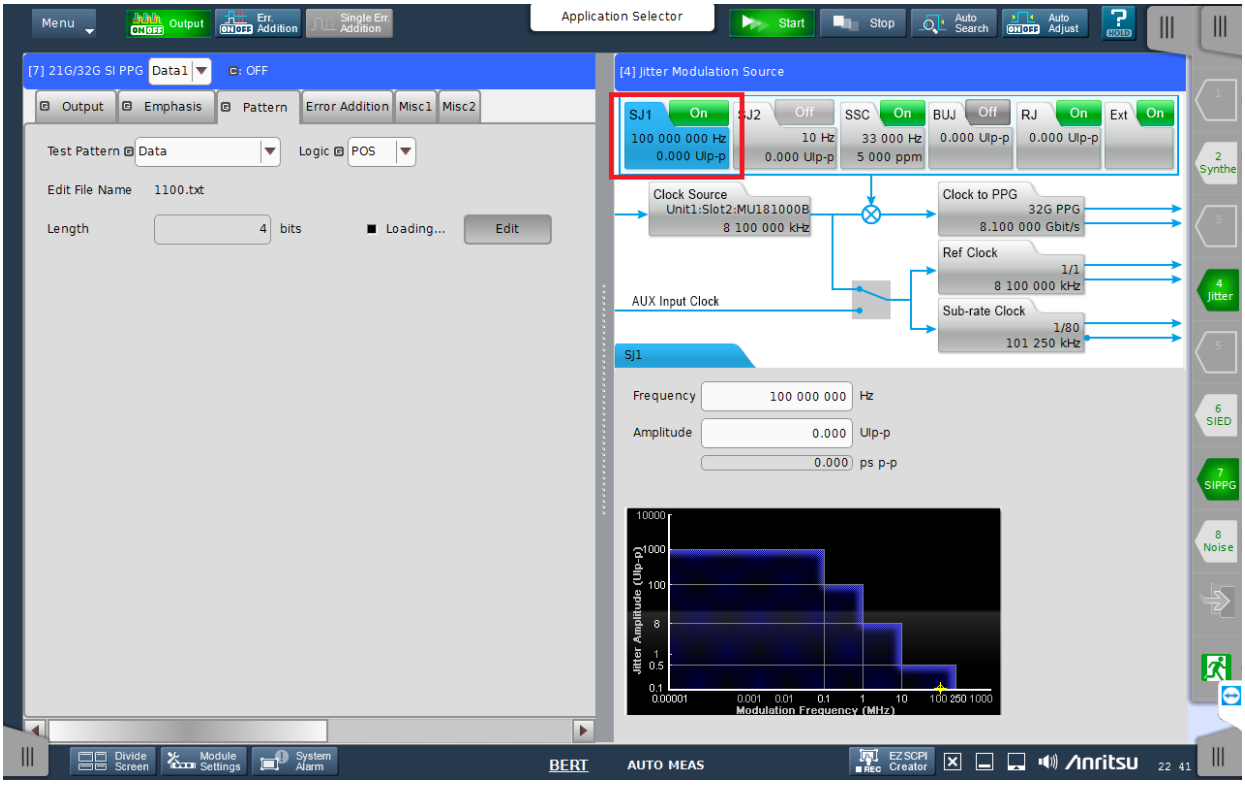


FIGURE 57. MP1900A SJ_{SWEEP} ADJUSTMENT

b) Adjust the SINE JITTER amplitude on the MP1900A BERT while using the Single function on the Scope SW to calibrate Pj to the target values.

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FIGURE 58. HBR3 SJ_{SWEEP} MEASUREMENT EXAMPLE ON KEYSIGHT SCOPE

Note: In the above example, PJ is measured at 143.3mUI.

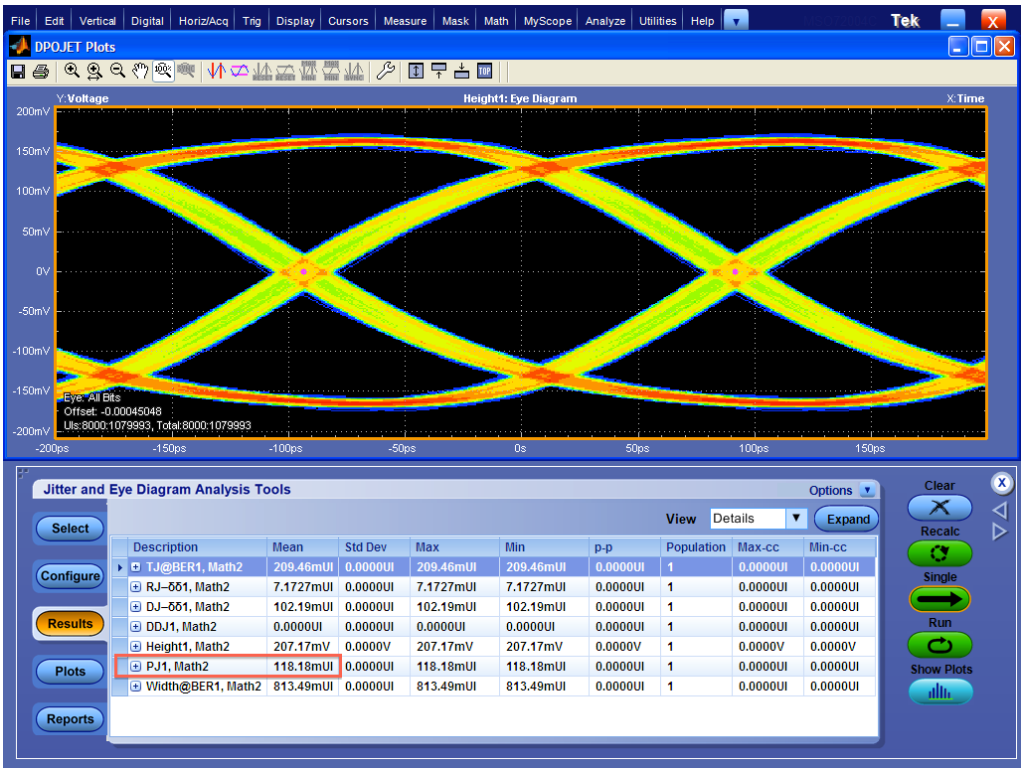


FIGURE 59. HBR2 SJ_{SWEEP} MEASUREMENT EXAMPLE ON TEKTRONIX SCOPE

Note: In the above example, PJ is measured at 118.2mUI.

5. Set up the equipment for TP3 calibration. Measure the ISI at TP3_EQ to the target ISI values specified in the CTS for HBR, HBR2 and HBR3 respectively. Apply the PRBS7 test pattern for HBR, CP2520 for HBR2 or TPS4 for HBR3. Set the clock recovery of the JMD to 2nd Order as described in the CTS. For RBR, apply the PRBS7_X2 test pattern and calibrate the ISI at TP3 without equalization.

   Note: Ensure that adequate ISI at TP3_EQ (for HBR, HBR2 and HBR3) or TP3 (for RBR) is achieved by the ISI generator being used as required in the CTS.

   Note: Actual ISI calibration results may vary depending on cables and adapters used in the physical setup. Additional cables and adapters may be needed to achieve a calibration value that is within +/-5% of the target value. It is recommended to capture the screenshot of the calibrated ISI and keep it with the test results for future reference.

RBR ISI Procedure	HBR ISI Procedure	HBR2 ISI Procedure	HBR3 ISI Procedure
On MP1900A > SI PPG > Pattern: ▪ Pattern = PRBS7_X2 (Double Pattern) ▪ Outputs On/Off: On On Scope: ▪ Recall Scope setup file to make DDJ measurements: For KS Scope: <*C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\RBR_PLL_Eye.set*> For Tek Scope: <*C:\TekApplications\DPOJET\Setups\DisplayPort\RBR_PLL_Eye.set*> ▪ For Tek Scope: DPOJET Sequence menu: Single	On MP1900A > SI PPG > Pattern: ▪ Pattern = PRBS7 ▪ Outputs On/Off: On On Scope: ▪ Recall Scope setup file to apply TP3_EQ filter and make DDJ measurements: For KS Scope: <*C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR_PLL_Eye.set*> For Tek Scope: <*C:\TekApplications\DPOJET\Setups\DisplayPort\HBR_PLL_Eye.set*> ▪ For Tek Scope: DPOJET Sequence menu: Single ▪ Measure ISI =	On MP1900A > SI PPG > Pattern: ▪ Pattern = Data File = *Anritsu DisplayPort Sink Test 1.4/HBR2_Compliance_2520bits_Pattern1.txt*. ▪ Outputs On/Off: On On Scope: ▪ Recall Scope setup file to apply TP3_EQ filter and make DDJ measurements: For KS Scope: <*C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR2_PLL_Eye.set*> For Tek Scope: <*C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2_*	On MP1900A > SI PPG > Pattern: ▪ Pattern = Data File = *Anritsu DisplayPort Sink Test 1.4/HBR3_TPS4.txt*. ▪ Outputs On/Off: On On Scope: ▪ Recall Scope setup file to apply TP3_EQ filter and make DDJ measurements: For KS Scope: <*C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR3_PLL_Eye.set*> For Tek Scope: <*C:\TekApplications\DPOJET\Setups\DisplayPort\HBR3_PLL_Eye.set*> ▪ For Tek Scope:

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▪ Measure ISI = **570mUI +/- 5%** ▪ Capture and save scope screenshot for compliance records	**161mUI +/-5%** ▪ Capture and save scope screenshot for compliance records	*PLL_Eye.set>* ▪ For Tek Scope: DPOJET Sequence menu: Single ▪ Measure ISI = **220mUI +/-5%** ▪ Capture and save scope screenshot for compliance records	DPOJET Sequence menu: Single ▪ Measure ISI = **240mUI +/-5%** ▪ Capture and save scope screenshot for compliance records

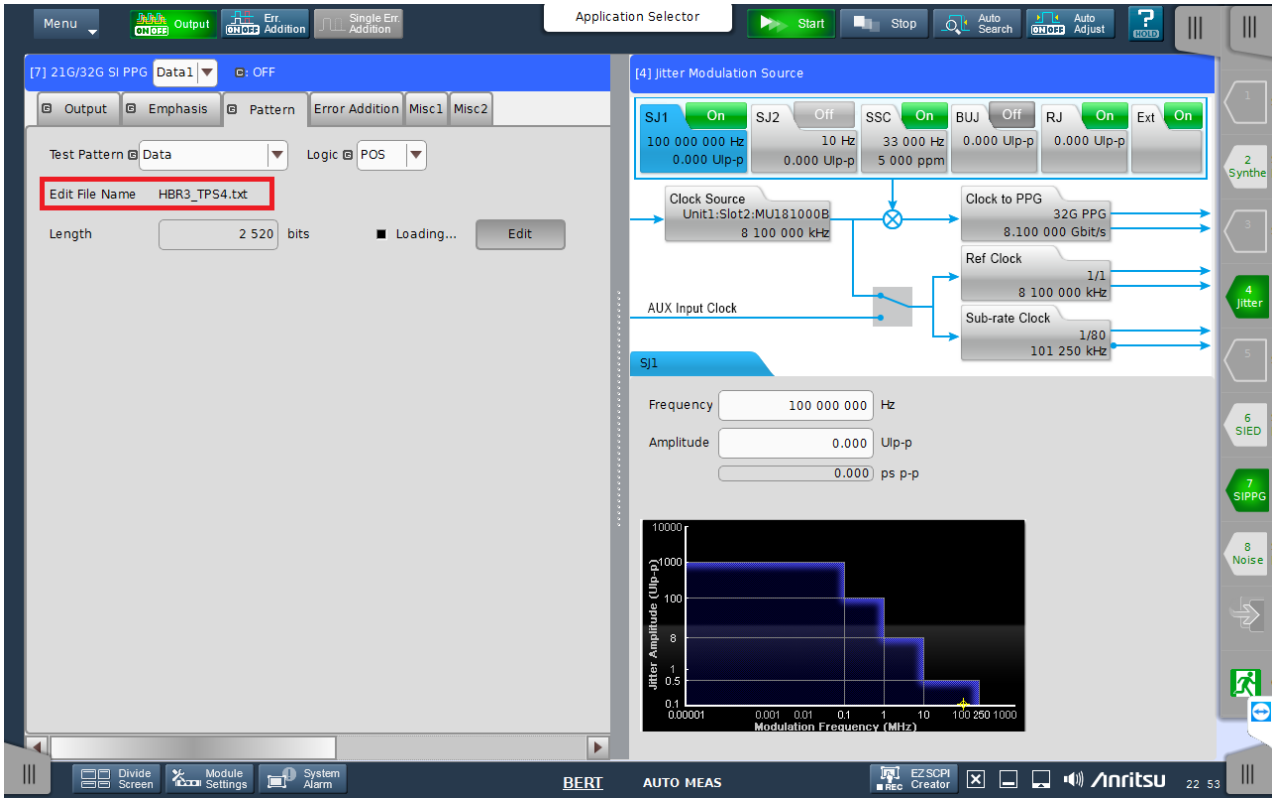


FIGURE 60. MP1900A HBR3 ISI SETUP EXAMPLE



FIGURE 61. HBR3 ISI MEASUREMENT EXAMPLE ON KEYSIGHT SCOPE

Note: The ISI value in the above example is measured at 69.2mUI.

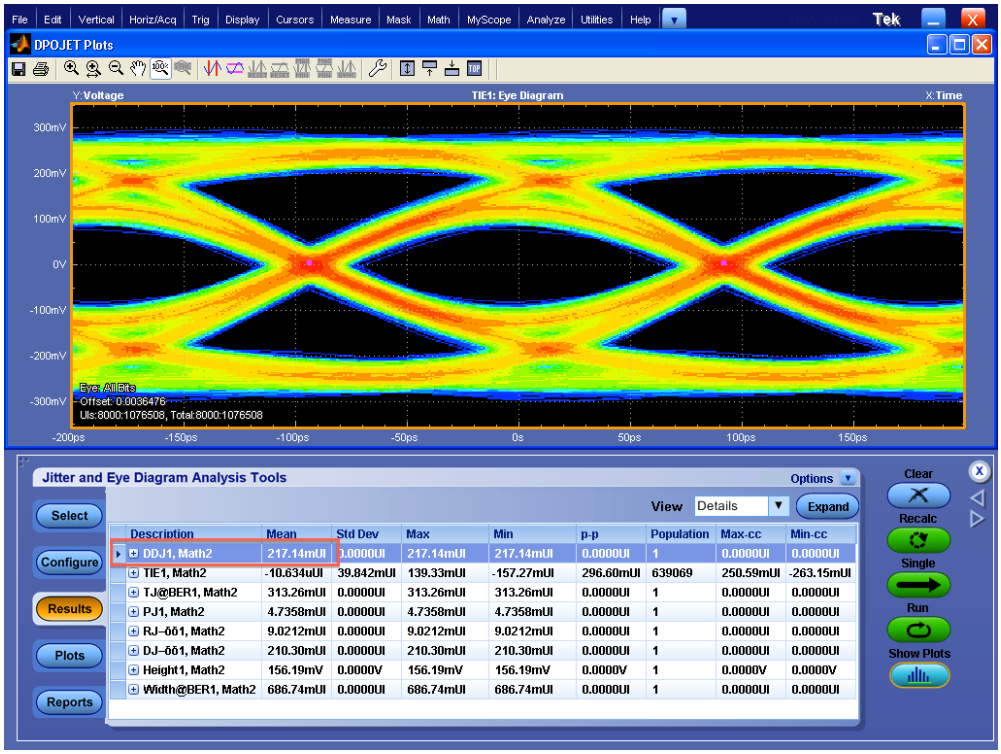


FIGURE 62. HBR2 ISI MEASUREMENT EXAMPLE ON TEKTRONIX SCOPE

Note: The ISI value in the above example is measured at 217mUI.

Note: It is recommended to capture and save the screenshot of the scope measurement to demonstrate that the proper value has been achieved.

Note: To achieve the best measurements on the scope, ensure that its vertical signals are properly scaled without clipping before applying the Ch1-Ch3 function and Equalization.

6. On the MP1900A BERT, make sure that the test pattern is set to PRBS7_X2 (Double Pattern for RBR), PRBS7 (for HBR), CP2520 (for HBR2) and TPS4 (for HBR3) from the previous step. In case the pattern has been changed, re-select as follows:
   a) For HBR3, select the User Pattern and import *HBR3_TPS4.txt* from the DisplayPort folder. For RBR, select PRBS7_X2, while for HBR, select PRBS7 and for HBR2 select *HBR2_Compliance_2520bits_Pattern1.txt* from the Pattern menu.

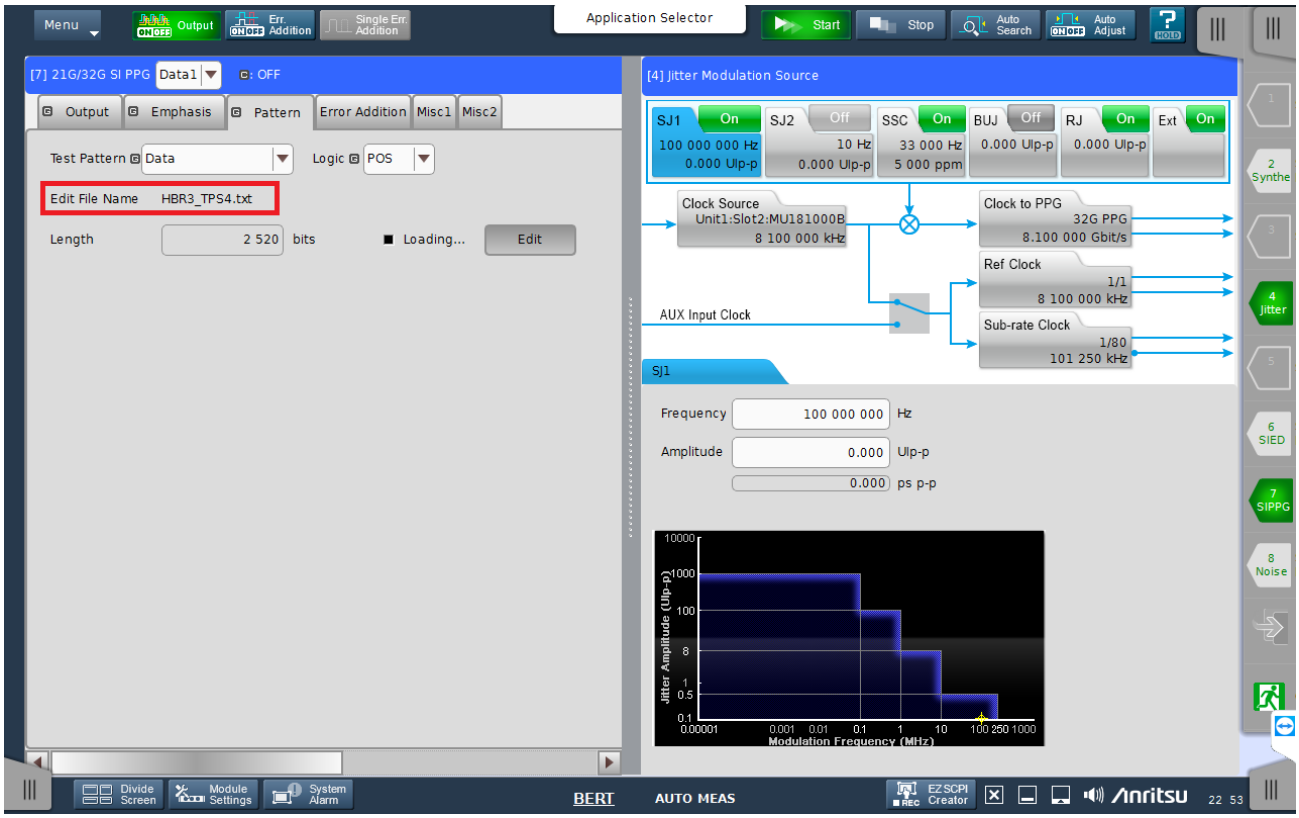


FIGURE 63. HBR3 COMPLIANCE EYE PATTERN SETUP EXAMPLE

7. On the MP1900A BERT, enable ISI, RJ, SJ_{FIXED}, SJ_{SWEEP}, and SSC.
   a) ISI is achieved in Step 5.
   b) Return the Amplitude of RJ (RANDOM JITTER) to the value calibrated in Step 2.
   c) For HBR2, return the Amplitude of SJ_{FIXED} (HIGH FREQ SINE JITTER) to the value calibrated in Step 3.
   d) Turn on SJ_{SWEEP} (SINE JITTER) as calibrated in Step 4.

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e) Turn on SSC with 33kHz frequency and 5000ppm with a triangle profile.

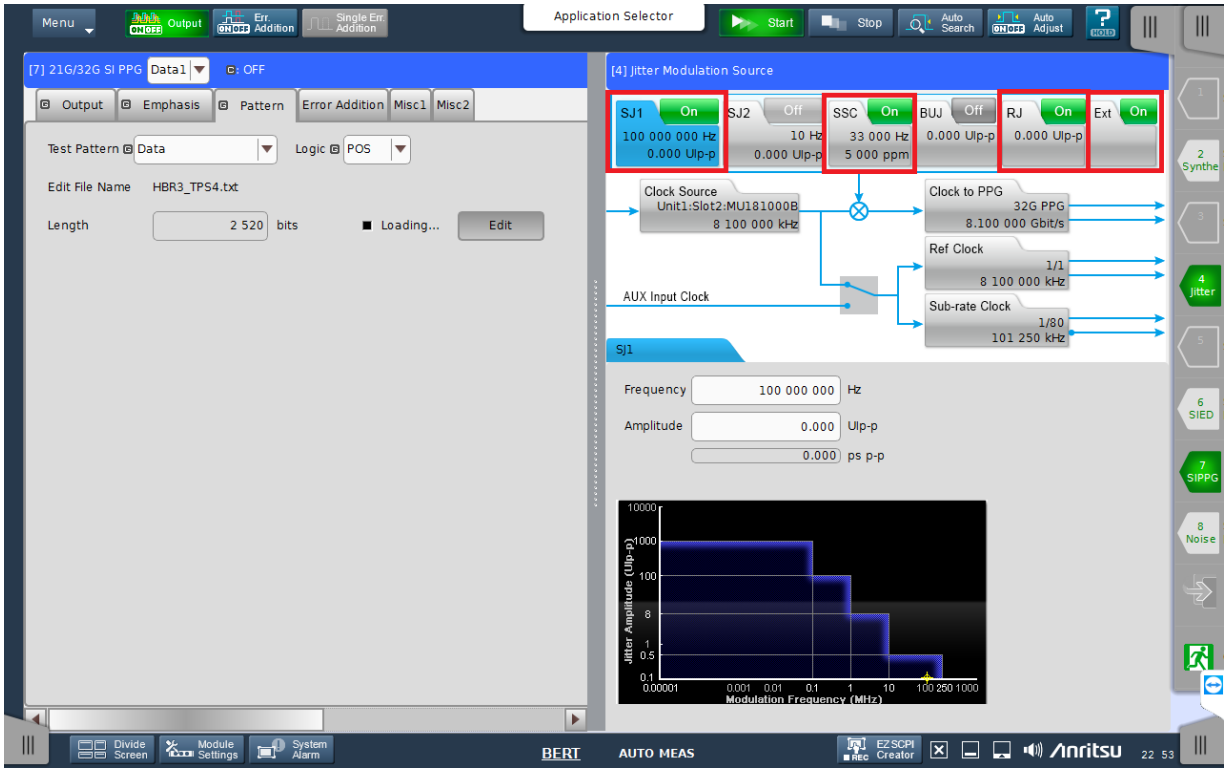


FIGURE 64. ALL STRESSES ENABLED EXCEPT CROSSTALK FOR HBR3

8. Perform calibration at TP3_EQ for the MP1900A Amplitude to reach the target Eye Height of 150mV for HBR, 100.0mV without crosstalk for HBR2 or 50mV without crosstalk for HBR3. Set the 2nd order clock recovery function for JMD as described in the DP specification.

   a) On the Keysight or Tektronix Scope, acquire and analyze the signal using the following setup files for each data rate:

      For Keysight Scope:

      - *C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR3_RjPj.set*
      - *C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR2_RjPj.set*
      - *C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\HBR_RjPj.set*
      - *C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 1.4\RBR_RjPj.set*

      For Tektronix Scope:

      - *C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2_PLL_Eye.set*
      - *C:\TekApplications\DPOJET\Setups\DisplayPort\HBR_PLL_Eye.set*
      - *C:\TekApplications\DPOJET\Setups\DisplayPort\RBR_PLL_Eye.set*

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b) Select SI PPG > Output on the MP1900A BERT and adjust the DATA Amplitude while using the Single function on the Infiniium Software to measure the Eye Height to the following target values:

- RBR: **56mV (+/- 3%)**
- HBR: **160mV (+/- 3%)**
- HBR2: **100mV (+/- 3%)**
- HBR3: **50mV (+/- 3%)**

Note: To achieve a repeatable Eye Opening measurement, capture a minimum of 2mUI with the JMD. Measure the vertical Eye Height as described in the CTS.

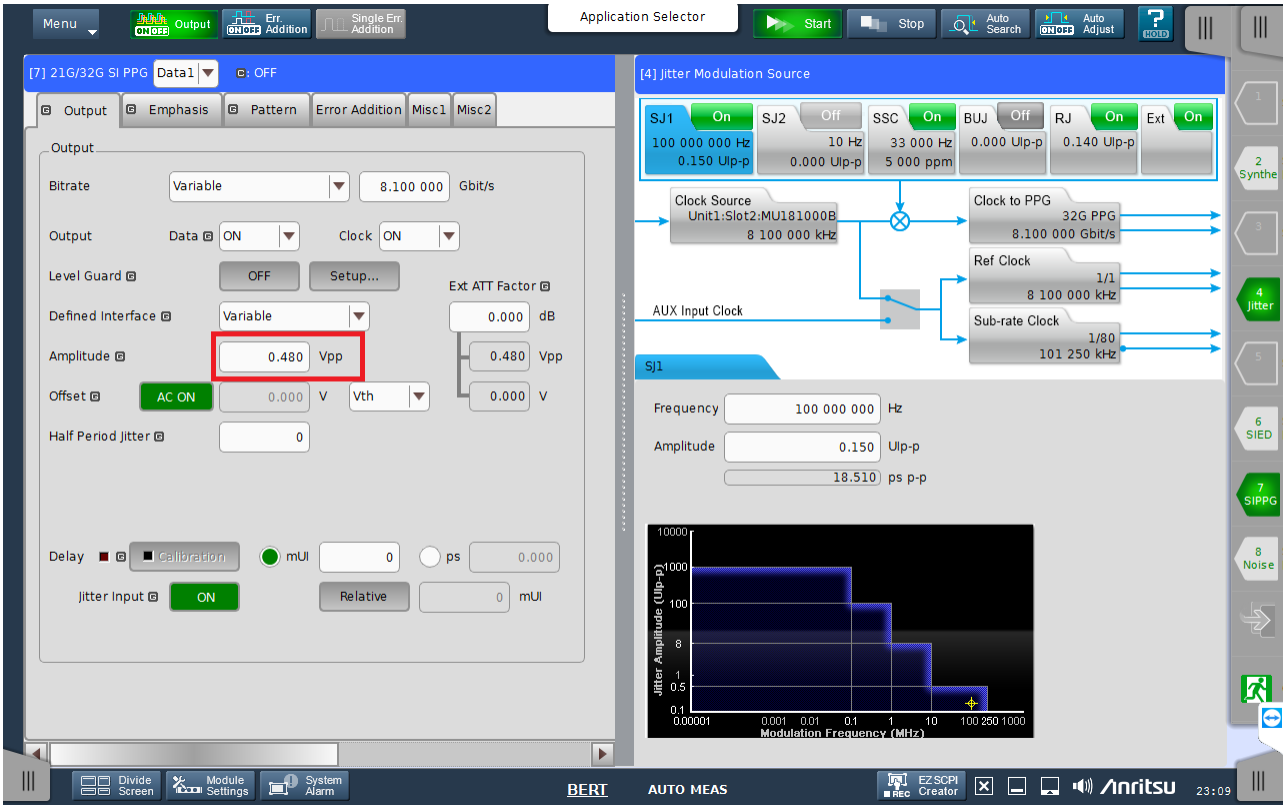


FIGURE 65. HBR3 EYE HEIGHT ADJUSTMENT EXAMPLE

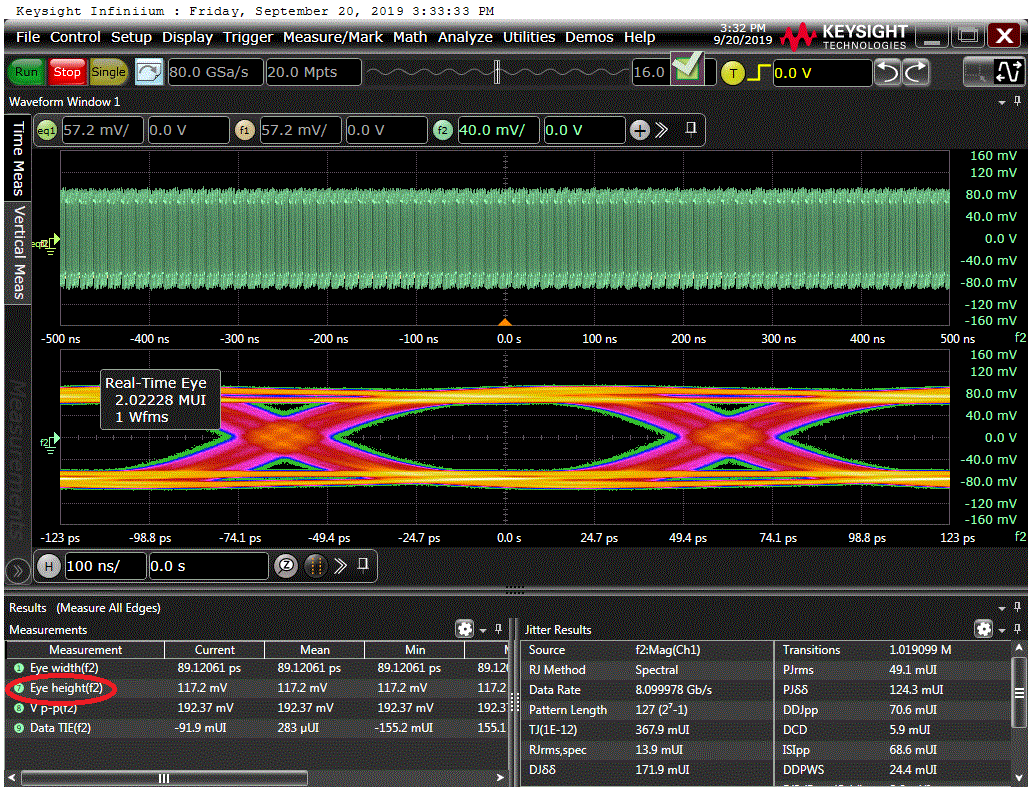


FIGURE 66. HBR3 EYE HEIGHT MEASUREMENT EXAMPLE ON KEYSIGHT SCOPE

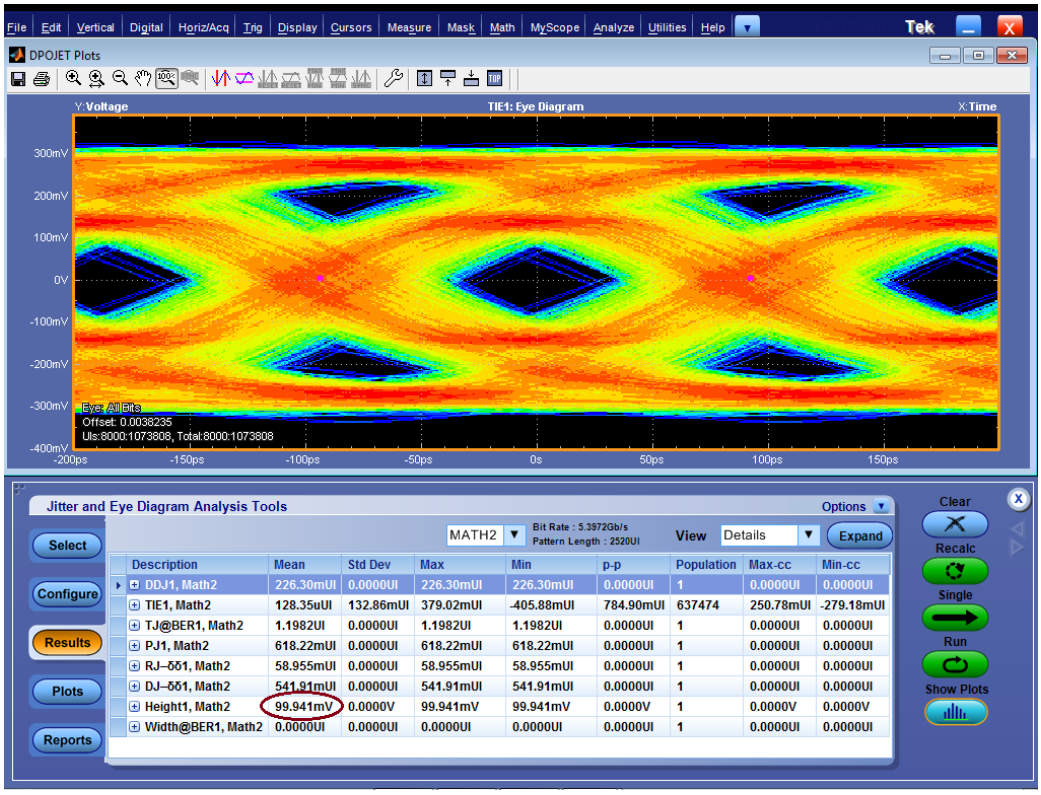


FIGURE 67. HBR2 EYE HEIGHT MEASUREMENT EXAMPLE ON TEKTRONIX SCOPE

9. On the Scope, apply a non-phase aligned crosstalk aggressor signal to Ch2-Ch4 for all data rates. Use the D24.3 pattern and set the Differential amplitude to 800mV for the crosstalk signal. Adjust the crosstalk signal Amplitude to reach the target value for the appropriate link rate.

   Note: The Edge rate of the crosstalk signal is set to 130ps (20/80) measured at TP3.

   Note: Crosstalk amplitude is dependent on the receptacle fixture being used. Refer to the respective manufacturer for details.

   a) Select SI PPG > Data2 (Second channel) on the MP1900A BERT and set the test pattern as 1100.txt.

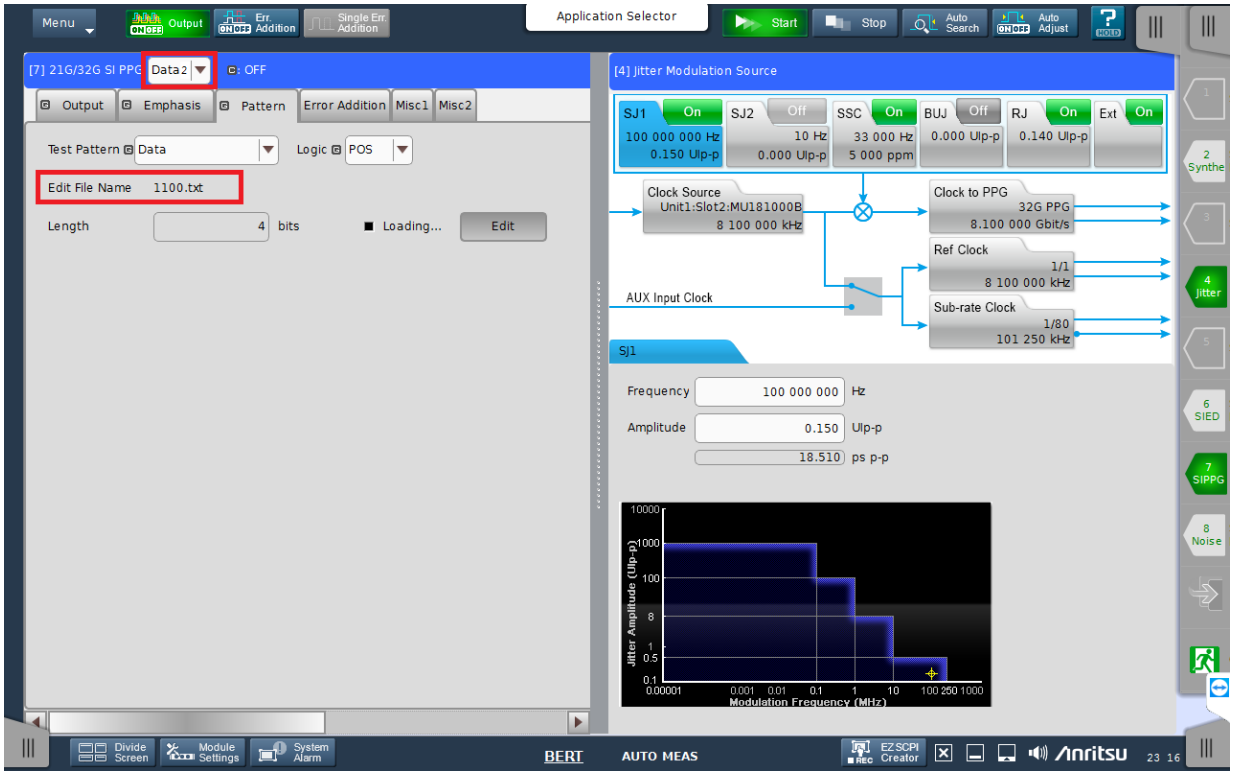


FIGURE 68. CROSSTALK PATTERN SETTING

   b) Adjust the DATA Amplitude while using the Single function on the Infiniium software to measure Voltage pk-pk to the following target values:

   - RBR: **138mV +/- 2%**
   - HBR: **450mV +/- 2%**
   - HBR2: **300mV +/- 2%**
   - HBR3: **300mV +/- 2%**

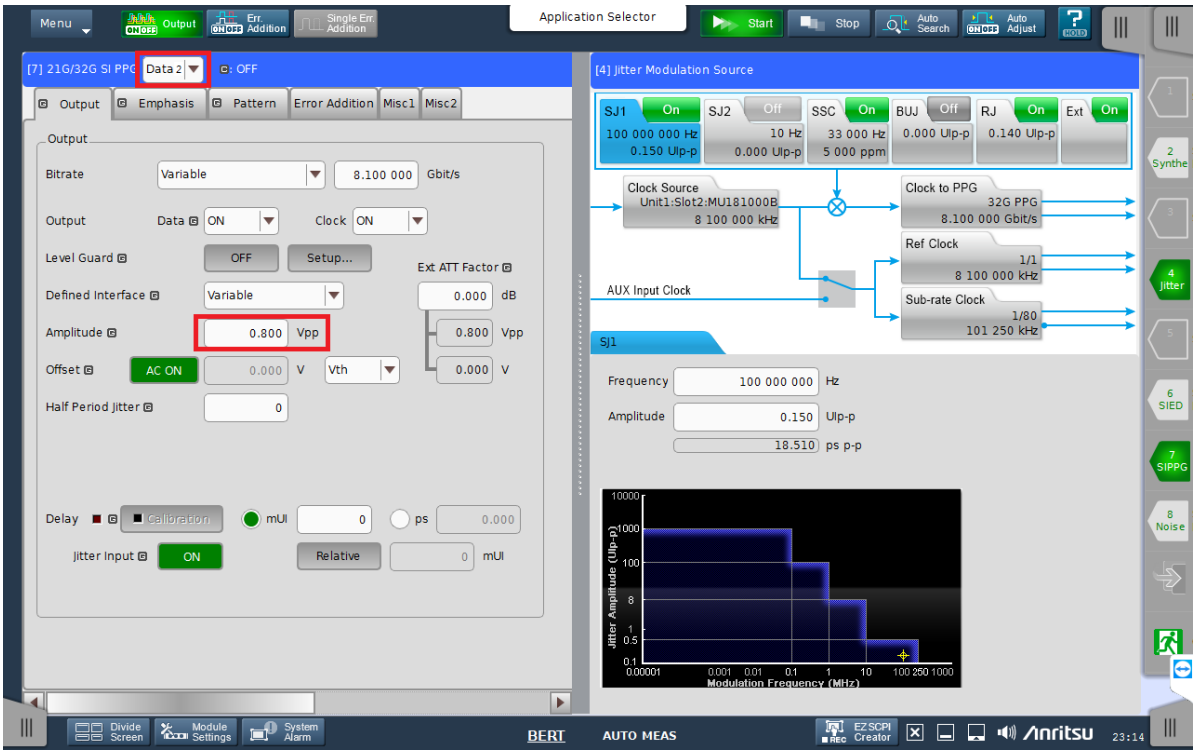


FIGURE 69. HBR3 EYE HEIGHT MEASUREMENT WITH CROSSTALK ADJUSTMENT

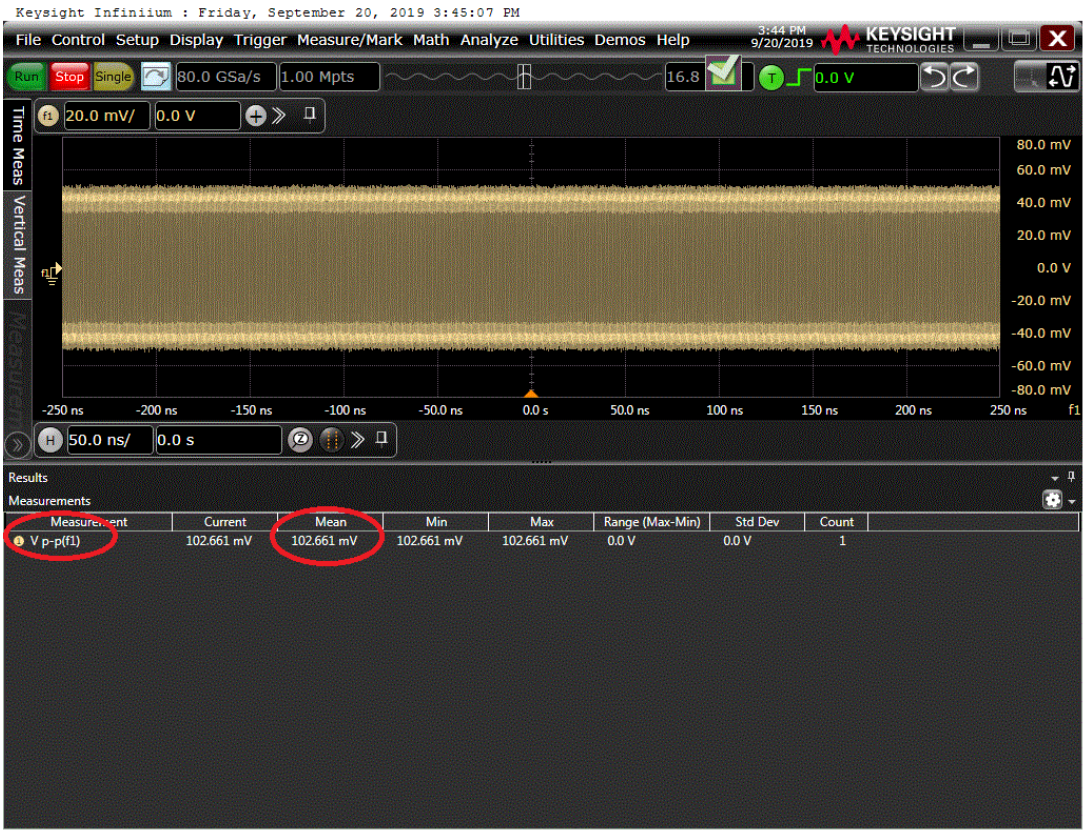


FIGURE 70. HBR3 CROSSTALK MEASUREMENT ON KEYSIGHT SCOPE



FIGURE 71. HBR2 CROSSTALK MEASUREMENT ON TEKTRONIX SCOPE

9.2.2 DUT Test Setup and Procedure

The following diagram shows the typical setup for testing the DUT. At TP3, disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing. Connect crosstalk lanes between the 'P' type adapter and crosstalk source.

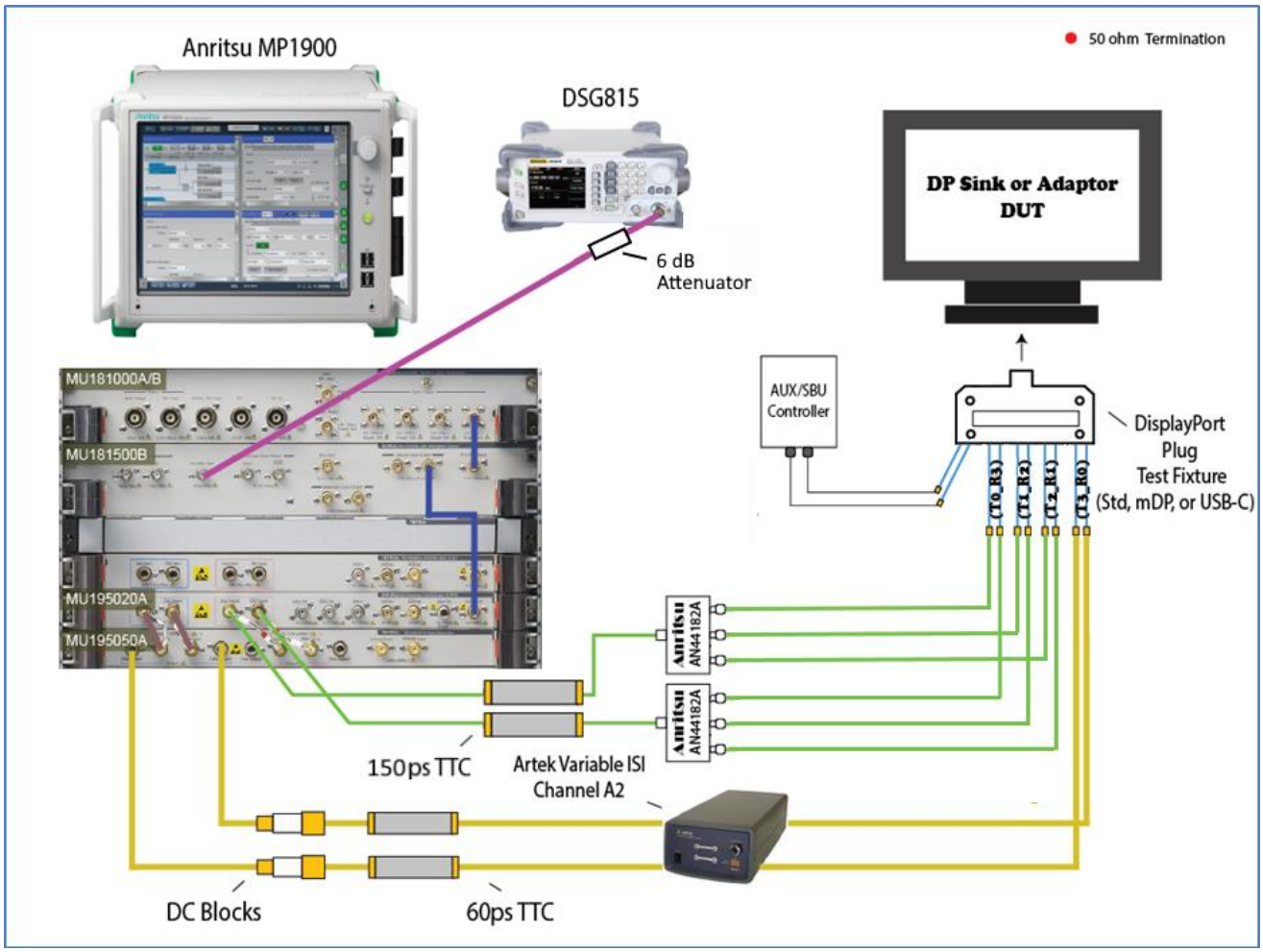


FIGURE 72. TYPICAL DUT TEST SETUP

Test the DUT for each frequency as follows:

1. Verify Frequency Lock using the D10.2 clock pattern for each data rate.
2. Verify Symbol Lock using the Symbol Lock pattern for each data rate and each frequency.
3. Inject Errors with the PRBS7_X2 pattern (for RBR) or PRBS7 pattern (for HBR) or CP2520 Compliance Eye Pattern (for HBR2) and confirm the correct number of errors is being detected.
4. Test the DUT at each data rate and duration as described in Table 4-3 of the CTS.

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Table 4-3: BER Measurement Test Parameters

Jitter Frequency (MHz)	Number of Bits	Maximum Number of Allowable Bit Errors	Bit Rate	Observation Time (Seconds)[a]	Data Rate Offset
2	10^{12}	1000	HBR3	123	0
			HBR2	185	
			HBR	370	
			RBR	620	
10	10^{11}	100	HBR3	13	+350ppm
			HBR2	19	
			HBR	37	
			RBR	62	
20	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	
			RBR	62	
100	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	

a. To evaluate, the number of bits shall be multiplied by the unit interval (UI) in picoseconds (e.g., for HBR, 10^{11} bits at HBR = 370ps/UI × 10^{11}UI = 37 seconds).

FIGURE 73. TABLE OF TEST TIMES FOR EACH LINK RATE PER CTS

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10 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon (will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

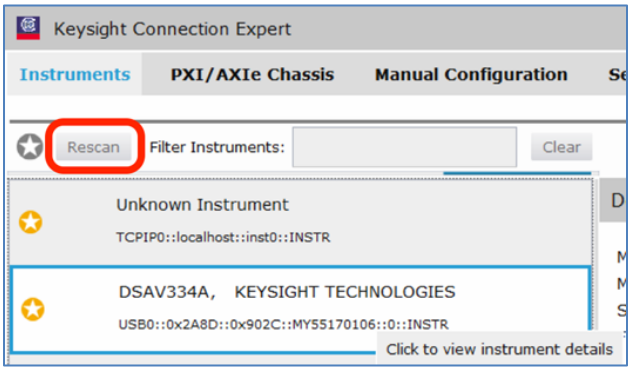


FIGURE 74. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

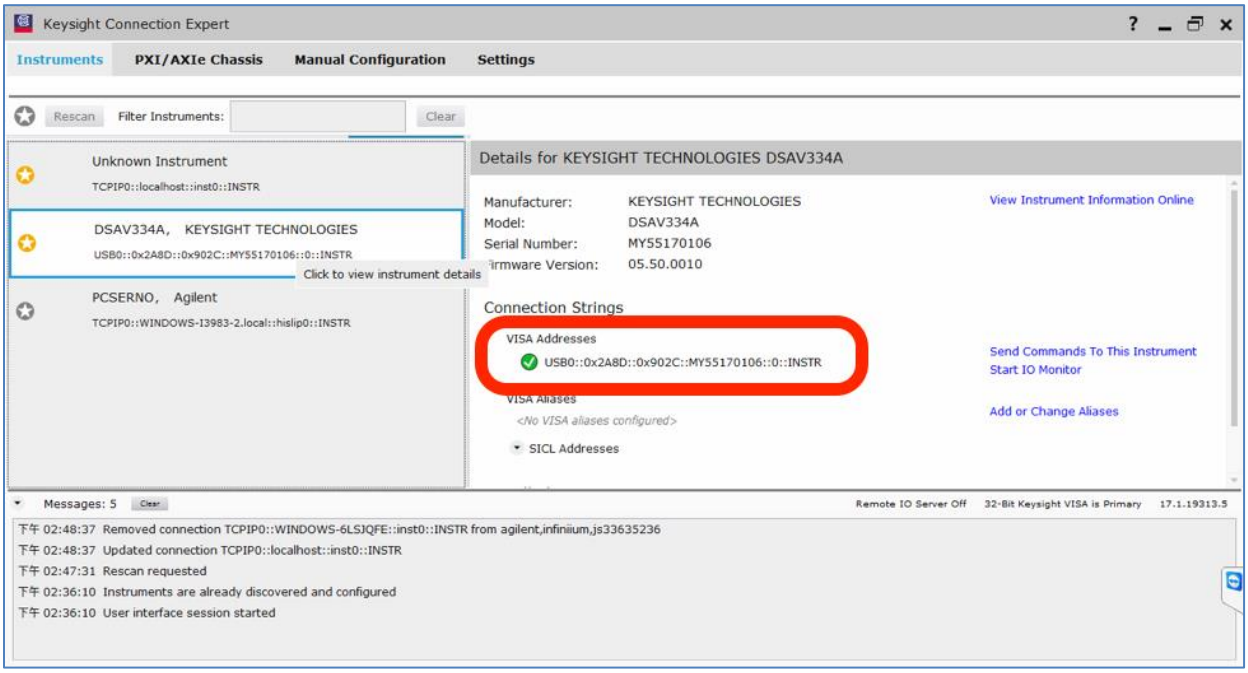


FIGURE 75. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the ‘Address’ field on the Equipment Setup page of the GRL PCIe CEM 4.0 Rx Test Application. If connected via LAN, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to ***omit*** the Port number from the address.

11 Appendix C: Artek CLE1000-A2 Installation

11.1 Install ISI Generator Driver

If using the Artek CLE1000-A2 for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the CLE1000-A2 to a controller PC using a USB 2.0 cable.
2. Turn on the front panel power switch on the CLE1000-A2.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for the CLE1000-A2 has been installed, you will see a 'bang' in the Device Manager.

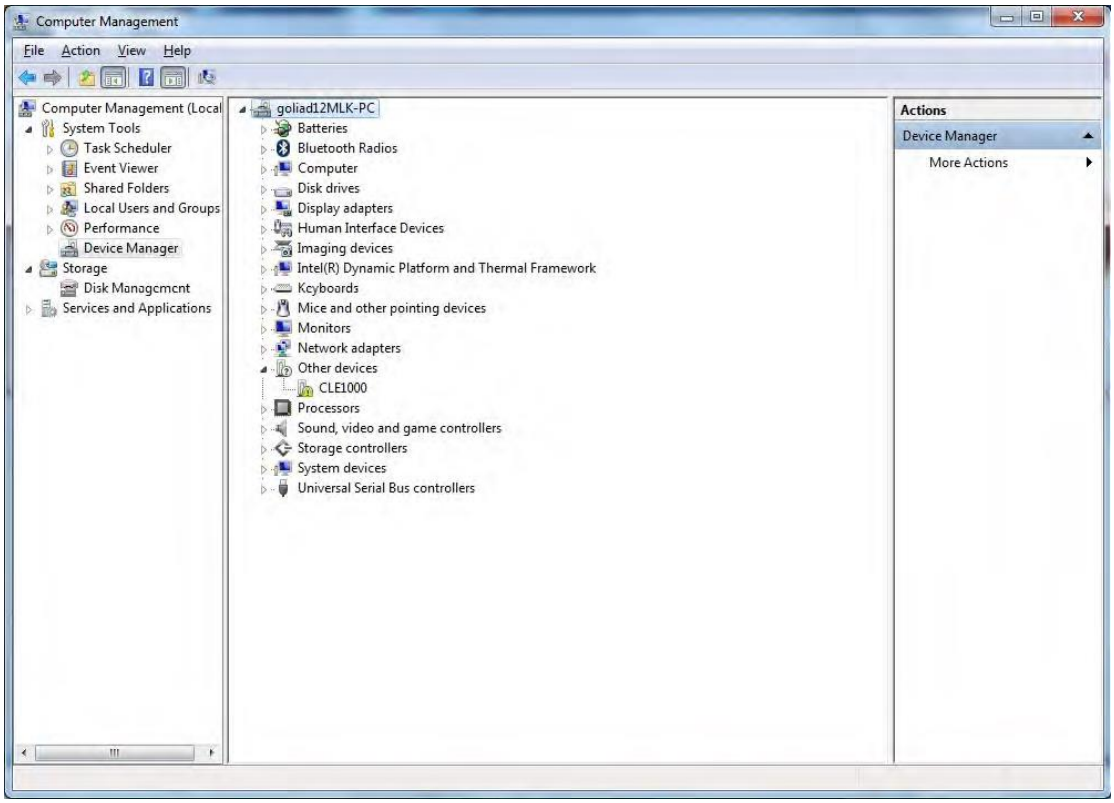


FIGURE 76. DEVICE MANAGER WINDOW

4. To install the CLE1000-A2, go to http://www.aceunitech.com/support.html and download the Control Software package for the CLE1000.
5. Unpack the CLE1000 Software .zip file.
6. Install the CLE1000 Driver:
   a) In Device Manager, right-click on **CLE1000** > **Update Driver**.
   b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 77.
   c) Browse to the root directory of the unzipped CLE1000 Software folder.
   d) Click **Next**. You will be asked to confirm your request to install a driver. See Figure 78.
   e) Click **Install**. The driver software will complete the installation.

7. Once installation has completed, the CLE1000 should appear in Device Manager as shown in Figure 79.

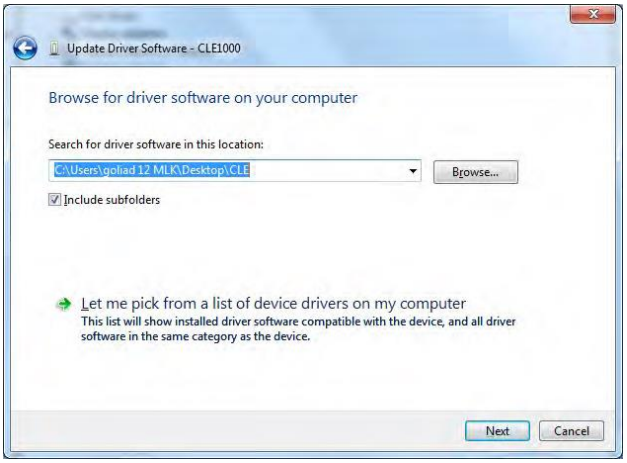


FIGURE 77. UPDATE DRIVER WINDOW

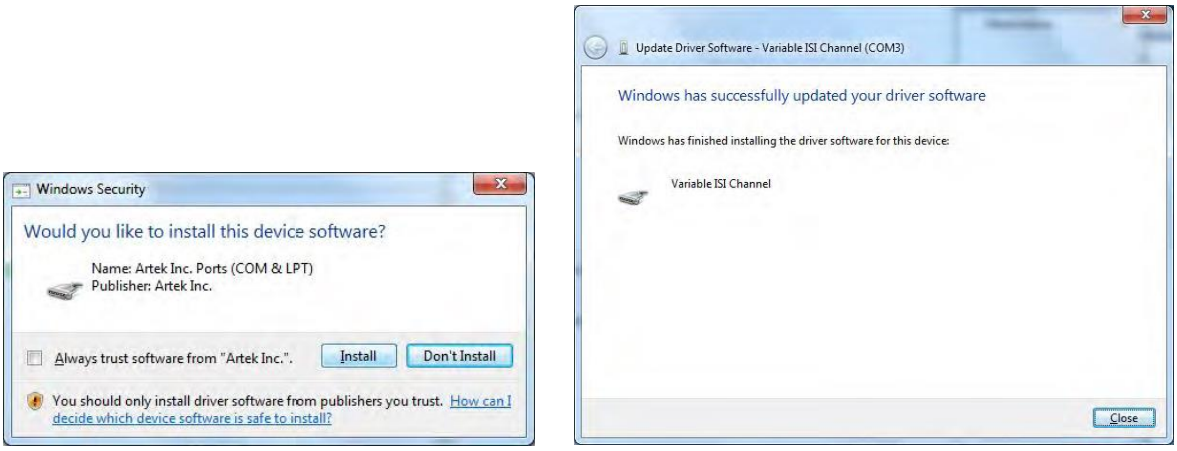
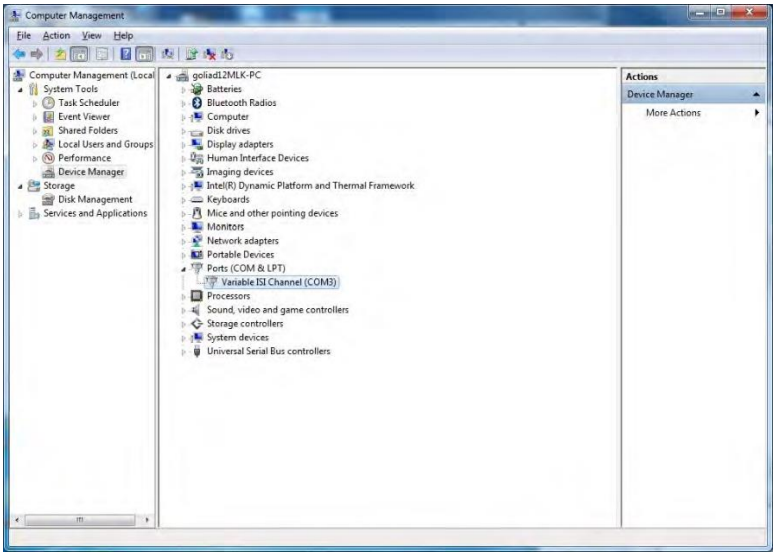


FIGURE 78. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW



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FIGURE 79. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE1000 software driver is now installed and the CLE1000-A2 can now be selected for use remotely using the GRL software.

11.2 Install CLE1000 GUI

It may also be useful to install the CLE1000 GUI, so that the ISI channel can also be controlled manually from the controller PC. To install the software, do the following:

1. In the CLE1000 SW folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you do not want to have manual control.

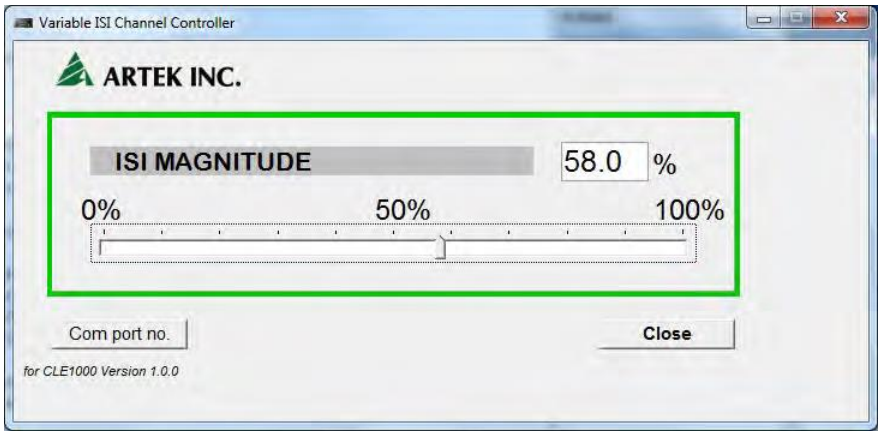


FIGURE 80. CLE1000 GUI

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12 Appendix D: AUX Controller Driver Installation

12.1 Install Unigraf DPT-200 Driver

If the Unigraf DPT-200 is being used as the AUX controller, follow these steps to install the DPT-200 driver before selecting it as the AUX controller in the GRL software.

1. Attach the Unigraf DPT-200 to a USB port on the oscilloscope.
2. On the scope, right-click on **My Computer > Manage > Device Manager**. If the DPT-200 driver has not been installed, it will appear as follows:

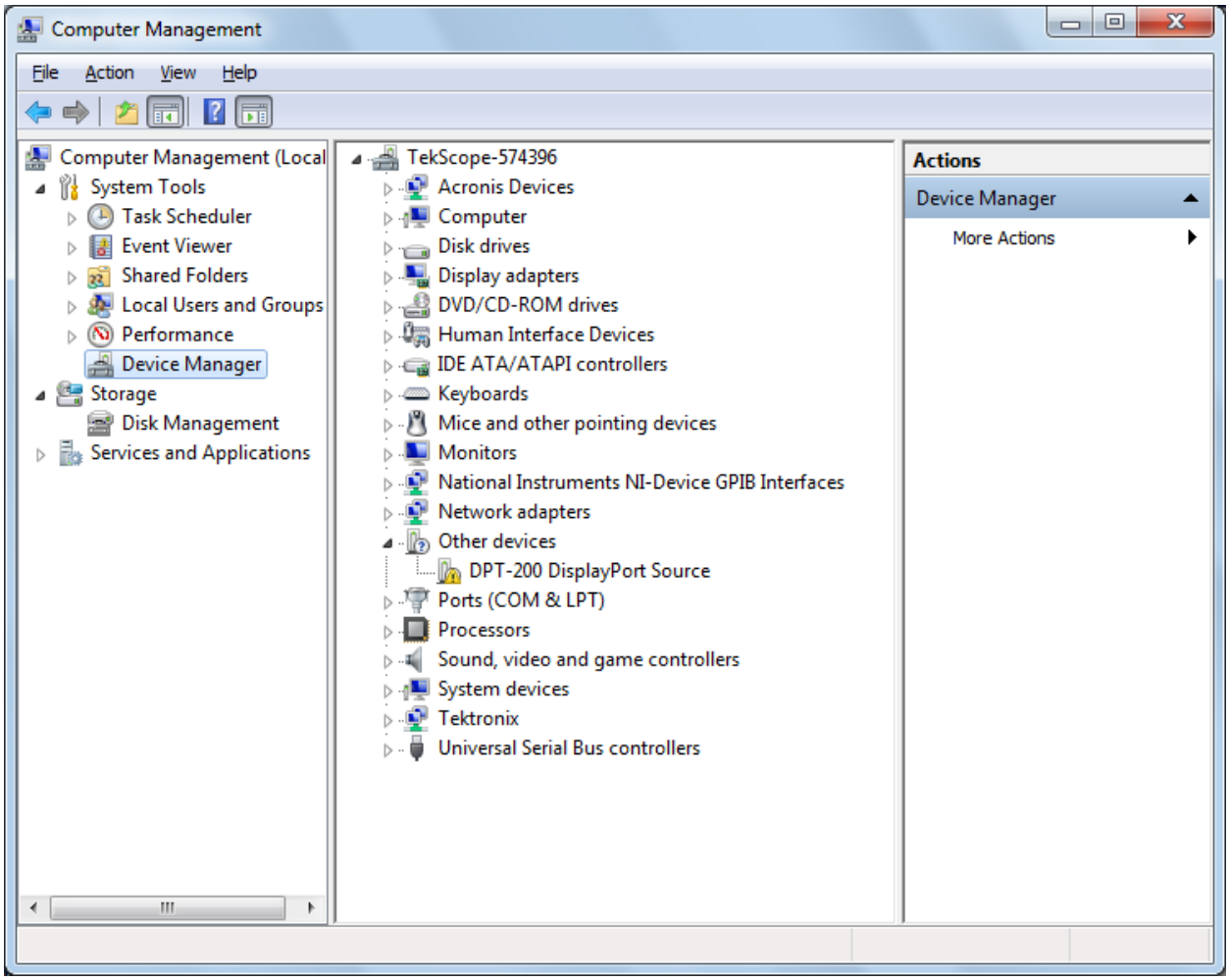


FIGURE 81. DEVICE MANAGER WINDOW

3. To install the DPT-200 driver software, go to http://www.unigraf.fi.unixtemp.saunalahti.fi/files/download/DisplayPort/Reference%20Controller/UGDP-Reference-Controller-1_0.zip and download the Installer package to the hard drive of your PC.
4. Open the Installer package .zip file and install the DPT-200 driver:

a) Run the setup installer file to start the installation and follow the instructions on the screen.
b) During installation, the following dialog will appear. Select 'Install this driver software anyway' to proceed.

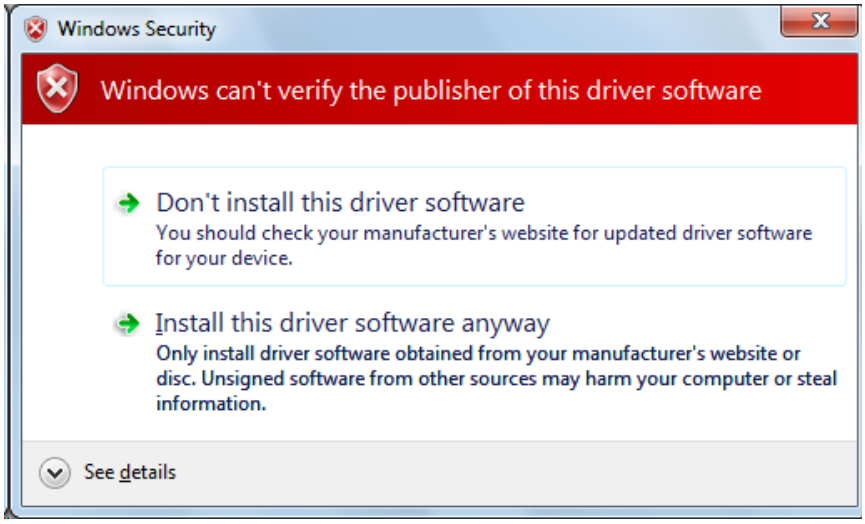


FIGURE 82. INSTALLATION DIALOG

c) Once installation has completed, the DPT-200 will appear in Device Manager as follows:

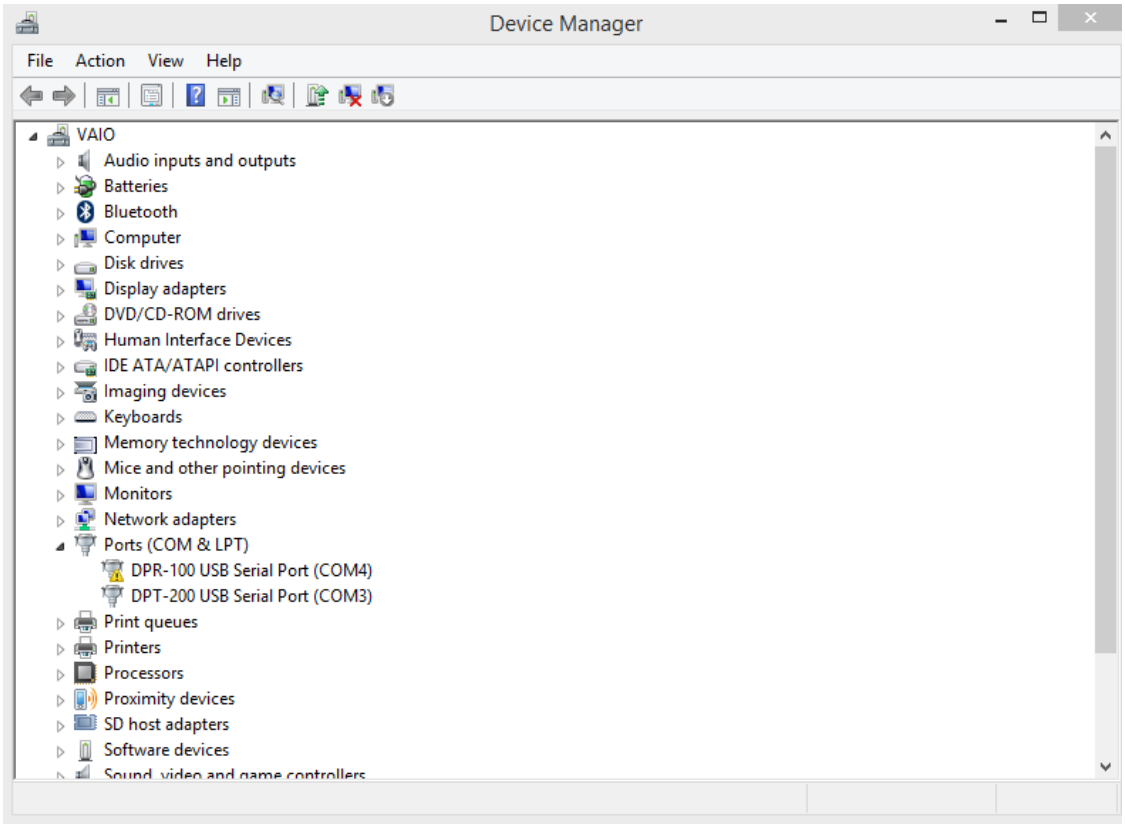


FIGURE 83. DPT-200 INSTALLATION COMPLETED

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